(v) Preliminary Specifications
( ) Final Specifications

Module	**8”(8.0”) WUXGA 16:10 Color TFT-LCD with LED Backlight design**
Model Name	B080UAN02.0(H/W: 0A)
Note ( )	***LED Backlight without driving circuit design***

Customer **Date**	**Approved by** **Date** 9/11/2015
Checked & Approved by **Date**	**Prepared by** 9/11/2015
Note: This Specification is subject to change without notice.	**MPBU Marketing Division AU Optronics corporation**

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2015/9/11	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B080UAN02.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 , 1200(H) x1920(V) screen and 16.7M colors (RGB 8-bits data driver) without LED backlight driving circuit. All input signals are MIPI interface compatible.

B080UAN02.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

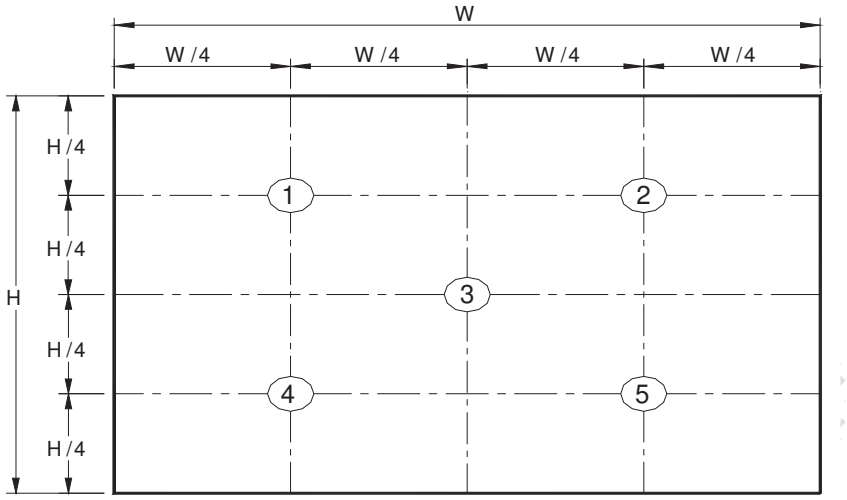
Items	Unit	Specifications			
Screen Diagonal	[mm]	203.09 (8")			
Active Area	[mm]	107.64(H) x 172.224(V)			
Pixels H x V		1200 x 3(RGB) x 1920			
Pixel Pitch	[mm]	0.0897 X 0.0897			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED=20mA) **(Note: ILED is LED current)**	[cd/m^2]	400 typ. (5 points average)			
Luminance Uniformity		80% max. (5 points) 65% max (13 points)			
Contrast Ratio		1000 typ			
Response Time	[ms]	27 typ / 35 max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	1.67			
Weight	[Grams]	80 max			
Physical Size **without bracket**	[mm]		Min.	Typ.	Max.
		Length		114.6	114.8
		Width		184.1	184.3
		Thickness	---	---	3.95
Electrical Interface		4 lane MIPI			
Glass Thickness	[mm]	0.2			
Surface Treatment(panel only)		Glare			
Support Color		RGB 8-bit			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -10 to +60 -20 to +70			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

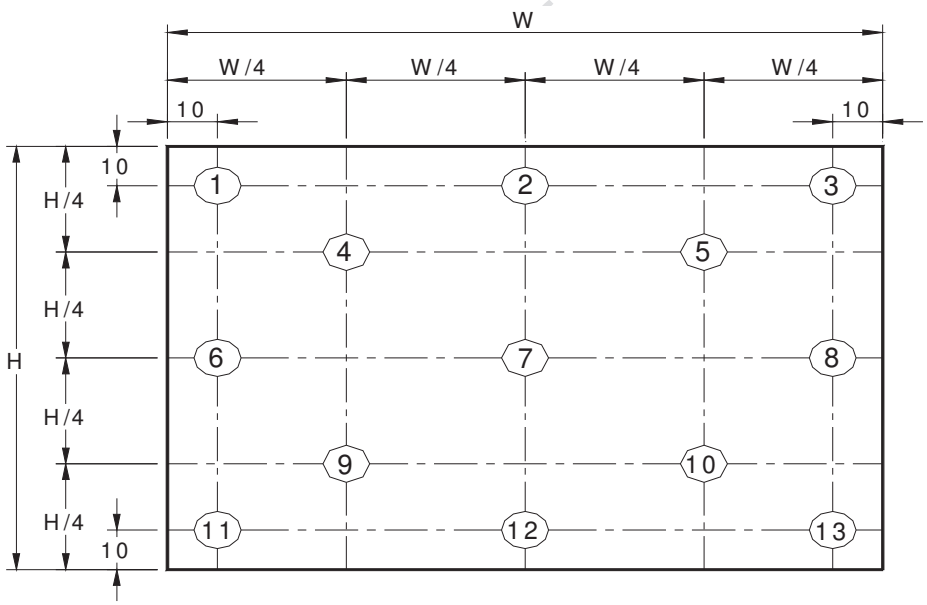
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			5 points average	340	400	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10		85	---	degree	4, 9
		θ_L	(Left)		85	---		
		ψ_H	Vertical (Upper) CR = 10		85	---		
		ψ_L	(Lower)		85	---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	80%		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	65%		2, 3, 4
Contrast Ratio		CR		800	1000	-		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	27	35	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.574	0.604	0.634		4
		Ry		0.315	0.345	0.375		
	Green	Gx		0.288	0.318	0.348		
		Gy		0.575	0.605	0.635		
	Blue	Bx		0.120	0.150	0.180		
		By		0.073	0.103	0.133		
	White	Wx		0.270	0.300	0.330		
		Wy		0.290	0.320	0.350		
NTSC		%		-	60	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

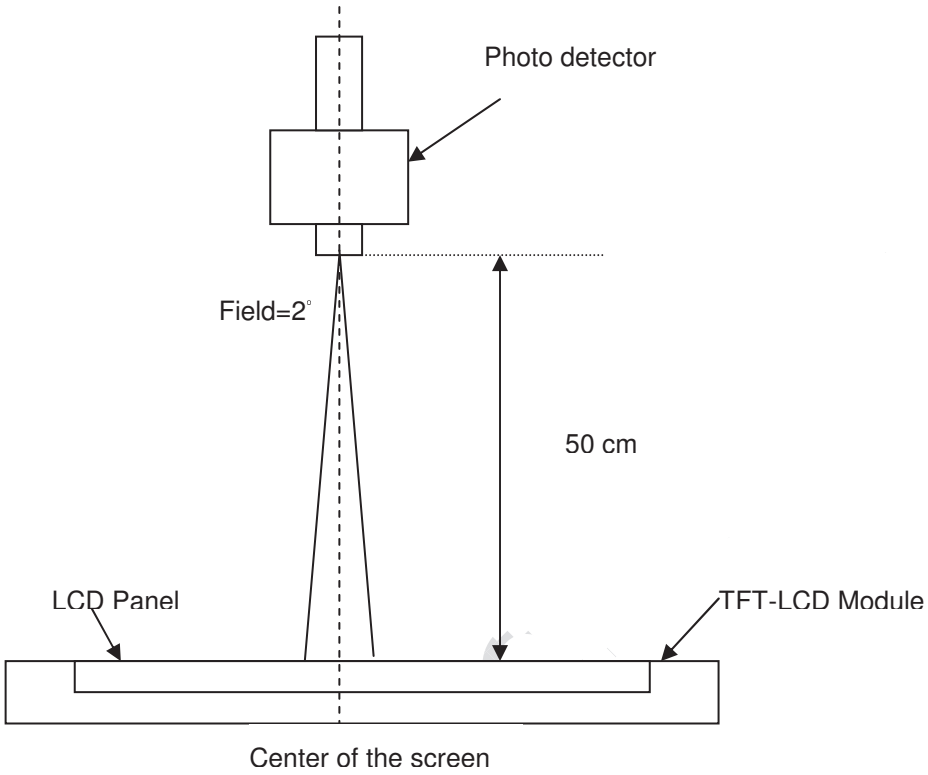
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5: Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

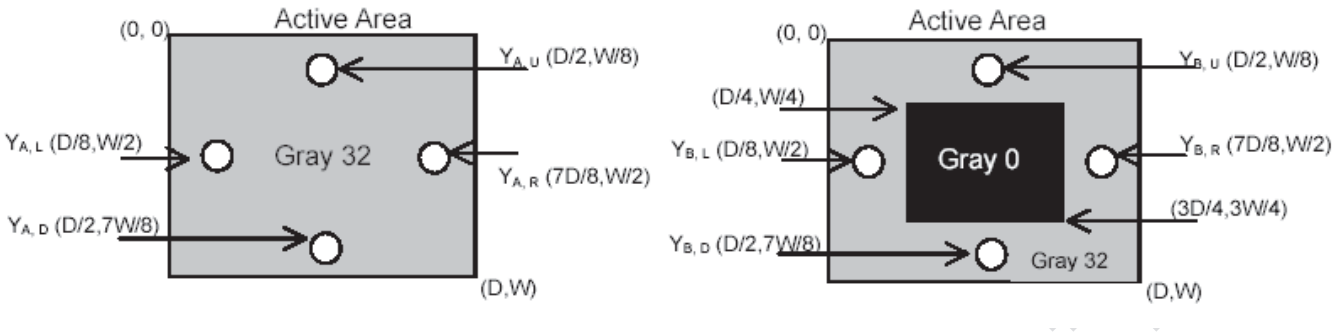
Note 7: Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$$

Where

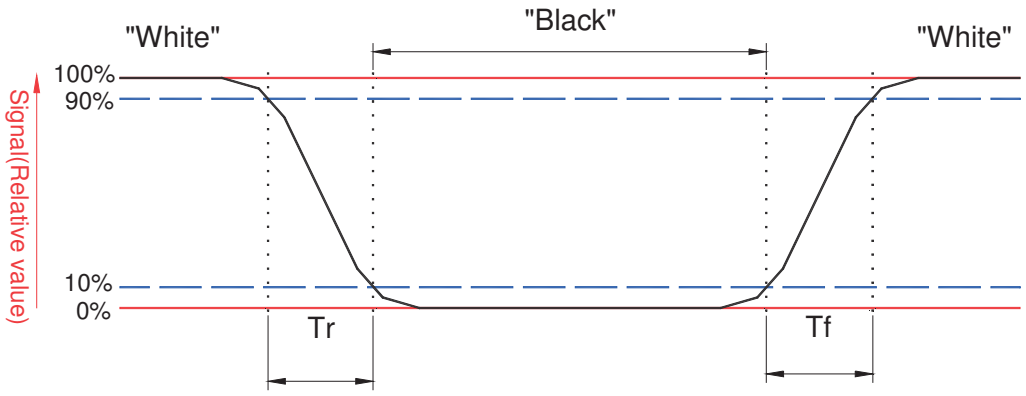
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



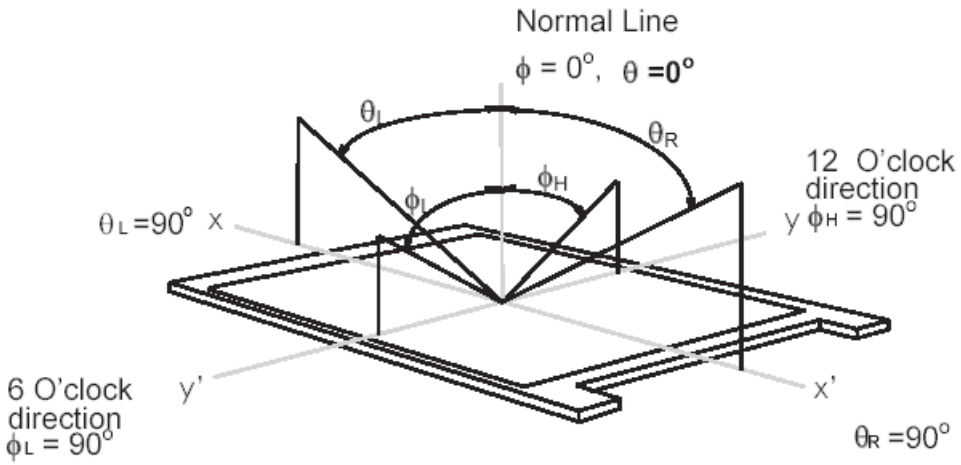
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



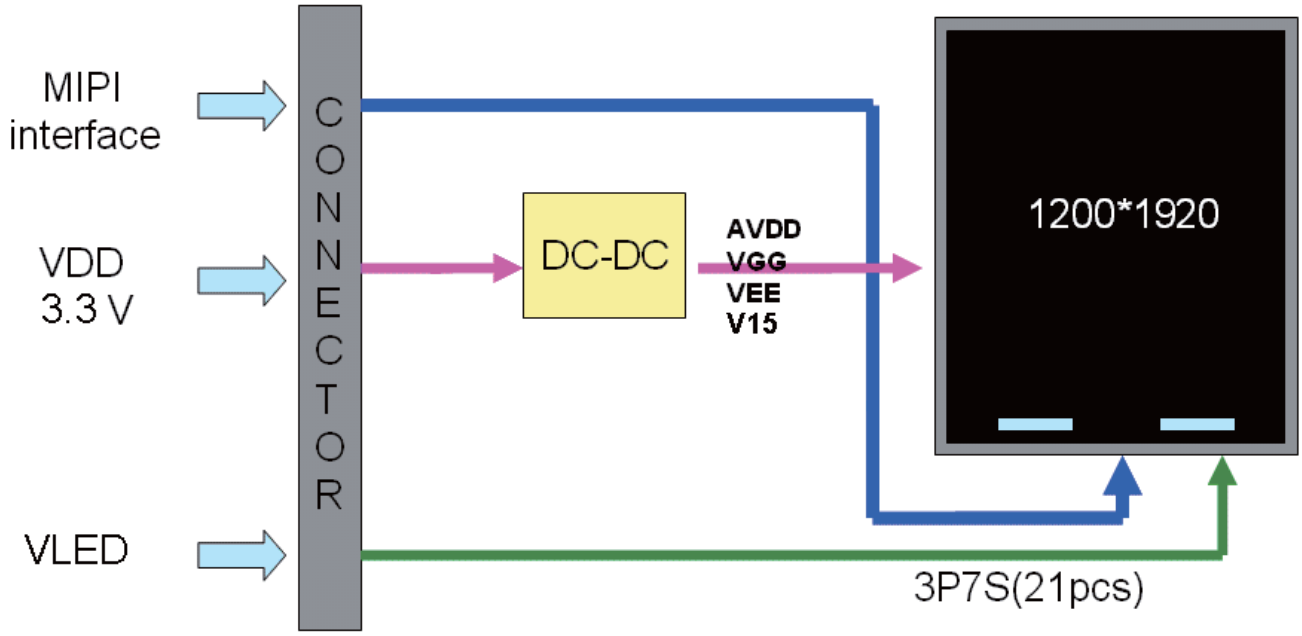
Note 9: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 8 inches wide Color TFT/LCD 31 Pin four channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

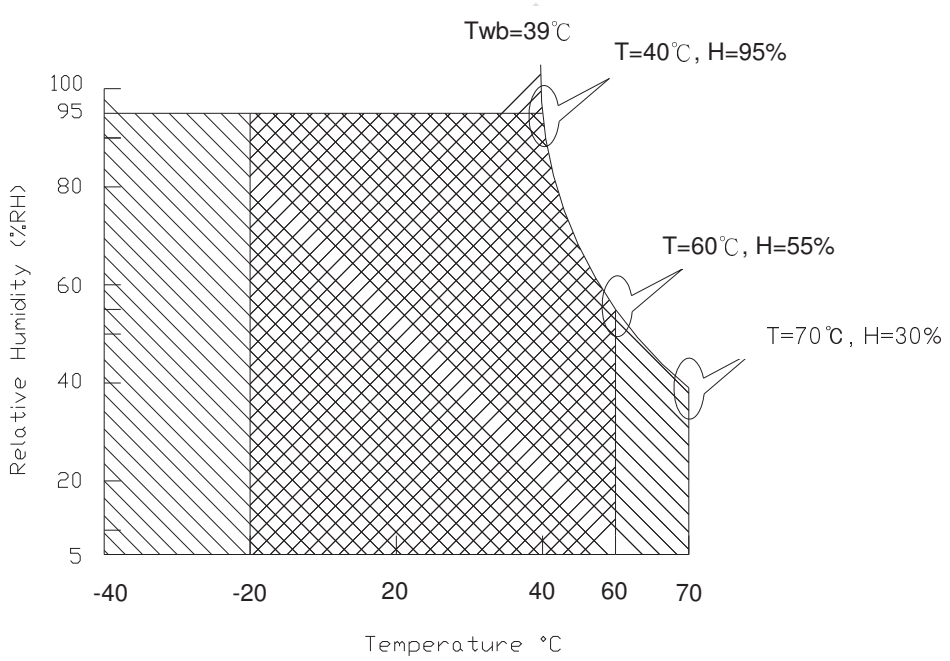
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-10	+60	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+70	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

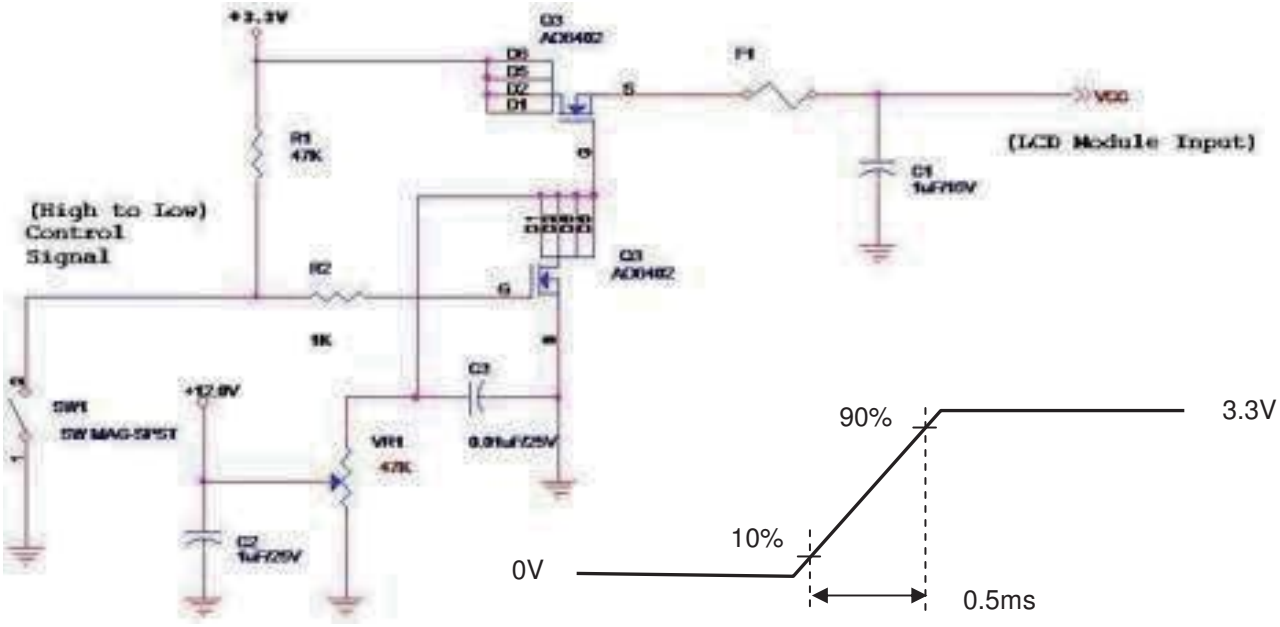
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			0.46	[Watt]	Note 1
IDD	IDD Current			153	[mA]	Note 1
IRush	Inrush Current			1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1: Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3}$ x I_{black})

Note 2: Measure Condition



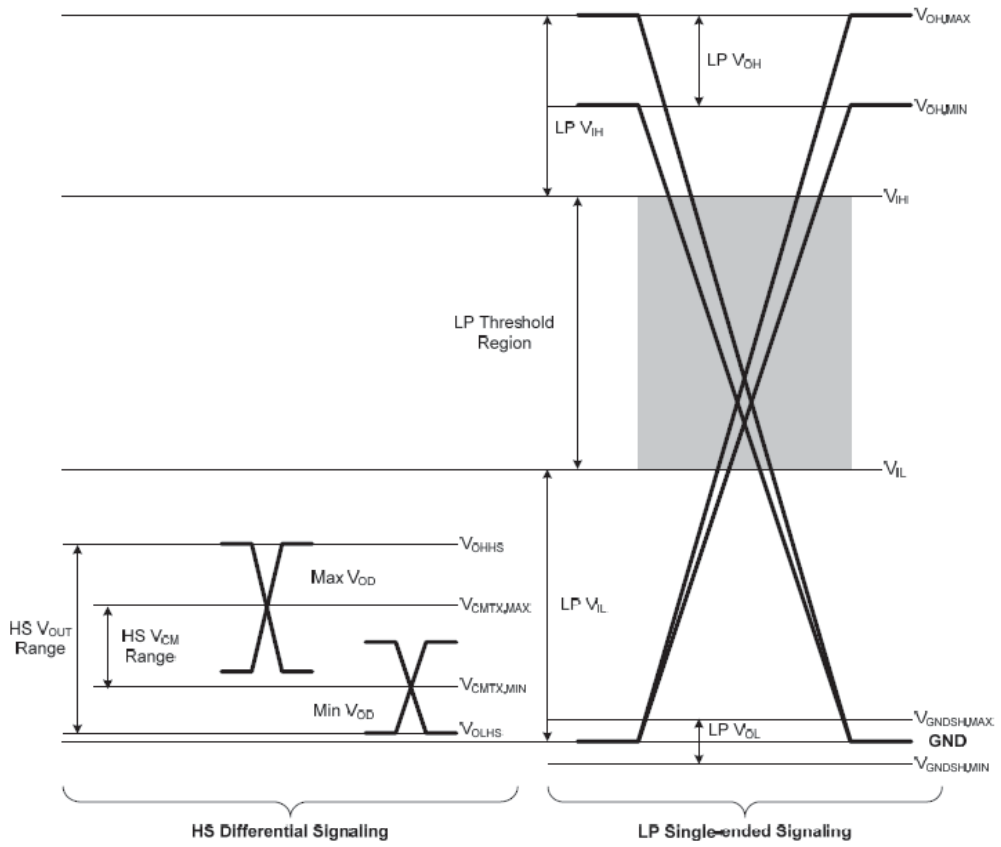
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

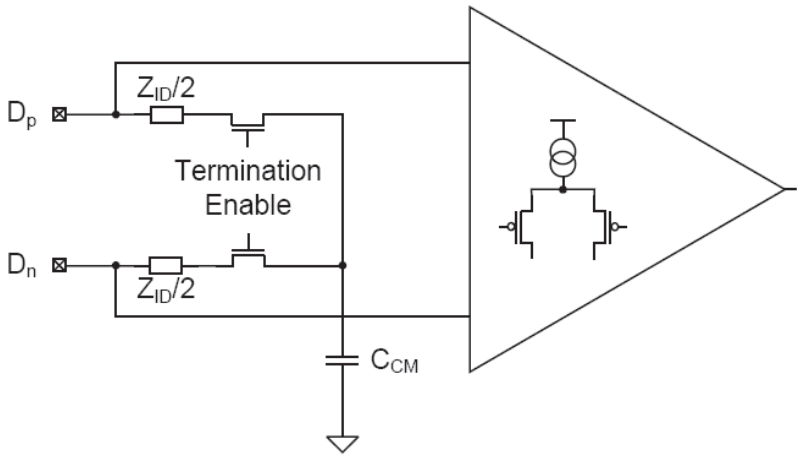
MIPI DC characteristics are as follows:

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps
V_{CMRX}	Common-mode voltage(HS Rx mode)	155	-	330	mV
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880			mV
V_{ILLP}	Logic 0 input voltage (LP Rx mode)			550	mV



MIPI Receiver Differential Input (AC Characteristics)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous		1		12.5	ns

HS RX Scheme

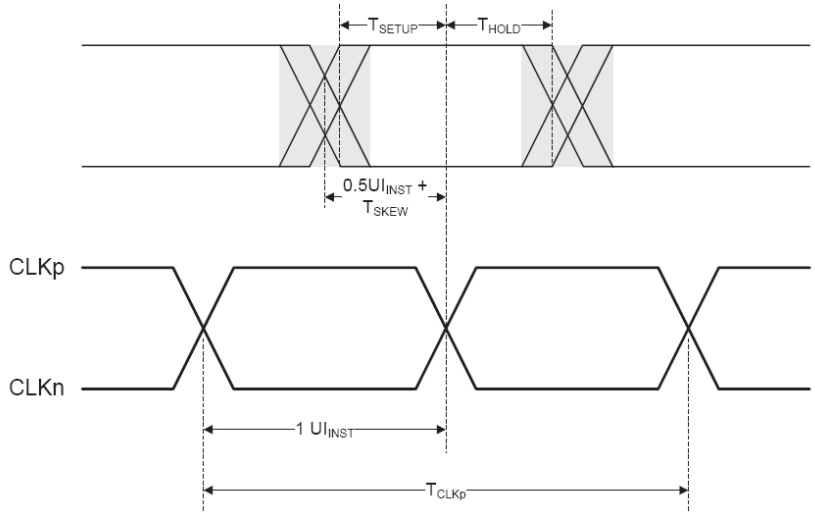


Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.25			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.25			UI_{INST}	2

Note:

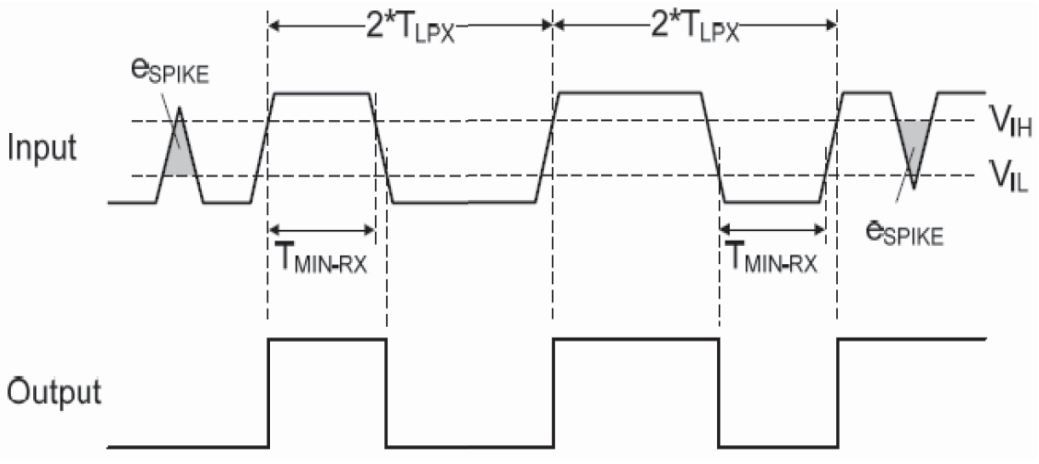
1. Total silicon and package delay budget of 0.25*UI_{INST}
2. Total setup and hold window for receiver of 0.5 *UI_{INST}

High Speed Data Transmission: Data to Clock Timing



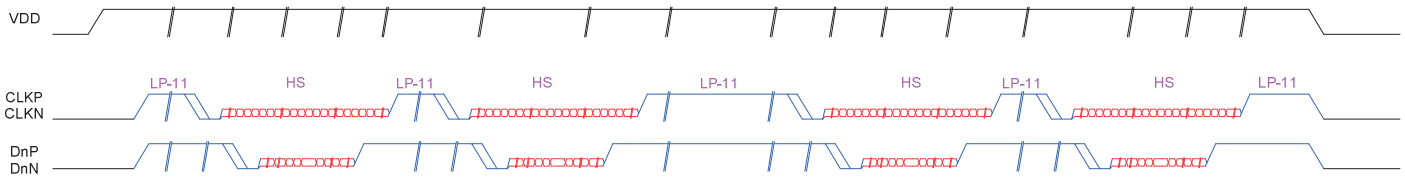
LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		50	-	-	ns
V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and

stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of			105 ns +	ns

	THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			12*UI	
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

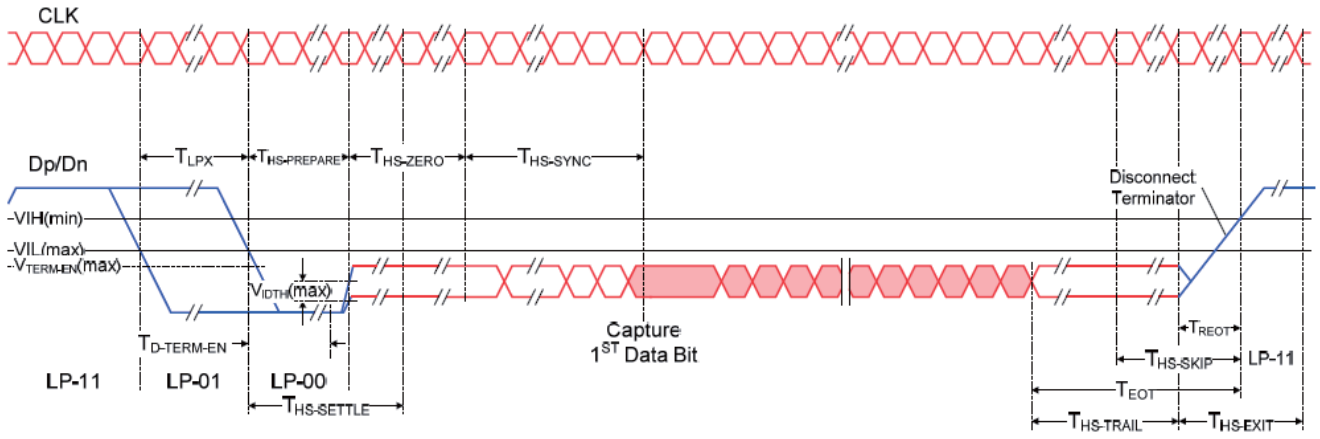
Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

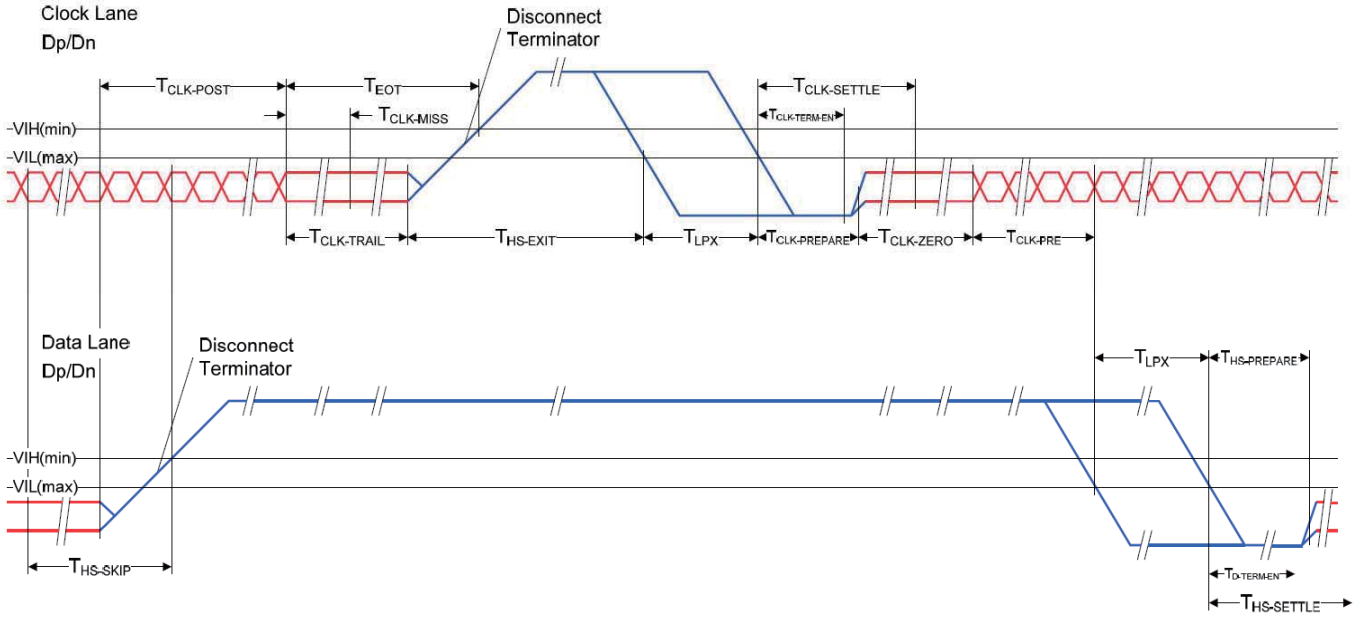
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

3. The I-chip of AUO use is not support BTA (BTA define ignore).

High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.26	[Watt]	(Ta=25℃) Note1.
LED Life-Time	N/A	15,000			Hour	(Ta=25℃) Note2.
LED Forward Voltage	VF	-	2.9	3.0	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	-	20.3	21	[Volt]	(Ta=25℃) Note3.
LED Forward Current	IF	-	20	-	[mA]	(Ta=25℃)

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

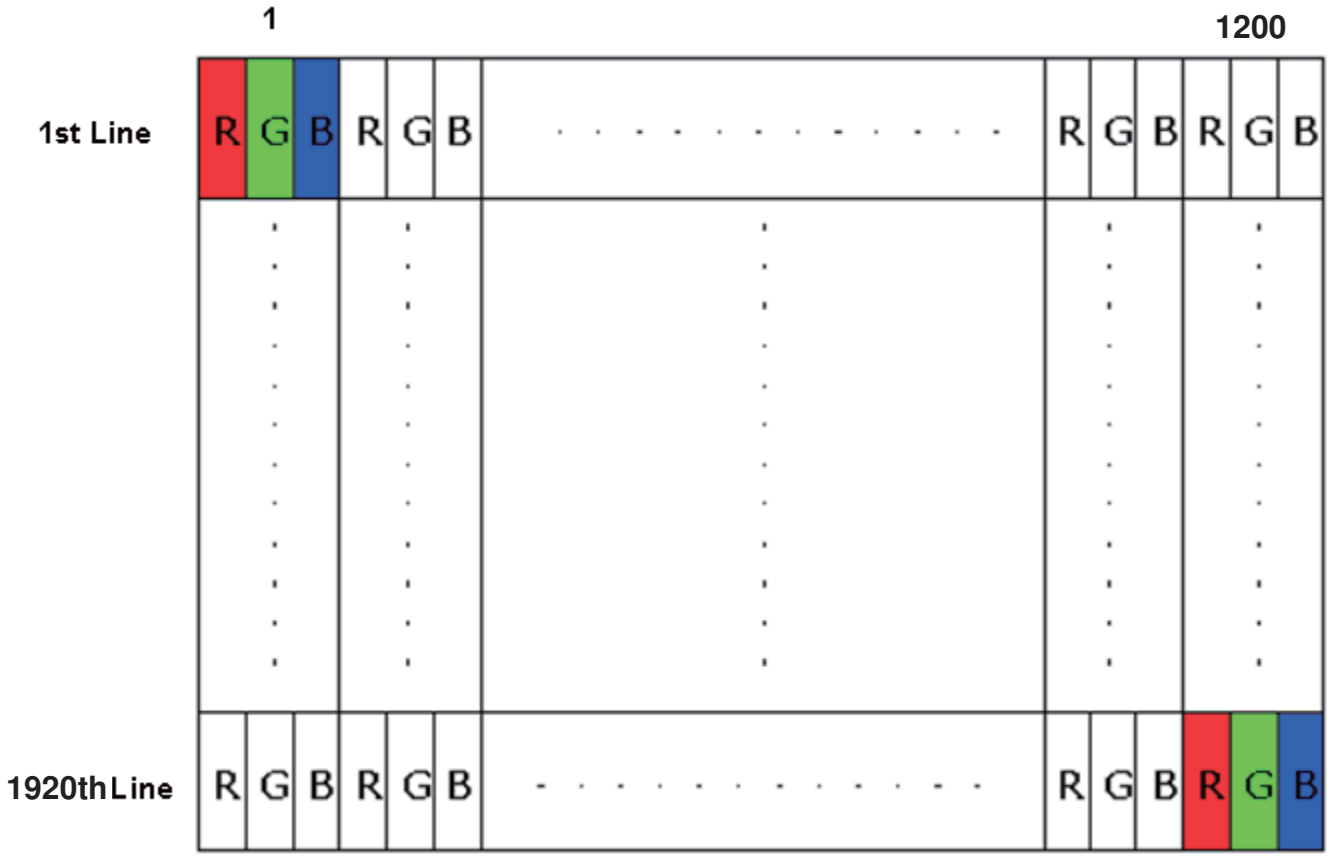
Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 3: LED array is 3 parallels * 7 series, total 21 LEDs

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

MIPI connector:

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	FH26W-45S-0.3SHW(05)

TP connector:

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	FH34SRJ-8S-0.5SH

6.2.2 Pin Assignment

MIPI lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin No.	Symbol	Description	I/O
1	GND	Ground	P
2	GND	Ground	P
3	GND	Ground	P
4	NC	NC (AUO only)	P
5	VCC	Power Supply 3.0V	P
6	VCC	Power Supply 3.0V	P
7	VCC	Power Supply 3.0V	P
8	NC	NC	-
9	FB3-	Cathode	P
10	FB2-	Cathode	P
11	FB1-	Cathode	P
12	NC	NC	-
13	LED+	Anode	P
14	LED+	Anode	P
15	NC	NC	P
16	GND	Ground	P

17	MIPI_DATA0_P	MIPI Differential Data Input	I
18	MIPI_DATA0_N	MIPI Differential Data Input	I
19	GND	Ground	P
20	MIPI_DATA1_P	MIPI Differential Data Input	I
21	MIPI_DATA1_N	MIPI Differential Data Input	I
22	GND	Ground	P
23	MIPI_CLK_P	MIPI Differential Clock Input	I
24	MIPI_CLK_N	MIPI Differential Clock Input	I
25	GND	Ground	P
26	MIPI_DATA2_P	MIPI Differential Data Input	I
27	MIPI_DATA2_N	MIPI Differential Data Input	I
28	GND	Ground	P
29	MIPI_DATA3_P	MIPI Differential Data Input	I
30	MIPI_DATA3_N	MIPI Differential Data Input	I
31	GND	Ground	P
32	NC	NC (AUO only)	-
33	ID0	ID0 (GND)	O
34	ID1	ID1 (NC)	O
35	GND	Ground	P
36	LEDPWMOUT	PWM Control Signal of LED Convert(3.3V)	O
37	NC	NC (AUO only)	-
38	NC	NC (AUO only)	-
39	I2C_SCL_TP	I2C CLK,TYP. 1.8V	I
40	I2C_SDA_TP	I2C SDA,TYP. 1.8V	I
41	TP_INT	Interrupt Pin	I
42	TP_RST	Reset Pin	I
43	AVDD_TP	Analog Power supply, TYP. 3.3V	P
44	DVDD_TP	I/O Digital Power supply, TYP. 1.8V	P
45	GND	Ground	P

TP Interface (Reference)

No.	Symbol	Description
1	DVDD_IO	I/O Digital Power supply, TYP. 1.8V
2	AVDD	Analog Power supply, TYP. 3.3V

3	GND	Ground
4	TOUCH_RESET	Reset Pin
5	TOUCH_INT	Interrupt Pin
6	GND	Ground
7	I2C_SDA	I2C SDA,TYP. 1.8V
8	I2C_SCL	I2C CLK,TYP. 1.8V

Remark: For LCD_ID Assignment, please to be notified by Huawei Engineer

For CTP noise issue, the LCD interface need output frame synchronization signal.

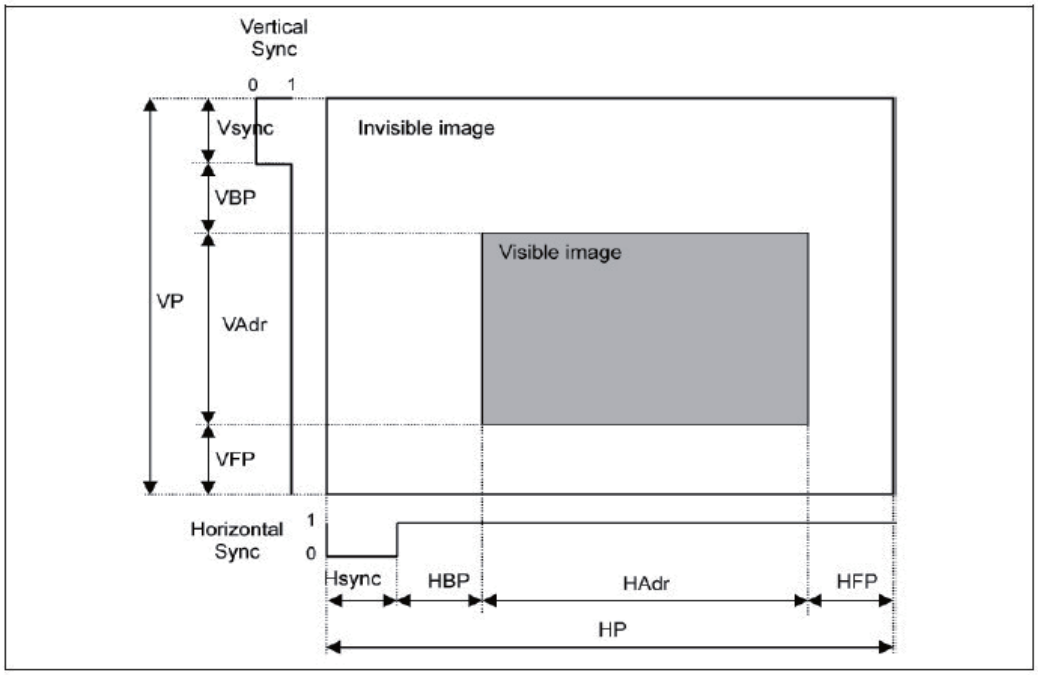
6.3 Interface Timing

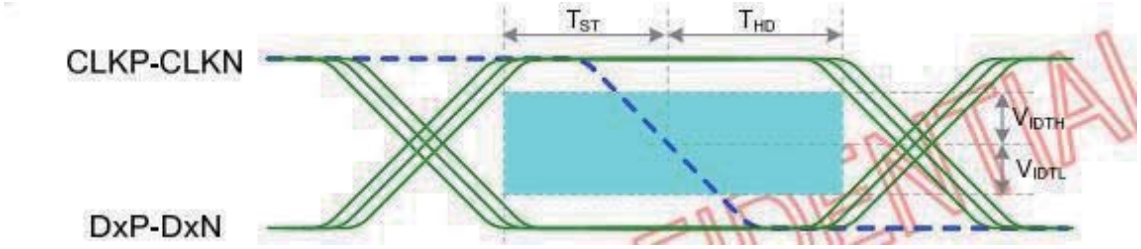
6.3.1 Timing Characteristics

Basically, interface timings should match the 1200 x 1920 /60 Hz manufacturing guide line timing.

ITEM			SYNBOL	min	typ	max	UNIT
LCD	Frame Rate		-	55	60		Hz
	Pixels Rate		-		159.4		MHz
Timing	DCLK	Frequency	fCLK			500	MHz
		Period	Tclk	1			ns
	Horizontal	Horizontal total time	tHP	1275	1341	1342	t_{CLK}
		Horizontal Active time	tHadr	1200			t_{CLK}
		Horizontal Pulse Width	tHsync	1	1	1	t_{CLK}
		Horizontal Back Porch	tHBP	32	60	60	t_{CLK}
		Horizontal Front Porch	tHFP	60	80	81	t_{CLK}
	Vertical	Vertical total time	tvp	1981	1981	1982	t_H
		Vertical Active time	tVadr	1920			t_H
		Vertical Pulse Width	tVsync	1	1	1	t_H
		Vertical Back Porch	tVBP	25	25	25	t_H
		Vertical Front Porch	tVFP	35	35	36	t_H
Differential Swing			VDswing	140			mV
Bit Rate			TX SPD	955	999	1000,	Mbps

	(MBPS)				
Pixel Fomat			8		Data bit/ pixel
Lane			1		Lane





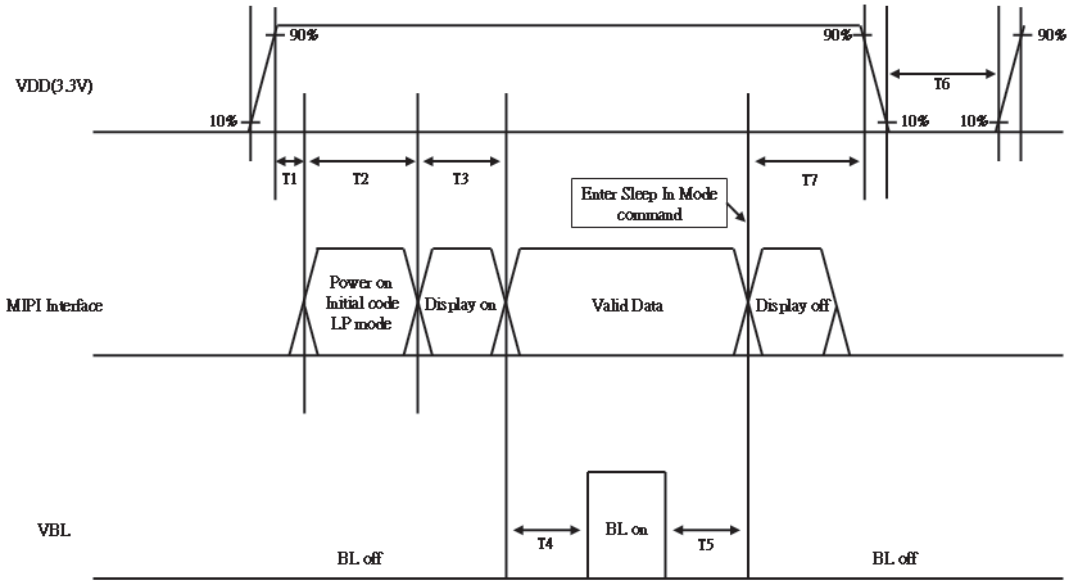
Note: VIDTH is the input high threshold and should >70mV

VIDTL is the input low threshold and should < -70mV

6.4 Power On Sequence

6.4.1 Power

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



Parameter	Value				Remark
	Min.	Typ.	Max.	Unit	
T1	5	-	-	ms	
T2	180	-	-	ms	
T3	100	-	-	ms	
T4	200	-	-	ms	
T5	200	-	-	ms	
T6	500	-	-	ms	
T7	120	-	-	ms	

6.4.2 MIPI Command

NO	Document No.	Type	Attachment file
1	NT51021 AN-017 V01 20140110 I2C Enforce Mode.pdf	切換控制權 (MIPI LP mode)	NT51021 AN-017 V01 20140110 I2C E
2	NT51021 AN-002 V01 20140926 MIPI Video Input.pdf	IC noise for MIPI	NT51021 AN-002 V01 20140926 MIPI `
3	NT51021 AN-023 V2.0 ALS Application Notice	ALS	NT51021 AN-023 V2.0 ALS Application

	20140731.pdf		
4	NT51021 AN-024 V1.1 CABC Application Notice .pdf	CABC_EN	NT51021 AN-024 V1.1 CABC Applicati
5	NT51021 AN-021 V0.1 Color Enhancement Application Note 20140128.pdf	CE_EN	NT51021 AN-021 V0.1 Color Enhancem
6	NT51021 AN-003 V03 20140930 MIPI AC Timing Fine Tune.pdf	MIPI AC Timing Fine tune	NT51021 AN-003 V03 20140930 MIPI
7		Sleep in/ out	Page 0 : Sleep in:0x10, sleep out:0x11,

Double-Click the “Attachment Icon” above for opening attachment file.

Remark: initialization code must include the code for GAMMA 2.2 in the Power Supply condition for the module。

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

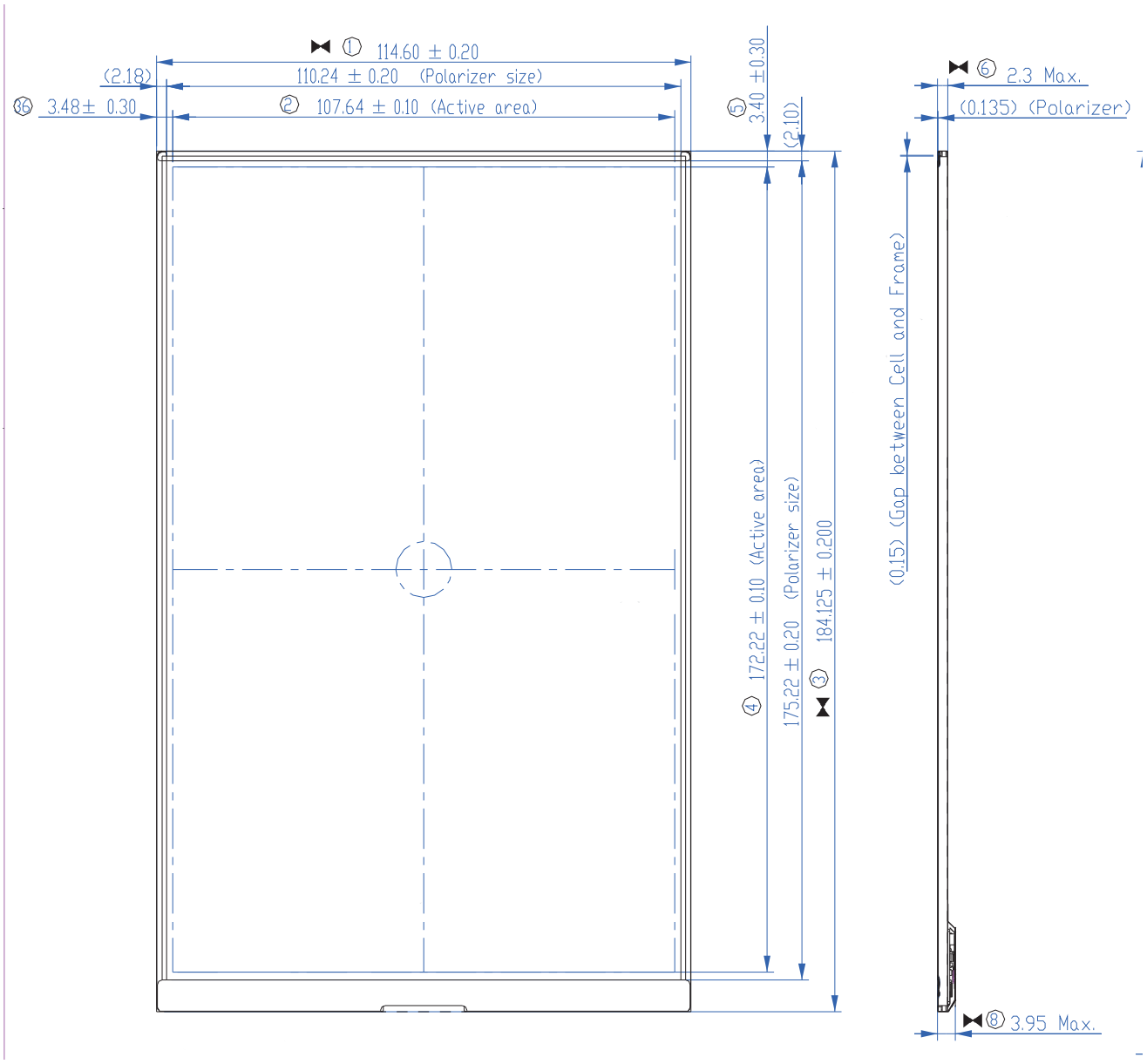
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 60℃, Dry, 240h	
Low Temperature Operation	Ta= -10℃, 240h	
High Temperature Storage	Ta= 70℃, 240h	
Low Temperature Storage	Ta= -20℃, 240h	
Thermal Shock Test	Ta=-20℃ to 70℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

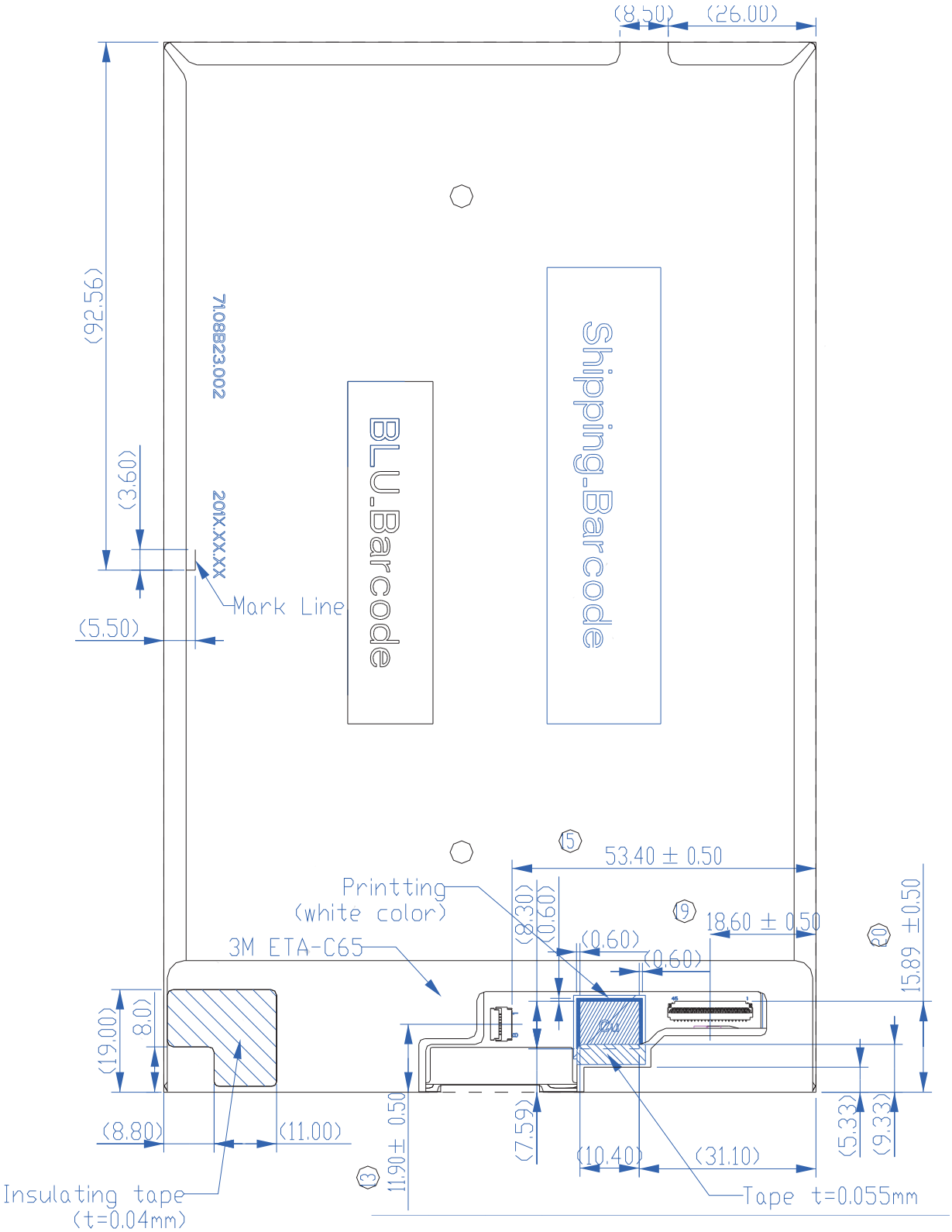
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 Standard Front View



8.2 Standard Back View



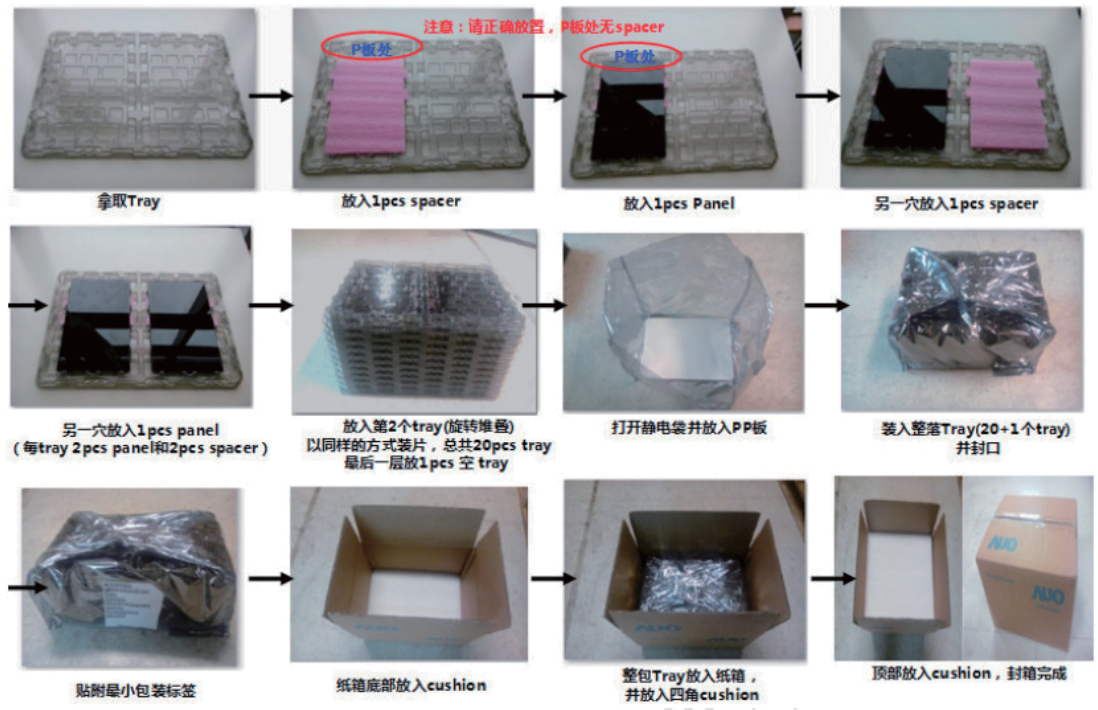
9. Shipping and Package

9.1 Shipping Label Format

Shipping label:

9.2 Carton Package

filled EPE cushion around(as below), then seal the carton, finish the package.



9.3 Shipping Package of Palletizing Sequence