# Product Specification

AU OPTRONICS CORPORATION

**( ) Preliminary Specifications**
**(V ) Final Specifications**

| | |
|---|---|
| **Module** | **10.1”(10.01”) WXGA 16:10 Color TFT-LCD** |
| **Model Name** | **B101EAN01.5 (H/W: 0A) LCM** |
| **Note ( )** | ***LED Backlight with driving circuit design*** |

| | |
|---|---|
| **Customer** **Date** | **Approved by** **Date** |
| | YW Lee Aug 28, 2014 |
| **Checked & Approved by** **Date** | **Prepared by** |
| | NC Yeh Aug 28, 2014 |
| Note: This Specification is subject to change without notice. | **MPBU Marketing Division AU Optronics corporation** |

# Contents

# Record of Revision

| Version and Date | Page | Old description | New Description | Remark |
|---|---|---|---|---|
| 0.1 08/14/2013 | | First Edition for Customer | | |
| 0.2 09/13/2013 | 12,23 | | Modify Absolute Ratings of Environment<br>Add Panel Reliability Test | |
| 0.3 10/02/2013 | 26,27 | | Modify 9.1 & 9.2 Label<br>Add 10.1 EDID Description | |
| 0.4 10/23/2013 | 20 | MIPI Pin 28<br>“NC”, Not Connection | MIPI Pin 28<br>“GND”, Ground | |
| 0.5 11/14/2013 | 24 | Front View Drawing<br>Upper Pol Size&Position | Front View Drawing<br>Upper Pol Size&Position | |
| 0.6 11/29/2013 | 11,22 | | Functional Block Diagram (Add P Gamma)<br>Power ON/OFF Sequence (No SMBUS) | |
| 0.7 12/17/2013 | 18 | | Add 5.2 Backlight Unit<br>5.2.1 LED characteristics | |
| 0.8 01/09/2014 | 06<br>18 | | Update 2.2 Optical Characteristics<br>5.2 Backlight Unit | |
| 0.9 04/01/2014 | 23 | | Update 6.4 Power ON/OFF Sequence | |
| 0.10 04/25/2014 | 18<br>20<br>21 | | Update 5.2.2 Backlight input signal characteristics<br>Update 6.2.2 MIPI Pin Assignment | |
| 0.11 2014/04/28 | 05 | General Specification<br>Physical Size :<br>Length & Width | Length : Min. : 227.42 mm<br>Width : Min . : 147.5 mm | |
| 0.12 2014/05/05 | 06 | Response Time | Response Time : 38 msec (Max.) | |
| 0.13 2014/05/20 | 21 | | Update 6.3.1 Timing Characteristics<br>Horizontal Section:<br>Period(TH) : 1,340 Min. ; 1,480 Typ.<br>Blanking(THB) : 60 Min. | |
| 0.14 2014/06/03 | 27 | | Update 9.1 Shipping Label Format | |
| 0.15 2014/07/18 | 20<br>21<br>23 | | Update 6.2.2 MIPI Pin Assignment<br>Update 6.4 Power ON/OFF Sequence | |
| 0.16 2014/07/30 | 05<br>25<br>27 | Width : 147.8 +/- 0.3mm | Width : 148.3 +/- 0.3mm<br>Update 8.1 Standard Front View<br>Update Label HW : 0A -> 1A | |

## 1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

## 2. General Description

B101EAN01.5 is a 10.1 inch-wide Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The display supports the 16:10 WXGA, 1280(H) x800(V) screen and 16.7M colors (RGB 6-bits data driver with FRC). All input signals are MIPI interface compatible.

## 2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

| Items | Unit | Specifications | | | |
|---|---|---|---|---|---|
| Screen Diagonal | [mm] | 255.85 (10.07 inch) | | | |
| Active Area | [mm] | 216.96(H) x 135.6(V) | | | |
| Pixels H x V | | 1280 x 3(RGB) x 800 | | | |
| Pixel Pitch | [mm] | 0.1695 X 0.1695 | | | |
| Pixel Format | | R.G.B. Vertical Stripe | | | |
| Display Mode | | AHVA, Normally Black | | | |
| White Luminance ($I_{LED}$=24mA) **(Note: ILED is LED current)** | [cd/m2] | 350 typ. (5 points average)<br>295 min. (5 points average) | | | |
| Luminance Uniformity | | 1.25 max. (5 points) | | | |
| Contrast Ratio | | TYP. 800:1 / Min 600:1 | | | |
| Response Time | [ms] | Typ. 30 (White to black) | | | |
| Nominal Input Voltage VDD | [Volt] | 3.3V typ | | | |
| Power Consumption | [Watt] | 3.05 W(Max) w/ LED driver | | | |
| Weight | [Grams] | 145g Max | | | |
| Physical Size **Include bracket** | [mm] | | Min | Typ | Max |
| | | Length | 227.42 | 227.72 | 228.02 |
| | | Width | 148.0 | 148.3 | 148.6 |
| | | Thickness Panel Side | | 2.37 | 2.6 |
| | | Thickness PCBA Side | | | 4.6 |
| Electrical Interface | | MIPI | | | |
| Glass Thickness | [mm] | 0.25/0.25 (w/o PF) | | | |
| Surface Treatment (panel only) | | HC (Glare) | | | |

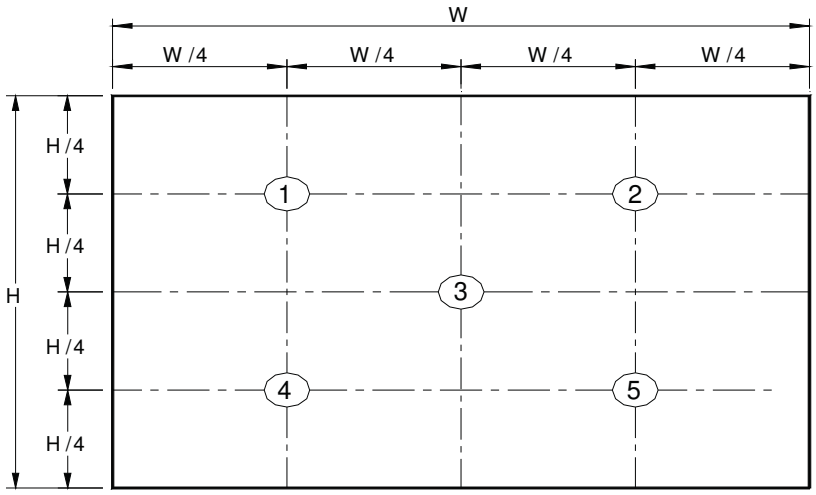
| | | |
|---|---|---|
| Support Color | | 16.7M colors ( RGB 6-bit +FRC ) |
| Temperature Range<br>Operating | [°C]<br>[°C] | 0 to + 50℃<br>-20 to +60℃ |
| RoHS Compliance | | RoHS Compliance |

## 2.2 Optical Characteristics

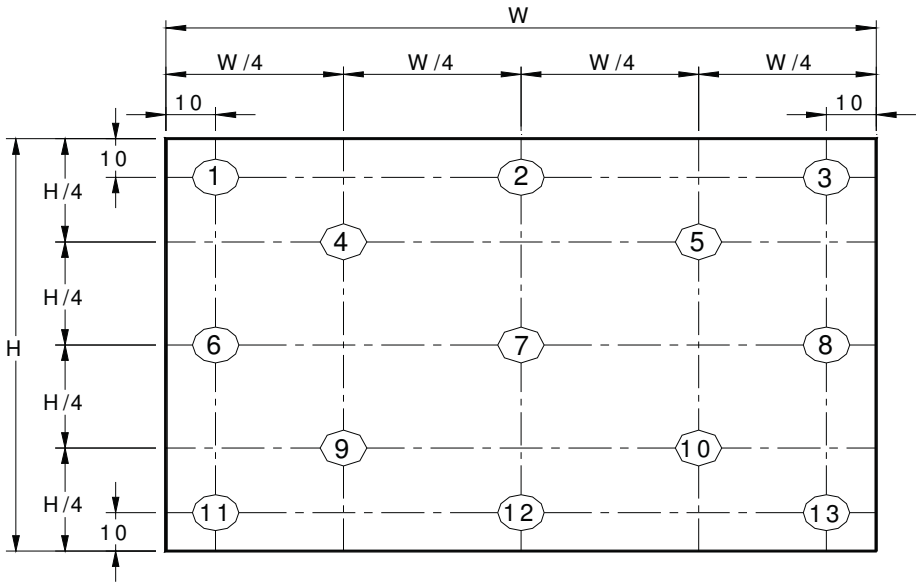
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

| Item | | Symbol | Conditions | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| White Luminance<br>$I_{LED}$=24mA | | | 5 points average | 295 | 350 | - | cd/m² | 1, 4, 5. |
| Viewing Angle | | $\theta_R$<br>$\theta_L$ | Horizontal (Right)<br>CR = 10 (Left) | | 85<br>85 | -<br>- | degree | 4, 9 |
| | | $\psi_H$<br>$\psi_L$ | Vertical (Upper)<br>CR = 10 (Lower) | | 85<br>85 | -<br>- | | |
| Brightness Uniformity | | $\delta_{5P}$ | 5 Points | | | 1.25 | | 1, 3, 4 |
| Brightness Uniformity | | $\delta_{13P}$ | 13 Points | | | 1.50 | | 1, 3, 4 |
| Contrast Ratio | | CR | | 600 | 800 | - | | 4, 6 |
| Response Time | | $T_{RT}$ | Rising + Falling | - | 30 | 38 | msec | 4, 8 |
| Color / Chromaticity Coodinates | Red | Rx | CIE 1931 | 0.568 | 0.598 | 0.628 | | 4 |
| | | Ry | | 0.314 | 0.344 | 0.374 | | |
| | Green | Gx | | 0.296 | 0.326 | 0.356 | | |
| | | Gy | | 0.554 | 0.584 | 0.614 | | |
| | Blue | Bx | | 0.124 | 0.154 | 0.184 | | |
| | | By | | 0.100 | 0.130 | 0.160 | | |
| | White | Wx | | 0.283 | 0.313 | 0.343 | | |
| | | Wy | | 0.299 | 0.329 | 0.359 | | |
| NTSC | | % | | | 50 | - | | |

**Note 1**: 5 points position (Ref: Active area)




**Note 2**: 13 points position (Ref: Active area)



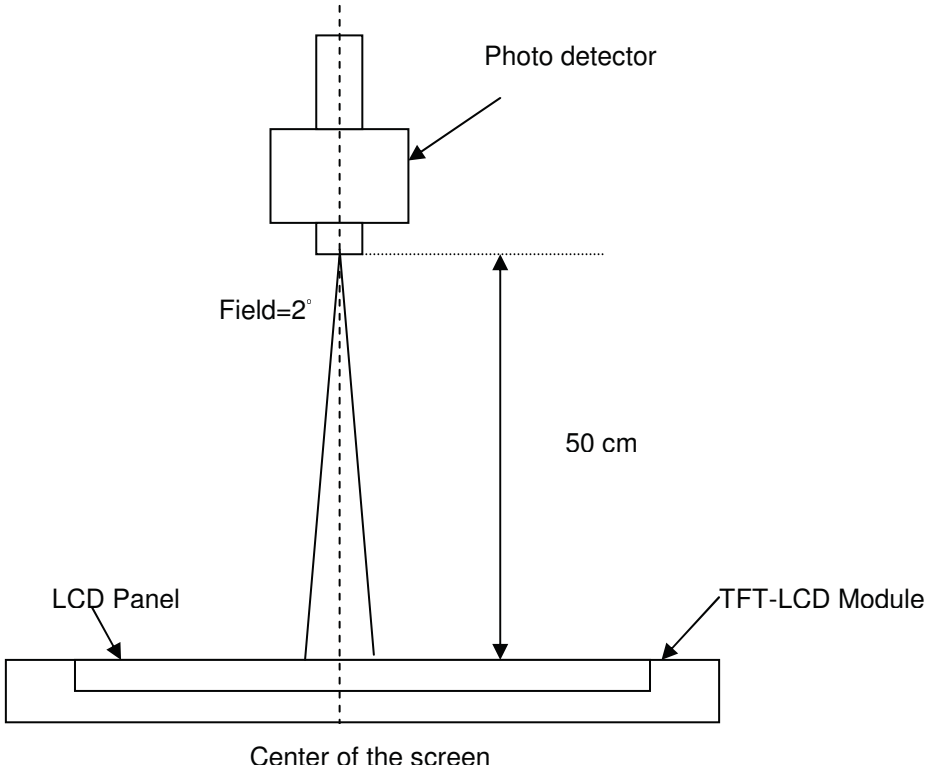

**Note 3**: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4**: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.




**Note 5**： Definition of Average Luminance of White ($Y_L$):

Measure the luminance of gray level 63 at 5 points，$Y_L$ = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6**： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

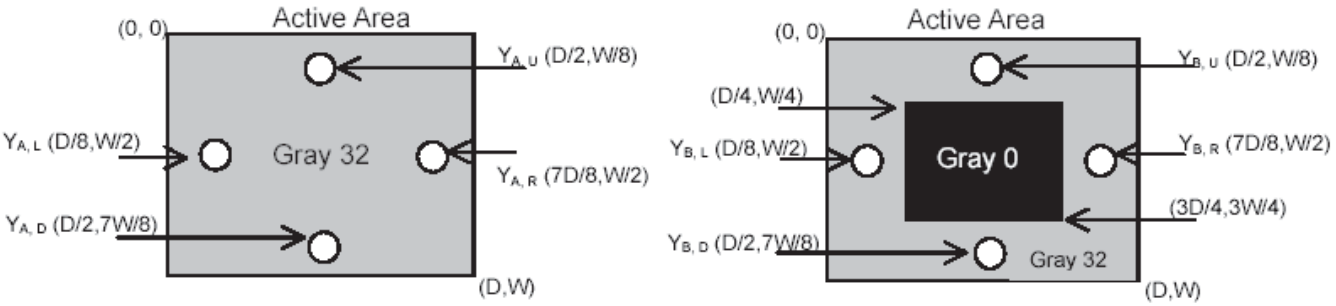
**Note 7**： Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Where

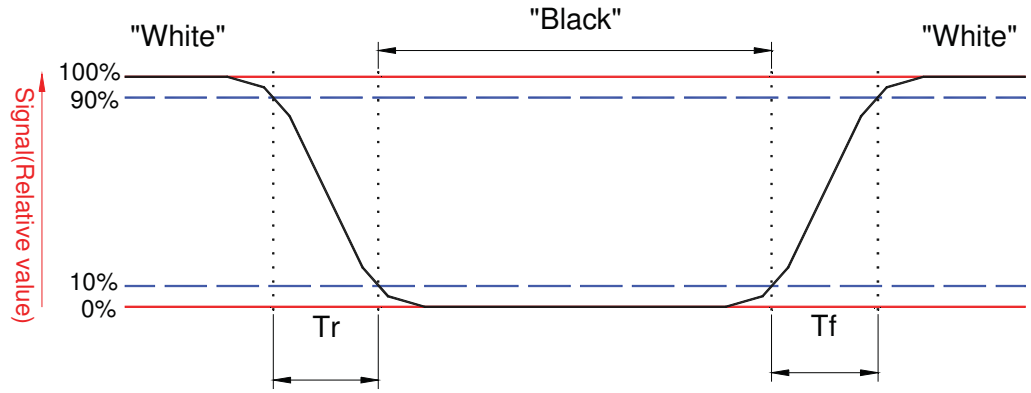
$Y_A$ = Luminance of measured location without gray level 0 pattern ($cd/m^2$)

$Y_B$ = Luminance of measured location with gray level 0 pattern (cd/m2)



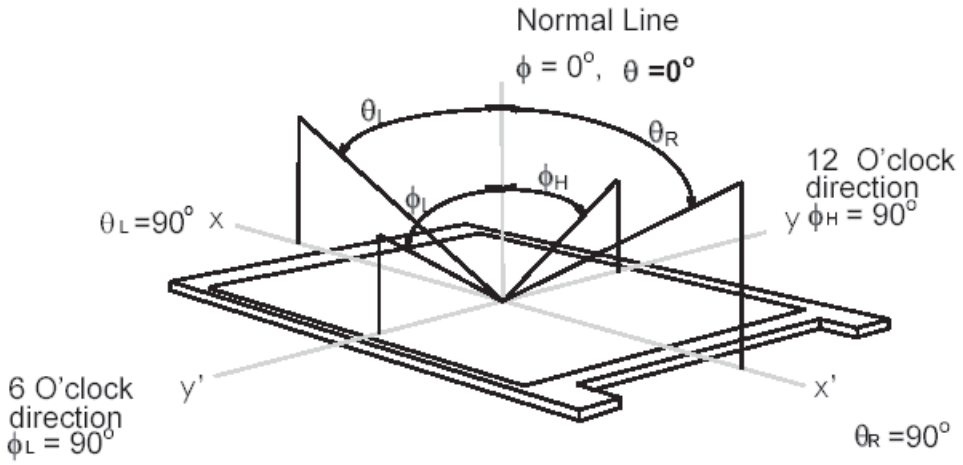

**Note 8**: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



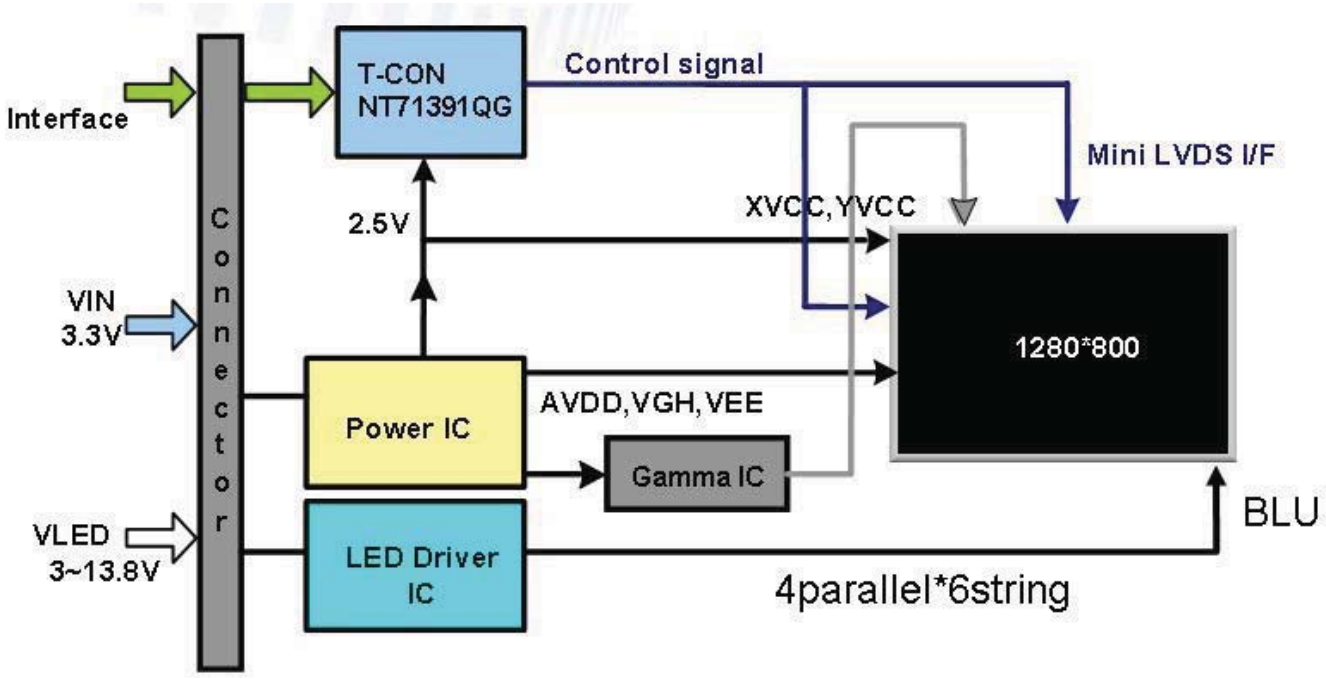
**Note 9**. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD.



# 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

## 4.1 Absolute Ratings of TFT LCD Module

| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Logic/LCD Drive Voltage | Vin | -0.3 | +4.0 | [Volt] | Note 1,2 |

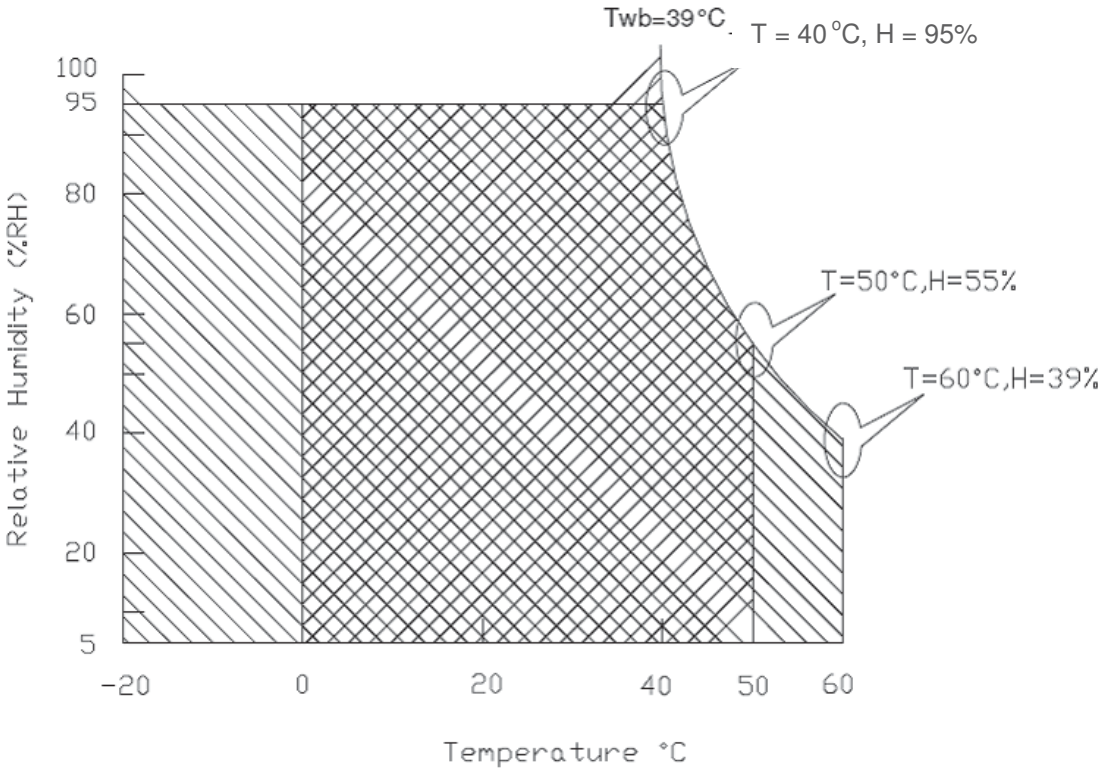
## 4.2 Absolute Ratings of Environment

| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Operating Temperature | TOP | 0 | +50 | [°C] | Note 3 |
| Operation Humidity | HOP | 0 | 90 | [%RH] | Note 3 |
| Storage Temperature | TST | -20 | +60 | [°C] | Note 3 |

Note 1: At Ta (25℃ )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).




Operating Range Storage Range +

# 5. Electrical Characteristics

## 5.1 TFT LCD Module

### 5.1.1 Power Specification

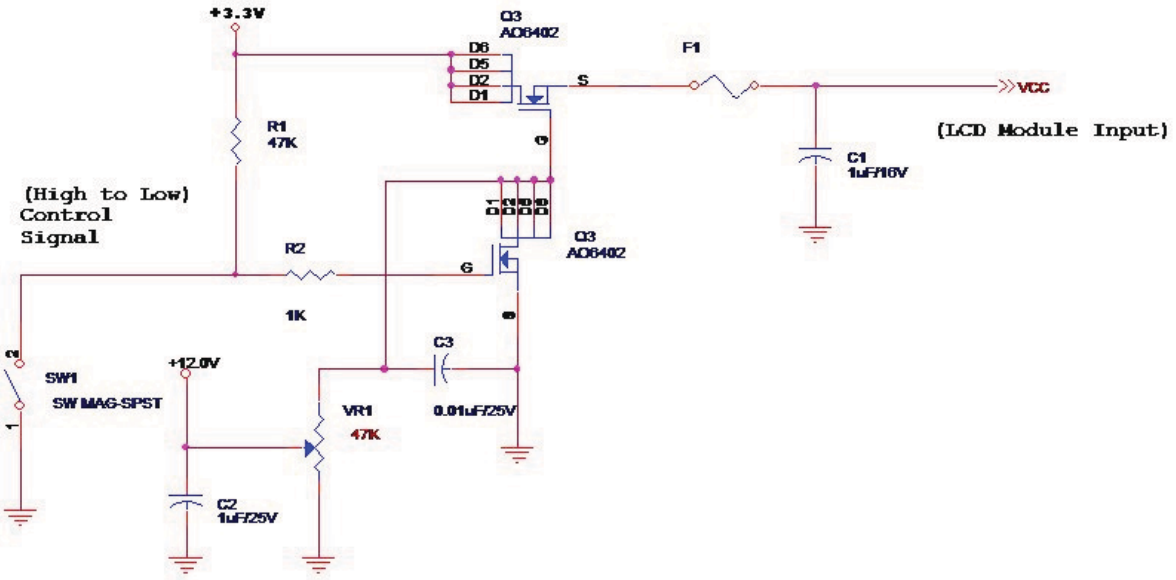
Input power specifications are as follows;

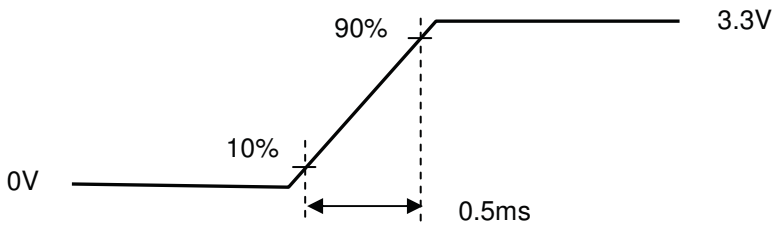
The power specification are measured under 25℃ and frame frenquency under 60Hz

| Symble | Parameter | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| VDD | Logic/LCD Drive Voltage | 3.1 | - | 3.6 | [Volt] | |
| PDD | VDD Power | - | - | 0.85 | [Watt] | Note 1 |
| IDD | IDD Current | - | - | 240 | [mA] | Note 1 |
| IRush | Inrush Current | - | - | 2000 | [mA] | Note 2 |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | - | - | 100 | [mV] p-p | |

Note 1 : Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2：Measure Condition




**Vin rising time**

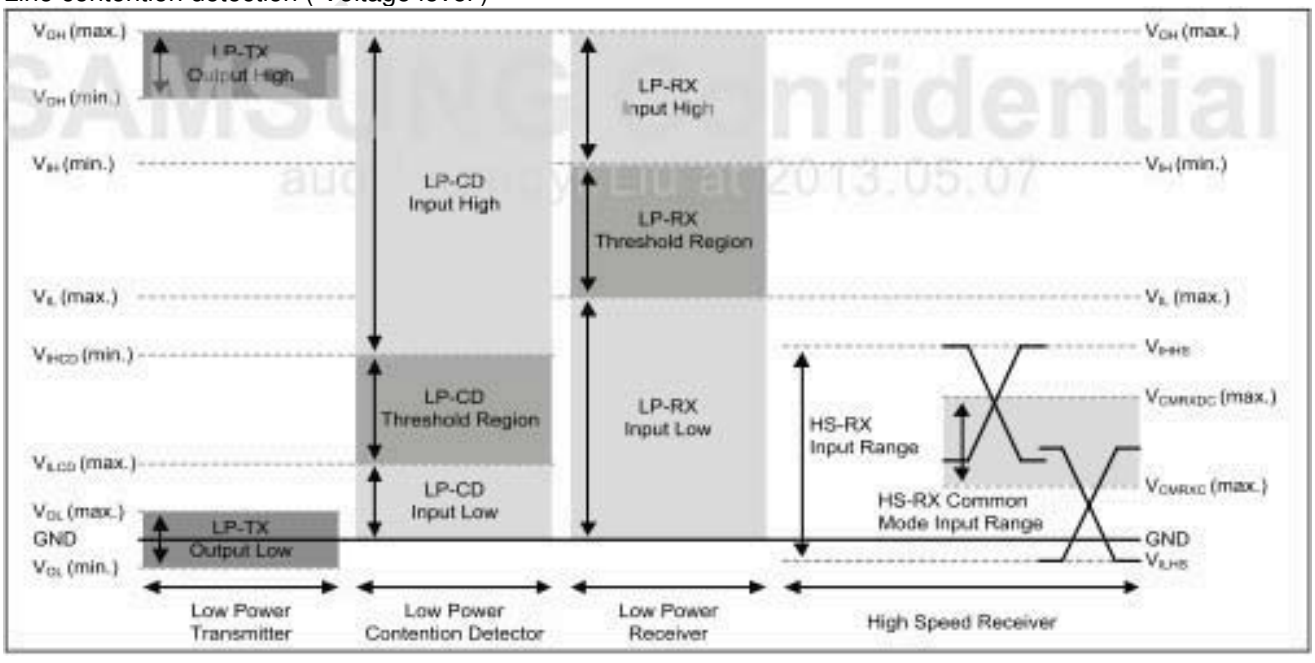
### 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

MIPI DC Characteristics are as follows;

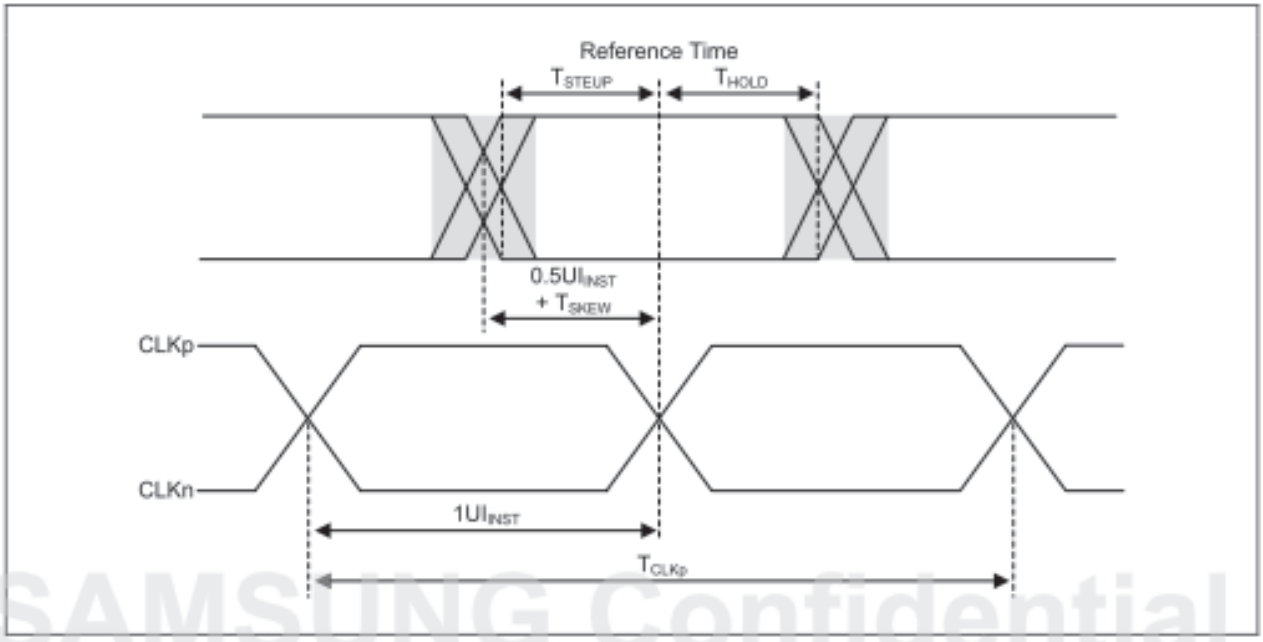
| MIPI Receiver Differential Input (DC Characteristics) | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Parameter | Min | Typ | Max | Unit |
| LP_CD | Logic 1 contention threshold | VIHCD | 450 | --- | --- | mV |
| | Logic 0 contention threshold | VILCD | --- | --- | 200 | mV |
| HS_RX | Common-mode voltage(HS Rx mode) | VCMRX(DC) | 70 | --- | 330 | mV |
| | Differential input high threshold (HS Rx mode) | VIDTH | --- | --- | 70 | mV |
| | Differential input low threshold (HS Rx mode) | VIDTL | -70 | --- | --- | mV |
| | Single-end input high voltage (HS Rx mode) | VIHHS | --- | --- | 460 | mV |
| | Single-end input low voltage (HS Rx mode) | VILHS | -40 | --- | --- | mV |
| | Single-ended threshold for HS termination enable | VTERM-EN | --- | --- | 450 | mV |
| | Differential input impedance | ZID | 80 | 100 | 125 | Ω |
| LP_RX | Logic 1 input voltage (LP Rx mode) | VIH | 880 | | | mV |
| | Logic 0 input voltage (LP Rx mode) | VIL | | | 550 | mV |
| | Input hysteresis | VHYST | 25 | --- | --- | mV |
| LP_TX | Output high level (LP Tx mode) | VOH | 1.1 | 1.2 | 1.3 | V |
| | Output low level (LP Tx mode) | VOL | -50 | | 50 | mV |
| | Output impedance of LP transmitter | ZOLP | 110 | --- | --- | Ω |

Line contention detection ( Voltage level )



MIPI High-Speed Data-clock Timing

Host sends a differential clock signal to the IC for data sampling. This signal is a DDR (half-rate) clock and has one transition per data bit time. The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in following figure.






| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{SKEW[TX]}$ | Data to Clock Skew (mesured at transmitter) | -0.15 | --- | 0.15 | --- | 1 |
| $T_{SETUP[RX]}$ | Data to Clock Setup Time (receiver) | 0.15 | --- | --- | $UI_{INST}$ | 2, 3 |
| $T_{HOLD[RX]}$ | Data to Clock Hold Time (receiver) | 0.15 | --- | --- | $UI_{INST}$ | 2, 3 |

Note:

1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of $0.3*UI_{INST}$
3. $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$ without FPCB and connector and guaranteed by design

The timing definitions are listed in below,

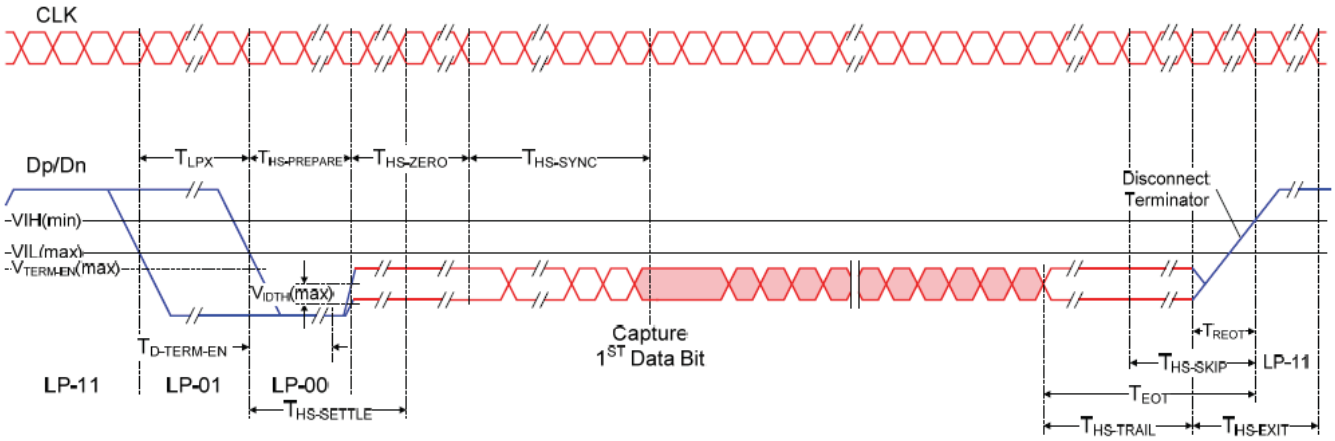
| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLK-MISS}$ | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX. | --- | --- | 60 | ns |
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL. | 60 ns + 52*UI | --- | --- | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | --- | --- | UI |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | --- | 95 | ns |
| $T_{CLK-SETTLE}$ | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE. | 95 | --- | 300 | ns |

| | | | | | |
|---|---|---|---|---|---|
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX. | Time for Dn to reach $V_{TERM-EN}$ | --- | 38 | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | --- | --- | ns |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | --- | --- | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX. | Time for Dn to reach $V_{TERM-EN}$ | --- | 35 ns + 4*UI | ns |
| $T_{EOT}$ | Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst. | --- | --- | 105 ns + 12*UI | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | --- | --- | ns |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40 ns + 4*UI | --- | 85 ns + 6*UI | ns |
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145 ns + 10*UI | --- | --- | ns |
| $T_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. | 85 ns + 6*UI | --- | 145 ns + 10*UI | ns |
| $T_{HS-SKIP}$ | Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst. | 40 | --- | 55 ns + 4*UI | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | Max(n*8 *UI, 60ns+ n*4*UI) | --- | --- | ns |
| $T_{INIT}$ | | --- | --- | --- | --- |
| $T_{LPX}$ | Transmitted length of any Low-Power state period | 50 | | | ns |
| Ratio $T_{LPX}$ | Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side | 2/3 | --- | 3/2 | |
| $T_{TA-GET}$ | Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | 5*TLPX | | | ns |
| $T_{TA-GO}$ | Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | 4*TLPX | | | ns |
| $T_{TA-SURE}$ | Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | TLPX | --- | 2*TLPX | ns |
| $T_{WAKEUP}$ | Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS | 1 | --- | --- | ms |

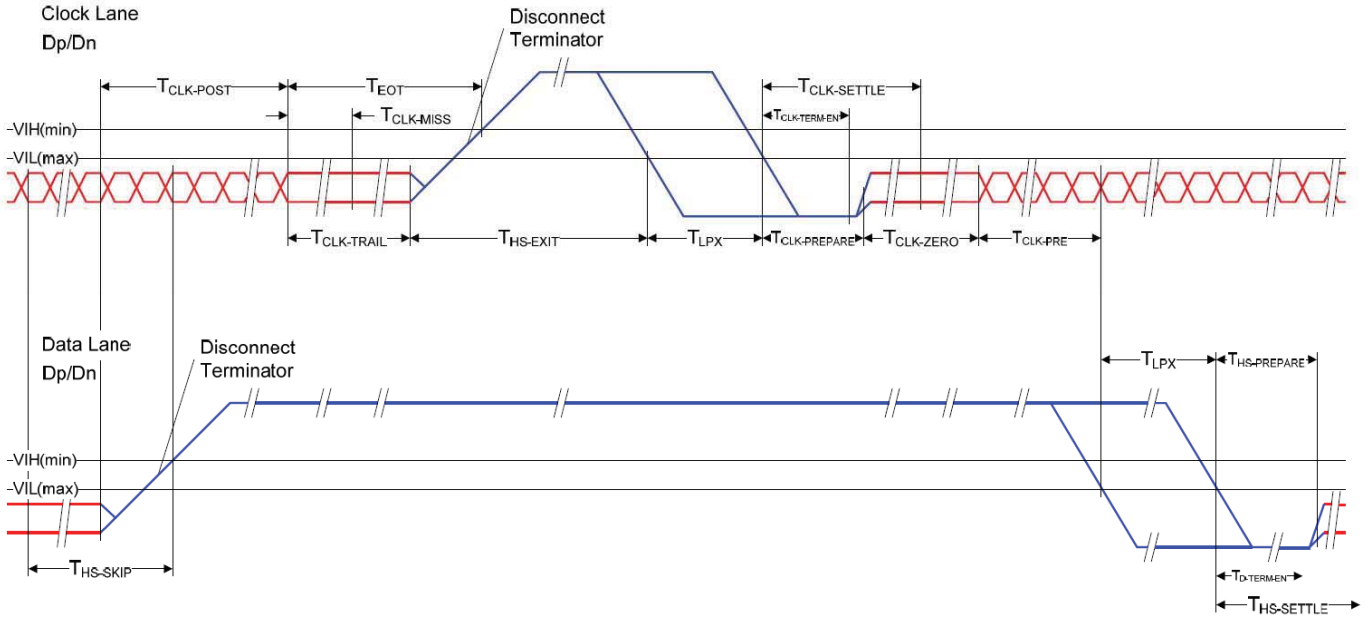
Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

## High-Speed Data Transmission in Bursts




Switching the Clock Lane between Clock Transmission and Low-Power Mode



## 5.2 Backlight Unit

### 5.2.1 LED characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| Backlight Power Consumption | PLED | - | - | 2.2 | [Watt] | (Ta=25℃), Note 1 Vin =4.2V |
| LED Life-Time | N/A | 15,000 | - | - | Hour | (Ta=25℃), Note 2 $I_F$=20 mA |

**Note 1:** Calculator value for reference $P_{LED}$ = $V_F$ (Normal Distribution) * $I_F$ (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

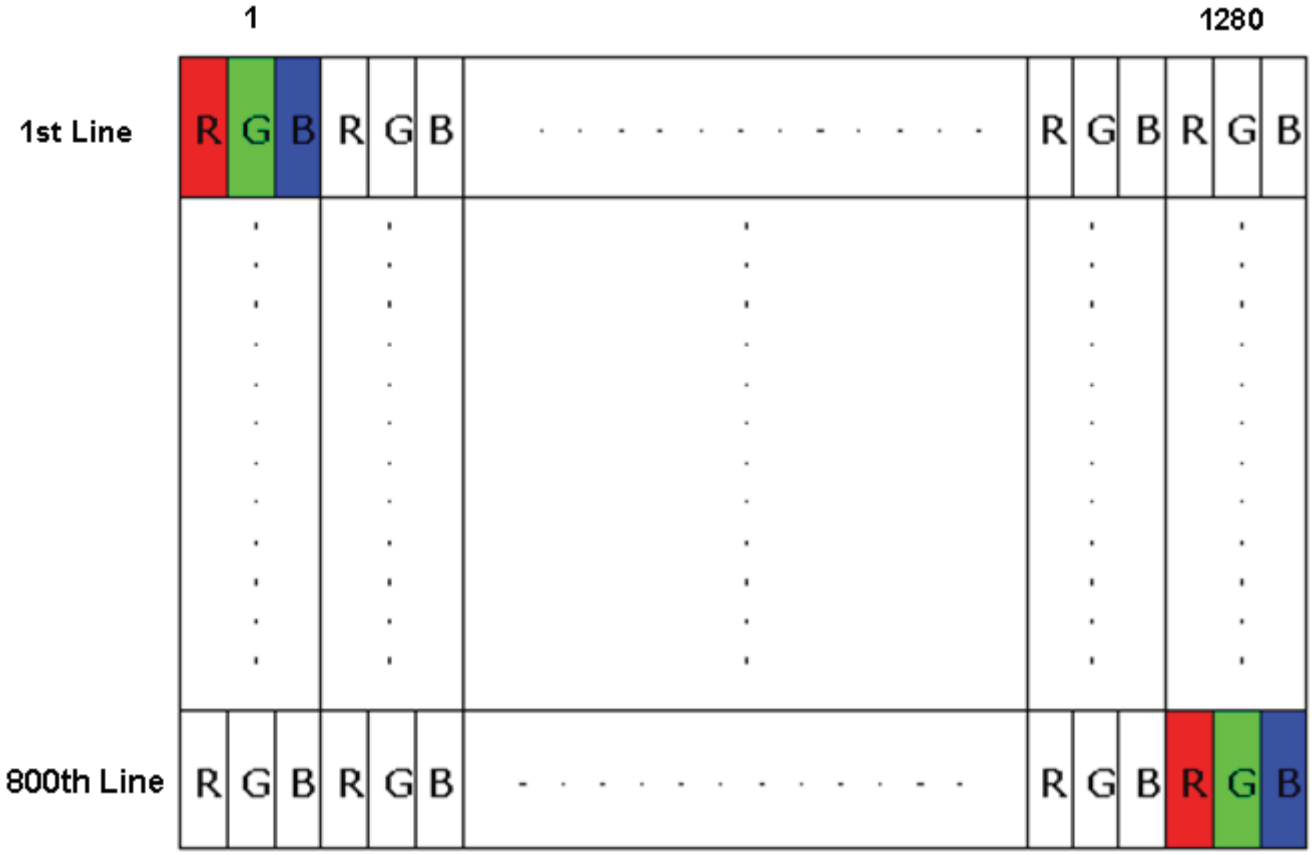
### 5.2.2 Backlight input signal characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Remark |
|---|---|---|---|---|---|---|
| LED Power Supply | VLED | 3 | 5 | 13.8 | [Volt] | Define as Connector Interface (Ta=25℃) |
| LED Enable Input High Level | LED_EN | 2.4 | - | 5.0 | [Volt] | |
| LED Enable Input Low Level | | - | - | 0.8 | [Volt] | |
| PWM Logic Input High Level | LED_PWM | 2.4 | - | 5.0 | [Volt] | |
| PWM Logic Input Low Level | | - | - | 0.8 | [Volt] | |
| PWM Input Frequency | FPWM | 700 | 1K | 2K | Hz | |
| PWM Duty Ratio | Duty | 1 | -- | 100 | % | |

# 6. Signal Interface Characteristic

## 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



## 6.2 Integration Interface Requirement

### 6.2.1 MIPI Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation | For Signal Connector |
|---|---|
| Manufacturer | HIROSE |
| Type / Part Number | FH34SJ-34S-0.5SH(50) |
| Mating Housing/Part Number | FPC Cable |

### 6.2.2 MIPI Pin Assignment

MIPI is a differential signal technology for LCD interface and high speed data transfer device.

| No. | Pin Name | Description |
|---|---|---|
| 1 | VDD | DC-DC circuit supply voltage (3.1V~3.6V) |
| 2 | VDD | DC-DC circuit supply voltage (3.1V~3.6V) |
| 3 | NC | Not Connection |
| 4 | LED_EN | LED driver Enable Input (VIH=1.8V) |
| 5 | LED_PWM | Backlight LED driver PWM Input (VIH=1.8V) |
| 6 | EDID_SDA | EDID Data Input (VIH=VDD*0.7) |
| 7 | EDID_SCL | EDID Clock Input (VIH=VDD*0.7) |
| 8 | NC | Not Connection |
| 9 | GND | Ground |
| 10 | DSI_D2P/Rx-IN2P | MIPI data pair 2 positive signal |
| 11 | DSI_D2N/Rx-IN2N | MIPI data pair 2 negative signal |
| 12 | GND | Ground |
| 13 | DSI_D1P/Rx-IN1P | MIPI data pair 1 positive signal |
| 14 | DSI_D1N/Rx-IN1N | MIPI data pair 1 negative signal |
| 15 | GND | Ground |
| 16 | DSI_CLKP/Rx-CLKP | MIPI Clock positive signal |
| 17 | DSI_CLKN/Rx-CLKN | MIPI Clock negative signal |
| 18 | GND | Ground |
| 19 | DSI_D0P/Rx-IN0P | MIPI data pair 0 positive signal |
| 20 | DSI_D0N/Rx-IN0N | MIPI data pair 0 negative signal |
| 21 | GND | Ground |
| 22 | DSI_D3P/Rx-IN3P | MIPI data pair 3 positive signal |
| 23 | DSI_D3N/Rx-IN3N | MIPI data pair 3 negative signal |

| | | |
|---|---|---|
| 24 | GND | Ground |
| 25 | GND | Ground |
| 26 | GND | Ground |
| 27 | GND | Ground |
| 28 | GND | Ground |
| 29 | Aging | Aging Mode Power Supply (AUO only) |
| 30 | NC | Not Connection |
| 31 | LED+ | LED Power Supply (3V – 13.8V) |
| 32 | LED+ | LED Power Supply (3V – 13.8V) |
| 33 | LED+ | LED Power Supply (3V – 13.8V) |
| 34 | LED+ | LED Power Supply (3V – 13.8V) |

**PS. EDID_SDA/SCL must be GND except the period of EDID reading**

## 6.3 MIPI Interface Timing

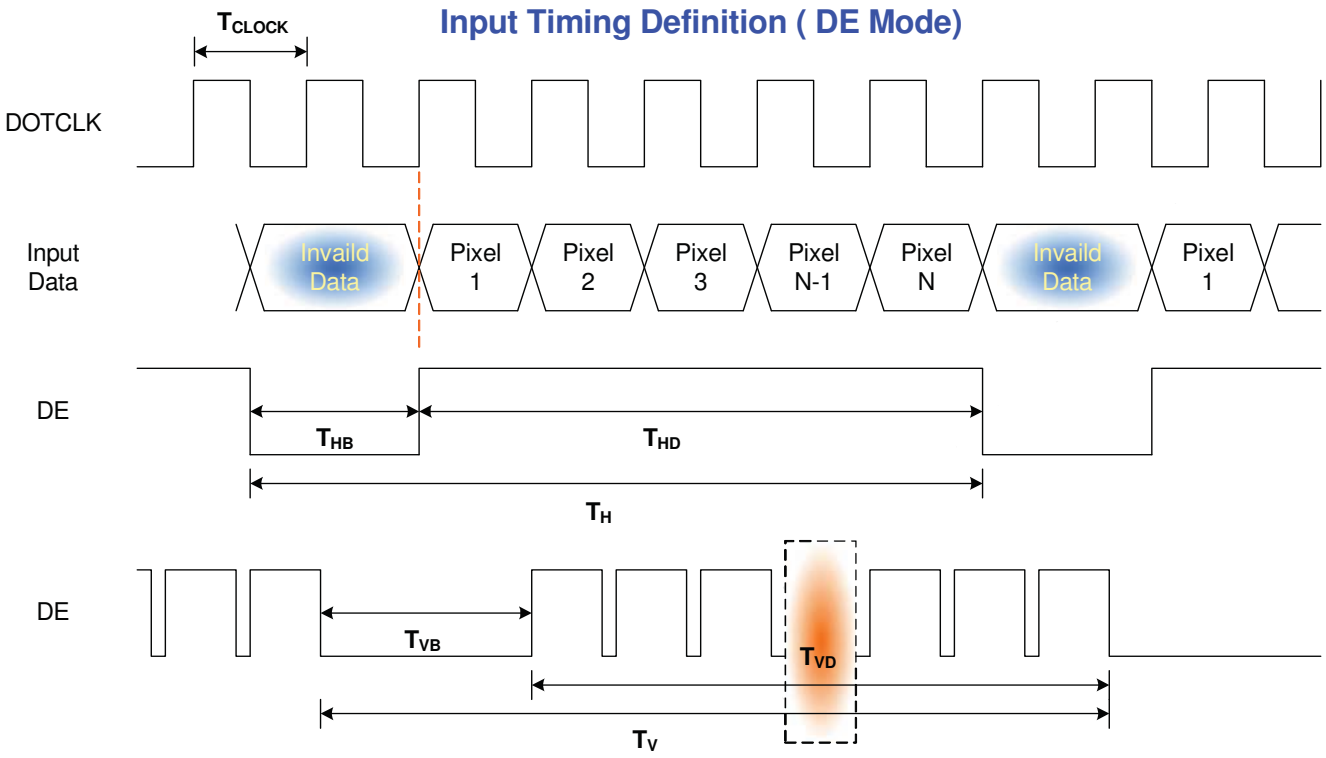
### 6.3.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Frame Rate | | --- | --- | 60 | --- | Hz |
| Clock frequency | | 1/ $T_{Clock}$ | 64 | 72.46 | 85 | MHz |
| Vertical Section | Period | $T_V$ | 808 | 816 | 1023 | $T_{Line}$ |
| | Active | $T_{VD}$ | 800 | | | |
| | Blanking | $T_{VB}$ | 8 | 16 | 223 | |
| Horizontal Section | Period | $T_H$ | 1340 | 1480 | 2047 | $T_{Clock}$ |
| | Active | $T_{HD}$ | 1280 | | | |
| | Blanking | $T_{HB}$ | 60 | 200 | 767 | |

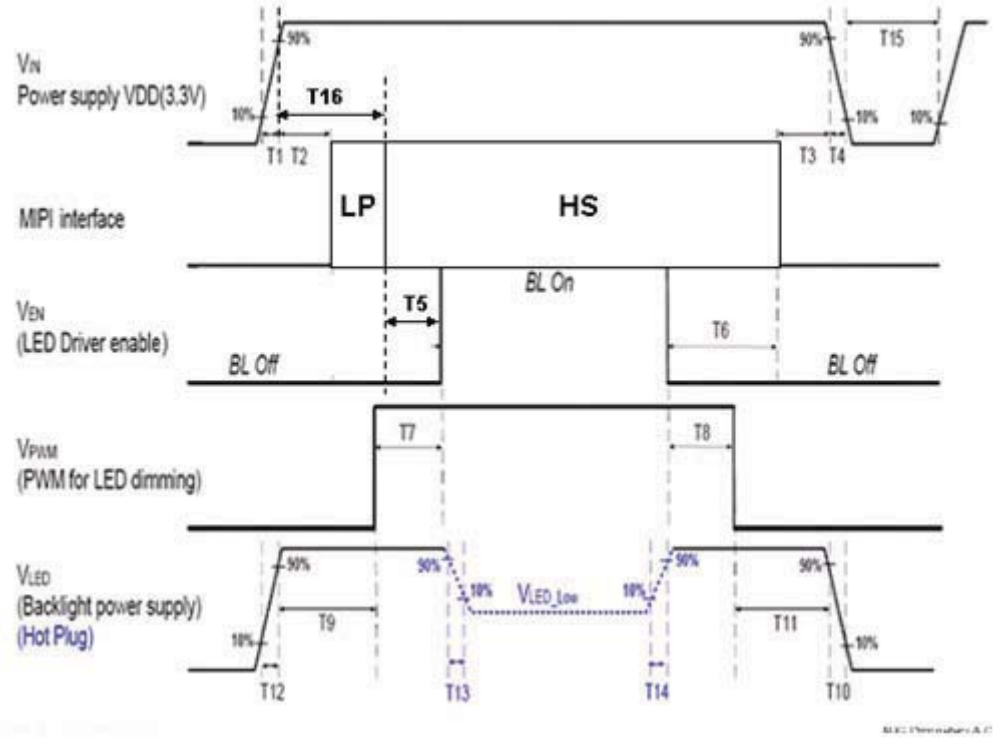
Note : DE mode only

### 6.3.2 Timing diagram



## 6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off




| Parameter | Value | | Units |
|---|---|---|---|
| | Min. | Max. | |
| T1 | 0.5 | 10 | ms |
| T2 | 30 | | |
| T3 | 50 | - | |
| T4 | 0.5 | 10 | |
| T5 | 20 | - | |
| T6 | 20 | - | |
| T7 | 10 | - | |
| T8 | 10 | | |
| T9 | 10 | | |
| T10 | 0.5 | 10 | |
| T11 | 10 | | |
| T12 | 0.5 | 10 | |
| T13 | K | | |
| T14 | K | | |
| T15 | 500 | | |
| T16 | 90 | | |

**# Noraml : K=1, No Flash: K=5xTpwm**
*** Tpwm =1/PWM Frequecny**

# 7. Panel Reliability Test

## 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

## 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

## 7.3 Reliability Test

| Items | Required Condition | Note |
|---|---|---|
| Temperature Humidity Bias | Ta= 40℃, 90%RH, 300h | |
| High Temperature Operation | Ta= 50℃, Dry, 300h | |
| Low Temperature Operation | Ta= 0℃, 300h | |
| High Temperature Storage | Ta= 60℃, 300h | |
| Low Temperature Storage | Ta= -20℃, 300h | |
| Thermal Shock Test | Ta=-20℃to 60℃, Duration at 30 min, 100 cycles | |
| ESD | Contact : ±8 KV<br>Air : ±15 KV | Note 1 |

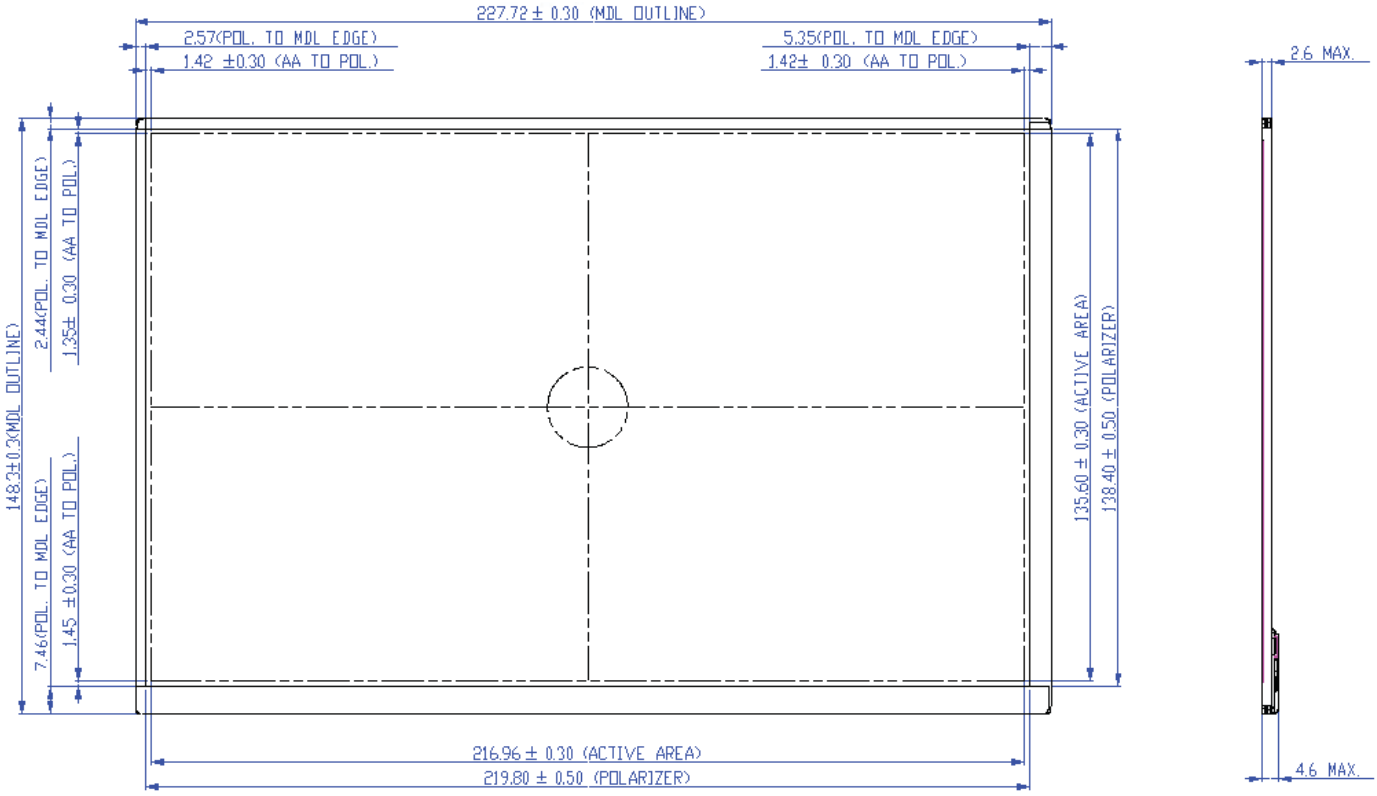
**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

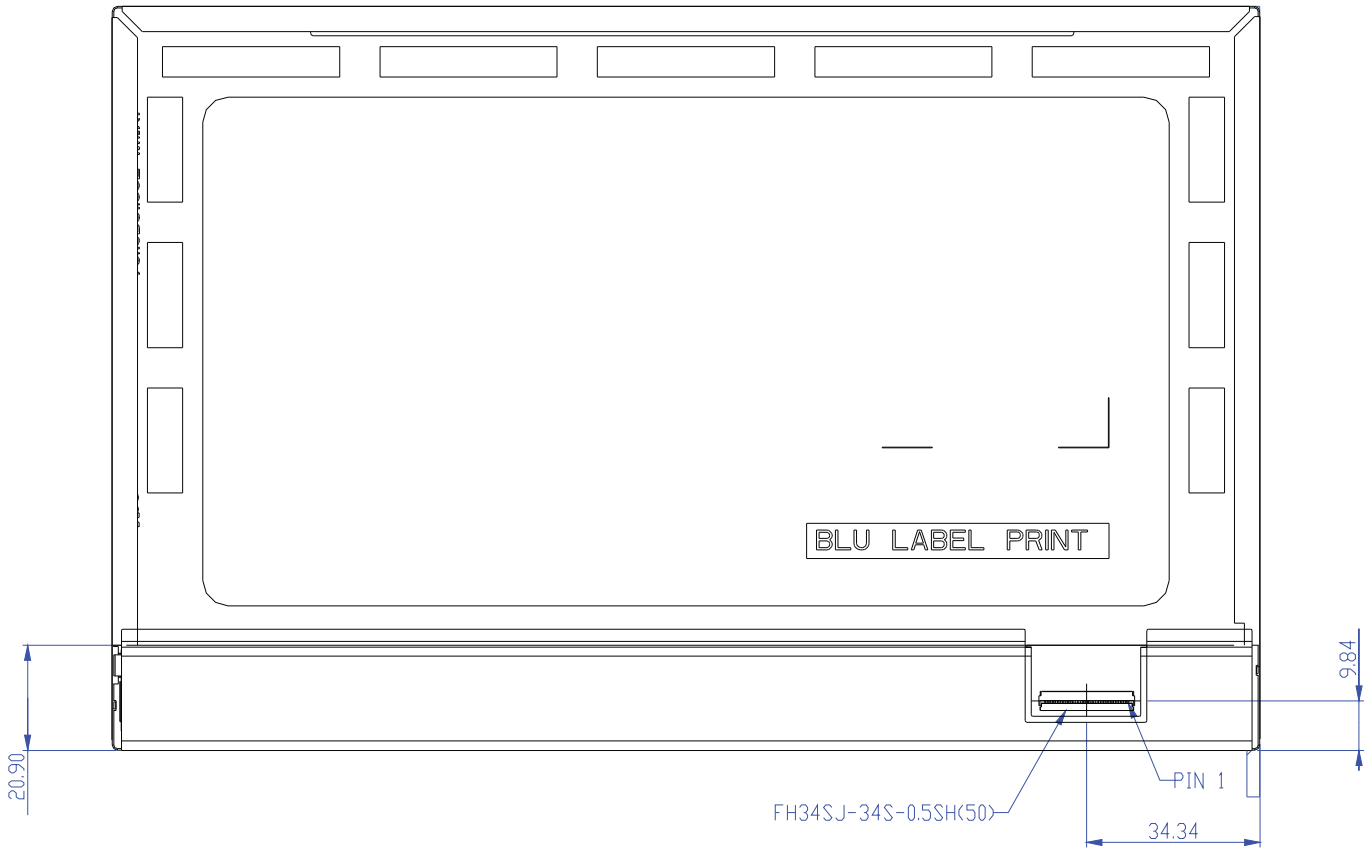
**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

# 8. Mechanical Characteristics

## 8.1 Standard Front View



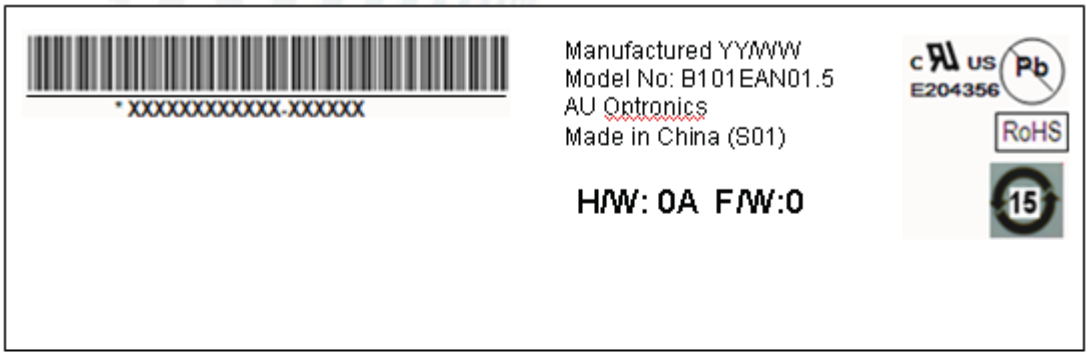
## 8.2 Standard Rear View

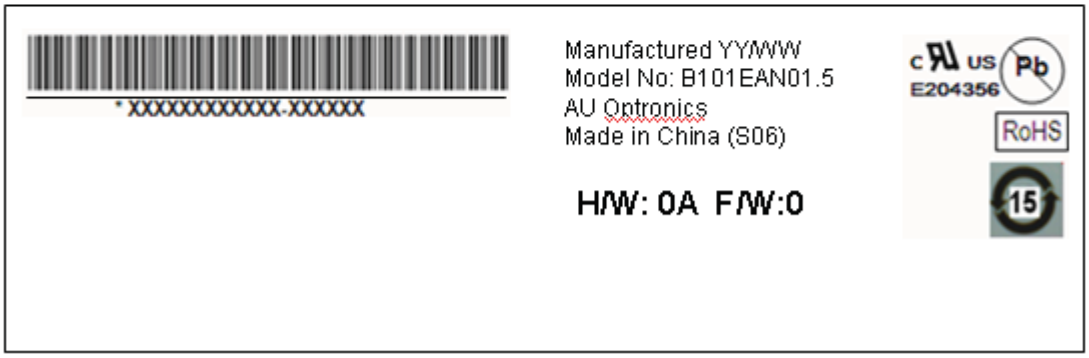



**Note : Back Bezel (Material : SUS 304 ; 0.2mm)**

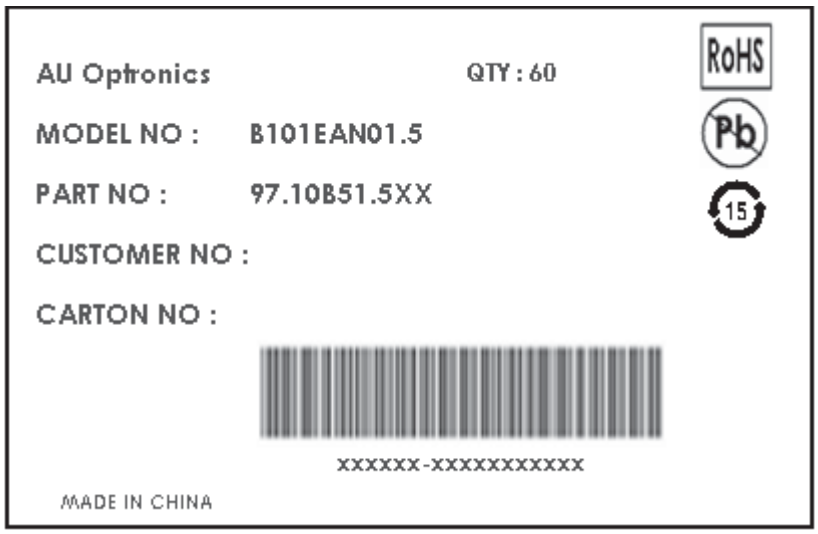
# 9. Shipping and Package

## 9.1 Shipping Label Format




## 9.2 Carton Label Format



# 10. Appendix

## 10.1 EDID Description

### B101EAN01 5 EDID Code

| Address | FUNCTION | Value | Value | Value | Note |
|---|---|---|---|---|---|
| HEX | | HEX | BIN | DEC | |
| 00 | Header | 00 | 00000000 | 0 | |
| 01 | | FF | 11111111 | 255 | |
| 02 | | FF | 11111111 | 255 | |
| 03 | | FF | 11111111 | 255 | |
| 04 | | FF | 11111111 | 255 | |
| 05 | | FF | 11111111 | 255 | |
| 06 | | FF | 11111111 | 255 | |
| 07 | | 00 | 00000000 | 0 | |
| 08 | EISA Manuf. Code LSB | 06 | 00000110 | 6 | |
| 09 | Compressed ASCII | AF | 10101111 | 175 | |
| 0A | Product Code | D4 | 11010100 | 212 | |
| 0B | hex, LSB first | 15 | 00010101 | 21 | |
| 0C | 32-bit ser # | 00 | 00000000 | 0 | |
| 0D | | 00 | 00000000 | 0 | |
| 0E | | 00 | 00000000 | 0 | |
| 0F | | 00 | 00000000 | 0 | |
| 10 | Week of manufacture | 23 | 00100011 | 35 | |
| 11 | Year of manufacture | 17 | 00010111 | 23 | |
| 12 | EDID Structure Ver. | 01 | 00000001 | 1 | |
| 13 | EDID revision # | 04 | 00000100 | 4 | |
| 14 | **Video input def.** *(digital I/P, non-TMDS, CRGB)* | A0 | 10100000 | 160 | |
| 15 | **Max H image size** *(rounded to cm)* | 16 | 00010110 | 22 | |
| 16 | **Max V image size** *(rounded to cm)* | 0E | 00001110 | 14 | |
| 17 | **Display Gamma** *(=(gamma*100)-100)* | 78 | 01111000 | 120 | |
| 18 | **Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)* | 02 | 00000010 | 2 | |
| 19 | Red/green low bits **(Lower 2:2:2:2 bits)** | 99 | 10011001 | 153 | |
| 1A | Blue/white low bits **(Lower 2:2:2:2 bits)** | 85 | 10000101 | 133 | |
| 1B | Red x **(Upper 8 bits)** | 95 | 10010101 | 149 | |
| 1C | Red y/ highER 8 bits | 55 | 01010101 | 85 | |
| 1D | Green x | 56 | 01010110 | 86 | |
| 1E | Green y | 92 | 10010010 | 146 | |
| 1F | Blue x | 28 | 00101000 | 40 | |
| 20 | Blue y | 22 | 00100010 | 34 | |
| 21 | White x | 50 | 01010000 | 80 | |
| 22 | White y | 54 | 01010100 | 84 | |
| 23 | Established timing 1 | 00 | 00000000 | 0 | |
| 24 | Established timing 2 | 00 | 00000000 | 0 | |
| 25 | Established timing 3 | 00 | 00000000 | 0 | |
| 26 | Standard timing #1 | 01 | 00000001 | 1 | |

| | | | | | |
|---|---|---|---|---|---|
| **27** | | 01 | 00000001 | 1 | |
| **28** | Standard timing #2 | 01 | 00000001 | 1 | |
| **29** | | 01 | 00000001 | 1 | |
| **2A** | Standard timing #3 | 01 | 00000001 | 1 | |
| **2B** | | 01 | 00000001 | 1 | |
| **2C** | Standard timing #4 | 01 | 00000001 | 1 | |
| **2D** | | 01 | 00000001 | 1 | |
| **2E** | Standard timing #5 | 01 | 00000001 | 1 | |
| **2F** | | 01 | 00000001 | 1 | |
| **30** | Standard timing #6 | 01 | 00000001 | 1 | |
| **31** | | 01 | 00000001 | 1 | |
| **32** | Standard timing #7 | 01 | 00000001 | 1 | |
| **33** | | 01 | 00000001 | 1 | |
| **34** | Standard timing #8 | 01 | 00000001 | 1 | |
| **35** | | 01 | 00000001 | 1 | |
| **36** | Pixel Clock/10000 LSB | 52 | 01010010 | 82 | |
| **37** | Pixel Clock/10000 USB | 1C | 00011100 | 28 | |
| **38** | Horz active **Lower 8bits** | 00 | 00000000 | 0 | |
| **39** | Horz blanking **Lower 8bits** | C8 | 11001000 | 200 | |
| **3A** | HorzAct:HorzBlnk **Upper 4:4 bits** | 50 | 01010000 | 80 | |
| **3B** | Vertical Active **Lower 8bits** | 20 | 00100000 | 32 | |
| **3C** | Vertical Blanking **Lower 8bits** | 10 | 00010000 | 16 | |
| **3D** | Vert Act : Vertical Blanking **(upper 4:4 bit)** | 30 | 00110000 | 48 | |
| **3E** | HorzSync. Offset | 93 | 10010011 | 147 | |
| **3F** | HorzSync.Width | 20 | 00100000 | 32 | |
| **40** | VertSync.Offset : VertSync.Width | 44 | 01000100 | 68 | |
| **41** | Horz&Vert Sync Offset/Width **Upper 2bits** | 00 | 00000000 | 0 | |
| **42** | Horizontal Image Size **Lower 8bits** | D8 | 11011000 | 216 | |
| **43** | Vertical Image Size **Lower 8bits** | 87 | 10000111 | 135 | |
| **44** | Horizontal & Vertical Image Size **(upper 4:4 bits)** | 00 | 00000000 | 0 | |
| **45** | Horizontal Border *(zero for internal LCD)* | 00 | 00000000 | 0 | |
| **46** | Vertical Border *(zero for internal LCD)* | 00 | 00000000 | 0 | |
| **47** | Signal *(non-intr, norm, no stero, sep sync, neg pol)* | 18 | 00011000 | 24 | |
| **48** | Detailed timing/monitor | 00 | 00000000 | 0 | |
| **49** | descriptor #2 | 00 | 00000000 | 0 | |
| **4A** | | 00 | 00000000 | 0 | |
| **4B** | | 0F | 00001111 | 15 | |
| **4C** | | 00 | 00000000 | 0 | |
| **4D** | | 00 | 00000000 | 0 | |
| **4E** | | 00 | 00000000 | 0 | |
| **4F** | | 00 | 00000000 | 0 | |
| **50** | | 00 | 00000000 | 0 | |
| **51** | | 00 | 00000000 | 0 | |
| **52** | | 00 | 00000000 | 0 | |

| | | | | | |
|---|---|---|---|---|---|
| **53** | | 00 | 00000000 | 0 | |
| **54** | | 00 | 00000000 | 0 | |
| **55** | | 00 | 00000000 | 0 | |
| **56** | | 00 | 00000000 | 0 | |
| **57** | | 00 | 00000000 | 0 | |
| **58** | | 00 | 00000000 | 0 | |
| **59** | | 20 | 00100000 | 32 | |
| **5A** | Detailed timing/monitor | 00 | 00000000 | 0 | |
| **5B** | descriptor #3 | 00 | 00000000 | 0 | |
| **5C** | | 00 | 00000000 | 0 | |
| **5D** | | FE | 11111110 | 254 | |
| **5E** | | 00 | 00000000 | 0 | |
| **5F** | Manufacture | 41 | 01000001 | 65 | A |
| **60** | Manufacture | 55 | 01010101 | 85 | U |
| **61** | Manufacture | 4F | 01001111 | 79 | O |
| **62** | | 0A | 00001010 | 10 | |
| **63** | | 20 | 00100000 | 32 | |
| **64** | | 20 | 00100000 | 32 | |
| **65** | | 20 | 00100000 | 32 | |
| **66** | | 20 | 00100000 | 32 | |
| **67** | | 20 | 00100000 | 32 | |
| **68** | | 20 | 00100000 | 32 | |
| **69** | | 20 | 00100000 | 32 | |
| **6A** | | 20 | 00100000 | 32 | |
| **6B** | | 20 | 00100000 | 32 | |
| **6C** | Detailed timing/monitor | 00 | 00000000 | 0 | |
| **6D** | descriptor #4 | 00 | 00000000 | 0 | |
| **6E** | | 00 | 00000000 | 0 | |
| **6F** | | FE | 11111110 | 254 | |
| **70** | | 00 | 00000000 | 0 | |
| **71** | Manufacture P/N | 42 | 01000010 | 66 | B |
| **72** | Manufacture P/N | 31 | 00110001 | 49 | 1 |
| **73** | Manufacture P/N | 30 | 00110000 | 48 | 0 |
| **74** | Manufacture P/N | 31 | 00110001 | 49 | 1 |
| **75** | Manufacture P/N | 45 | 01000101 | 69 | E |
| **76** | Manufacture P/N | 41 | 01000001 | 65 | A |
| **77** | Manufacture P/N | 4E | 01001110 | 78 | N |
| **78** | Manufacture P/N | 30 | 00110000 | 48 | 0 |
| **79** | Manufacture P/N | 31 | 00110001 | 49 | 1 |
| **7A** | Manufacture P/N | 2E | 00101110 | 46 | . |
| **7B** | Manufacture P/N | 35 | 00110101 | 53 | 5 |
| **7C** | | 20 | 00100000 | 32 | |
| **7D** | | 0A | 00001010 | 10 | |
| **7E** | Extension Flag | 00 | 00000000 | 0 | |

| | | | | | |
|---|---|---|---|---|---|
| **7F** | Checksum | D9 | 11011001 | 217 | |
| | | | SUM | 6400 | |
| | | | SUM to HEX | 1900 | |