( ) Preliminary Specifications
(V) Final Specifications

Module	**10.1”(10.01”) WXGA 16:10 Color TFT-LCD**
Model Name	**B101EAN01.8 (H/W: 0A)**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
	MM/DD/YYYY	YW Lee	03/31/2015
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Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.0 2015/03/06	All	First Edition for Customer		
0.1 2015/03/20	25 26		Modify 8.1 LCM Outline Dimension	
0.2 2015/03/31	29		Modify 10. EDID Code	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101EAN01.8 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WXGA, 1280(H) x800(V) screen and 16.7M colors (RGB 6-bits data driver with Hi-FRC). All input signals are eDP 1.2 interface compatible.

B101EAN01.8 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	255.85 (10.07W")			
Active Area	[mm]	216.96(H) x 135.6(V)			
Pixels H x V		1280 x 3(RGB) x 800			
Pixel Pitch	[mm]	0.1695 X 0.1695			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
White Luminance (I_{LED}=21mA) **(Note: ILED is LED current)**	[cd/m^2]	250 typ. (5 points average) 213 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	30 Typ.			
Nominal Input Voltage VDD	[Volt]	3.3V			
Power Consumption	[Watt]	2.7W Max.			
Weight	[Grams]	145g Max			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	227.22	227.72	228.22
		Width	147.3	147.8	148.3
		Thickness Panel Side			2.6
		Thickness PCBA Side			4.4
Electrical Interface		1 Lane eDP 1.2			
Glass Thickness	[mm]	0.25/0.25			
Surface Treatment		Glare, Hardness 3H			
Support Color		16.7M colors			

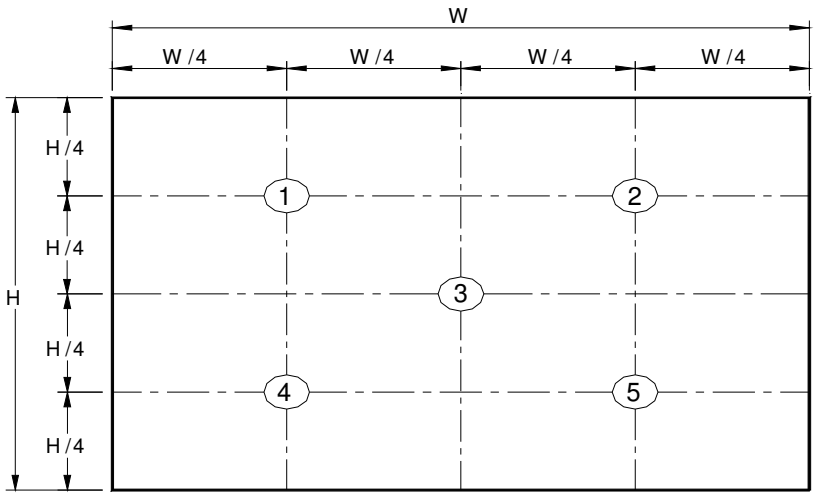
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

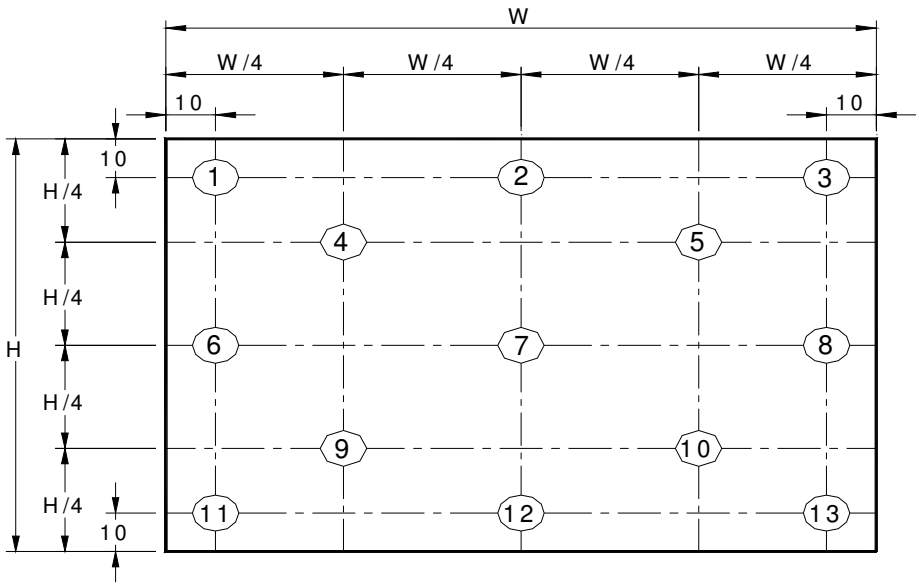
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=21mA			5 points average	213	250	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10 (Left)	80	85	-	degree	4, 9
		θ_L		80	85	-		
		ϕ_H	Vertical (Upper) CR = 10 (Lower)	80	85	-		
		ϕ_L		80	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR		600	800	-		4, 6
Cross talk		%				2		4, 7
Response Time		T_{RT}	Rising + Falling	-	30	38	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931		TBD			4
		Ry			TBD			
	Green	Gx			TBD			
		Gy			TBD			
	Blue	Bx			TBD			
		By			TBD			
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



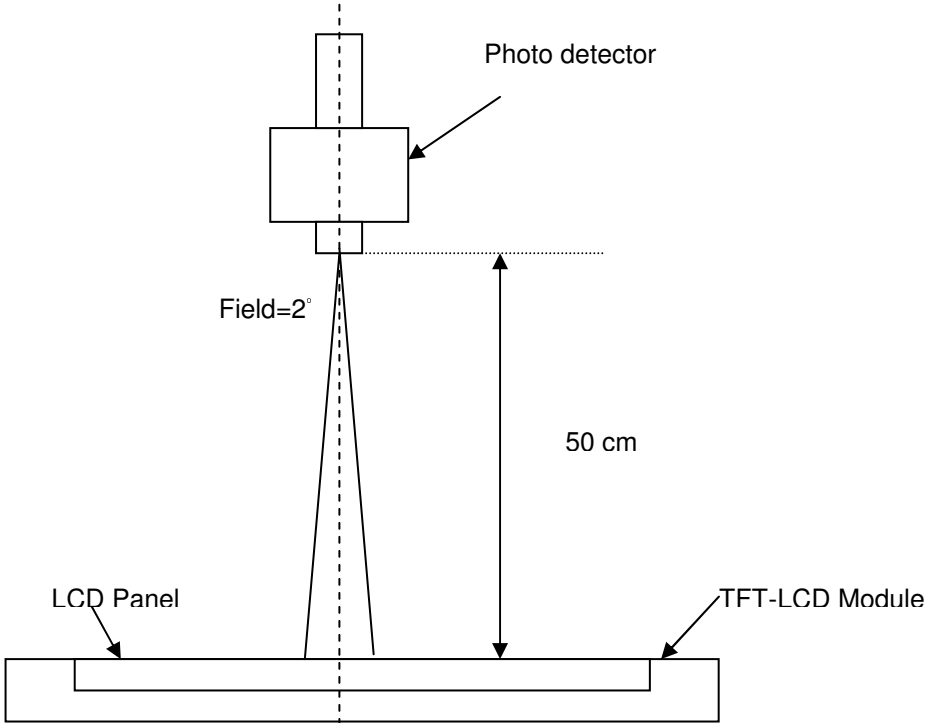
Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

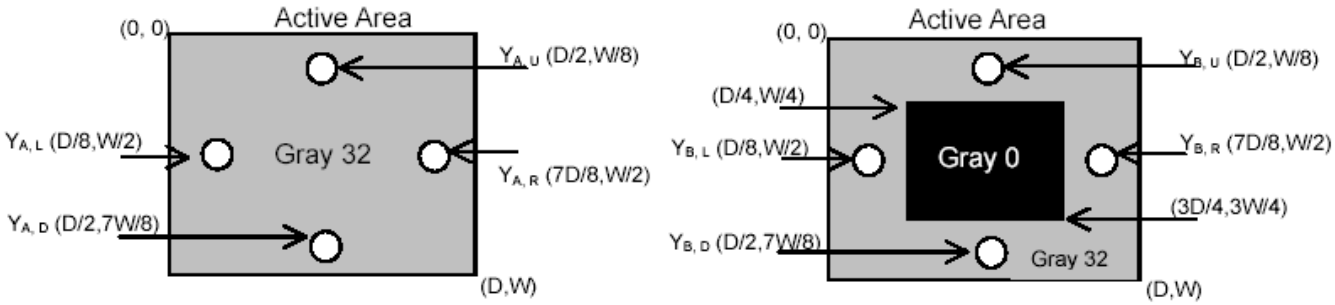
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

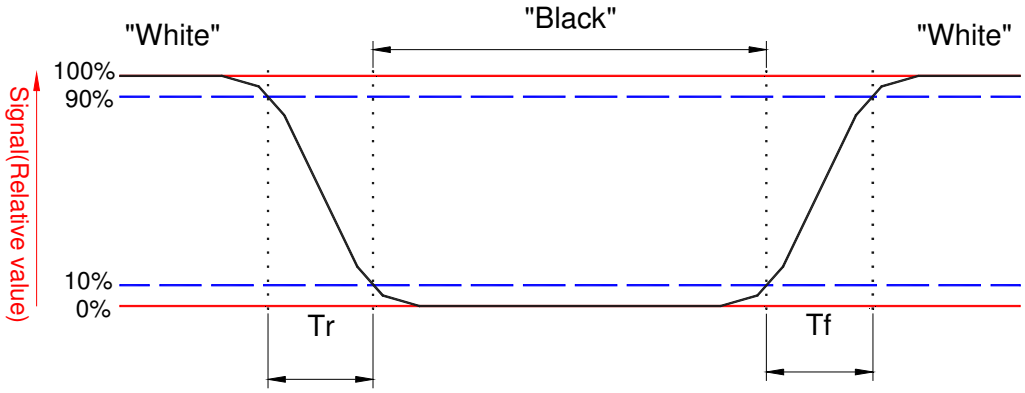
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



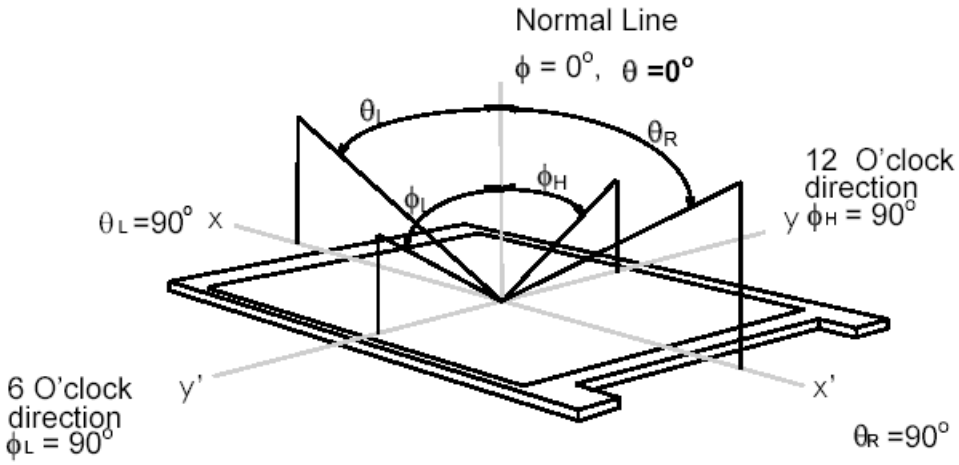
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



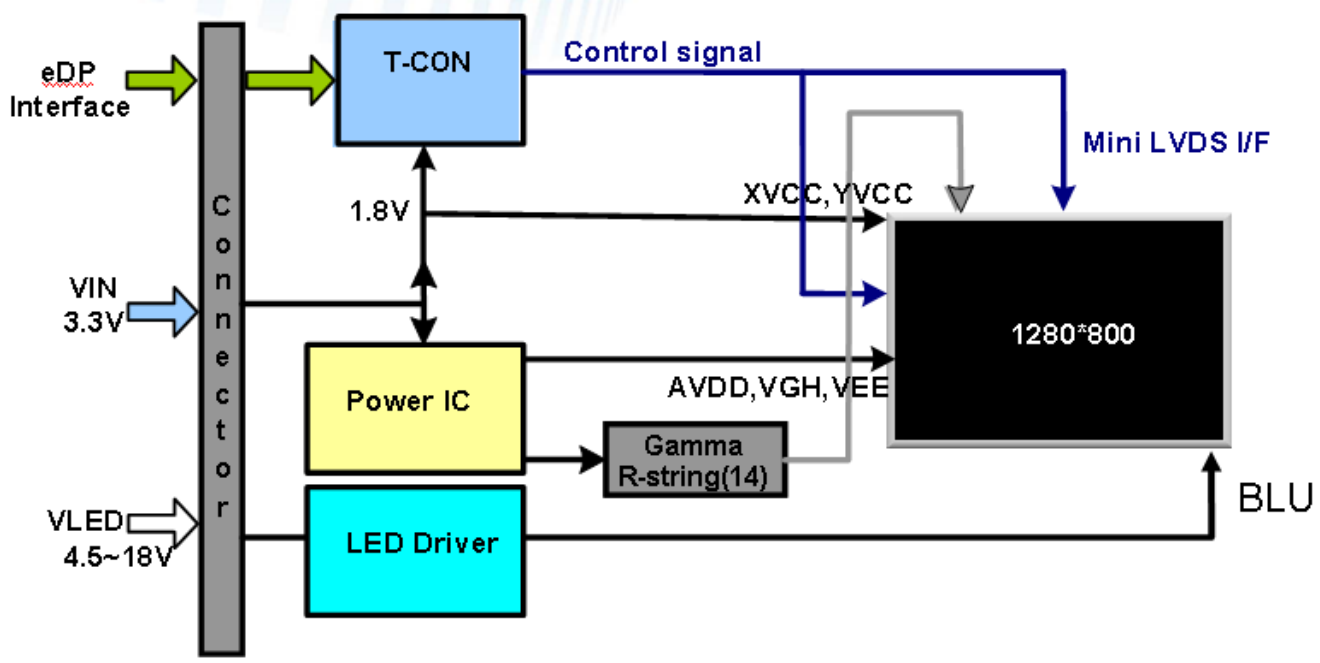
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

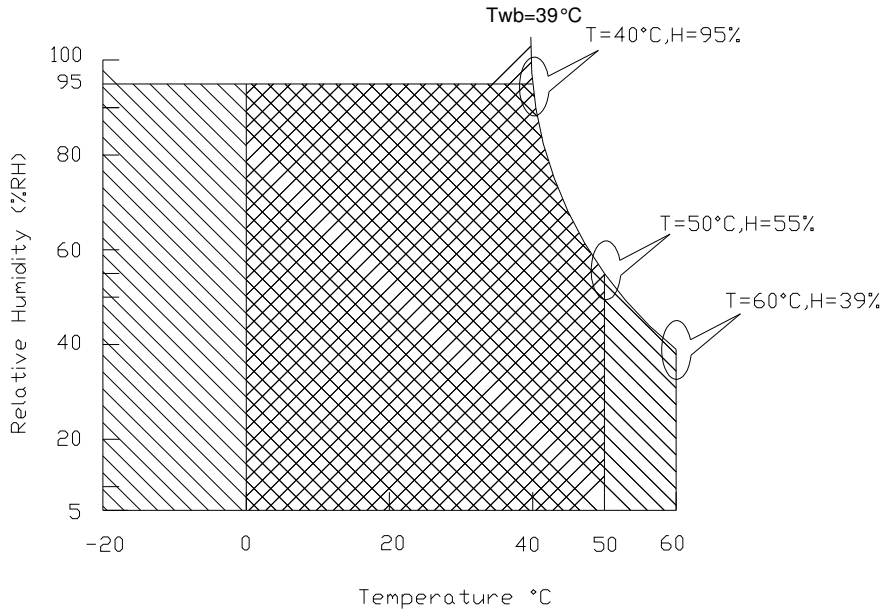
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

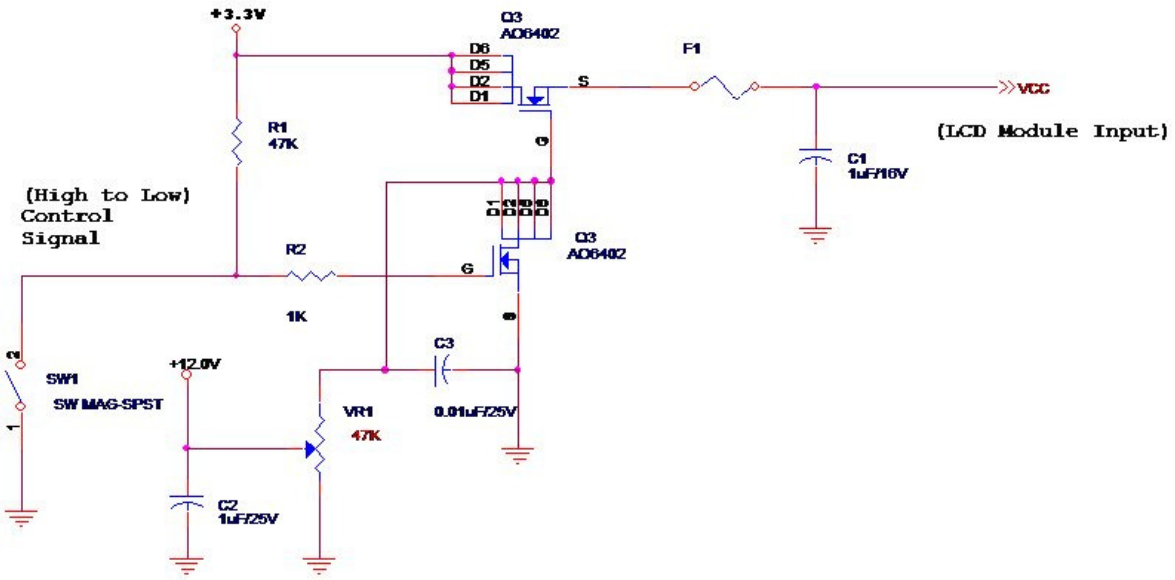
Input power specifications are as follows;

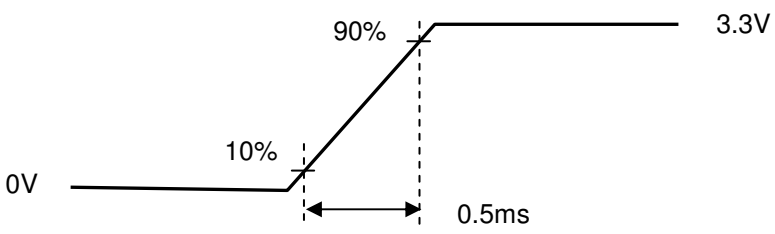
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	242	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. (P_{max}=$V_{3.3}$ x I_{black})

Note 2 : Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

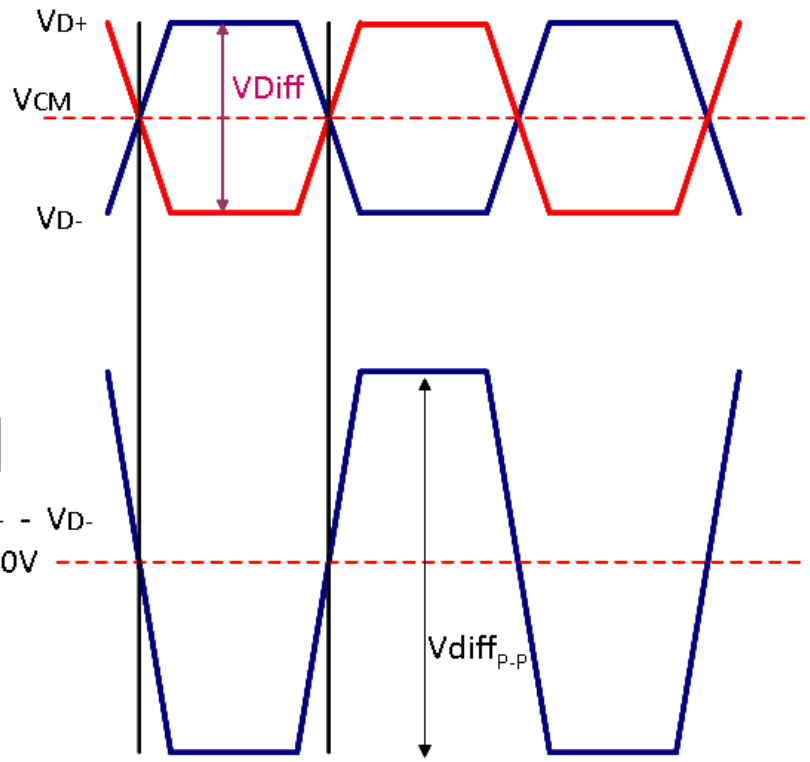
Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

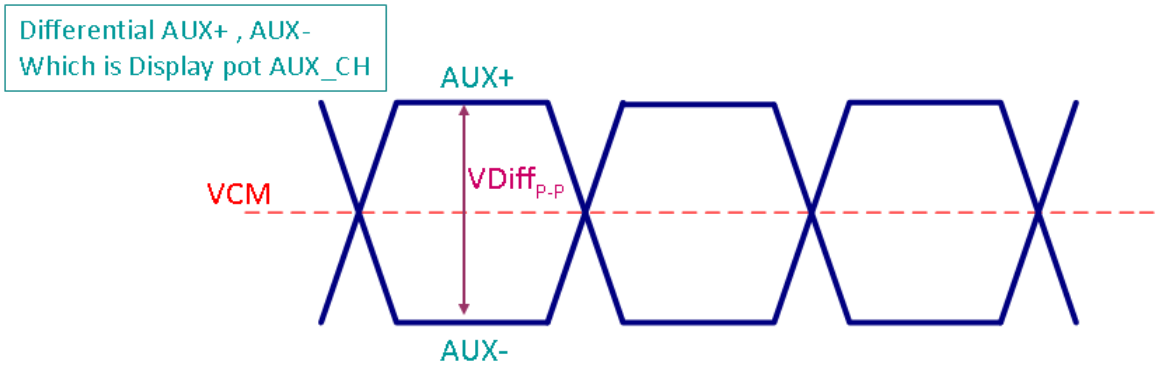


$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$

Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard

Display Port AUX_CH signal:



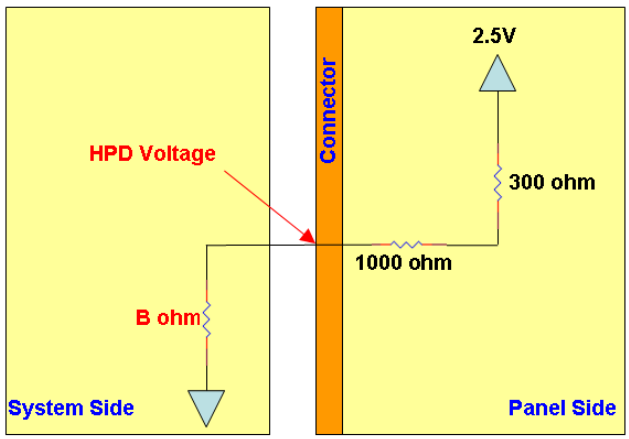
Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	0.98*A	A	1.02*A	V

Note 1 : A = 2.5*[B/(1000+300+B)]
Note 2 : B = Resistance of the system
Note 3 : HPD Voltage =2.25V~3.6V (VESA display port standard)



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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.8	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=21 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	4.5 (*Note2)	--	18	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.2	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.2	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	20K	Hz	
PWM Duty Ratio	Duty	1 (*Note 3)	-	100	%	

Note1: LED Power Supply is evaluated by Lextar LED.

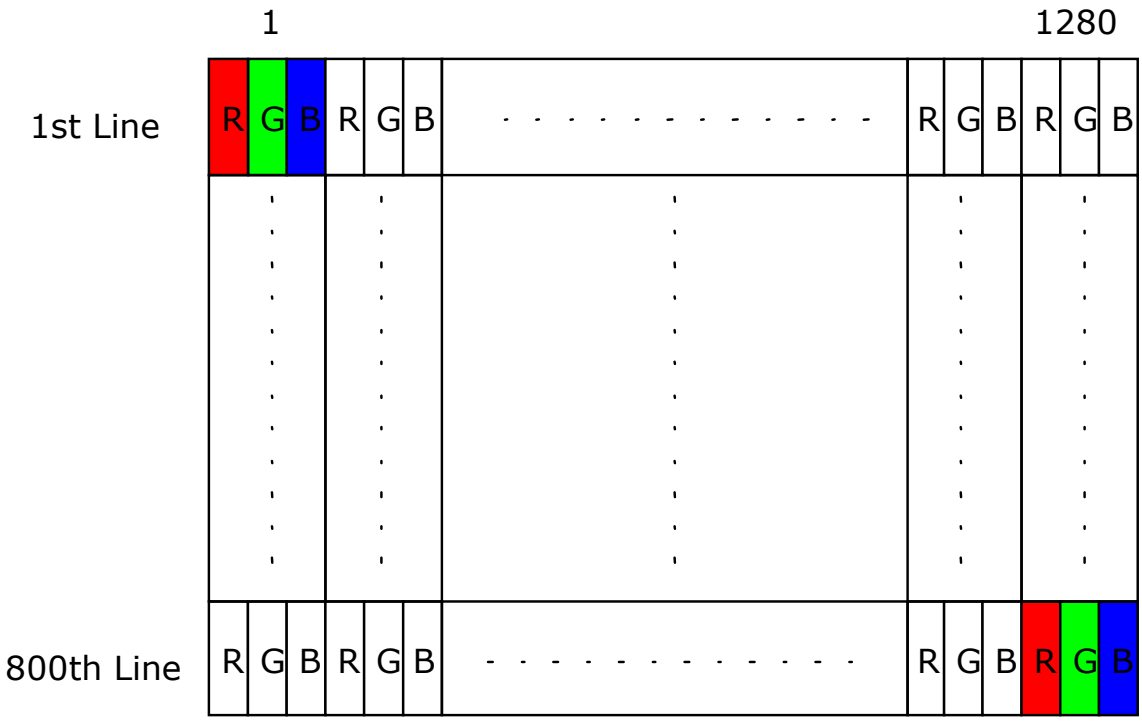
Note 2: Measured in panel VIN

Note 3: If the PWM duty ratio(min) is set between 5% to 1%, the PWM input frequency should be set below 1KHz. The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STM
Type / Part Number	MSAK24025P30 or compatible
Mating Housing/Part Number	I-PEX 20453-030T-11 or compatible

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal Name	Description
1	NC	NC
2	GND	Ground
3	NC	NC
4	NC	NC
5	GND	Ground
6	Lane0_N	Signal Link Lane 0_N
7	Lane0_P	Signal Link Lane 0_P
8	GND	Ground
9	AUX _P	Signal Auxiliary Channel_P
10	AUX _N	Signal Auxiliary Channel_N
11	GND	Ground
12	VDD	LCD logic and driver power
13	VDD	LCD logic and driver power
14	NC(AGING)	LCD Panel Self Test(do not connect)
15	GND	Ground
16	GND	Ground
17	HPD	HPD signal pin
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	LED_EN	Backlight On/Off
23	LED_PWM	System PWM signal input for dimming

24	NC-Reserved	Reserved for LCD manufacture's use(EDID_CLK)
25	NC-Reserved	Reserved for LCD manufacture's use(EDID_DATA)
26	V_LED	Backlight power
27	V_LED	Backlight power
28	V_LED	Backlight power
29	V_LED	Backlight power
30	NC	NC

Note1: Input signals shall be low or High-impedance state when VDD is off.

Note2: Input signals shall be low or High-impedance state when VDD is off.
internal circuit of **eDP inputs** are as following.

6.3 Interface Timing

6.3.1 Timing Characteristics

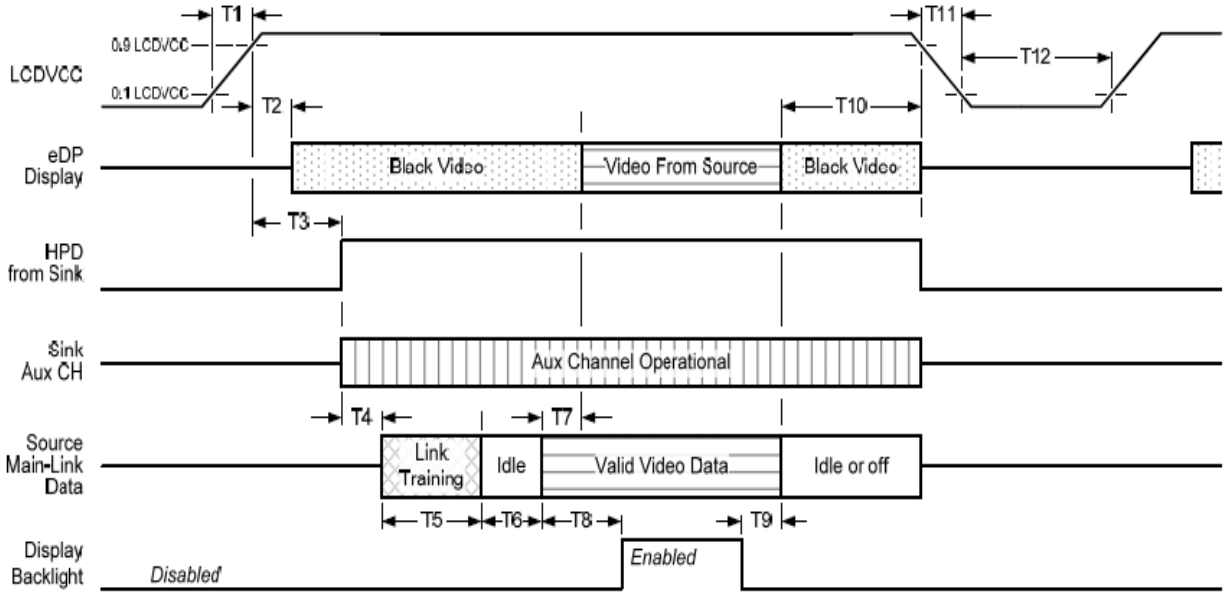
Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	65.3	68.93	75	MHz
Vertical Section	Period	T_V	812	816	800+A	T_{Line}
	Active	T_{VD}	800			
	Blanking	T_{VB}	12	16	A	
Horizontal Section	Period	T_H	1340	1408	1280+B	T_{Clock}
	Active	T_{HD}	1280			
	Blanking	T_{HB}	60	128	B	

Note 1: The above is as optimized setting
Note 2: The maximum clock frequency = (800+A)*(1280+B)*60 < 75 MHz

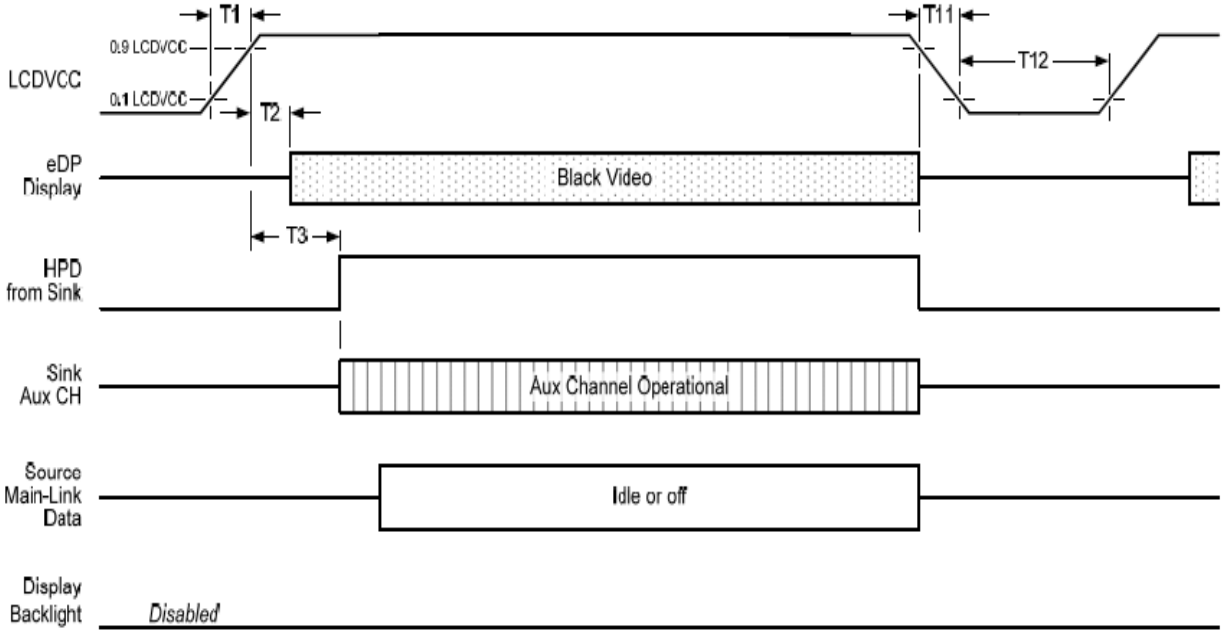
6.4 Power ON / OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

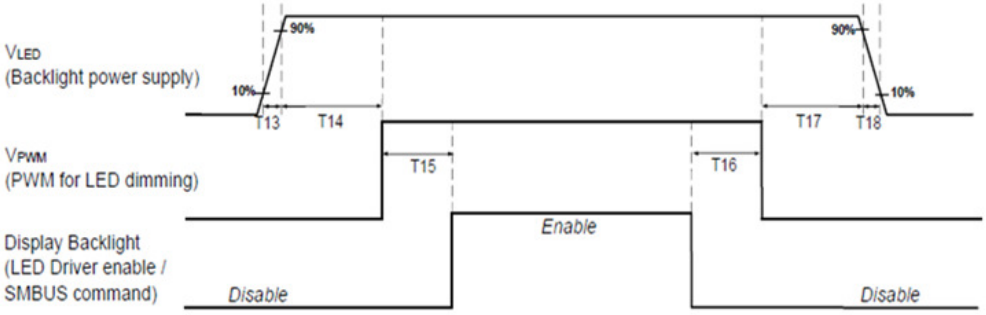
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

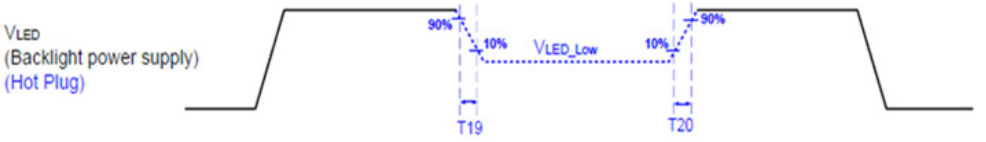


	Min (ms)	Max (ms)
T13	0.2	10
T14	0	-
T15	0	-
T16	0	-
T17	0	-
T18	0.2	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Note 1 : If T14,T15,T16,T17<10ms，The display garbage may occur. We suggest T14,T15,T16,T17>10ms to avoid the display garbage.

Note 2 : If T13 or T18<0.5ms，the inrush current may cause the damage of fuse. If T13 or T18<0.5ms，the inrush current I^2t is under typical melt of fuse Spec.，there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

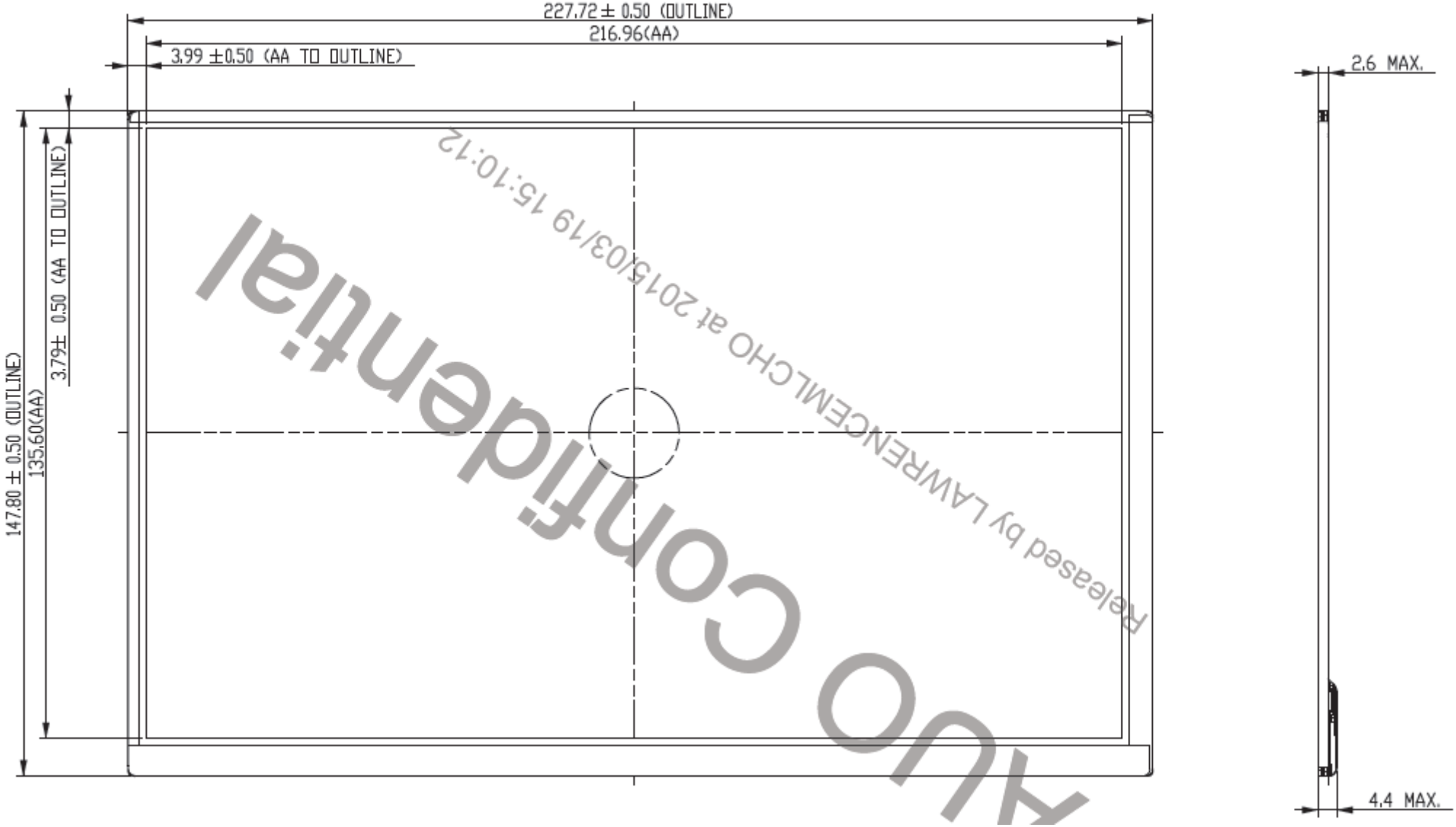
7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

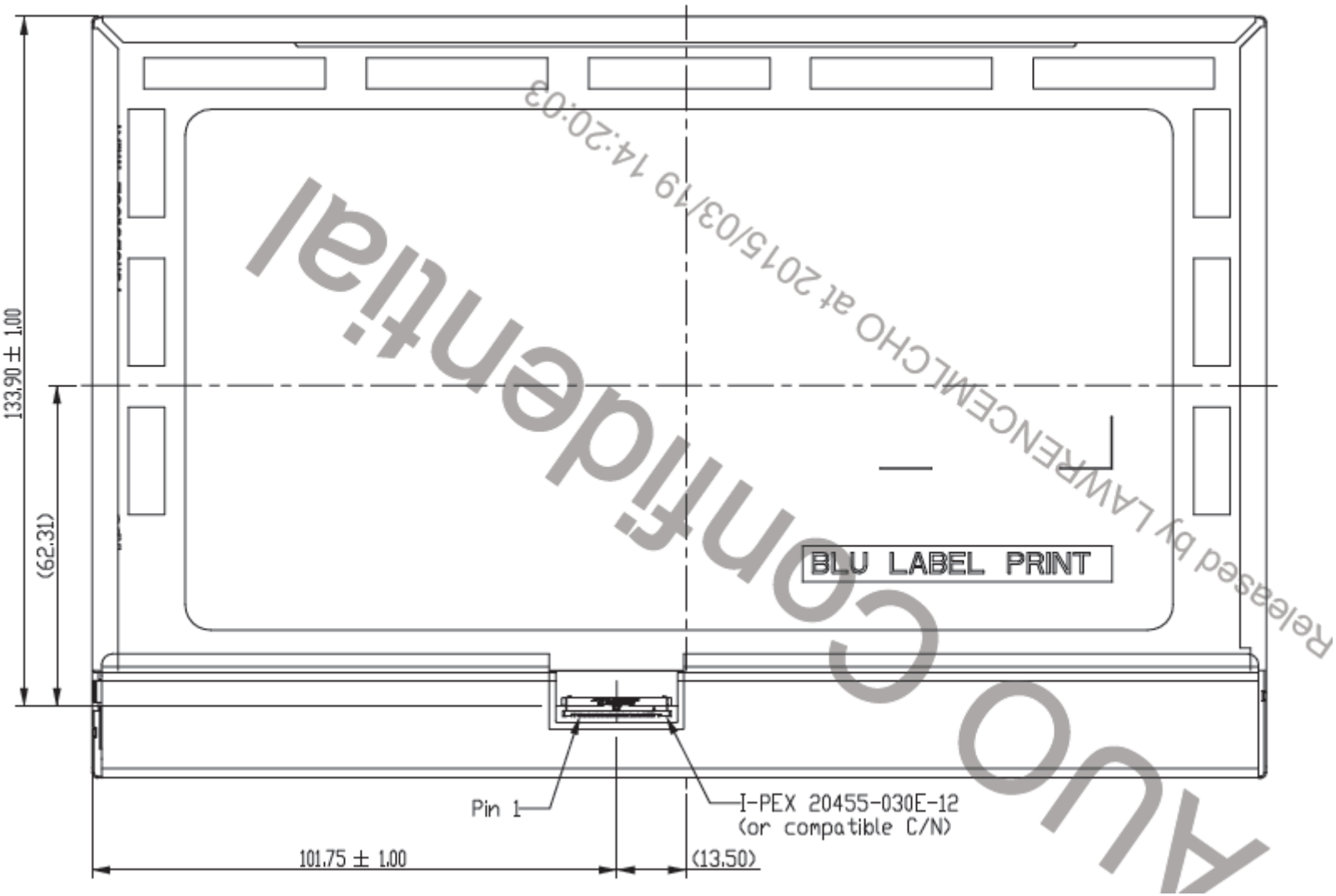
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics
8.1 LCM Outline Dimension
Front View



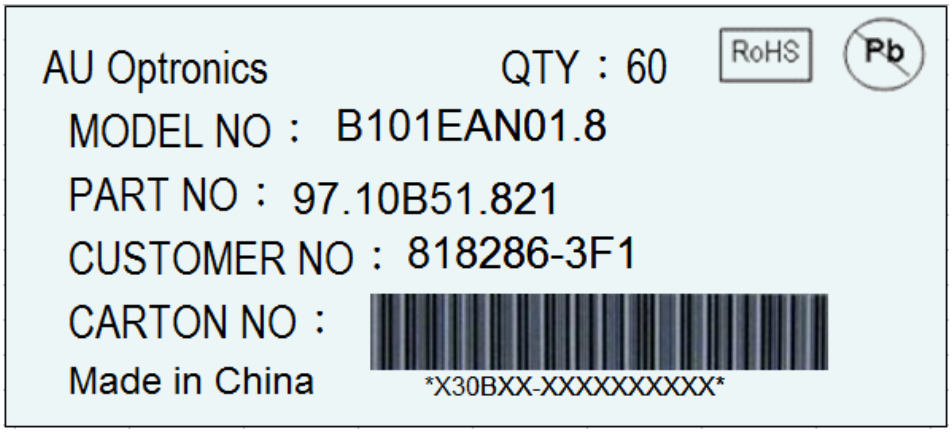
Back View



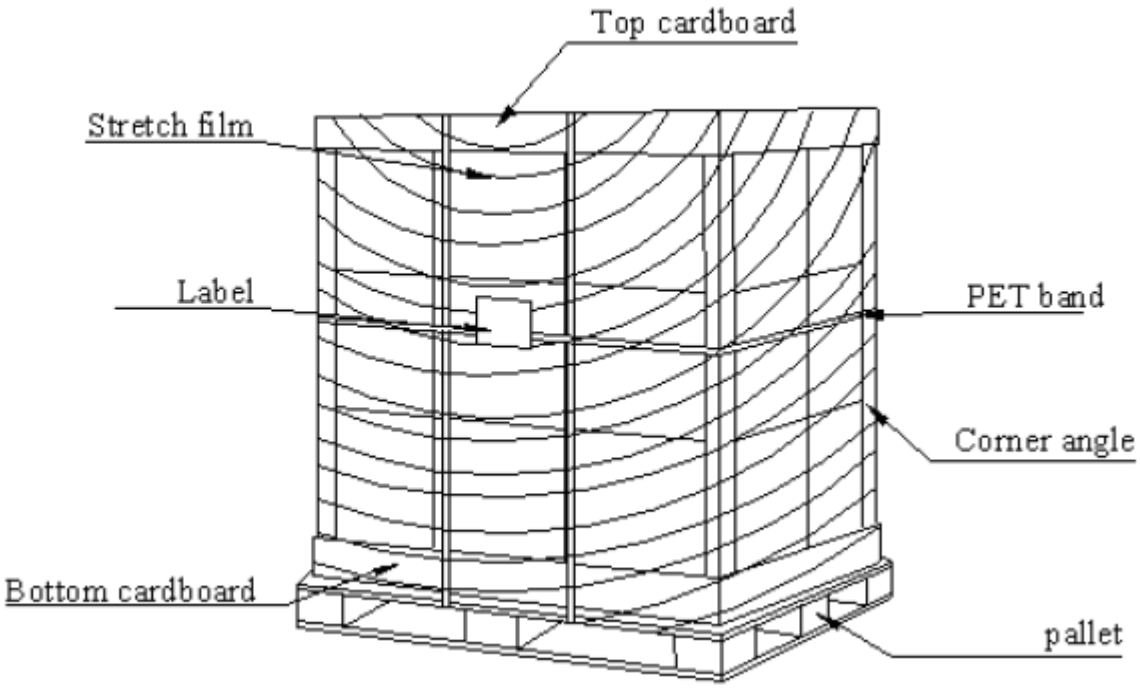
9. Shipping and Package

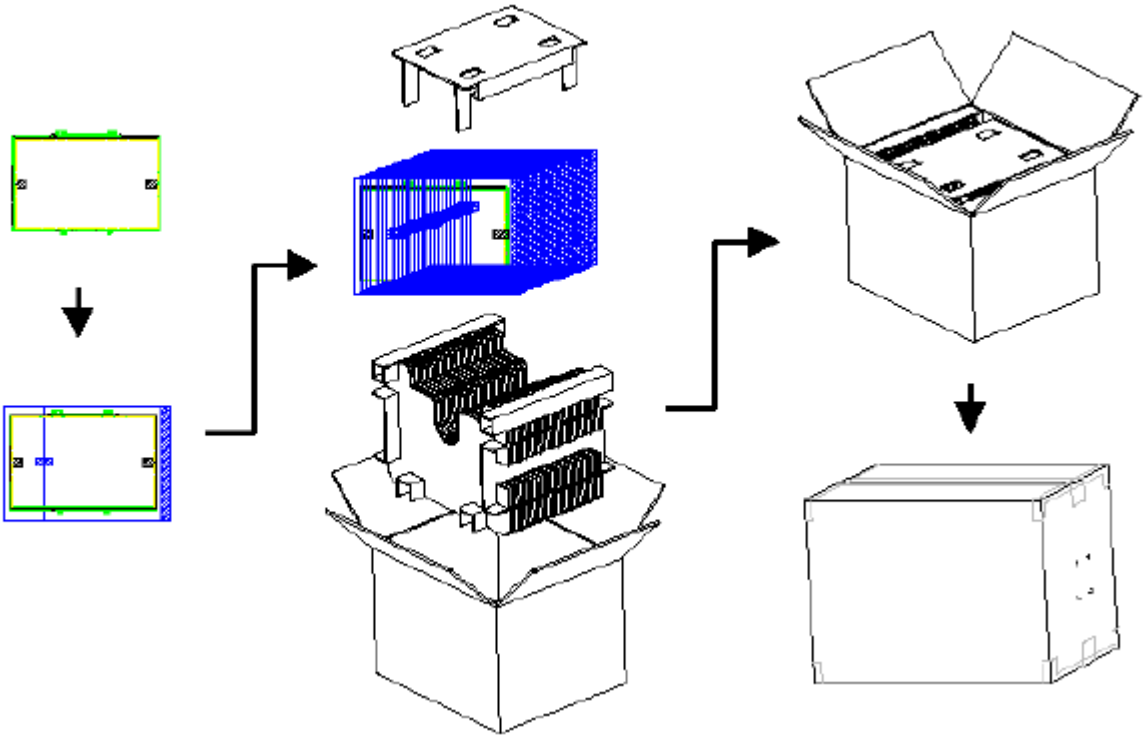
9.1 Label Format

Shipping Label



9.2 Shipping Package of Palletizing Sequence





10. EDID

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	D4	11010100	212
0B	hex, LSB first	18	00011000	24
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	23	00100011	35
11	Year of manufacture	17	00010111	23
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A0	10100000	160
15	**Max H image size** *(rounded to cm)*	16	00010110	22
16	**Max V image size** *(rounded to cm)*	0E	00001110	14
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2
19	Red/green low bits **(Lower 2:2:2:2 bits)**	99	10011001	153
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	85	10000101	133
1B	Red x **(Upper 8 bits)**	95	10010101	149
1C	Red y/ highER 8 bits	55	01010101	85
1D	Green x	56	01010110	86
1E	Green y	92	10010010	146
1F	Blue x	28	00101000	40
20	Blue y	22	00100010	34
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1

2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	DE	11011110	222
37	Pixel Clock/10000 USB	1C	00011100	28
38	Horz active **Lower 8bits**	00	00000000	0
39	Horz blanking **Lower 8bits**	C8	11001000	200
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80
3B	Vertical Active **Lower 8bits**	20	00100000	32
3C	Vertical Blanking **Lower 8bits**	20	00100000	32
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48
3E	HorzSync. Offset	93	10010011	147
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	44	01000100	68
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	D8	11011000	216
43	Vertical Image Size **Lower 8bits**	87	10000111	135
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Pixel Clock/10,000 (LSB)	3F	00111111	63
49	Pixel Clock/10,000 (MSB)	13	00010011	19
4A	Horizontal Addressable Pixels, lower 8 bits	00	00000000	0
4B	Horizontal Blanking Pixels, lower 8 bits	C8	11001000	200
4C	H Pixels, upper nibble : H Blanking, upper nibble	50	01010000	80
4D	Vertical Addressable Lines, lower 8 bits	20	00100000	32
4E	Vertical Blanking Lines, lower 8 bits	20	00100000	32
4F	V lines, upper nibble : V blanking, upper nibble	30	00110000	48
50	Horizontal Front Porch, lower 8 bits	93	10010011	147
51	Horizontal Sync Pulse, lower 8 bits	20	00100000	32
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	44	01000100	68
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0
54	Horizontal Image Size in mm, lower 8 bits	D8	11011000	216
55	Vertical Image Size in mm, lower 8 bits	87	10000111	135
56	H Image Size, upper nibble : V Image Size, upper nibble	00	00000000	0
57	Horizontal Border	00	00000000	0
58	Vertical Border	00	00000000	0
59	Bit Encode Sync Information	18	00011000	24
5A	DC	00	00000000	0
5B	HTOTAL	00	00000000	0

5C	HA	00	00000000	0
5D	HBL	00	00000000	0
5E	HFP	00	00000000	0
5F	HFPe	00	00000000	0
60	HBP	00	00000000	0
61	HB	00	00000000	0
62	HSO	00	00000000	0
63	HS	00	00000000	0
64	VTOTAL	00	00000000	0
65	VA	00	00000000	0
66	VBL	00	00000000	0
67	VFP	00	00000000	0
68	VBP	00	00000000	0
69	VB	00	00000000	0
6A	VSO	00	00000000	0
6B	VS	00	00000000	0
6C	Detail Timing Description #4	00	00000000	0
6D	Flag	00	00000000	0
6E	Reserved	00	00000000	0
6F	For Brightness Table and Power Consumption	02	00000010	2
70	Flag	00	00000000	0
71	PWM % [7:0] @ Step 0	10	00010000	16
72	PWM % [7:0] @ Step 5	3F	00111111	63
73	PWM % [7:0] @ Step 10	FF	11111111	255
74	Nits [7:0] @ Step 0	0F	00001111	15
75	Nits [7:0] @ Step 5	3C	00111100	60
76	Nits [7:0] @ Step 10	7D	01111101	125
77	Panel Electronics Power @ 32x32 Chess Pattern =	19	00011001	25
78	Backlight Power @ 60 nits =	14	00010100	20
79	Backlight Power @ Step 10 =	0C	00001100	12
7A	Nits @ 100% PWM Duty =	7D	01111101	125
7B	Flag	20	00100000	32
7C	Flag	20	00100000	32
7D	Flag	20	00100000	32
7E	Extension Flag	00	00000000	0
7F	Checksum	94	10010100	148