Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**10.1” WUXGA 16:10 Color TFT-LCD with LED Backlight design**
Model Name	**B101UAN01.7 (H/W: 0A)**
Note	***LED Backlight with driving circuit design***

Customer **Date**	**Approved by** **Date**
Checked & Approved by **Date**	**Prepared by**
Note: This Specification is subject to change without notice.	**MPBU Marketing Division AU Optronics corporation**

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2014/07/28	All	First Edition for Customer		
0.1 2014/08/01	29	AA tolerance +/- 0.3 mm	AA tolerance +/- 0.05 mm	
0.2 2014/12/12	31	Label : X10	Label : A00	
0.3 2014/12/31	29/30		Drawing Modification	
0.4 2015/01/16	29	LCM Outline Dimension	Add AA monitor Dim.	
0.5 2015/01/24	21	VLED Max. 5V	VLED Max. 10V	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B101UAN01.7 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA, 1920(H) x1200(V) screen and 16.7M colors (RGB 6-bits + Hi-FRC) with LED backlight driving circuit**.** All input signals are MIPI interface compatible.

B101UAN01.7 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	256.42 (10.1W")			
Active Area	[mm]	216.81 (H) x 135.50 (V)			
Pixels H x V		1920 x 3(RGB) x 1200			
Pixel Pitch	[mm]	0.11292 X 0.11292			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black (AHVA mode)			
White Luminance	[cd/m^2]	400 typ, 340 min			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800:1 typ., 600:1 min.			
Response Time	[ms]	25 Typ. / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption (max)	[Watt]	3.45W (VLED 3V min with LED driver IC)			
Weight	[Grams]	135 max.			
Physical Size (panel only)	[mm]		Min.	Typ.	Max.
		Length	227.22	227.72	228.22
		Width	147.30	147.80	148.30
		Thickness	---	---	2.45 (Panel side) 5.35 (PCBA side)

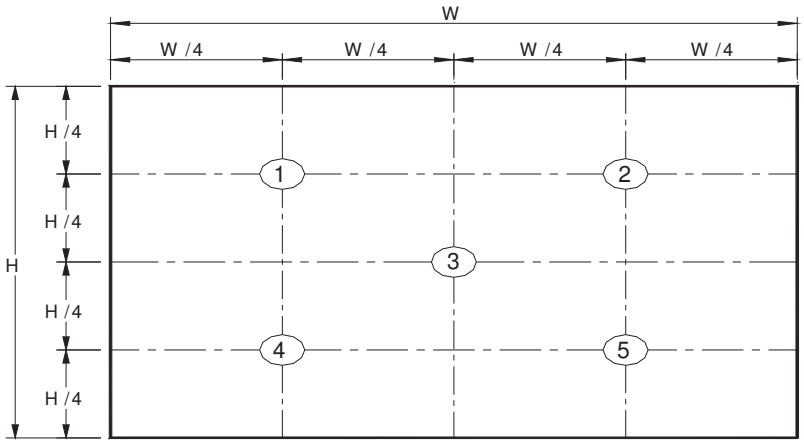
Electrical Interface		MIPI
Surface Treatment		Glare
Support Color		16.7M colors (RGB 6-bit + Hi-FRC)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

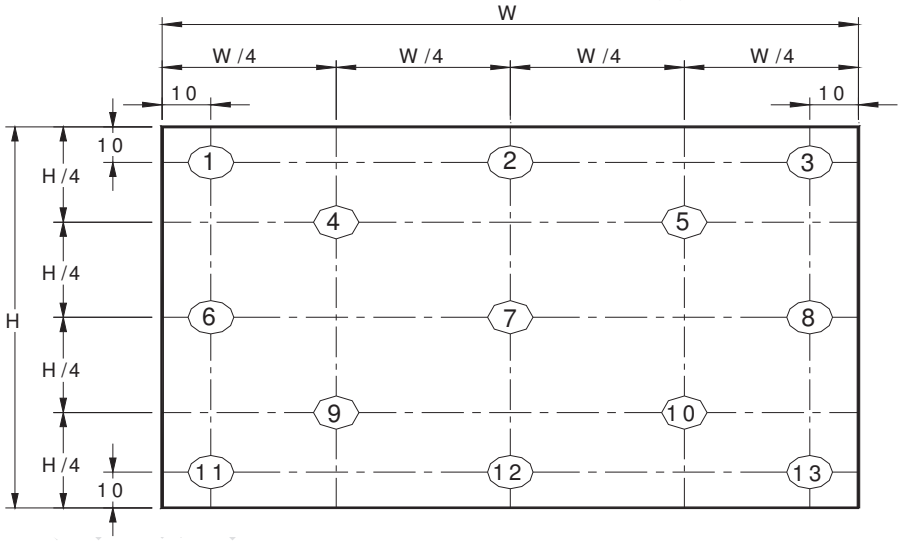
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance			5 points average	340	400	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR ≧ 10 (Left)	80 80	85 85	---	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR ≧ 10 (Lower)	80 80	85 85	---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.60		2, 3, 4
Contrast Ratio		CR		600	800	---		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.563	0.593	0.623		4
		Ry		0.311	0.341	0.371		
	Green	Gx		0.294	0.324	0.354		
		Gy		0.559	0.589	0.619		
	Blue	Bx		0.124	0.154	0.184		
		By		0.093	0.123	0.153		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



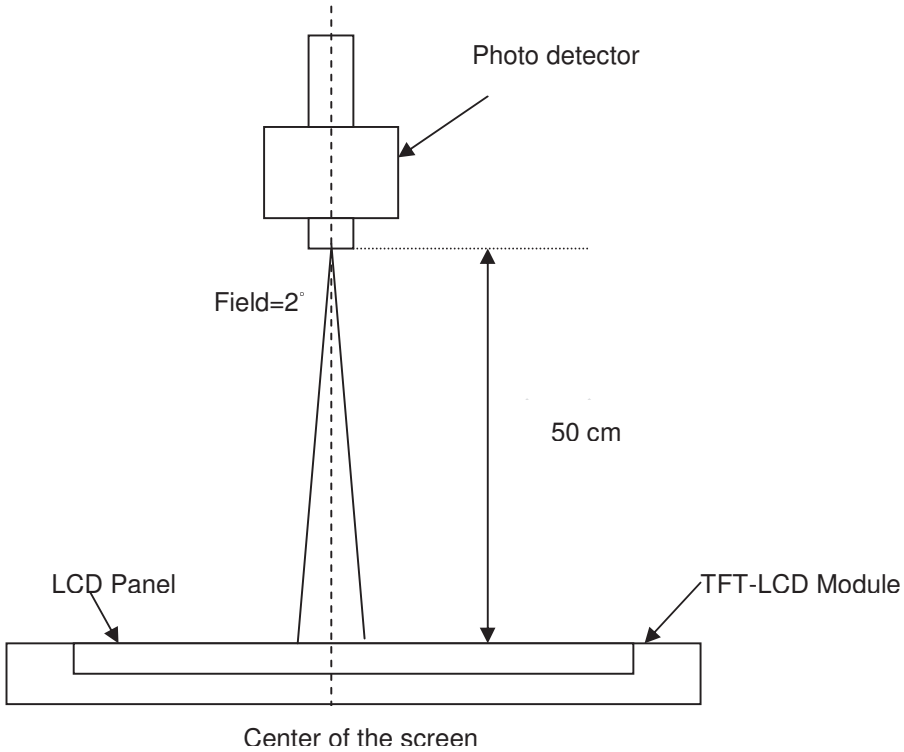
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

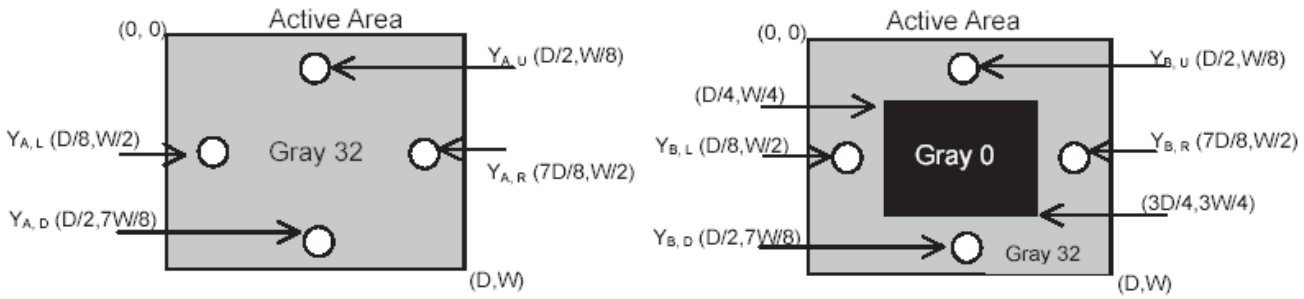
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

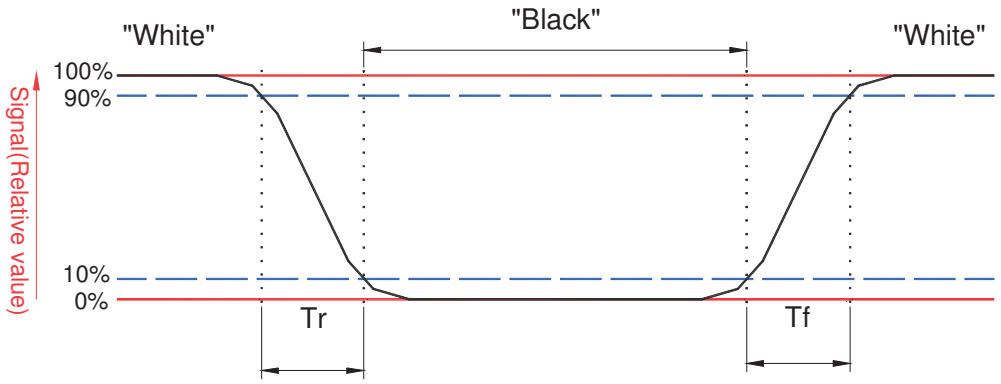
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



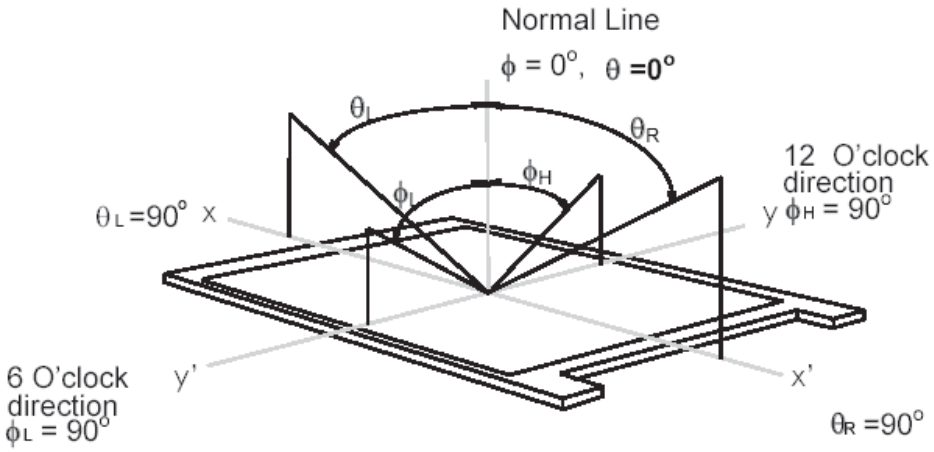
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



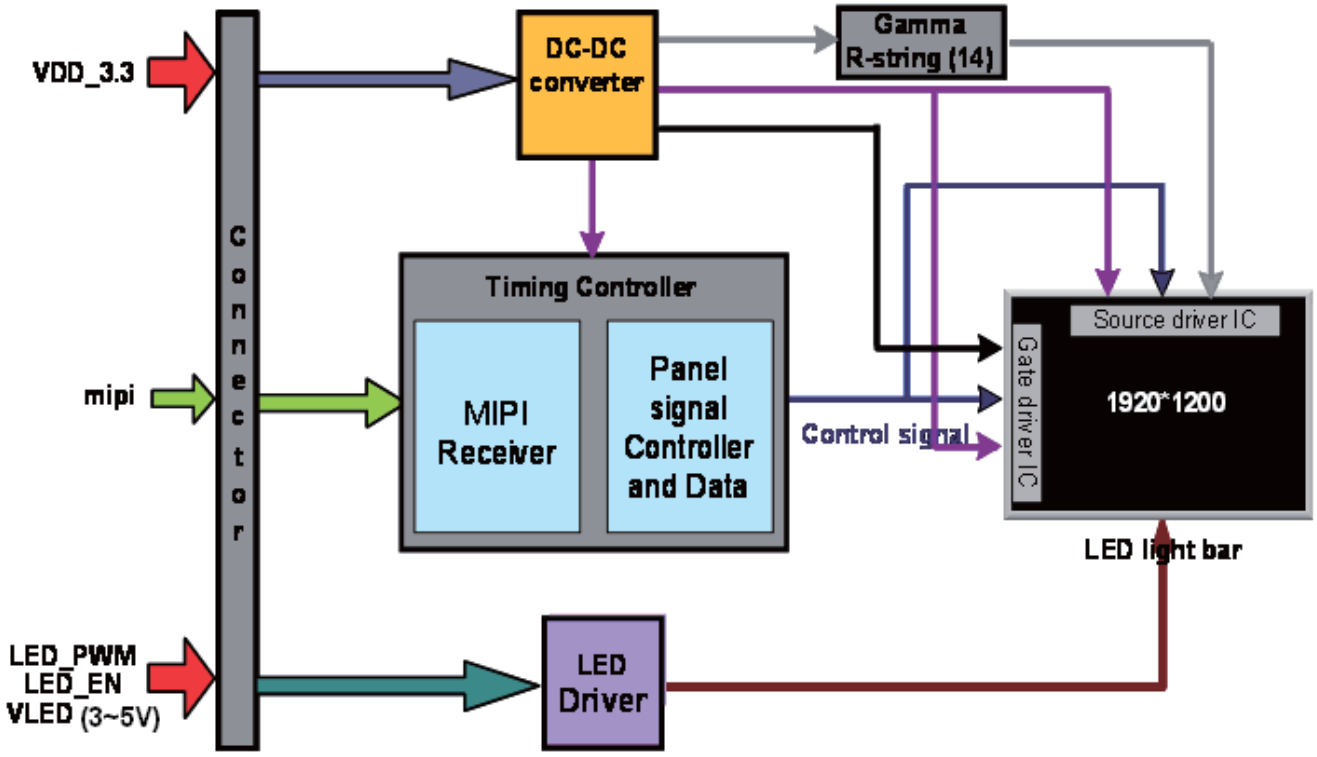
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 34 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.5	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

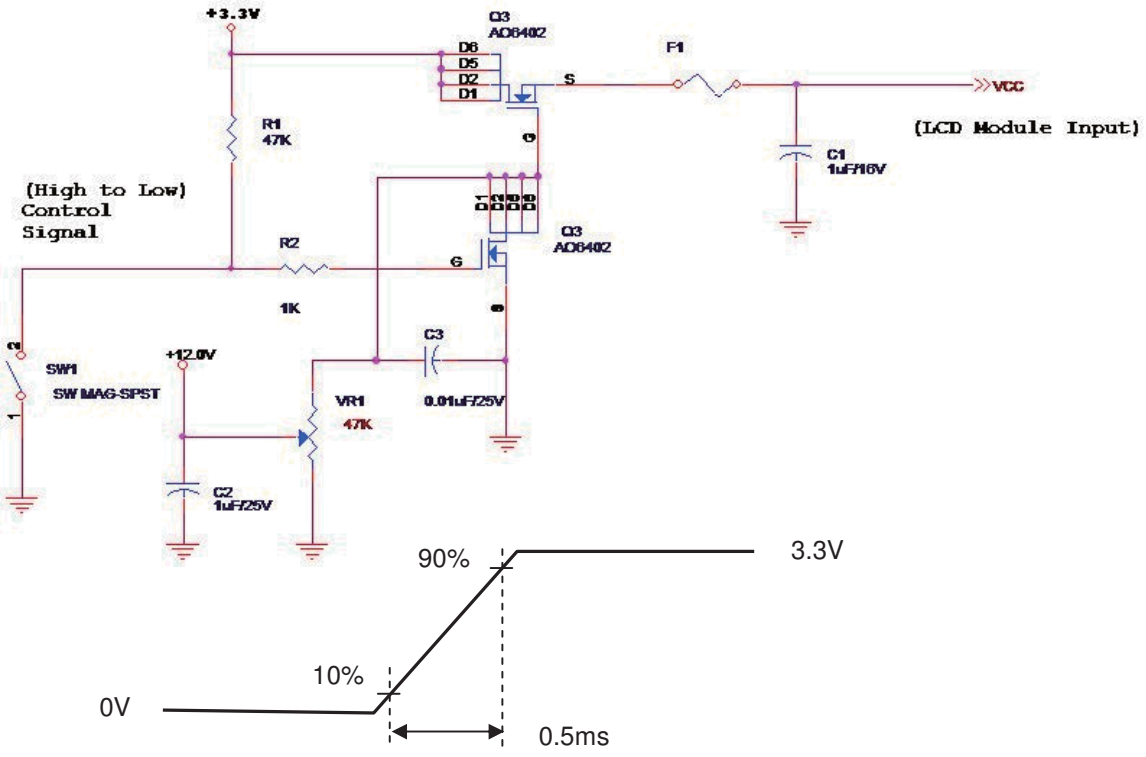
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	4.2	[Volt]	
PDD	VDD Power	_	-	0.95	[Watt]	Note 1
IDD	IDD Current	_	_	316	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2：Measure Condition



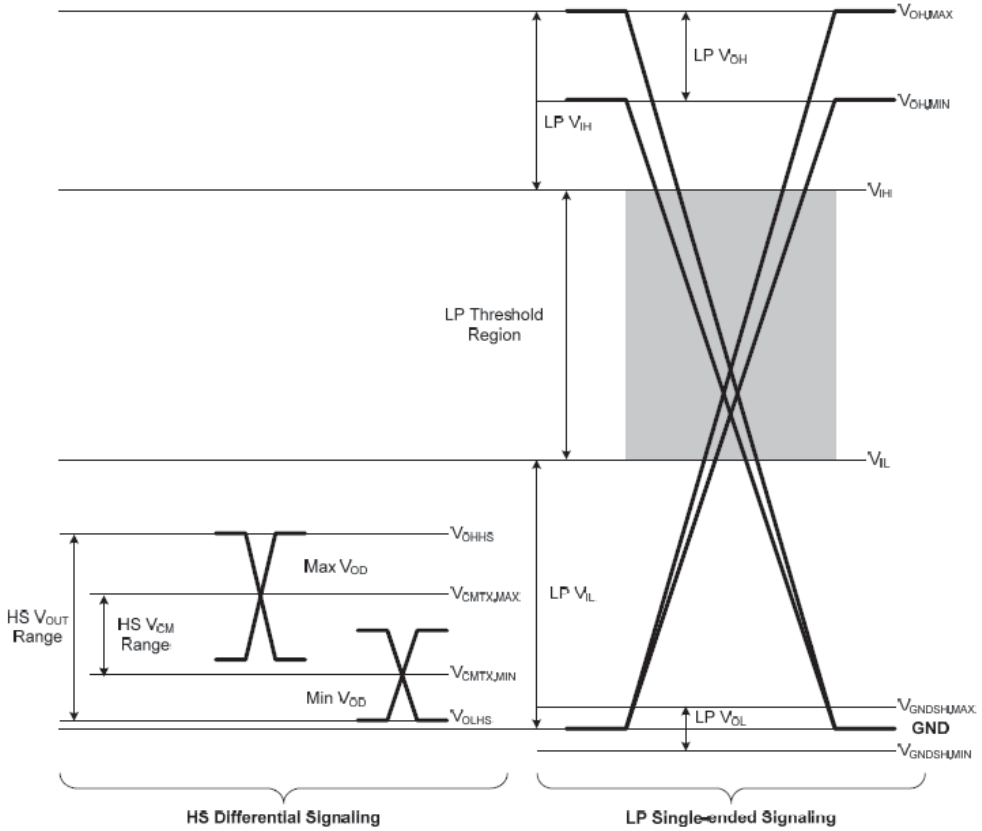
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

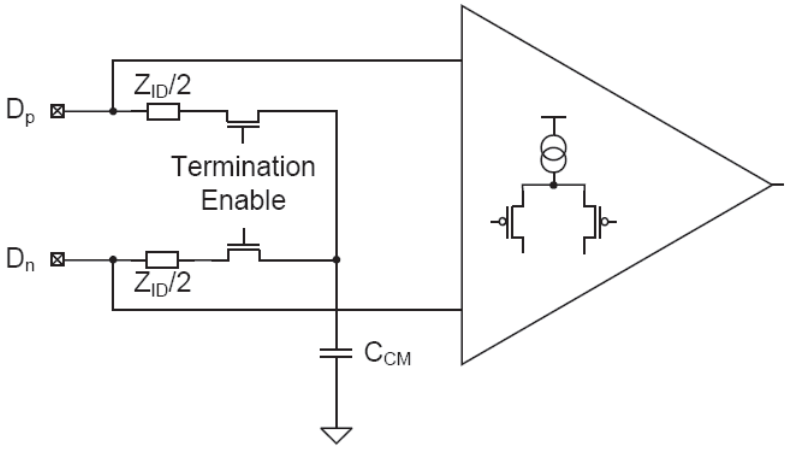
MIPI DC/AC Characteristics are as follows;

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps
V_{CMRX}	Common-mode voltage(HS Rx mode)	70	-	330	mV
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880			mV
V_{ILLP}	Logic 0 input voltage (LP Rx mode)			550	mV
V_{OH}	Output high level (LP Tx mode)	1.08	1.2	1.32	V
V_{OL}	Output low level (LP Tx mode)	-50		50	mV



MIPI Receiver Differential Input (AC Characteristics)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous		1		12.5	ns

HS RX Scheme

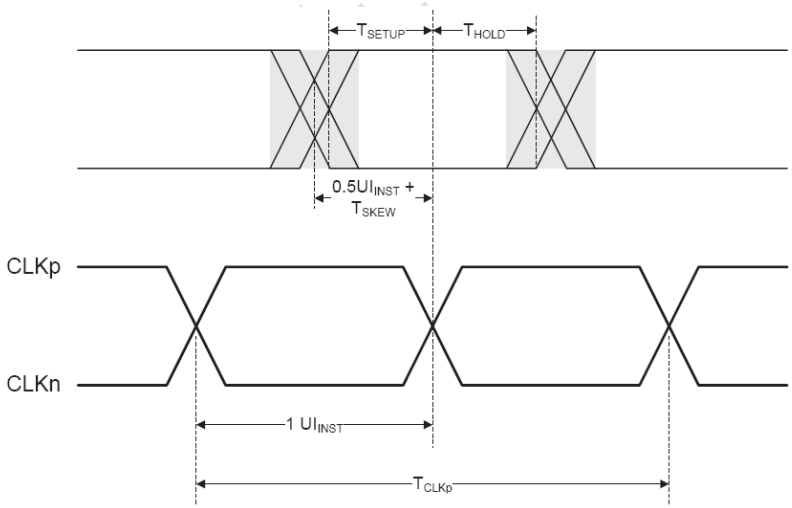


Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.15			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.15			UI_{INST}	2

Note:

1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of $0.3*UI_{INST}$

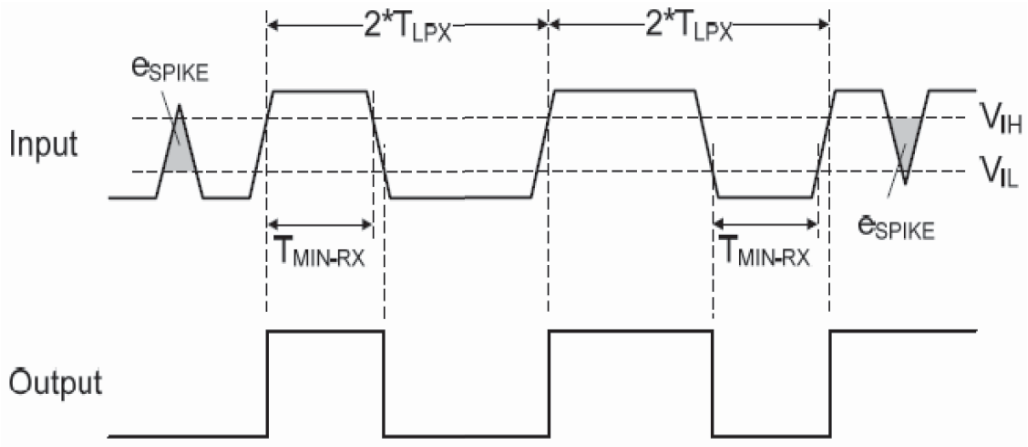
High Speed Data Transmission: Data to Clock Timing



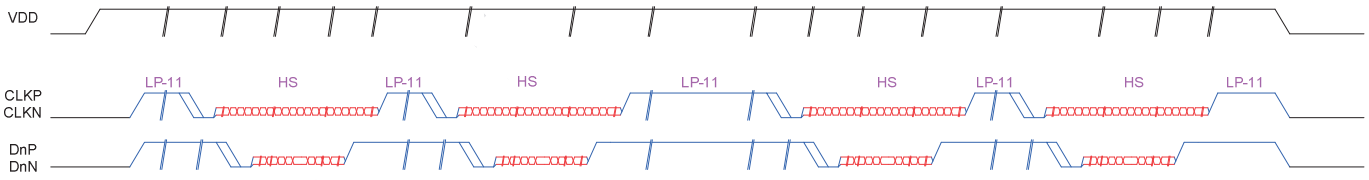
LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		50	-	-	ns

V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

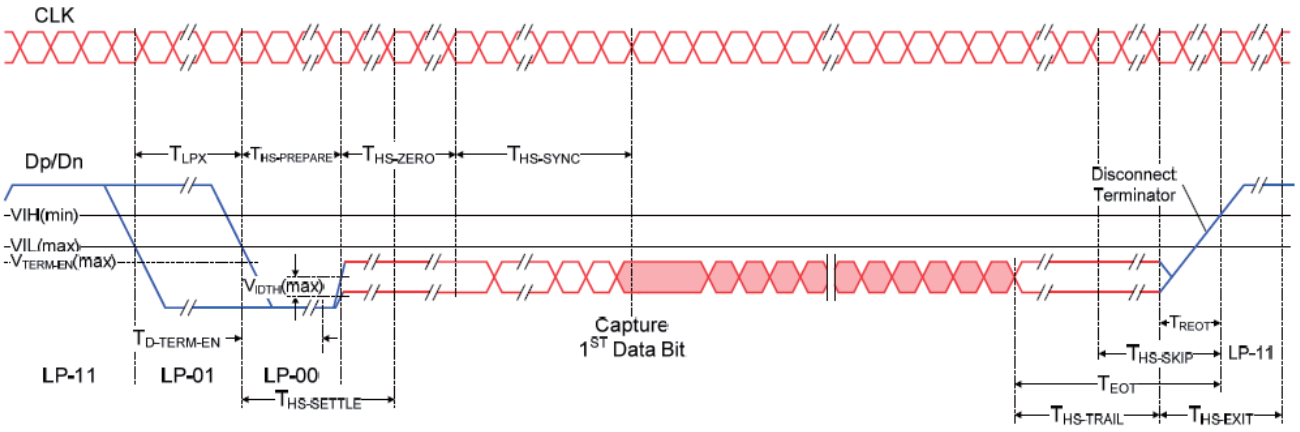
Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI

TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

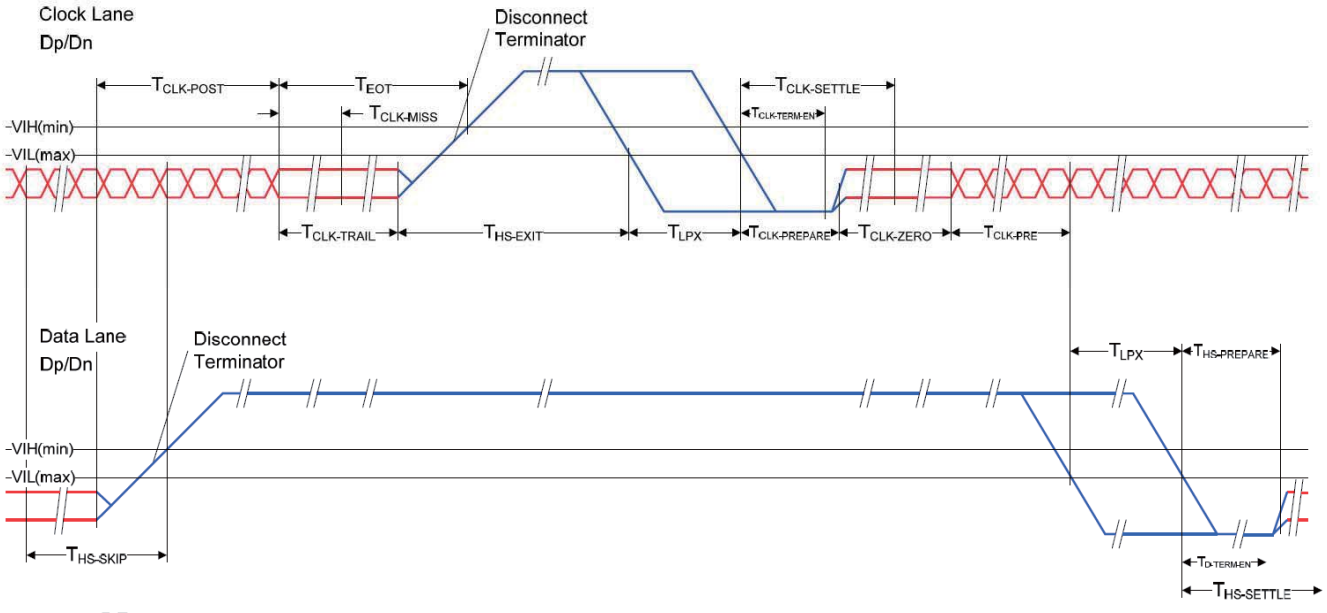
Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.5	[Watt]	(Ta=25℃@400nits)
LED Life-Time	N/A	12,000	-	-	Hour	(Ta=25℃@400nits) Note1.
LED Forward Voltage	VF	2.7	2.95	3.3	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	-	14.75	16.5	[Volt]	(Ta=25℃) Note2.
LED Forward Current	IF	-	22	-	[mA]	(Ta=25℃)

Note 1. The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	3		10	[Volt]	Define as Connector Interface (Ta=25℃) Note1.
LED Enable Input High Level	VLED_EN	1.8	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	1.8	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	-	10K	Hz	
PWM Duty Ratio	Duty	5		100	%	

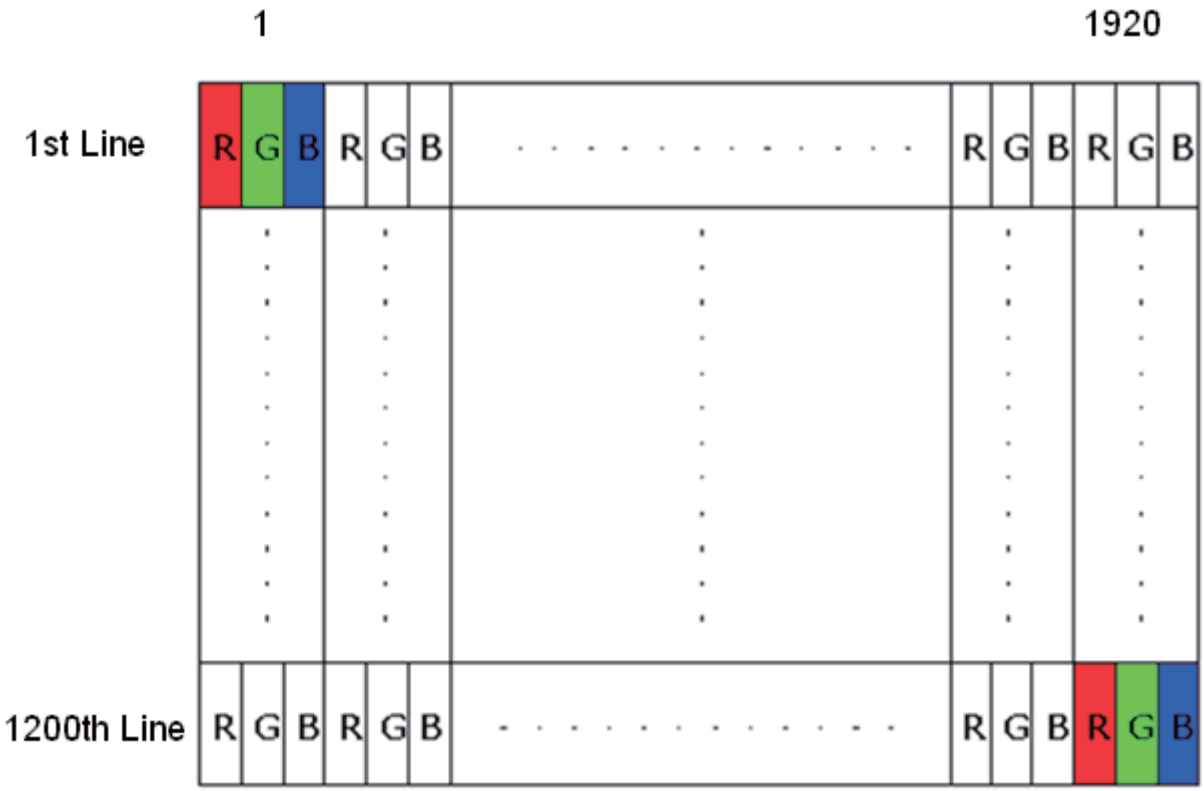
Note 1: The input high level voltage conversion to 2.5V by level shift circuit.

Note 2: The LED PWM Logic Input Low Level Voltage must have an output impedance close to 0 ohm in front of input connector.

6. Signal Interface Characteristic

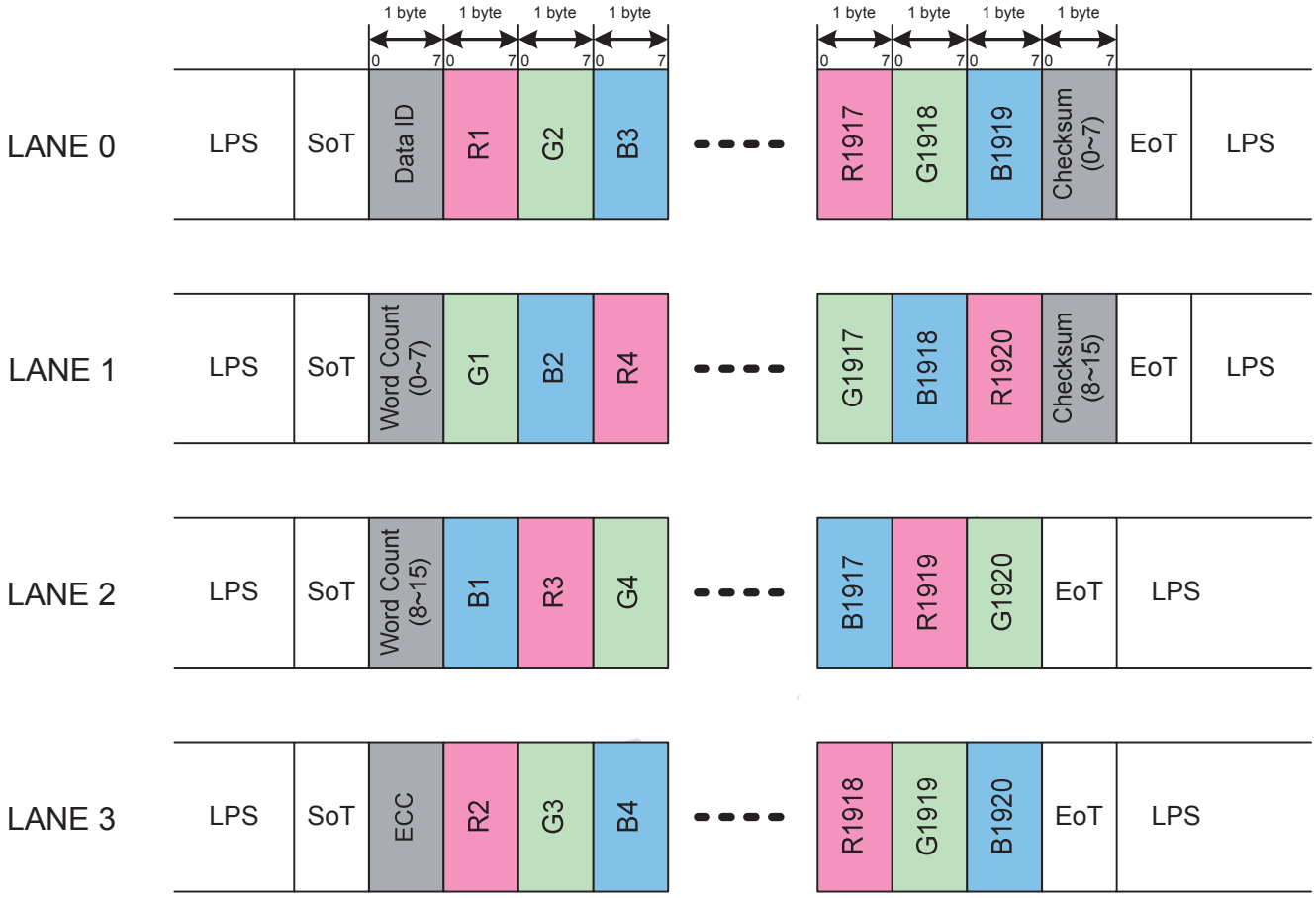
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format

Input Pixel Stream Format (1920RGB in 4 Lanes with RGB 8-8-8 format)



LPS : Low Power State
SoT : Start of Transmission
EoT : End of Transmission
ECC : Error-Correcting Code

6.3 Integration Interface Requirement

6.3.1 MIPI Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	FH34SJ-34S-0.5SH(50) or compatible
Mating Housing/Part Number	FPC Cable

6.3.2 MIPI Pin Assignment

MIPI is a differential signal technology for LCD interface and high speed data transfer device.

No.	Pin Name	Description
1	VDD	DC-DC circuit supply voltage
2	VDD	DC-DC circuit supply voltage
3	NC	Not Connection
4	LED_EN	LED driver Enable Input
5	LED_PWM	Backlight LED driver PWM Input
6	EDID_SDA	EDID Data Input (VIH=1.8V)
7	EDID_SCL	EDID Clock Input (VIH=1.8V)
8	NC	Not Connection
9	GND	Ground
10	DSI_D2P/Rx-IN2P	MIPI data pair 2 positive signal
11	DSI_D2N/Rx-IN2N	MIPI data pair 2 negative signal
12	GND	Ground
13	DSI_D1P/Rx-IN1P	MIPI data pair 1 positive signal
14	DSI_D1N/Rx-IN1N	MIPI data pair 1 negative signal
15	GND	Ground
16	DSI_CLKP/Rx-CLKP	MIPI Clock positive signal
17	DSI_CLKN/Rx-CLKN	MIPI Clock negative signal
18	GND	Ground
19	DSI_D0P/Rx-IN0P	MIPI data pair 0 positive signal
20	DSI_D0N/Rx-IN0N	MIPI data pair 0 negative signal
21	GND	Ground
22	DSI_D3P/Rx-IN3P	MIPI data pair 3 positive signal
23	DSI_D3N/Rx-IN3N	MIPI data pair 3 negative signal
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	ID	Not Connection
29	Aging	Aging Mode Power Supply (AUO only)
30	NC	Not Connection
31	LED+	LED Power Supply
32	LED+	LED Power Supply
33	LED+	LED Power Supply
34	LED+	LED Power Supply

6.4 MIPI Interface Timing

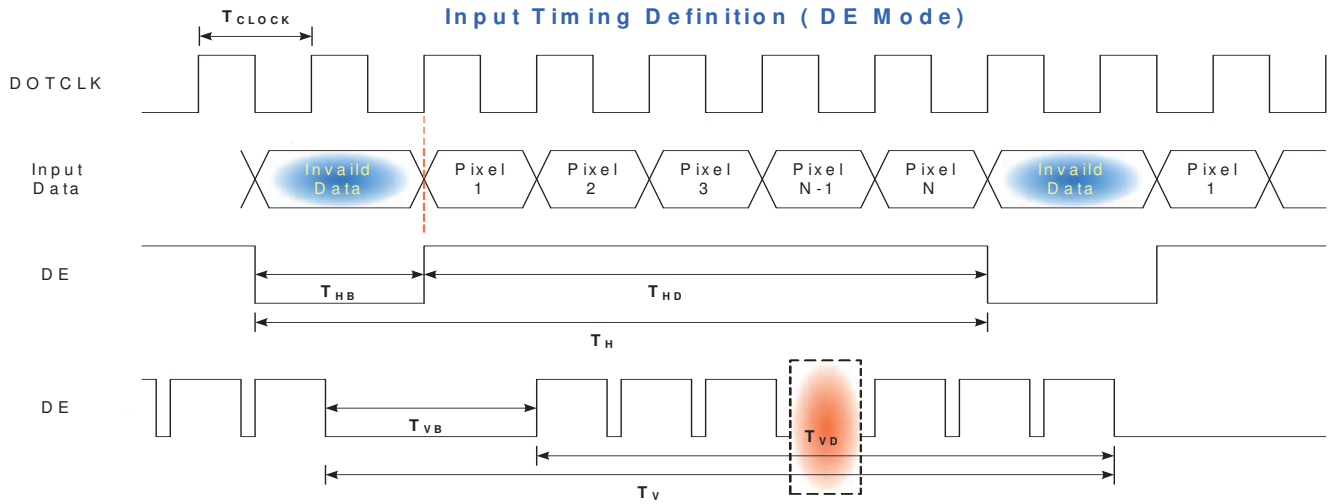
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	155.43	157.08	158.73	MHz
Vertical Section	Period	T_V	1206	1212	1218	T_{Line}
	Active	T_{VD}	1200			
	Blanking	T_{VB}	6	12	18	
Horizontal Section	Period	T_H	2148	2160	2172	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	228	240	252	

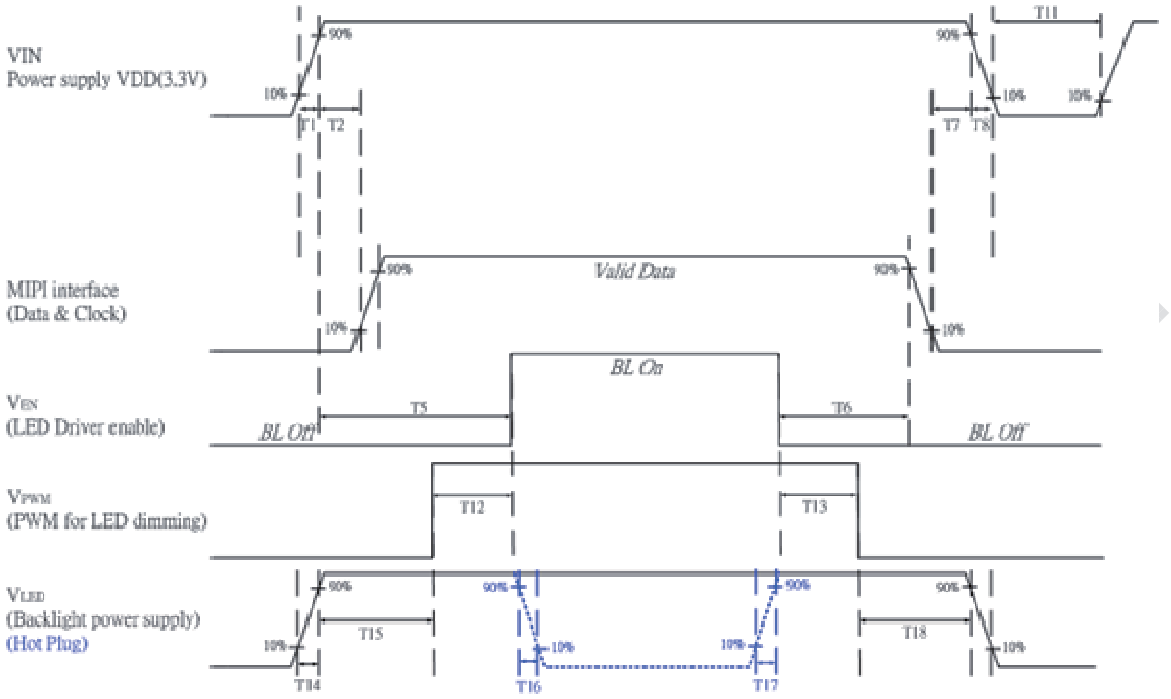
Note : 1. DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	50	
T5	200	-	
T6	200	-	
T7	0	50	
T8	0	10	
T11	500	-	
T12	10	-	
T13	10	-	
T14	0.5	10	
T15	10	-	
T16	1*	-	
T17	1*	-	
T18	10	-	

Note: LED_PWM must be pull low(GND) when it is not pull high.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

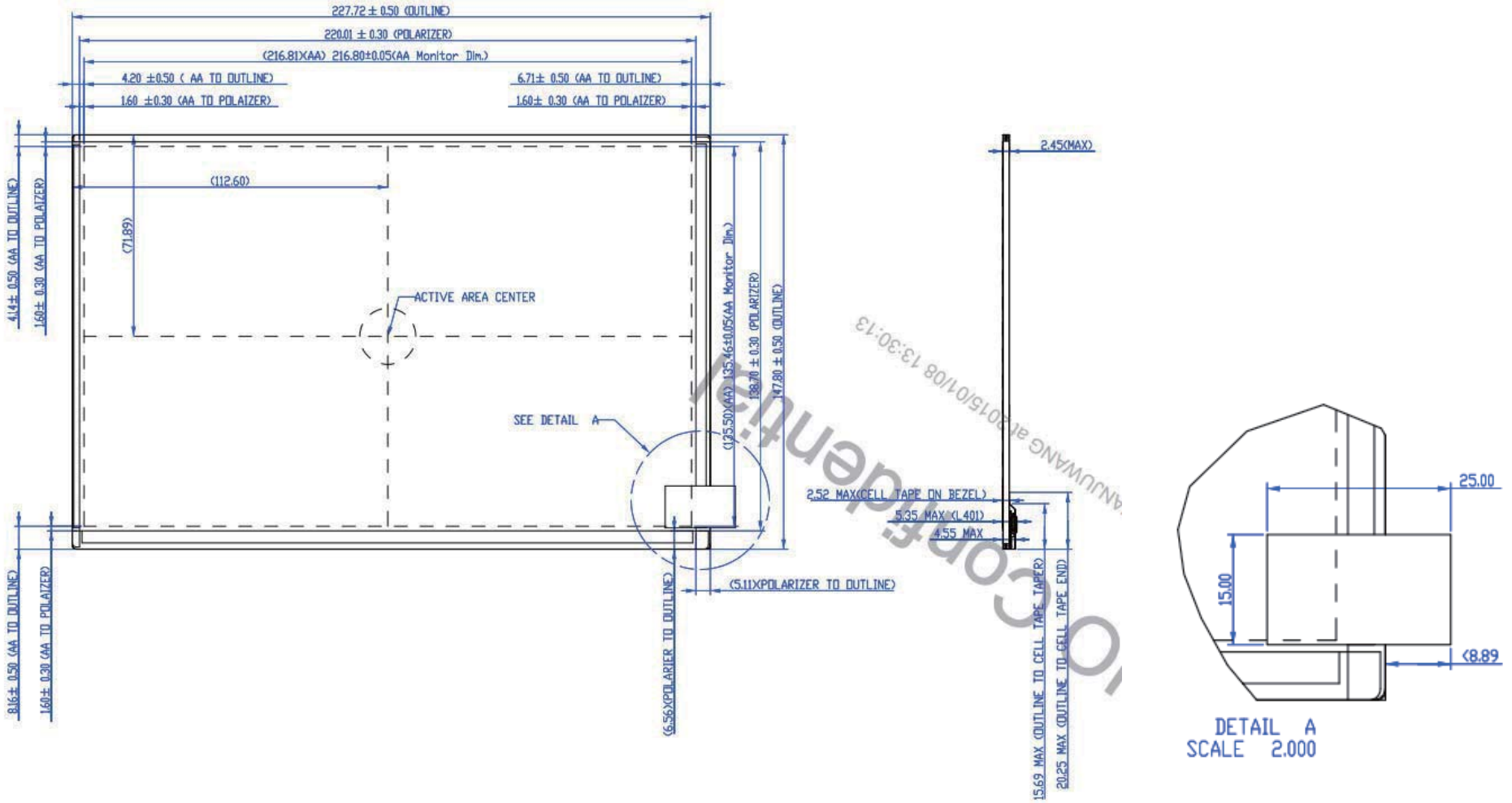
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

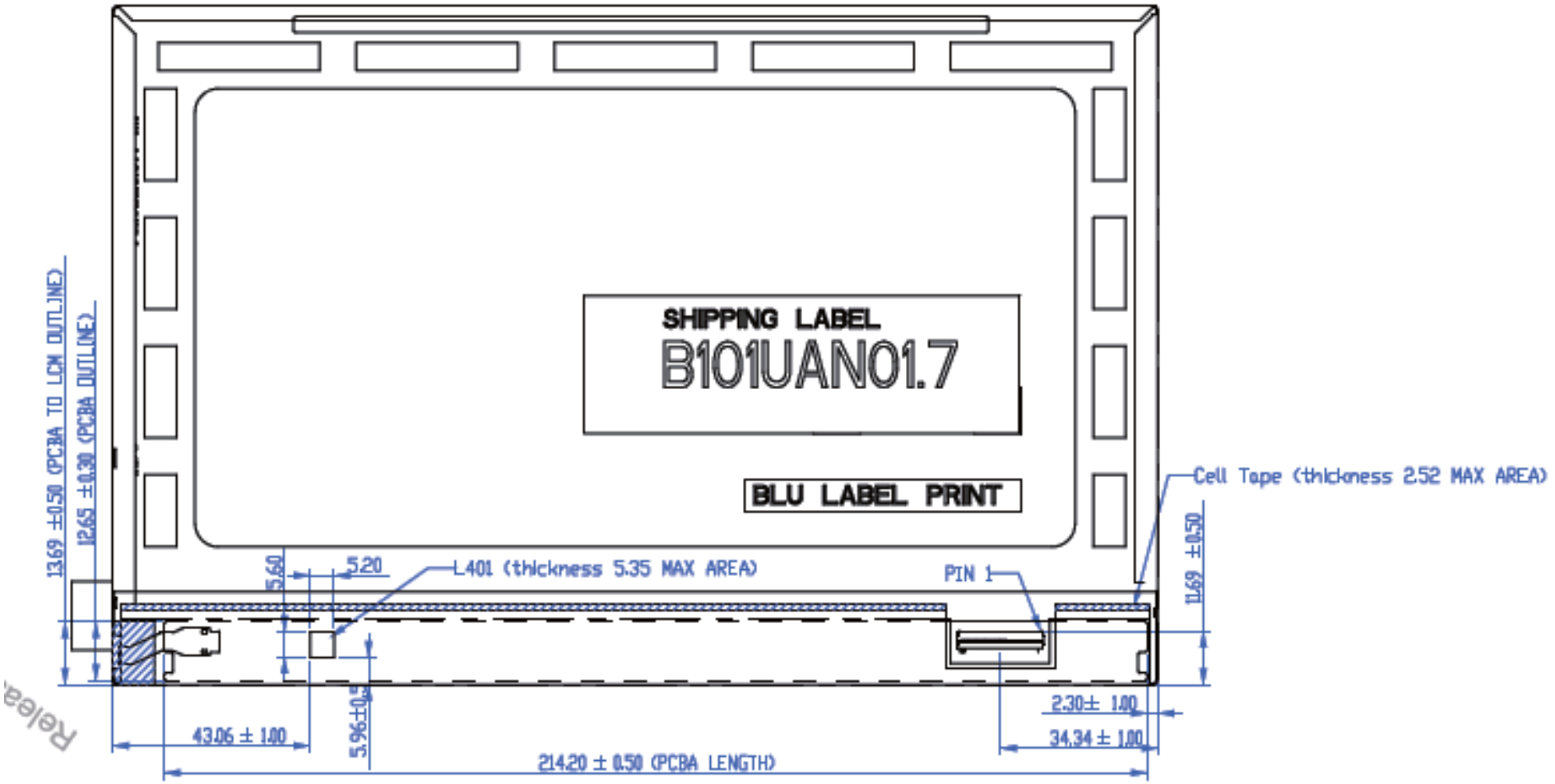
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View

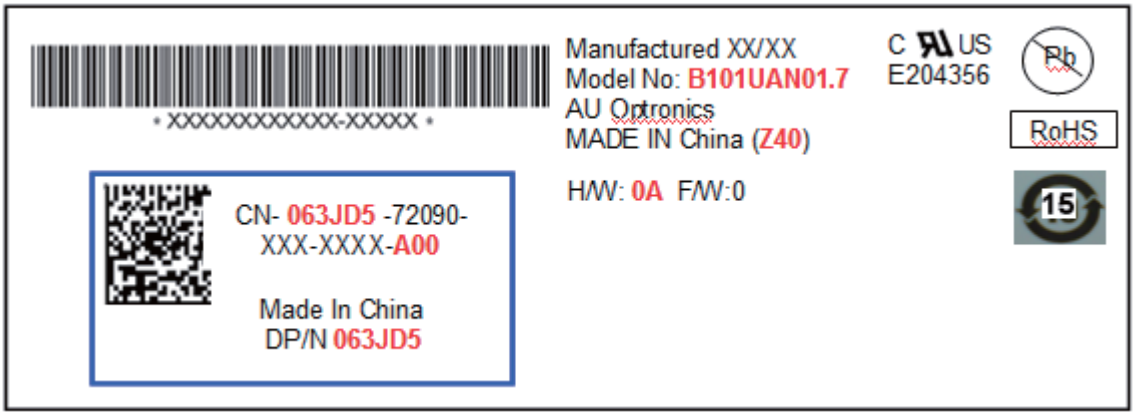


8.1.2 Standard Rear View

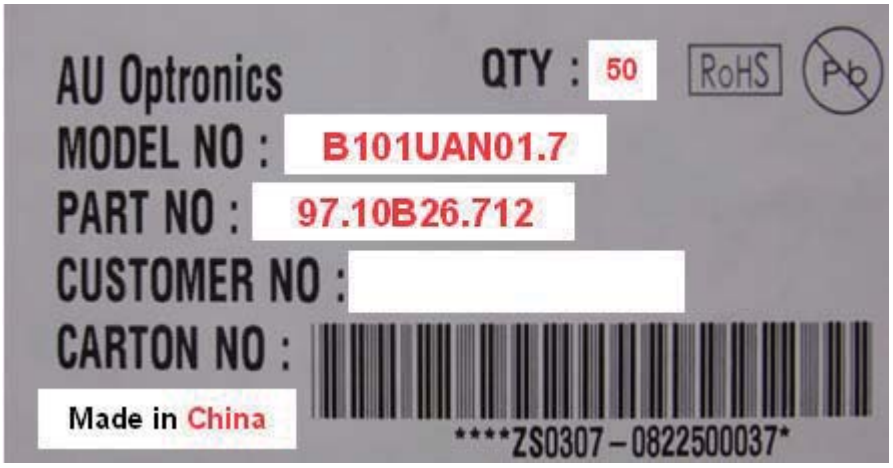


9. Shipping and Package

9.1 Shipping Label Format

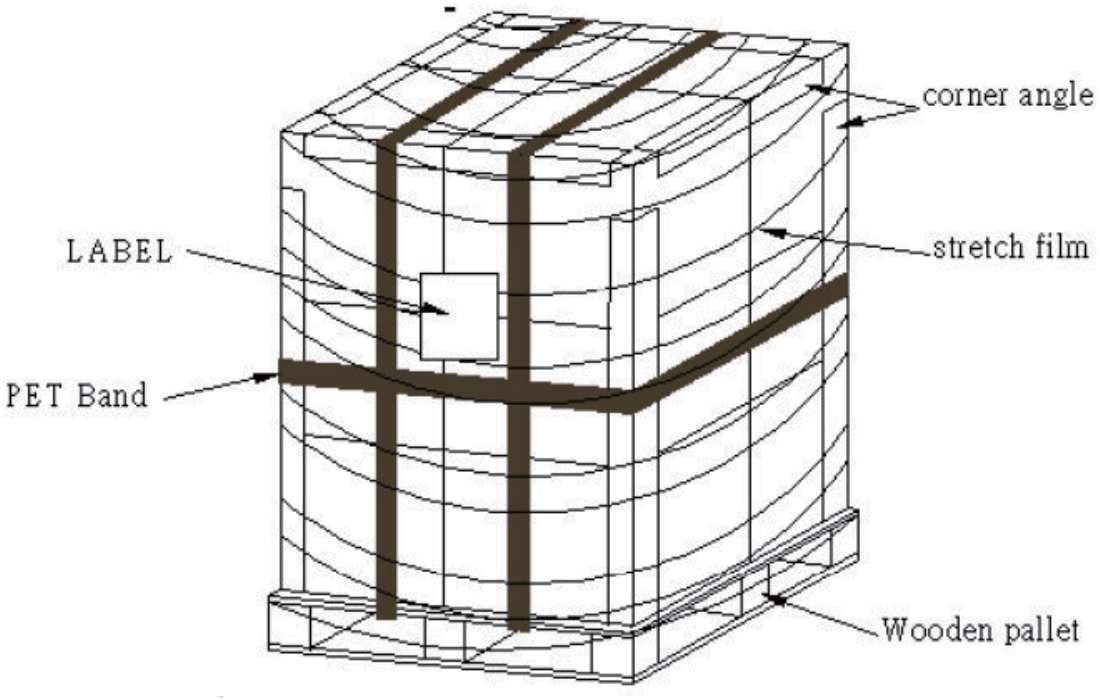


9.2 Carton Label Format



9.2 Carton Package

9.3 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

B101UAN01 7 EDID Code

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
Header	0	Header	00	00000000	0
	1	Header	FF	11111111	255
	2	Header	FF	11111111	255
	3	Header	FF	11111111	255
	4	Header	FF	11111111	255
	5	Header	FF	11111111	255
	6	Header	FF	11111111	255
	7	Header	00	00000000	0
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
	0A	Panel Supplier Reserved – Product Code	D8	11011000	216
	0B	Panel Supplier Reserved – Product Code	17	00010111	23
	0C	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	0D	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	0F	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	10	Week of manufacture	22	00100010	34
	11	Year of manufacture	18	00011000	24
	12	EDID structure version # = 1	01	00000001	1
	13	EDID revision # = 4	04	00000100	4
Display Parameters	14	Video I/P definition	A0	10100000	160
	15	Max H image size = ?? cm(Rounded to cm)	16	00010110	22
	16	Max V image size = ?? cm(Rounded to cm)	0E	00001110	14
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
	18	Feature support	02	00000010	2
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	D3	11010011	211
	1A	Blue/White Low bit (BxBy/WxWy)	A5	10100101	165
	1B	Red X Rx = 0.???	97	10010111	151
	1C	Red Y Ry = 0.???	57	01010111	87
	1D	Green X Rx = 0.???	53	01010011	83
	1E	Green Y Ry = 0.???	96	10010110	150
	1F	Blue X Rx = 0.???	27	00100111	39
	20	Blue Y Ry = 0.???	1F	00011111	31
	21	White X Rx = 0.???	50	01010000	80
	22	White Y Ry = 0.???	54	01010100	84
Established Timings	23	Established timings 1 (00h if not used)	00	00000000	0
	24	Established timings 2 (00h if not used)	00	00000000	0
	25	Manufacturer's timings (00h if not used)	00	00000000	0
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1
	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h if not used)	01	00000001	1
	2E	Standard timing ID5 (01h if not used)	01	00000001	1
	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	00000001	1
	35	Standard timing ID8 (01h if not used)	01	00000001	1
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	5E	01011110	94
	37	Pixel Clock/10,000 (MSB)	3D	00111101	61
	38	Horizontal Active = ???? pixels (lower 8 bits)	80	10000000	128
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	F0	11110000	240
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70	01110000	112
	3B	Vertical Active = ??? lines	B0	10110000	176
	3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	0C	00001100	12
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64
	3E	Horizontal Sync, Offset (Thfp) = ?? pixels	50	01010000	80
	3F	Horizontal Sync, Pulse Width = ??? pixels	50	01010000	80
	40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	44	01000100	68
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	42	Horizontal Image Size =??? mm	D8	11011000	216
	43	Vertical image Size = ??? mm	87	10000111	135
	44	Horizontal Image Size / Vertical image size	00	00000000	0
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26

Timing Descripter #2 (=Timing Descripter #1)	48	Pixel Clock/10,000 (LSB)	5E	01011110	94
	49	Pixel Clock/10,000 (MSB)	3D	00111101	61
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	80	10000000	128
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	F0	11110000	240
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70	01110000	112
	4D	Vertical Active = xxxx lines	B0	10110000	176
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	0C	00001100	12
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	50	01010000	80
	51	Horizontal Sync, Pulse Width = xxxx pixels	50	01010000	80
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	44	01000100	68
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	54	Horizontal Image Size =xxx mm	D8	11011000	216
	55	Vertical image Size = xxx mm	87	10000111	135
	56	Horizontal Image Size / Vertical image size	00	00000000	0
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
Timing Descripter #3 Dell specific information	5A	Flag	00	00000000	0
	5B	Flag	00	00000000	0
	5C	Flag	00	00000000	0
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
	5E	Flag	00	00000000	0
	5F	Dell P/N 1st Character	36	00110110	54
	60	Dell P/N 2nd Character	33	00110011	51
	61	Dell P/N 3rd Character	4A	01001010	74
	62	Dell P/N 4th Character	44	01000100	68
	63	Dell P/N 5th Character	35	00110101	53
	64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	0A	00001010	10
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	30	00110000	48
	68	Manufacturer P/N	31	00110001	49
	69	Manufacturer P/N	55	01010101	85
	6A	Manufacturer P/N	41	01000001	65
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	4E	01001110	78
Timing Descripter #4	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
	70	Flag	00	00000000	0
	71	Color Management	03	00000011	3
	72	Panel Structure	41	01000001	65
	73	Frame Rate	03	00000011	3
	74	Light Controller Interface and Luminance	A8	10101000	168
	75	Outdoor Features	01	00000001	1
	76	Multi-Media Features	01	00000001	1
	77	Multi-Media Features	00	00000000	0
	78	Special Features #1	00	00000000	0
	79	Special Features #2	03	00000011	3
	7A	Special Features #3	01	00000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
Chec	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	C9	11001001	201
					7936
				Sum	1F00