Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications
( ) Final Specifications

Module	**10.1”(10.1”) HD 16:9 Color TFT-LCD (RGB 6-bits+FRC) Without LED Backlight design**
Model Name	B101XAN01.3 (H/W:1A)
Note ( )	***Open Cell with LED driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		YW Lee	09/18/2013
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Terry Chien	09/18/2013
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.0 2013/03/12	All	Preliminary Edition for Customer		
0.1 2013/06/04	P26~ P27		Packing Update	
0.2 2013/09/18	P1		Update H/W code	
	P6		Update Color / Chromaticity Coodinates	
	P25		Update Shipping Label Format	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101XAN01.3 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit. The screen format is intended to support the 16:9 WXGA, 1,366(H) x768(V) screen and 16.7M colors without LED backlight driving circuit. All input signals are LVDS interface.

B101XAN01.3 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	255.28 (10.05inch)			
Active Area	[mm]	222.5214X 125.1072 typ			
Pixels H x V		1,366x3(RGB) x 768			
Pixel Pitch	[mm]	0.1629x 0.1629			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
Response Time	[ms]	25 typ / 35 Max			
Power Consumption (Column Inversion)	[Watt]	0.7W pattern (without LED driver)			
Weight	[Grams]	57g max (Open Cell Only)			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	230.42	230.62	230.82
		Width	135.61	135.81	136.01
		Thickness		0.805	0.865 (Panel Side) 1.8 (PCBA Side)
Electrical Interface		40 pin LVDS, with LED driver			
Glass Thickness	[mm]	0.25			
Surface Treatment		HC＋LR			

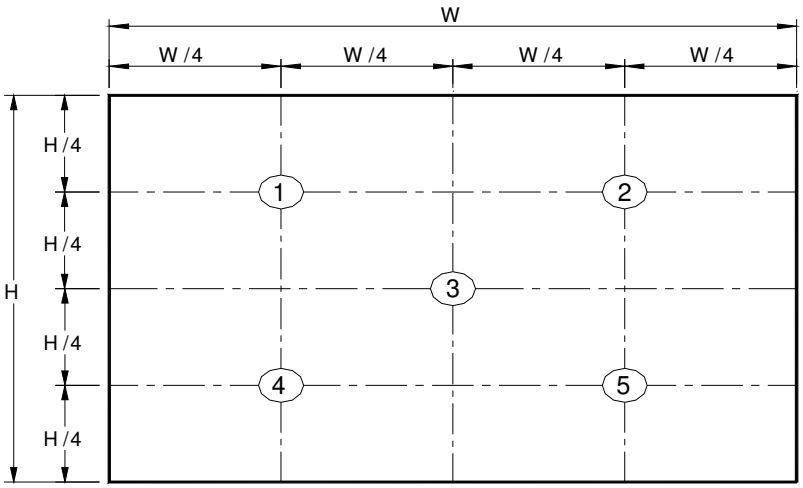
Support Color		16.7M colors (RGB 6-bits+FRC)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -20 to +60 -30 to +70
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

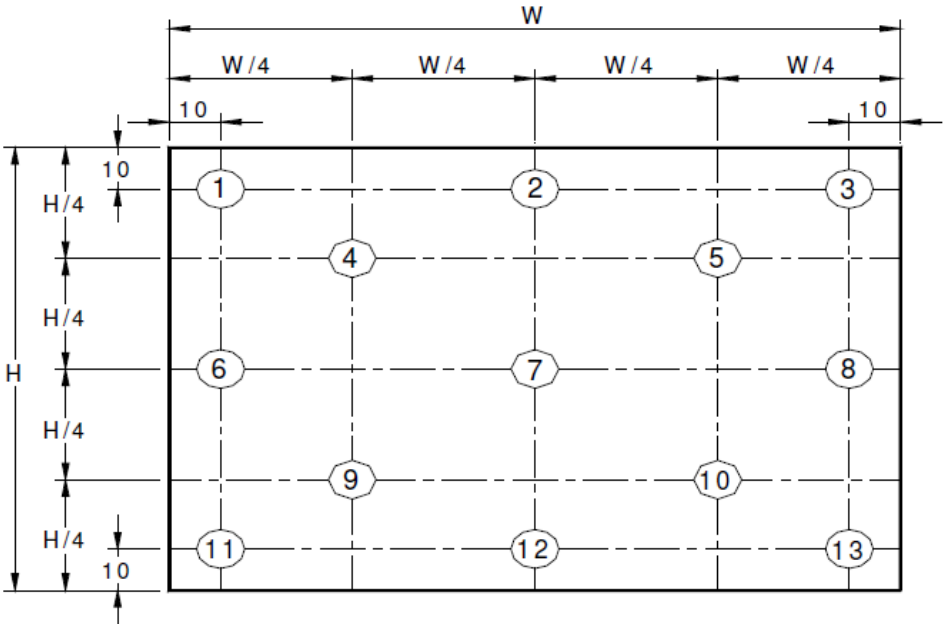
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	-	-	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	80	85	-	degree	4, 9
		θ_L	(Left)	80	85	-		
		ϕ_H	Vertical (Upper) CR = 10	80	85	-		
		ϕ_L	(Lower)	80	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	-		Open cell
Luminance Uniformity		δ_{13P}	13 Points	-	-	-		
Contrast Ratio		CR		700	900	1500		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	25	35	ms	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.558	0.588	0.618		Open cell
		Ry		0.318	0.348	0.378		
	Green	Gx		0.296	0.326	0.356		
		Gy		0.543	0.573	0.603		
	Blue	Bx		0.135	0.165	0.195		
		By		0.083	0.113	0.143		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



【Object to be managed by priority】

Minimum Brightness Uniformity : 70%

The hot spot & uniformity must be OK when check it by visual

【Measurement Condition】

Measurement Point : 13 point **(如上圖)**

Uniformity : (Min)/(Max) × 100%

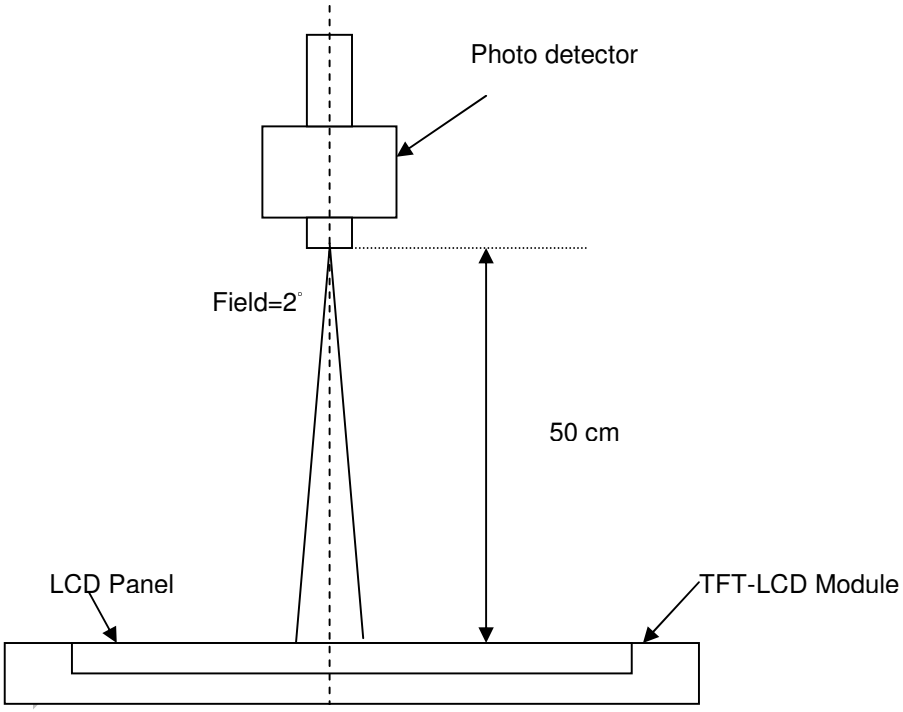
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

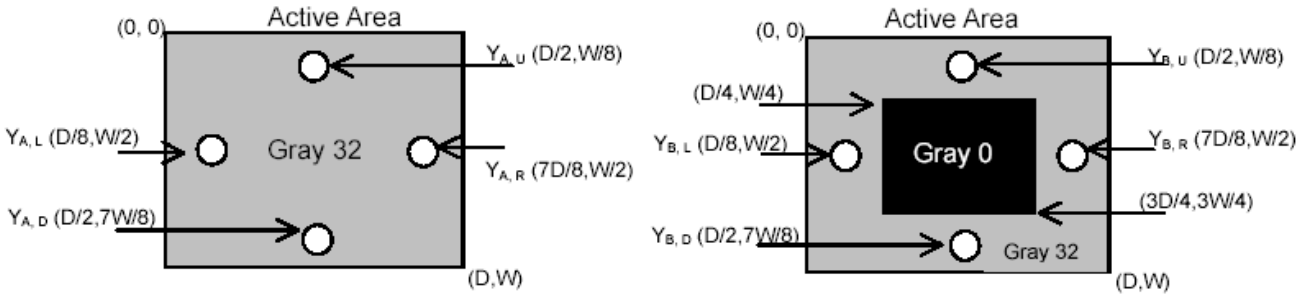
Note 7： Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Where

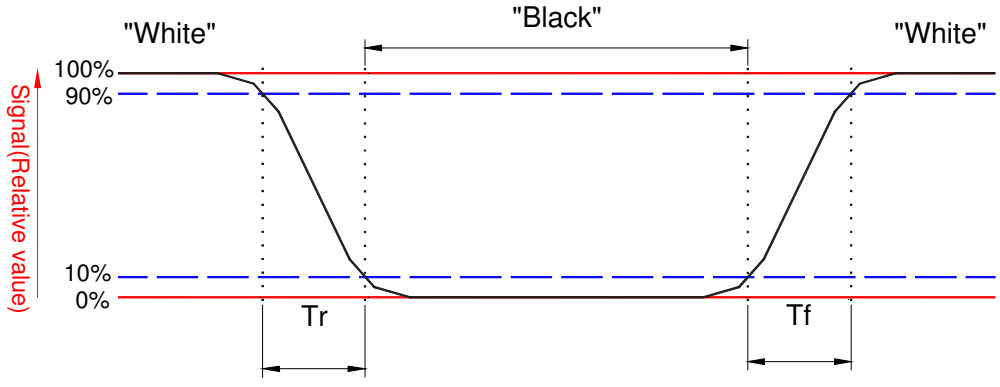
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



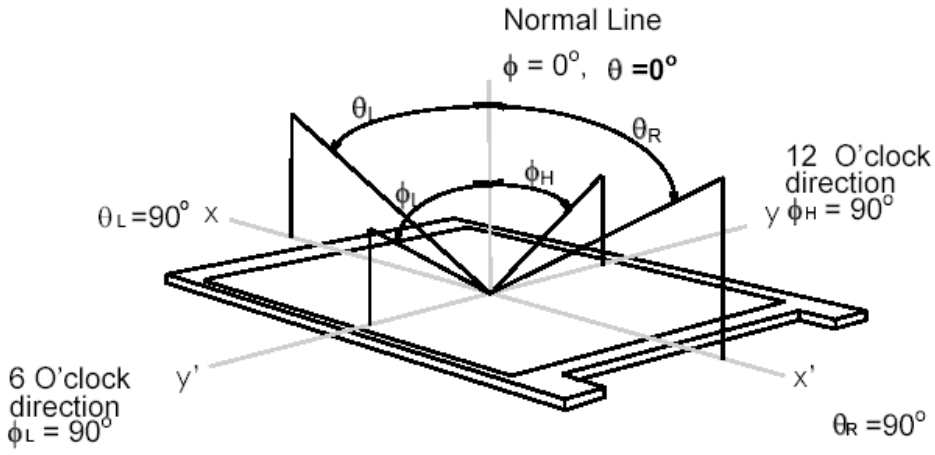
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

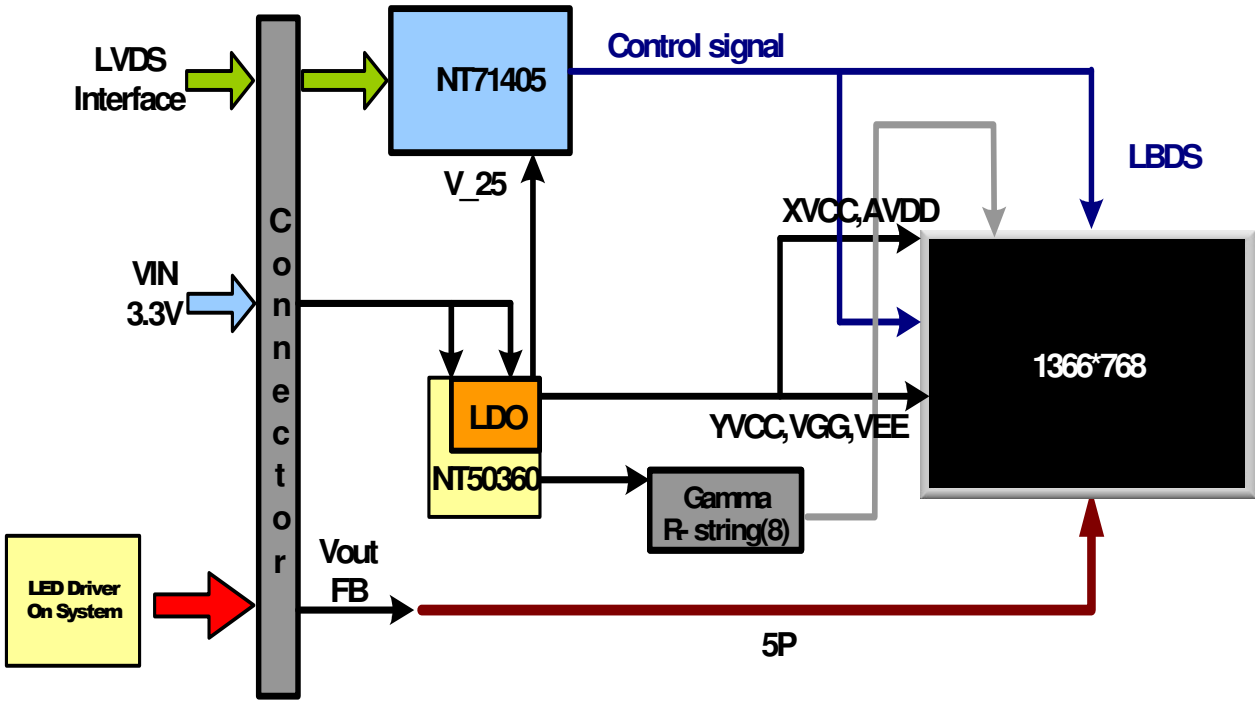


Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-20	+60	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-30	+70	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

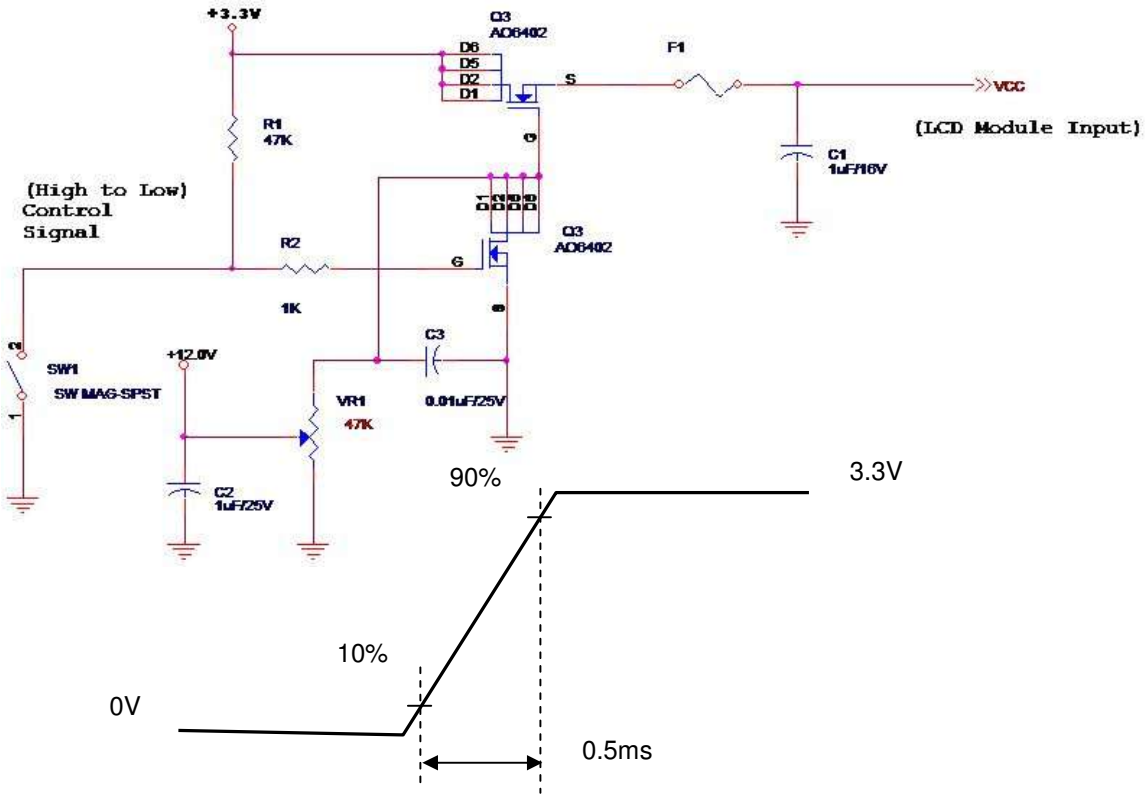
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	TBD	[Watt]	Note 1
IDD	IDD Current	-	-	TBD	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Measurement Condition：White Pattern at 3.3V driving voltage. (P_{max}=$V_{3.3}$ x I_{white})

Note 2：Measure Condition



Vin rising time

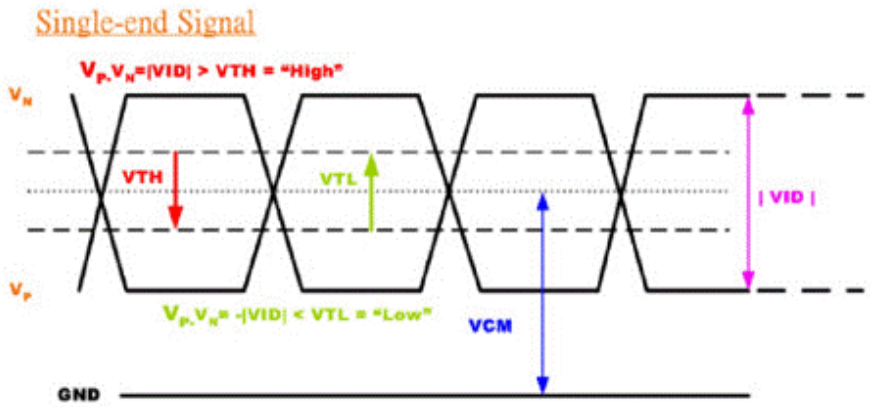
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
V_{ID}	Differential Input Voltage	TBD	TBD	[mV]
V_{cm}	Differential Input Common Mode Voltage	0.2	2.2	[V]

Note: LVDS Signal Waveform



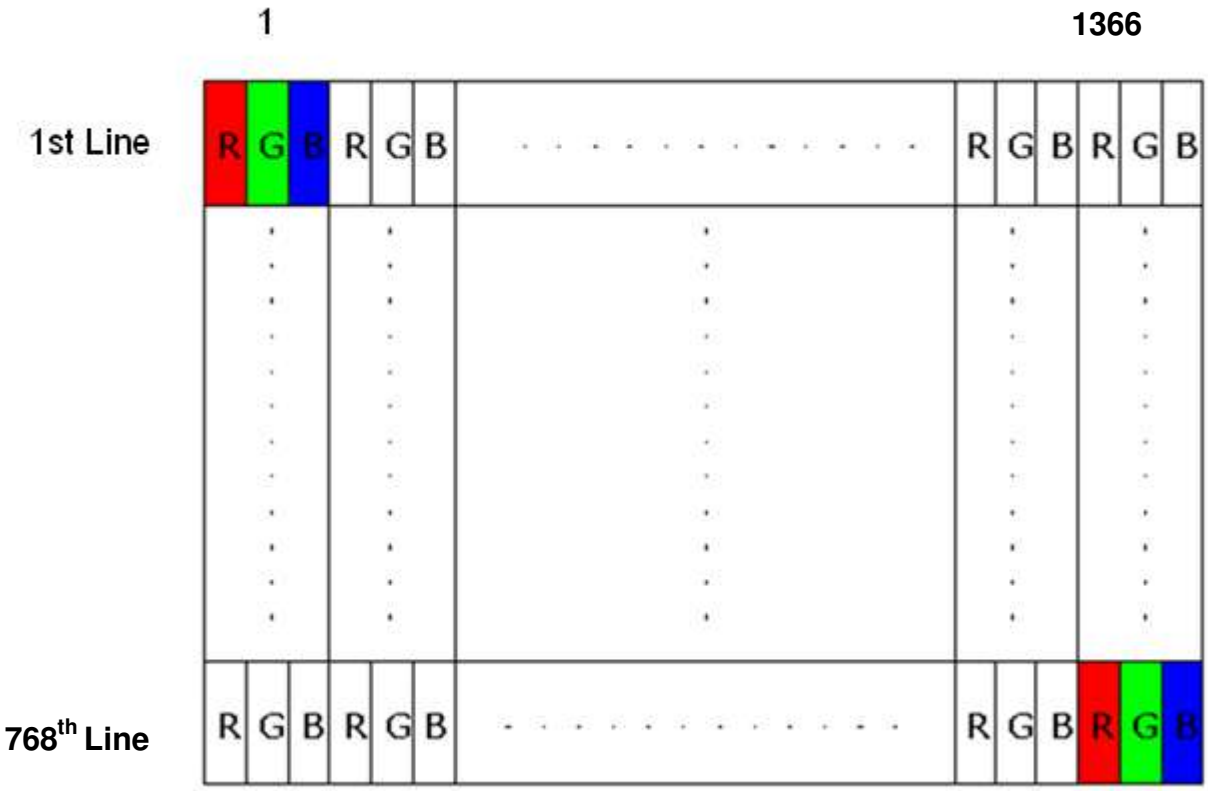
5.1.3 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.5		14	[Volt]	Define as Connector Interface (Ta=25℃)
PWM Logic Input High Level	VPWM_EN		2.5		[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	-	2k	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

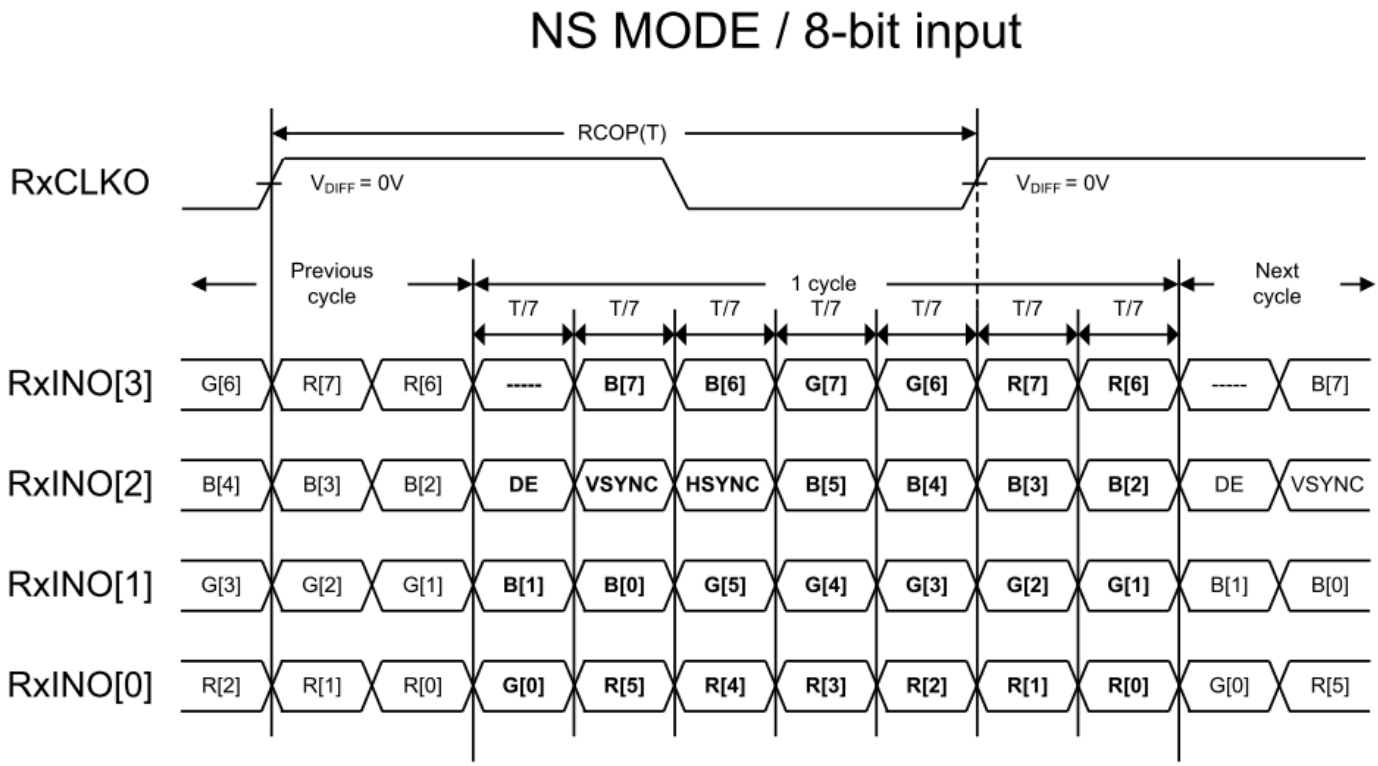
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.
G7 G6 G5 G4 G3 G2 G1 G0	Green Data 7(MSB) Green Data 6 Green Data 5 Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2	Blue Data 8(MSB) Blue Data 7 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.

B1 B0	Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note1: DE Mode Only.
Note 2: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	DDK
Type / Part Number	FPC / FF12-40A-R12BN-D3
Mating Housing/Part Number	NA

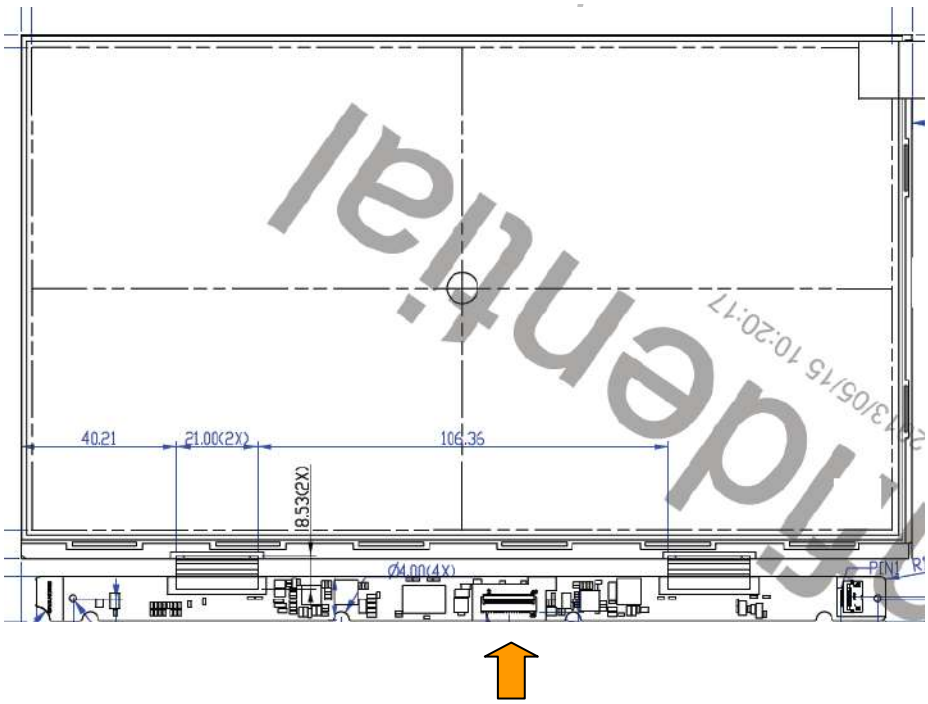
6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

No.	Pin Name	Description
1	VDD	Power Supply +3.3V
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	NC	Not Connection
5	SDA	EDID Data Input
6	SCL	EDID Clock Input
7	GND	Ground
8	GND	Ground
9	NC	Not Connection
10	LEDPWM	Backlight LED driver PWM Input
11	LED_EN	LED Enable Input
12	AGING	Aging Mode Power Supply (AUO only)
13	NC	Not Connection
14	GND	Ground
15	Rin0-	LVDS data pair 0 negative signal
16	Rin0+	LVDS data pair 0 positive signal
17	GND	Ground
18	Rin01-	LVDS data pair 1 negative signal
19	Rin1+	LVDS data pair 1 positive signal
20	GND	Ground
21	Rin02-	LVDS data pair 2 negative signal
22	Rin2+	LVDS data pair 2 positive signal

23	GND	**Ground**
24	DSI_CLKN/Rx-CLKN	**LVDS Clock negative signal**
25	DSI_CLKP/Rx-CLKP	**LVDS Clock positive signal**
26	GND	**Ground**
27	Rin3-	**LVDS data pair 3 negative signal**
28	Rin3+	**LVDS data pair 3 positive signal**
29	GND	**Ground**
30	LED-	**LED Ground**
31	LED-	**LED Ground**
32	LED-	**LED Ground**
33	LED-	**LED Ground**
34	NC	**Not Connection**
35	NC	**Not Connection**
36	NC	**Not Connection**
37	LED+	**LED Power Supply**
38	LED+	**LED Power Supply**
39	LED+	**LED Power Supply**
40	LED+	**LED Power Supply**

Connector 插入方向如下



6.4 Interface Timing

6.4.1 Timing Characteristics

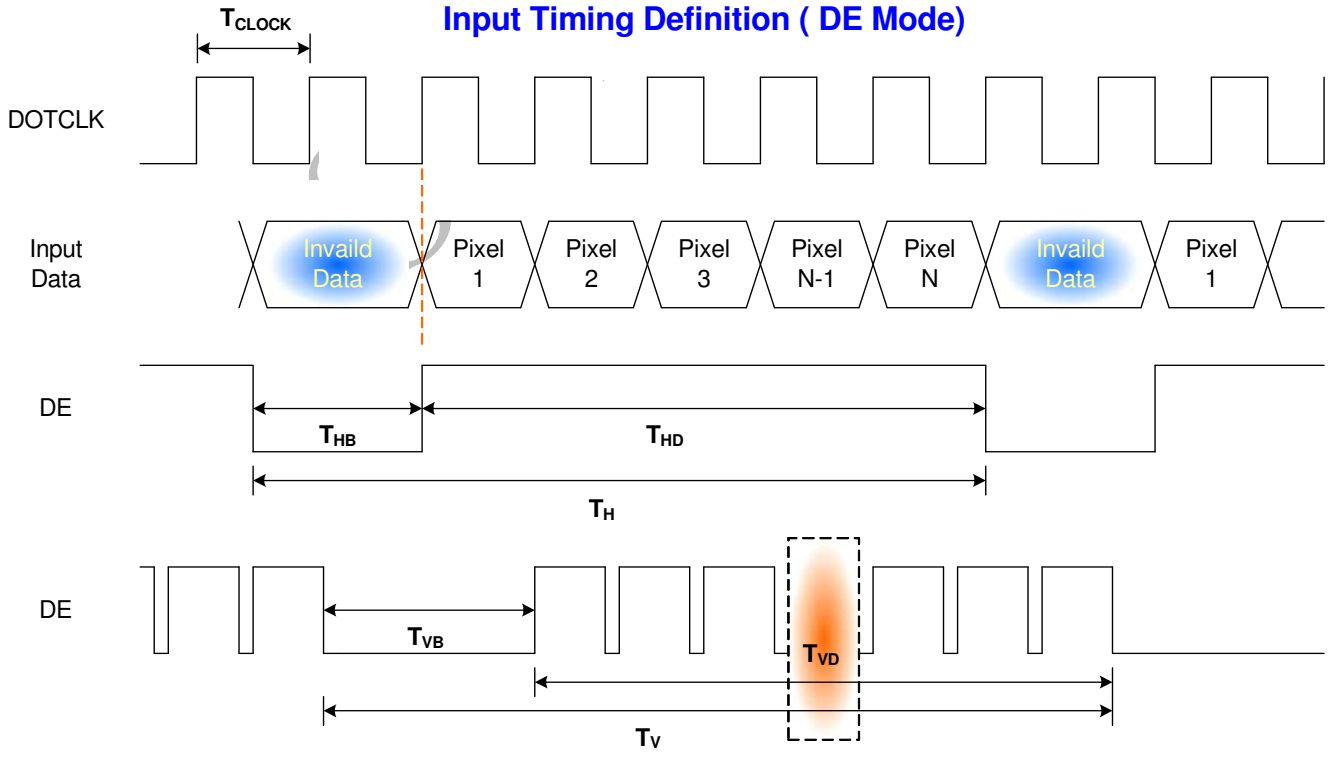
Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	66.9	70.7	80	MHz
Vertical Section	Period	T_V	777	797	808	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	20	29	40	
Horizontal Section	Period	T_H	1406	1478	2610	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	40	112	1244	

Note 1 : The above is as optimized setting
Note 2 : DE mode only
Note 3 : The maximum clock frequency = (1366+B)*(768+A)*60<80MHz

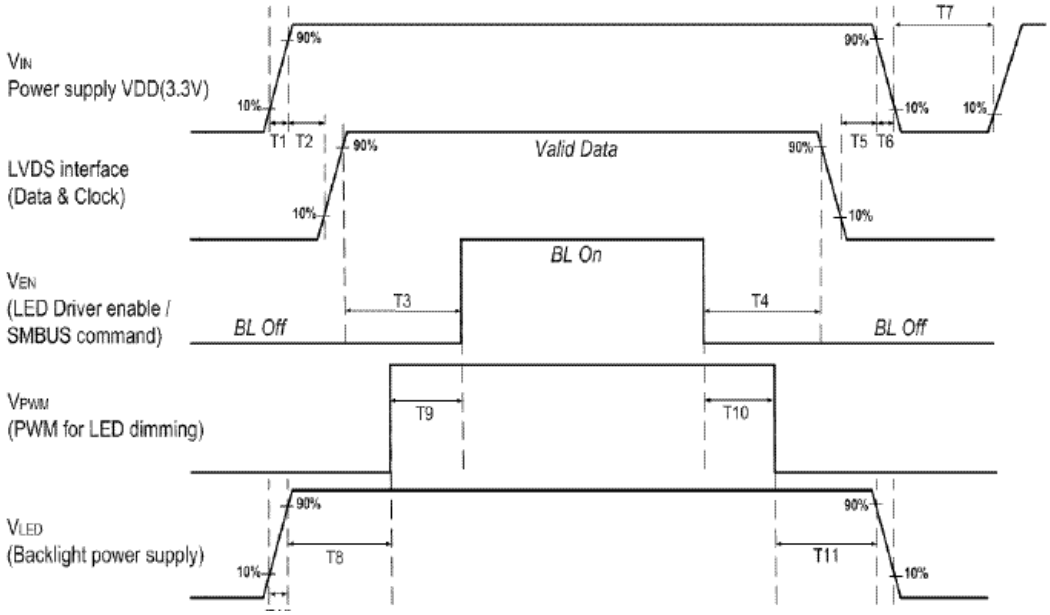
Note 4 : Clock frequency number is for reference, real setting value refer to EDID (Clock frequency 70.7MHz) --- This item only for Samsung, pls help to delete this item for other customer.

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



	Min (ms)	Max (ms)
T1	0.5	10
T2	0	50
T3	200	-
T4	200	-
T5	0	50
T6	0	10
T7	500	-
T8	10	-
T9	10	-
T10	10	-
T11	10	-
T12	0.5	10

Note 1 : If T3<200ms, the display garbage may occur. (T3>200ms is recommended)

Note 2 : If T1 or T12<0.5ms, the inrush current may cause the damage of fuse. If T1 or T12<0.5ms, the inrush current I^2t is under typical melt of fuse Spec, there is no mentioned problem.

Note 3 : T8,T9,T10,T11 value are recommended, T8,T9,T10,T11≧0 could be acceptable--- This item only for Samsung, pls help to delete this item for other customer.

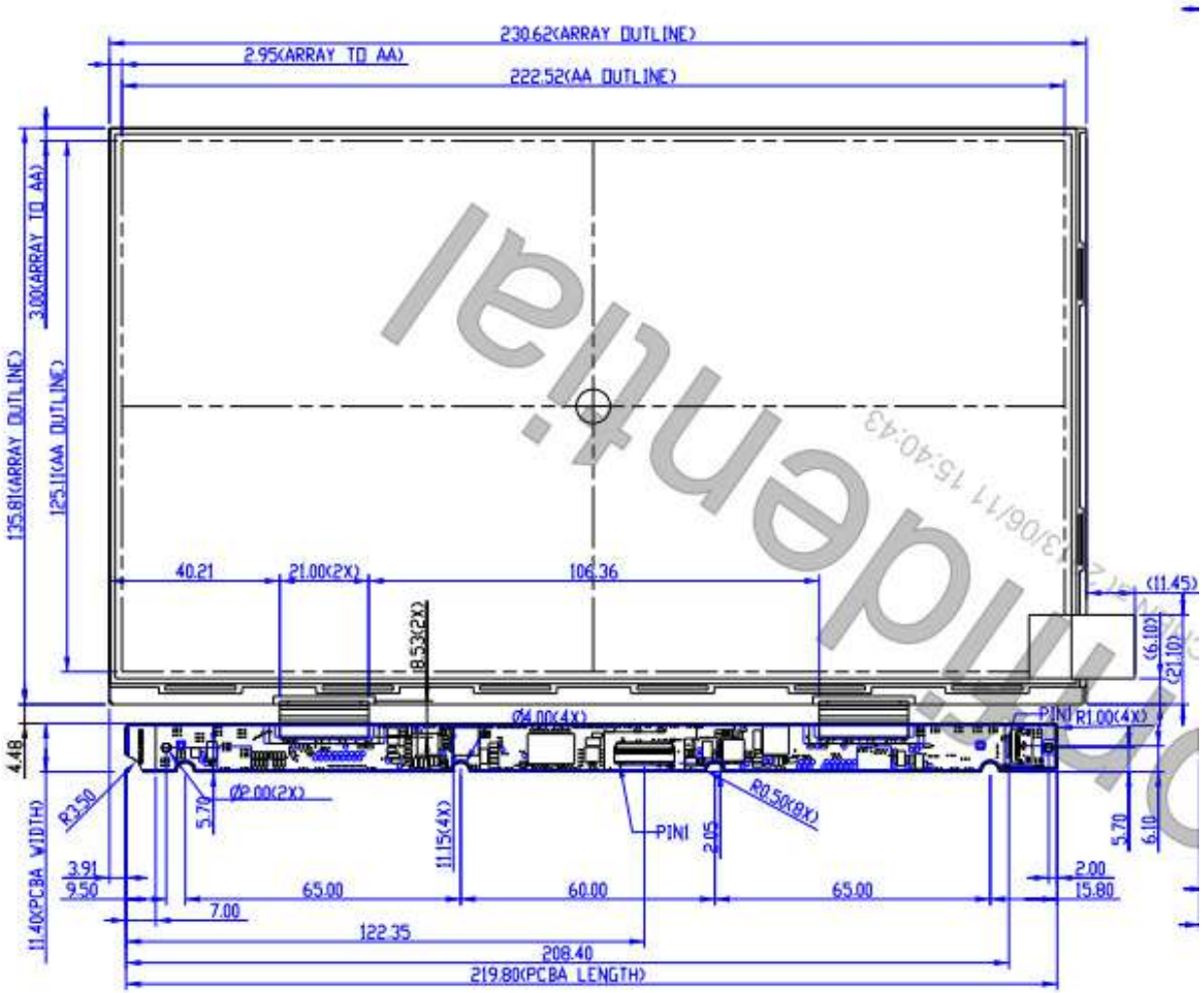
7. Panel Reliability Test

TBD

8. Mechanical Characteristics

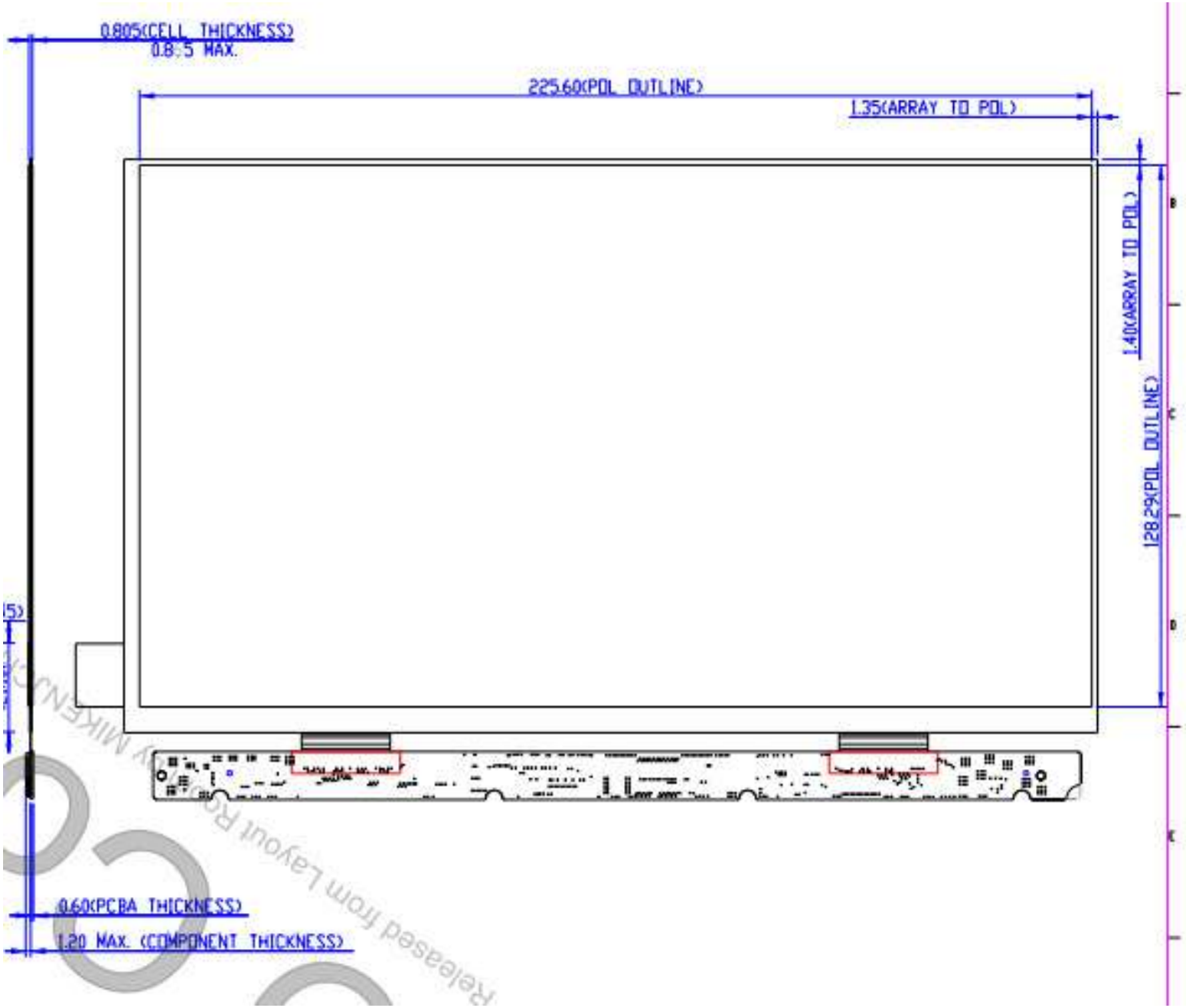
8.1 Open Cell Outline Dimension

8.1.1 Front View



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

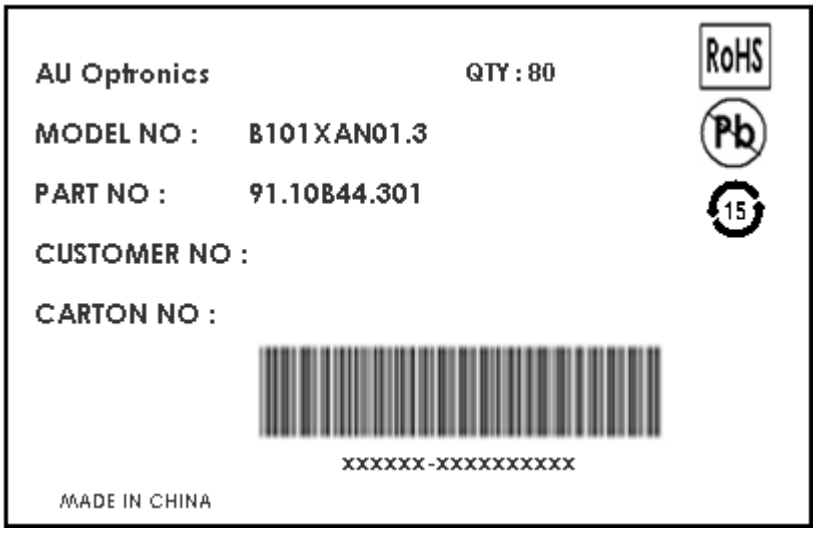
8.1.2 Rear View



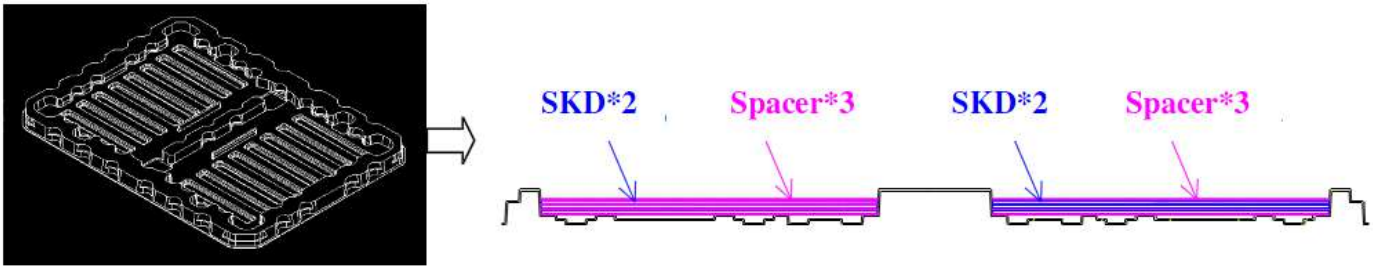
9. Shipping and Package

9.1 Shipping Label Format

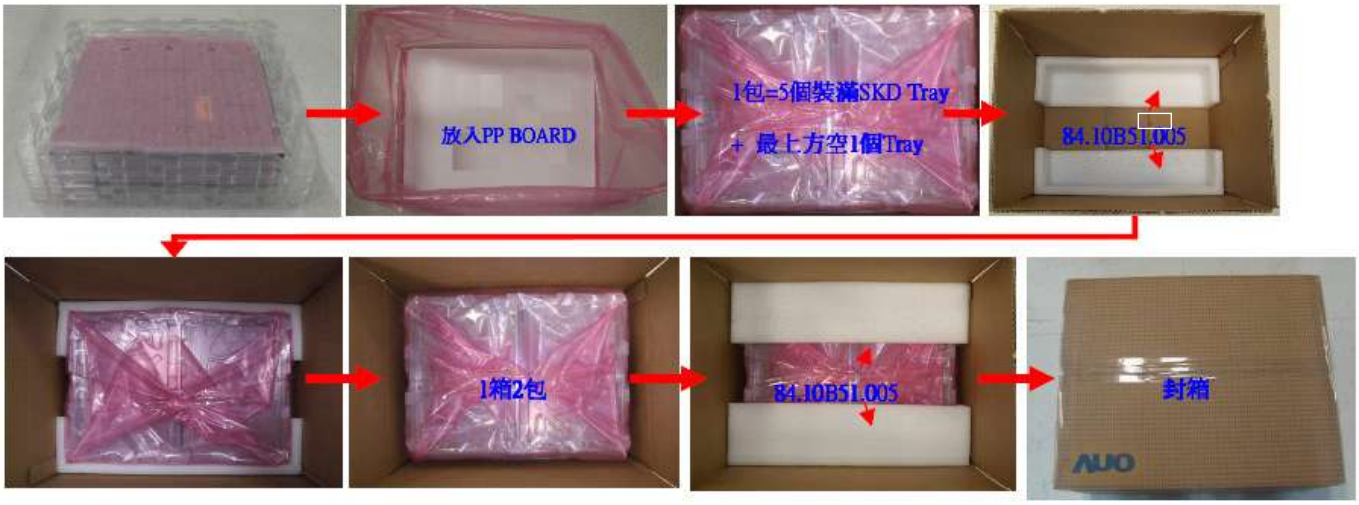
9.2 Carton Label Format



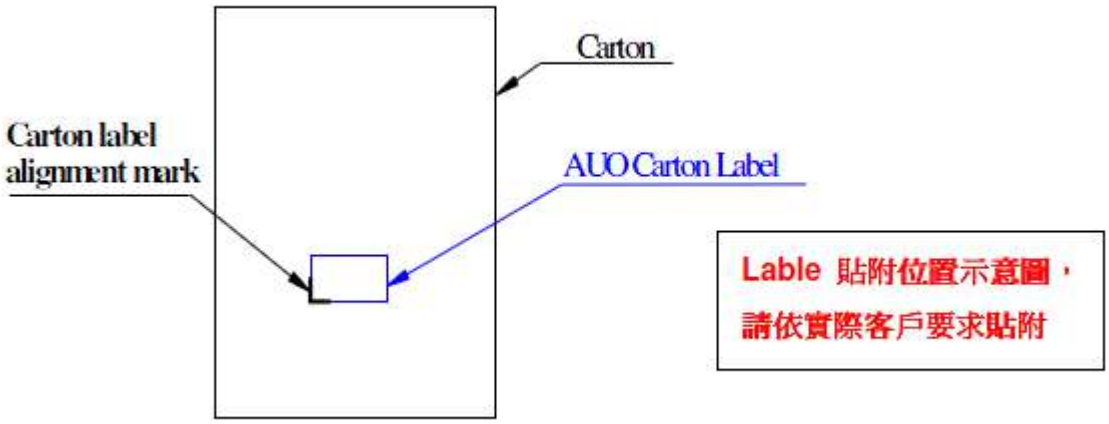
9.3 Packing Flow

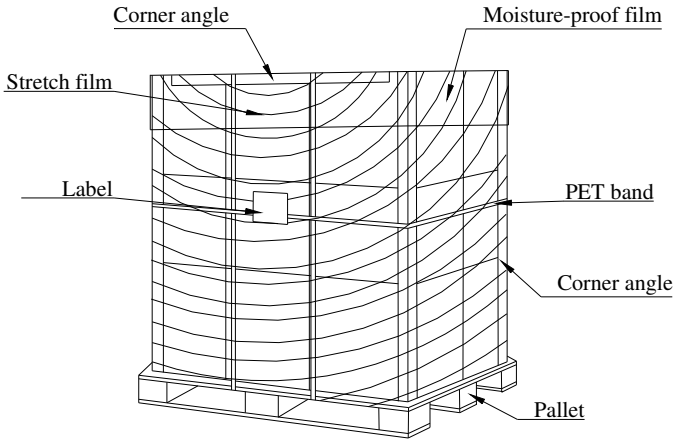


PET Tray 共 2 穴，每穴放 2pcs SKD(正面朝上放置)，Panel 中間以及上下各間隔放置 EPE spacer，故 1tray 共有 4pcs SKD，6pcs Spacer，放滿后於其上再放置 1pcs 空 tray，依序正向堆疊 tray 盤！



9.4 Shipping Package of Palletizing Sequence





10. Appendix: EDID Description

B101XAN01 3 EDID Code

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	DC	11011100	220	
0B	hex, LSB first	13	00010011	19	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	08	00001000	8	
11	Year of manufacture	17	00010111	23	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def. (digital I/P, non-TMDS, CRGB)**	A0	10100000	160	
15	**Max H image size (rounded to cm)**	16	00010110	22	
16	**Max V image size (rounded to cm)**	0D	00001101	13	
17	**Display Gamma (=(gamma*100)-100)**	78	01111000	120	
18	**Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)**	02	00000010	2	
19	Red/green low bits (Lower 2:2:2:2 bits)	99	10011001	153	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	85	10000101	133	
1B	Red x (Upper 8 bits)	95	10010101	149	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	56	01010110	86	
1E	Green y	92	10010010	146	
1F	Blue x	28	00101000	40	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	

27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	9E	10011110	158	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active Lower 8bits	56	01010110	86	
39	Horz blanking Lower 8bits	70	01110000	112	
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80	
3B	Vertical Active Lower 8bits	00	00000000	0	
3C	Vertical Blanking Lower 8bits	1D	00011101	29	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	46	01000110	70	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	DE	11011110	222	
43	Vertical Image Size Lower 8bits	7D	01111101	125	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	00	00000000	0	
45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	

53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	30	00110000	48	0
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	58	01011000	88	X
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	31	00110001	49	1
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	33	00110011	51	3
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	

7F	Checksum	0D	00001101	13	
			SUM	6144	
			SUM to HEX	1800	