( ) Preliminary Specifications
(V) Final Specifications

Module	**10.1”(10.05”) HD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B101XTN01.1 (H/W:1A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
	MM/DD/YYYY	YW Lee	09/16/2013
Checked & Approved by	**Date**	**Prepared by**	**Date**
	MM/DD/YYYY	Bing Ho	09/16/2013
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/08/23	All	First Edition for Customer	Renew shipping label and anti-glare	
0.2 2012/09/11	5	Anti-Glare, Hardness 3H, Low Reflection	Only “Anti-Glare, Hardness 3H”	
0.3 2012/09/17	26		Updated shipping & carton label	
0.4 2012/11/26	11 & 28		Updated Functional Block Diagram & Appendix: EDID Description	
0.5 2012/12/14	18& 19	Mating of MSAK24025P40 Led Power Supply:7V-21V	Led Power Supply:6V-21V Mating of MSAK24025P40 Or Compatible	
2012/12/24	6&12		Updated optical characteristic and Absolutel Rating of TFT LCD Module	
Final 2013/01/24	All	First Final Edition for Customer	Updated EDID format	
1.1 2013/05/31	28		Update Pixel Clock with 70MHz	
1.2 2013/09/16	26		Shipping label format UL Mark Alteration	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101XTN01.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B101XTN01.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	255.28			
Active Area	[mm]	222.52 x 125.11			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.1629X0.1629			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=20mA) **(Note: ILED is LED current)**	[cd/m^2]	200 typ. (5 points average)			
Luminance Uniformity		1.25 (5 points average)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.6 max. (Include Logic and Blu power)			
Weight	[Grams]	170 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	242.5	243.0	243.5
		Width	146.0	146.5	147.0
		Thickness	-	3.3	3.6
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti-Glare, Hardness 3H,			
Support Color		262K colors (RGB 6-bit)			

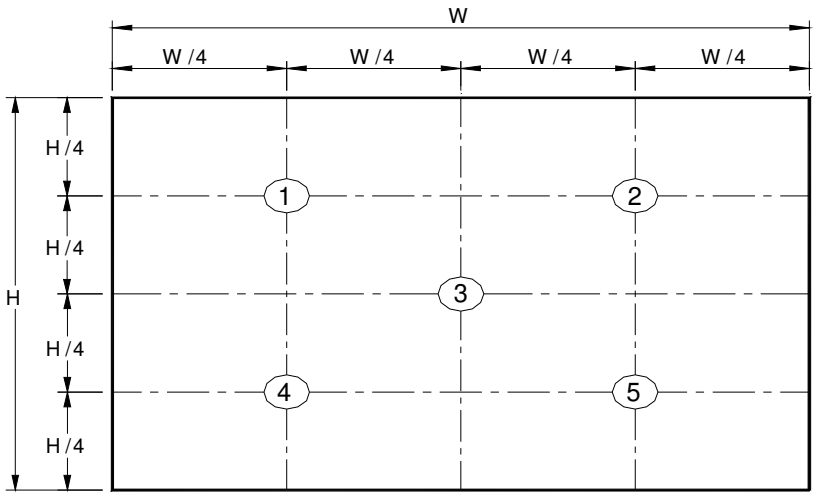
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

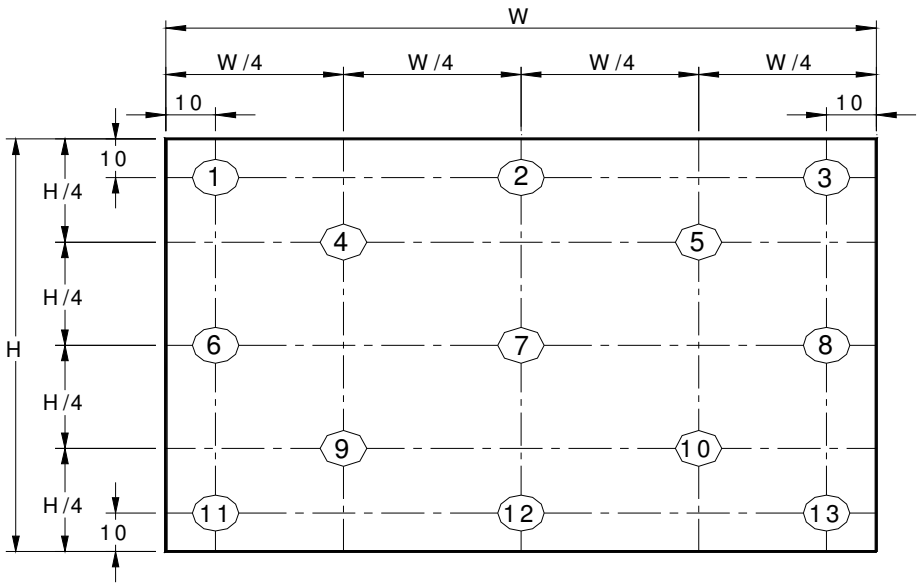
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	165	200	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
		ϕ_H ϕ_L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		300	400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.543	0.573	0.603		4
		Ry		0.303	0.333	0.363		
	Green	Gx		0.303	0.333	0.363		
		Gy		0.534	0.564.	0.594		
	Blue	Bx		0.128	0.158	0.188		
		By		0.103	0.133	0.163		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



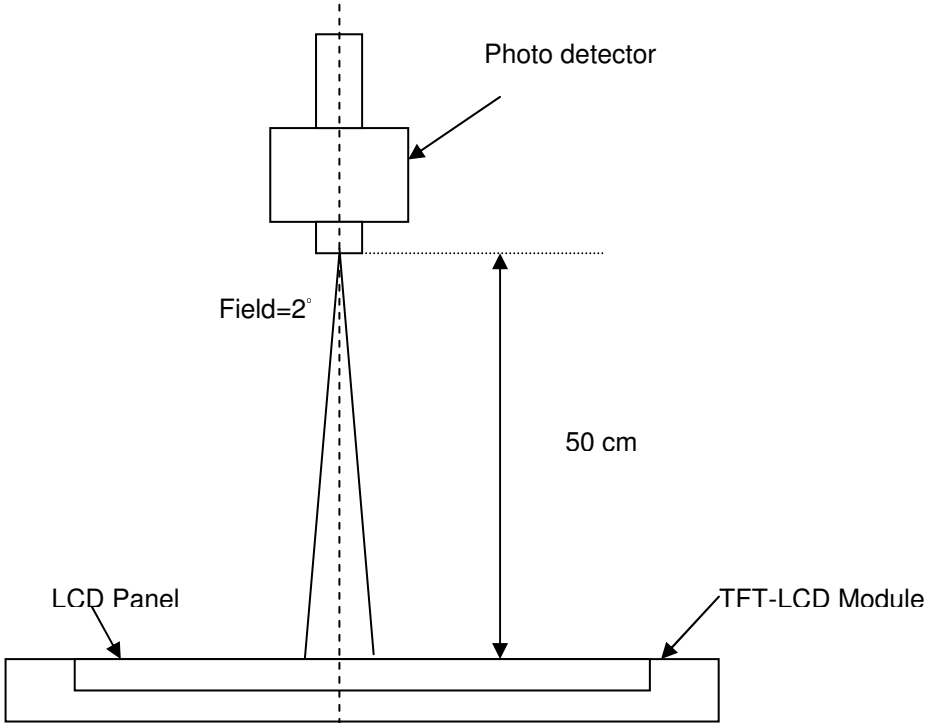
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

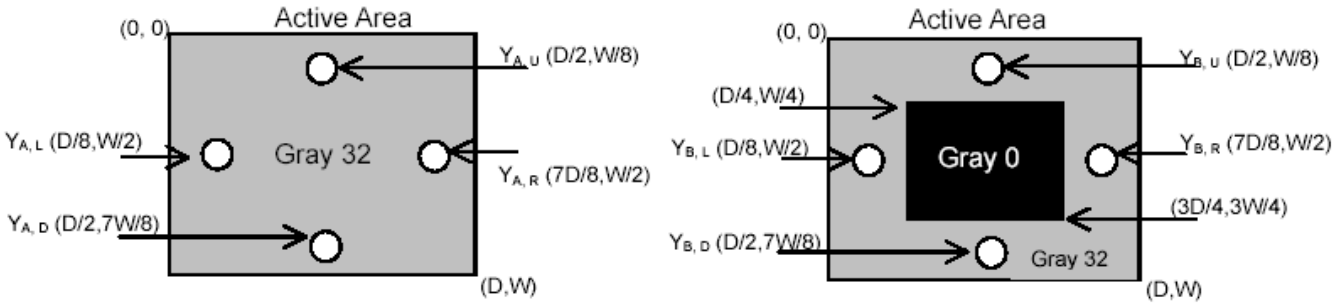
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

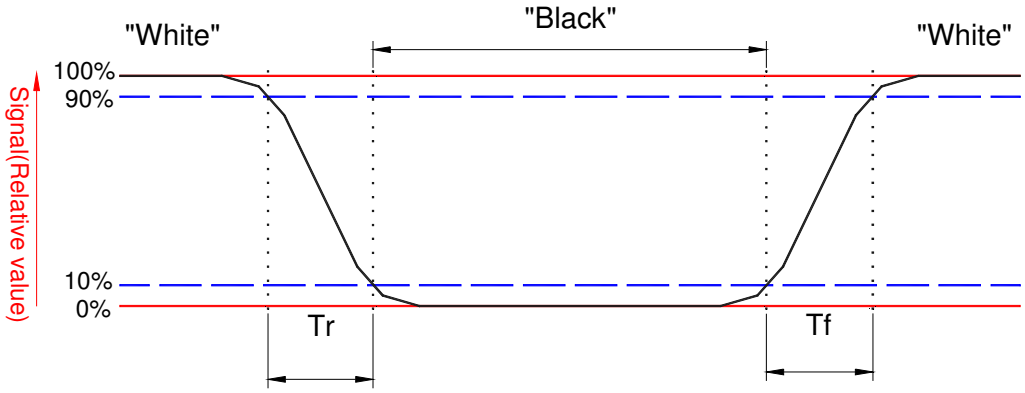
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



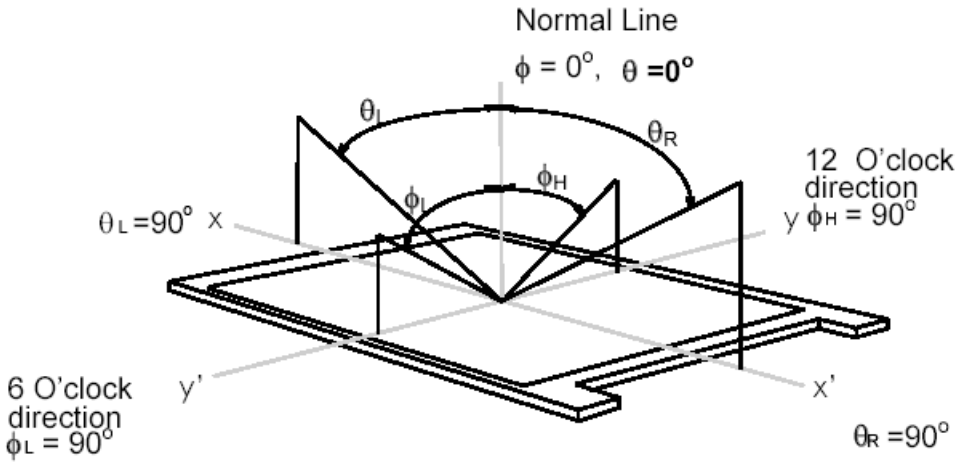
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



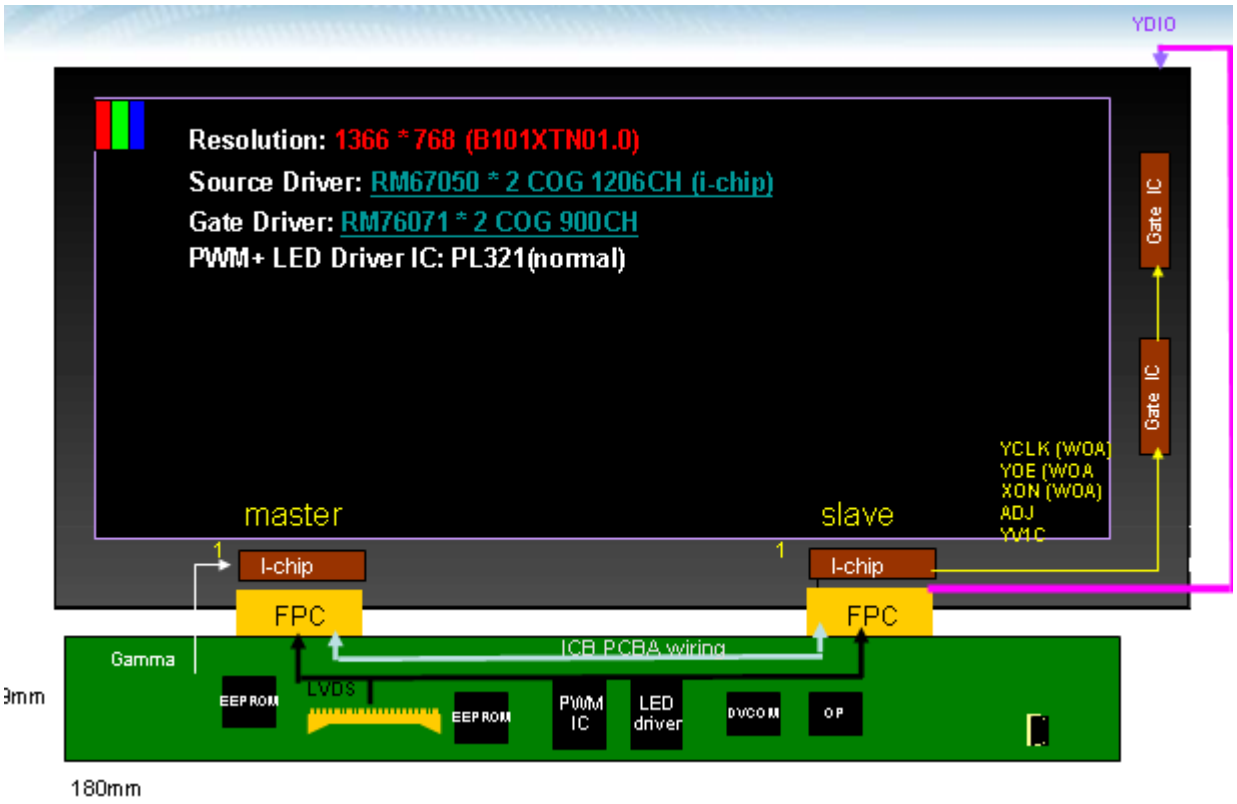
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	3.0	3.6	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

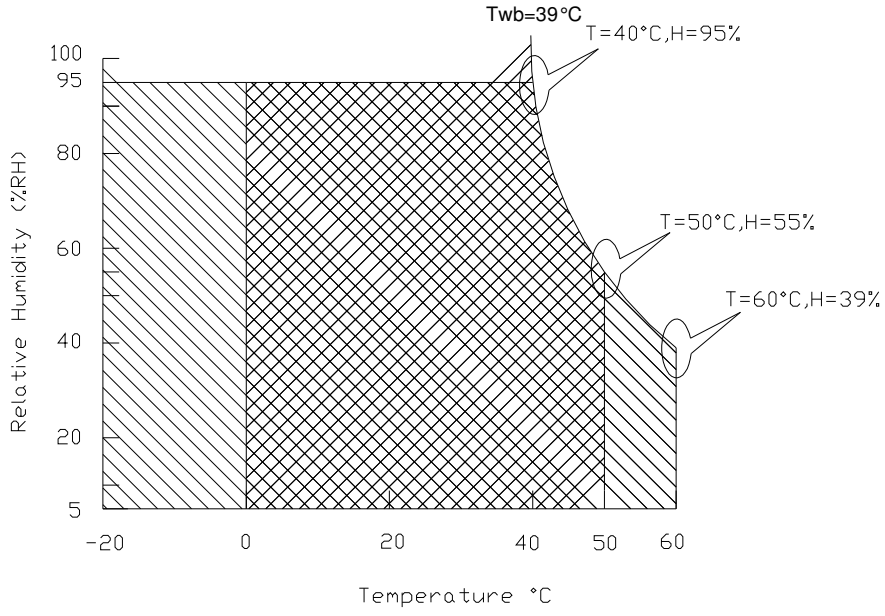
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

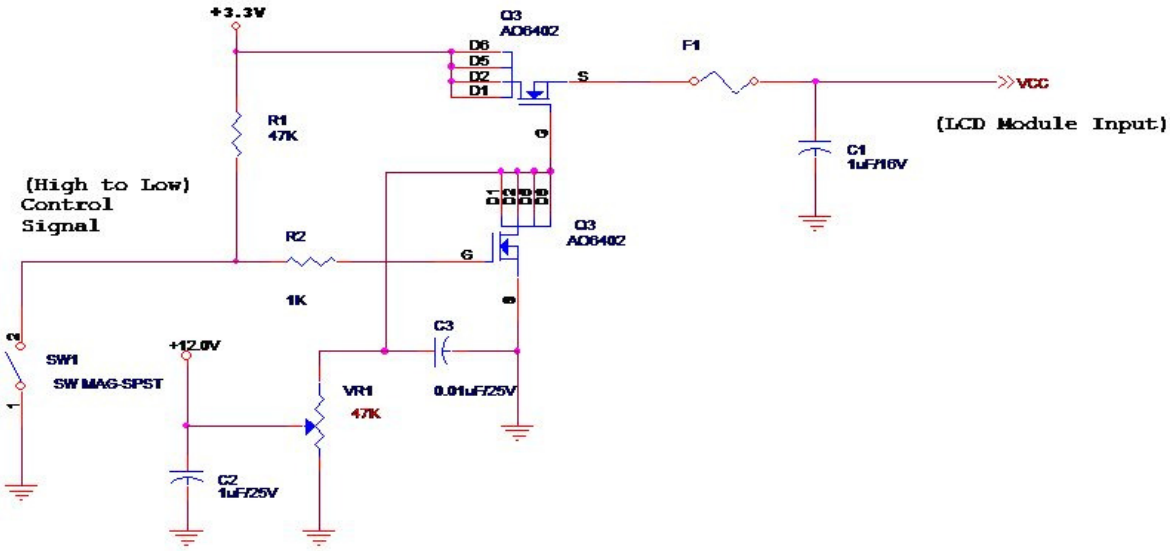
The power specification are measured under 25℃ and frame frenquency under 60Hz

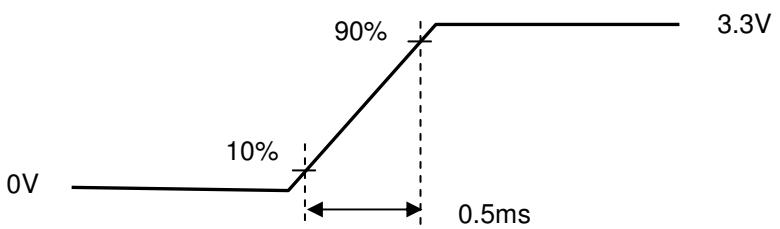
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	606	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition : Mosaic Pattern

Note 2 : Measure Condition





Vin rising time

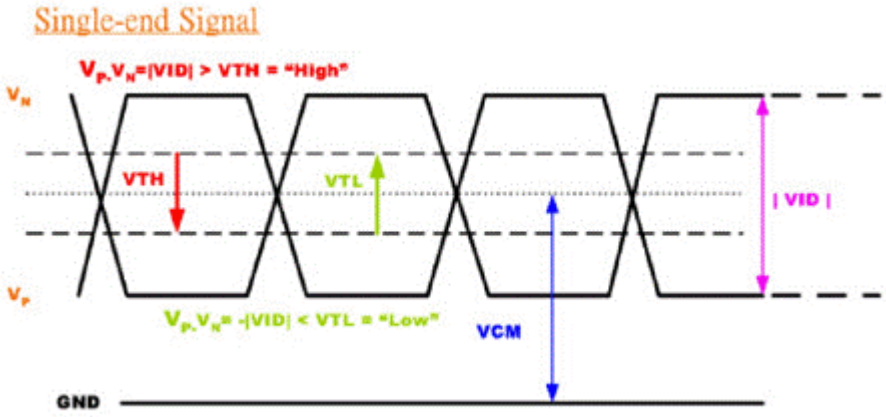
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
$\|V_{ID}\|$	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.8	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

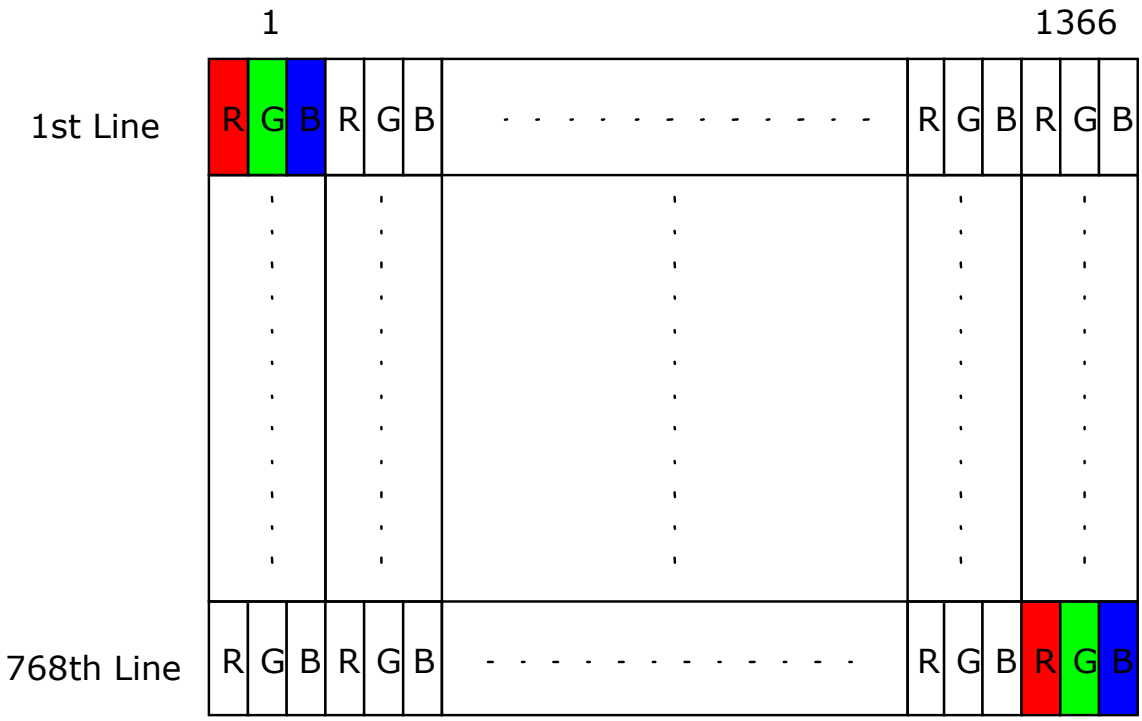
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

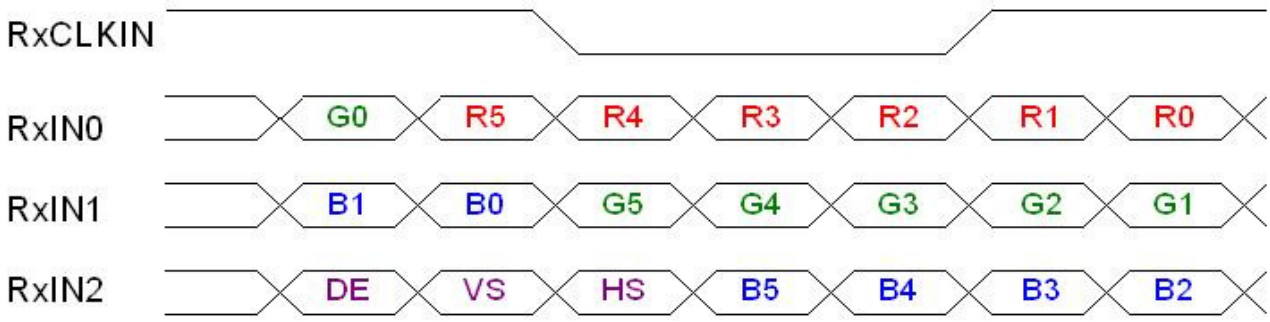
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STM
Type / Part Number	MSAK24025P40
Mating Housing/Part Number	Mating of MSAK24025P40

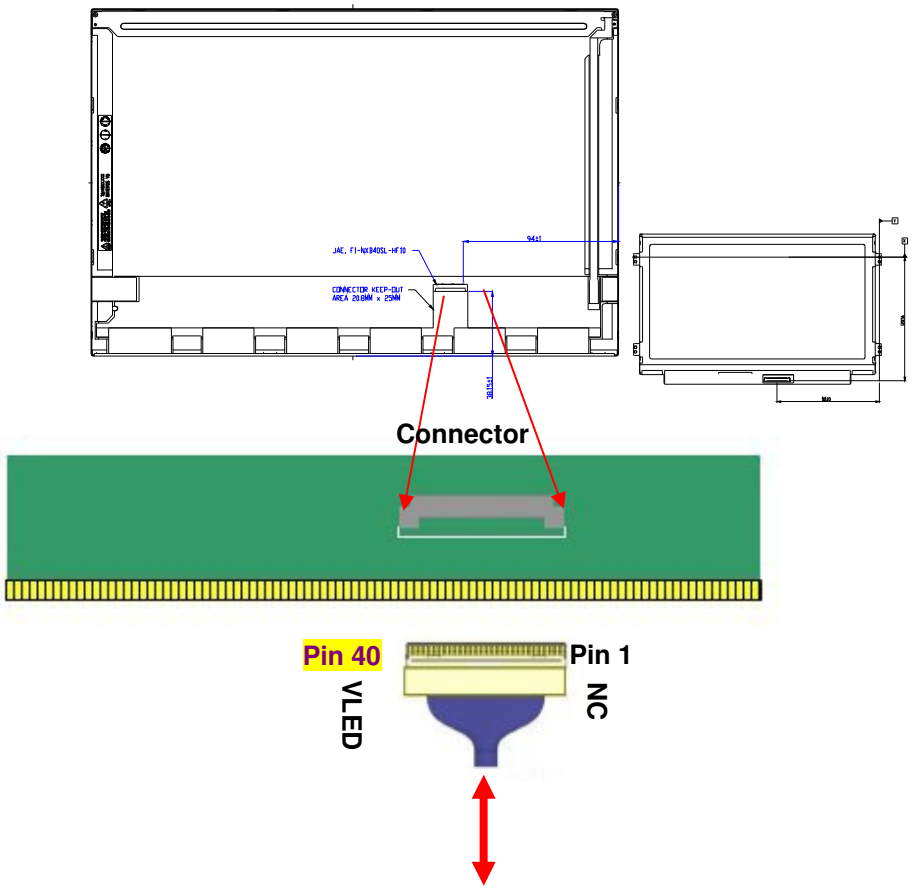
6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal	Description
1	Reserved	Reserved, AUO will use this pin.
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V EEDID	DDC 3.3V power
5	TEST	Panel Self Test
6	Clk EEDID	DDC Clock
7	DATA EEDID	DDC Data
8	Odd_Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels)
9	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels)
10	VSS	Ground – Shield
11	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
13	VSS	Ground – Shield
14	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
16	VSS	Ground – Shield
17	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
18	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
19	VSS	Ground – Shield
20	Reserved	Reserved
21	Reserved	Reserved
22	VSS	Ground – Shield
23	Reserved	Reserved

24	Reserved	Reserved
25	VSS	Ground – Shield
26	Reserved	Reserved
27	Reserved	Reserved
28	VSS	Ground – Shield
29	Reserved	Reserved
30	Reserved	Reserved
31	VSS_LED	Ground – LED
32	VSS_LED	Ground – LED
33	VSS_LED	Ground – LED
34	NC	No connection (Reserved)
35	PWM	System PWM Signal Input (+3.3V Swing)
36	LED_EN	LED enable pin (+3.3V Input)
37	Reserved	Reserved
38	VDDLED	LED Power Supply 6V – 21V
39	VDDLED	LED Power Supply 6V – 21V
40	VDDLED	LED Power Supply 6V – 21V

Note 1: Start from right side



Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

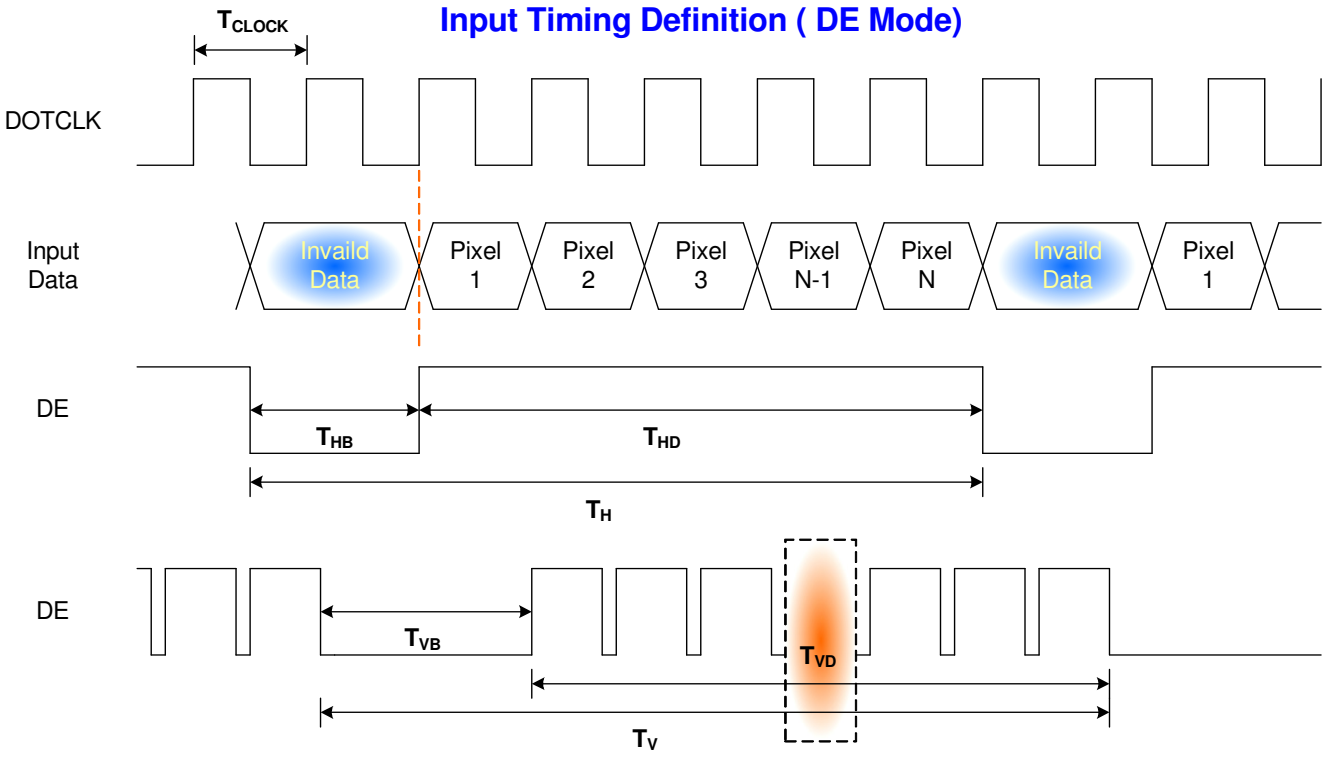
6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	66.9	72	80	MHz
Vertical Section	Period	T_V	788	824	768+A	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	20	56	A	
Horizontal Section	Period	T_H	1416	1456	1366+B	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	50	90	B	

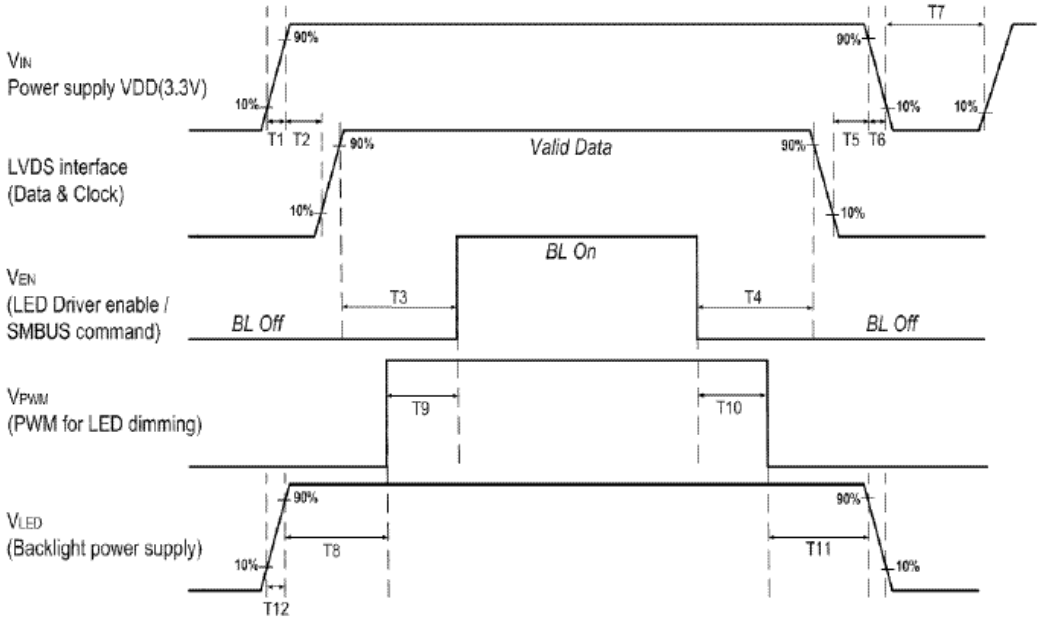
Note 1 : The above is as optimized setting
Note 2 : DE mode only
Note 3 : The maximum clock frequency = (1366+B)*(768+A)*60<80MHz
Note 4 : Clock frequency number is for reference, real setting value refer to EDID (Clock frequency TBD MHz)

6.4.2 Timing diagram

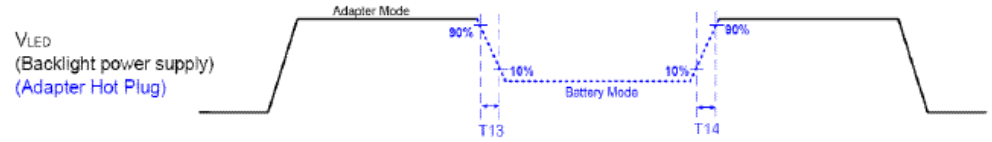


6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T1	0.5	10
T2	0	50
T3	200	-
T4	200	-
T5	0	50
T6	0	10
T7	500	-
T8	10	-
T9	10	-
T10	10	-
T11	10	-
T12	0.5	10
T13	1*	-
T14	1*	-

Seamless change: T13/T14 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note 1 : If T3<200ms, the display garbage may occur. (T3>200ms is recommended)

Note 2 : If T1 or T12<0.5ms, the inrush current may cause the damage of fuse. If T1 or T12<0.5ms, the inrush current I^2t is under typical melt of fuse Spec, there is no mentioned problem.

Note 3 : T8,T9,T10,T11 value are recommended, T8,T9,T10,T11≧0 could be acceptable

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

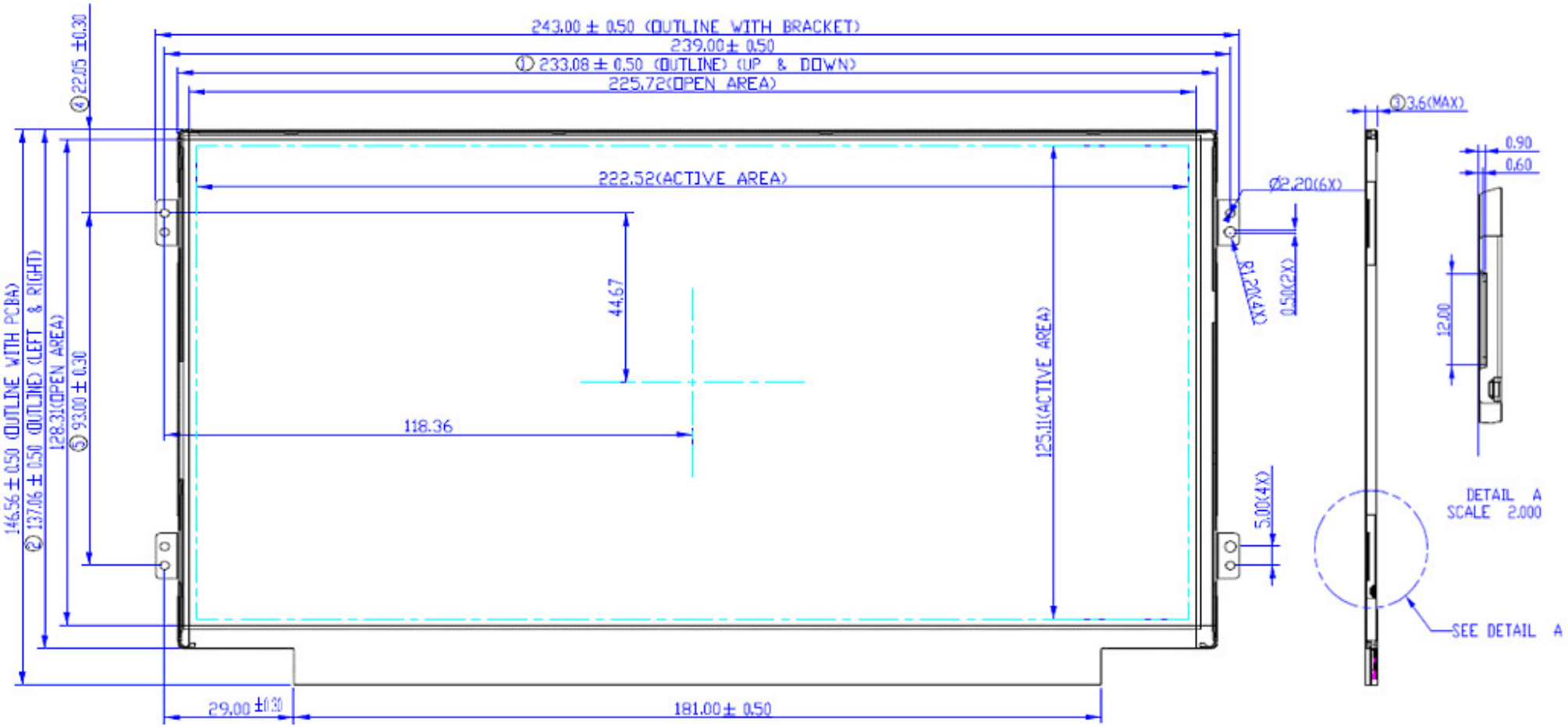
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

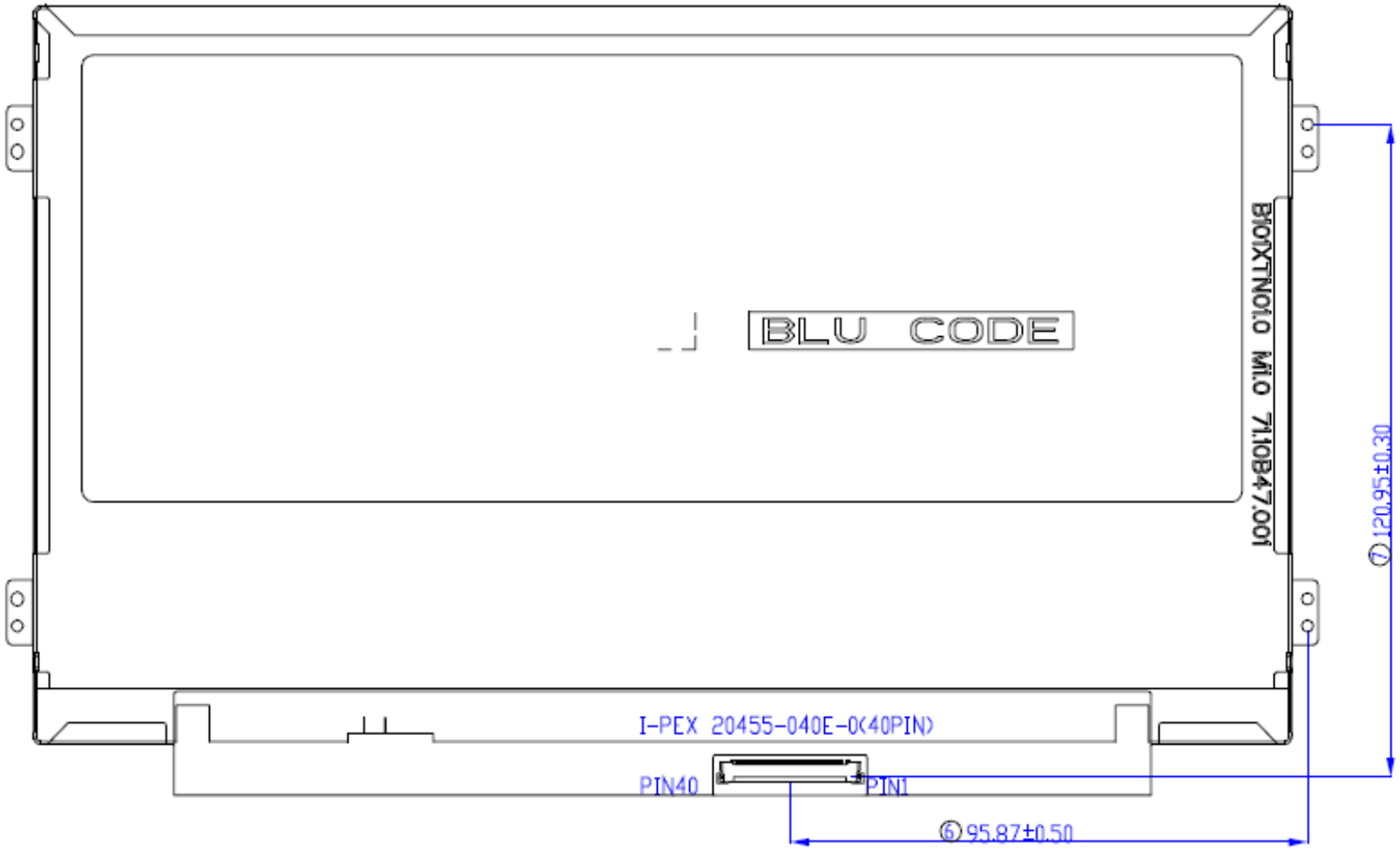
8. Mechanical Characteristics

8.1 LCM Outline Dimension

Front View

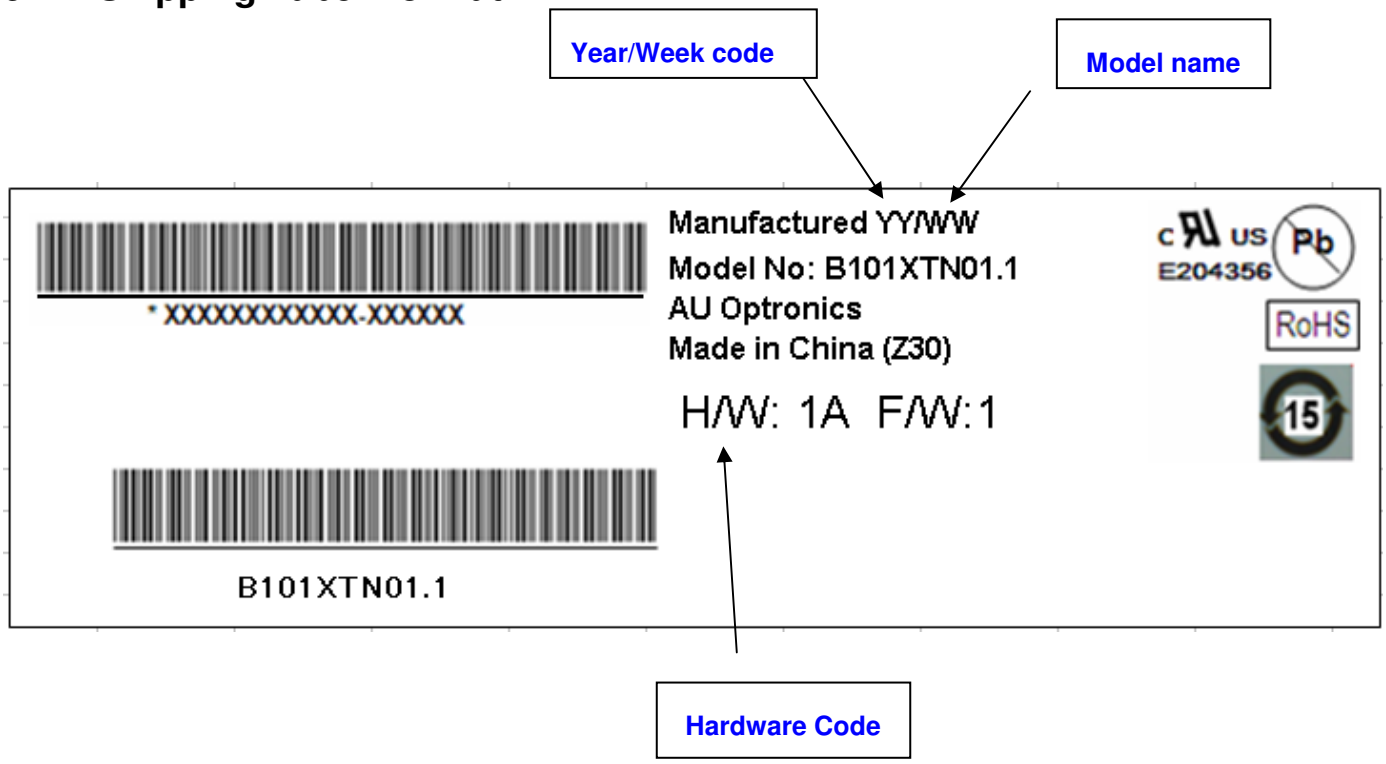


Back View


BLU CODE
B101XTN01.0 M10 7140B47001
⑦120.95±0.30
I-PEX 20455-040E-0(40PIN)
PIN40
PIN1
⑥95.87±0.50

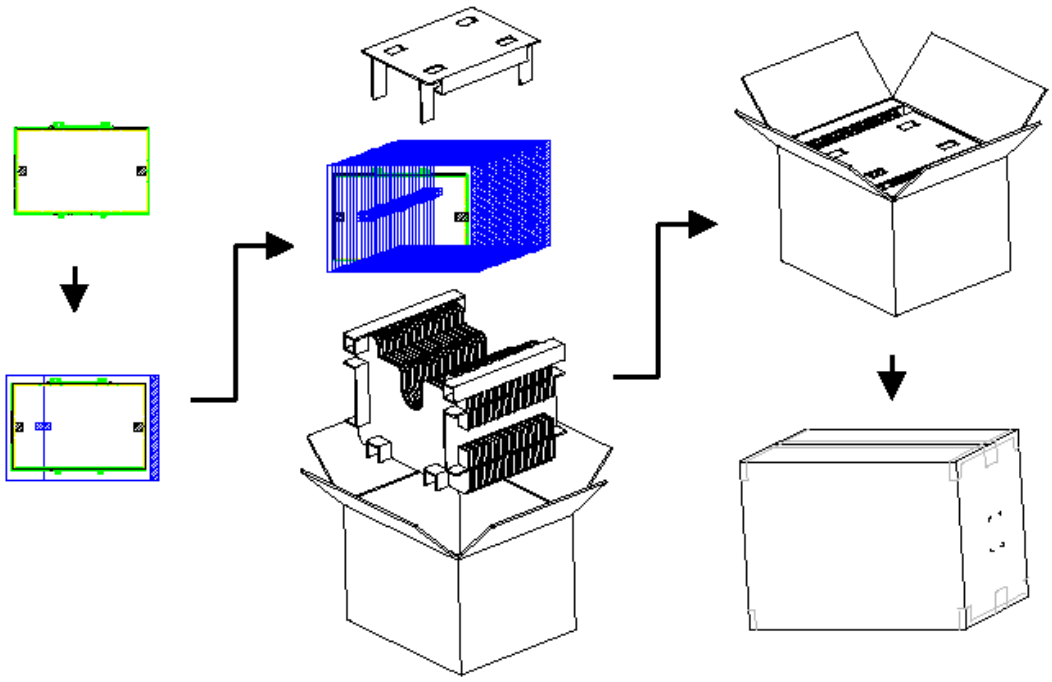
9. Shipping and Package

9.1.1 Shipping Label Format

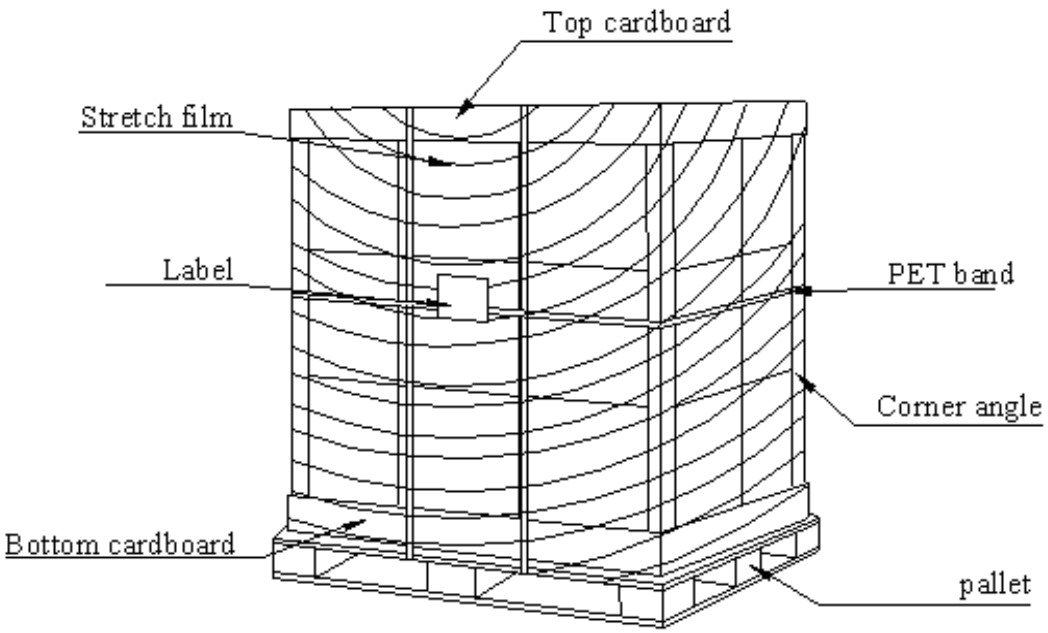


9.1.2 Carton Label Format

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	DC	11011100	220
0B	hex, LSB first	10	00010000	16
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	16	00010110	22
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	90	10010000	144
15	**Max H image size** *(rounded to cm)*	16	00010110	22
16	**Max V image size** *(rounded to cm)*	0D	00001101	13
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2
19	Red/green low bits **(Lower 2:2:2:2 bits)**	BB	10111011	187
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	F5	11110101	245
1B	Red x **(Upper 8 bits)**	94	10010100	148
1C	Red y/ highER 8 bits	55	01010101	85
1D	Green x	54	01010100	84
1E	Green y	90	10010000	144
1F	Blue x	27	00100111	39
20	Blue y	23	00100011	35
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0

24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	58	01011000	88
37	Pixel Clock/10000 USB	1B	00011011	27
38	Horz active **Lower 8bits**	56	01010110	86
39	Horz blanking **Lower 8bits**	5A	01011010	90
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80
3B	Vertical Active **Lower 8bits**	00	00000000	0
3C	Vertical Blanking **Lower 8bits**	1E	00011110	30
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48
3E	HorzSync. Offset	26	00100110	38
3F	HorzSync.Width	16	00010110	22
40	VertSync.Offset : VertSync.Width	36	00110110	54
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	DE	11011110	222
43	Vertical Image Size **Lower 8bits**	7D	01111101	125
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0

4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0
52		00	00000000	0
53		00	00000000	0
54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	30	00110000	48
74	Manufacture P/N	31	00110001	49
75	Manufacture P/N	58	01011000	88

76	Manufacture P/N	54	01010100	84
77	Manufacture P/N	4E	01001110	78
78	Manufacture P/N	30	00110000	48
79	Manufacture P/N	31	00110001	49
7A	Manufacture P/N	2E	00101110	46
7B	Manufacture P/N	30	00110000	48
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	0B	00001011	11
			SUM	6144
			SUM to HEX	1800