(V) Preliminary Specifications
( ) Final Specifications

Module	**11.6”(11.58 ”) 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B116HAN03.3 (H/W:0A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		Luke Lin	11/05/2013
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Lanie Huang	11/05/2013
Note: This Specification is subject to change without notice.		**DMPBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2013/11/05	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B116HAN03 V3 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 , 1920(H) x1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116HAN03 V3 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	294.09 (11.58W")			
Active Area	[mm]	256.32(H) x 144.18(V)			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.1335 X 0.1335			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
White Luminance (I_{LED}=19mA) **(Note: ILED is LED current)**	[cd/m^2]	400 typ. 340 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.4 W(max.) (Including BL Power & Logic Power)			
Weight	[Grams]	140 max. (Panel only)			
Physical Size **(Panel only) without bracket**	[mm]		Min.	Typ.	Max.
		Length	265.50	270.00	270.50
		Width	155.50	160.00	160.50
		Thickness	--	--	2.25 (Panel Side) 4.50 (PCBA Side)
Electrical Interface		2 lane eDP 1.3			
Glass Thickness	[mm]	0.2			
Surface Treatment		HC, Hardness 3H			

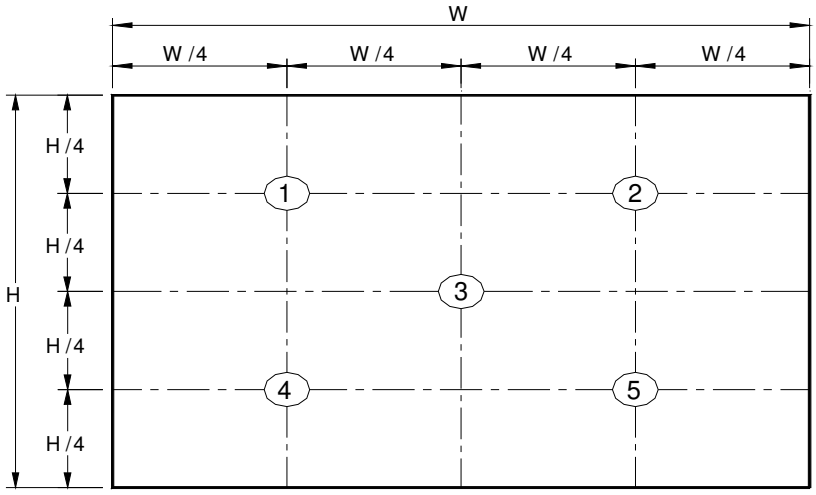
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -20 to +60 -20 to +70
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

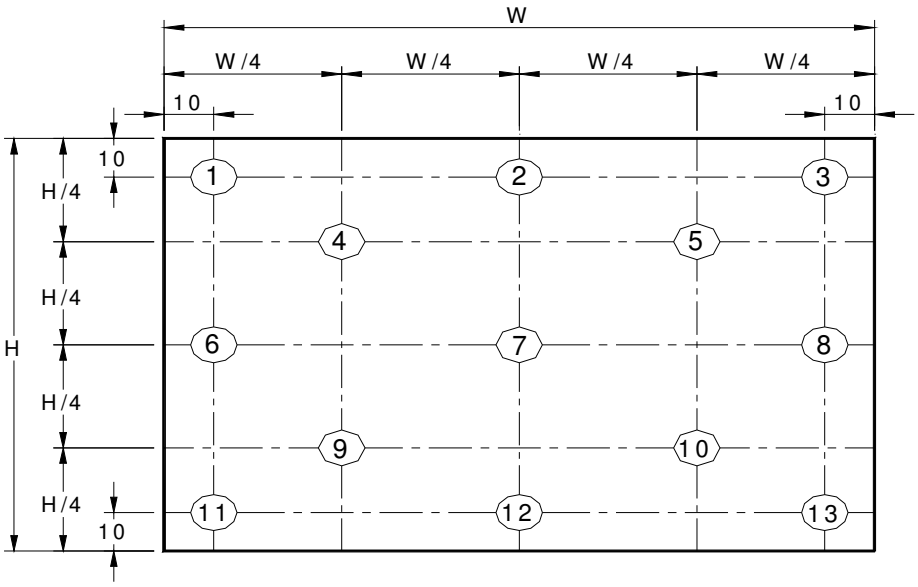
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=22mA			5 points average	340	400	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)		85 85	--- ---	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)		85 85	--- ---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.50		2, 3, 4
Contrast Ratio		CR			800	-		4, 6
Cross talk		%		---	---			4, 7
Response Time		T_{RT}	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	TBD	TBD	TBD		4
		Ry		TBD	TBD	TBD		
	Green	Gx		TBD	TBD	TBD		
		Gy		TBD	TBD	TBD		
	Blue	Bx		TBD	TBD	TBD		
		By		TBD	TBD	TBD		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	52	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



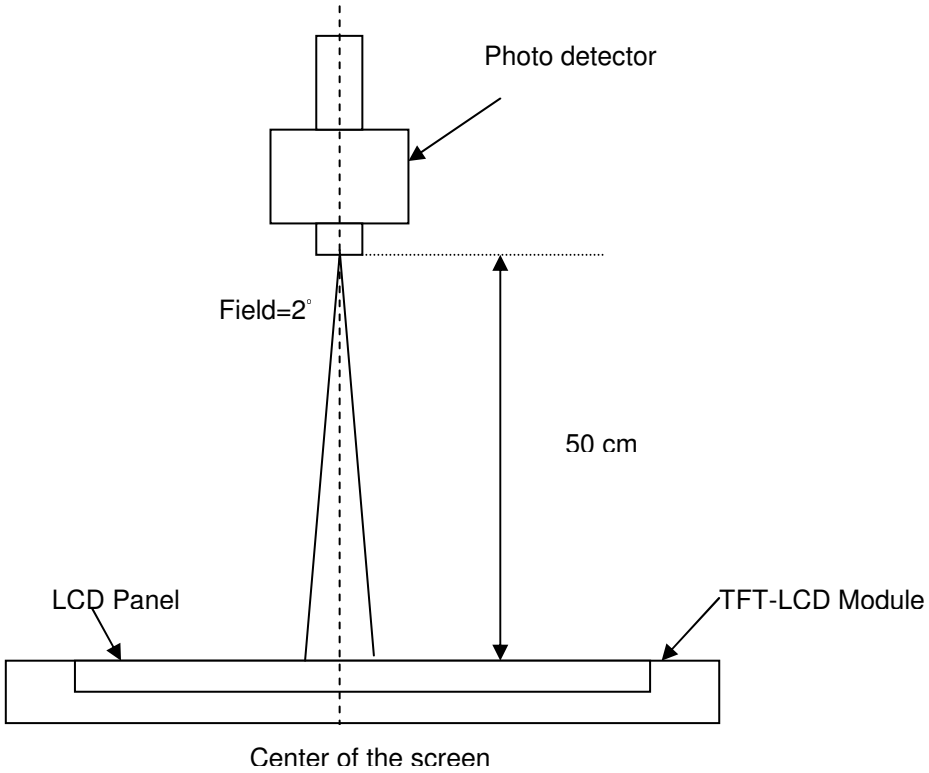
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points， Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

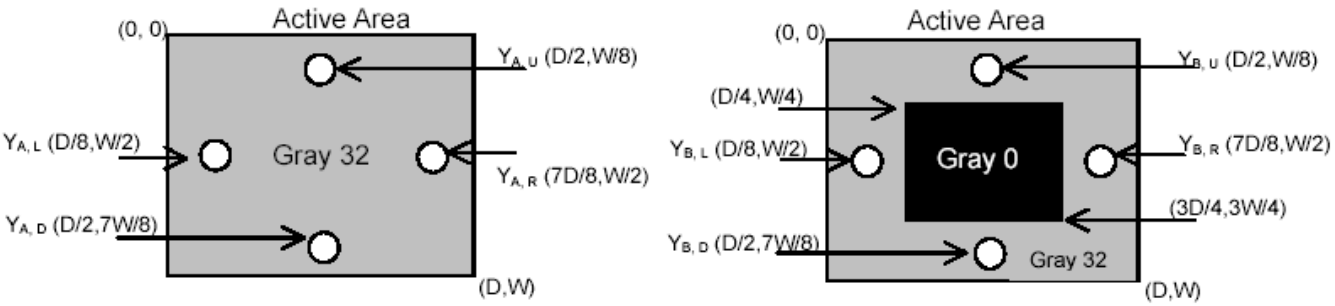
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

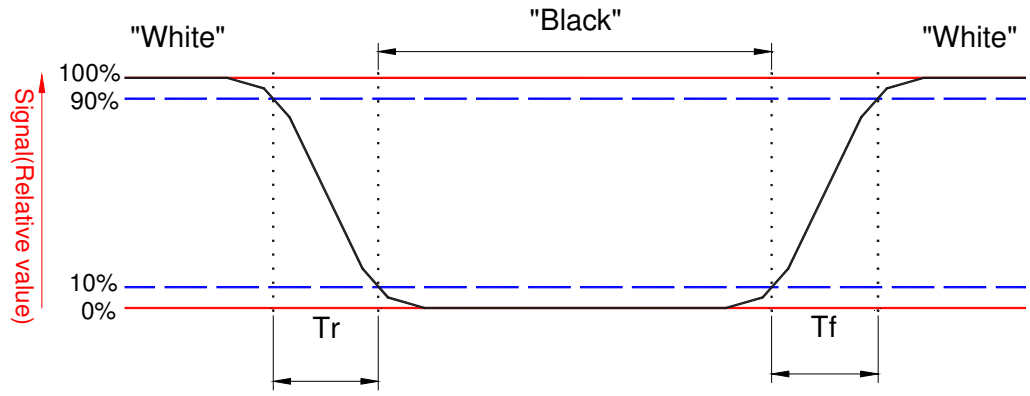
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



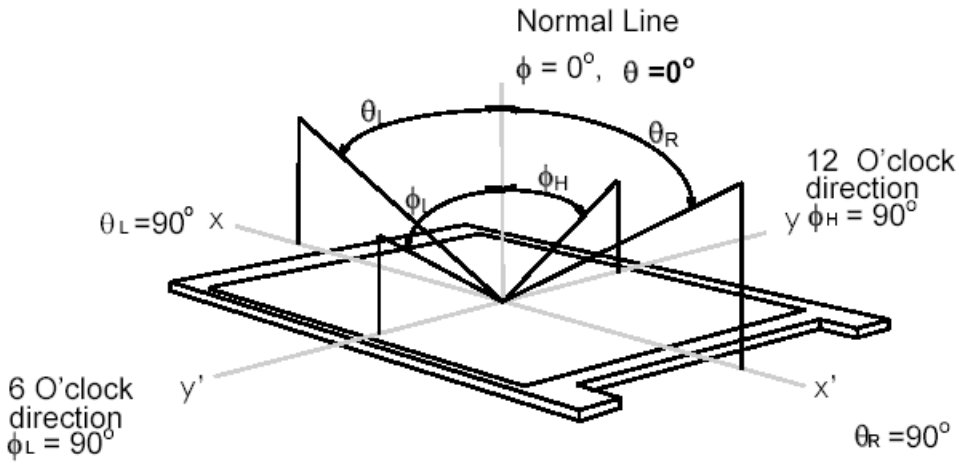
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



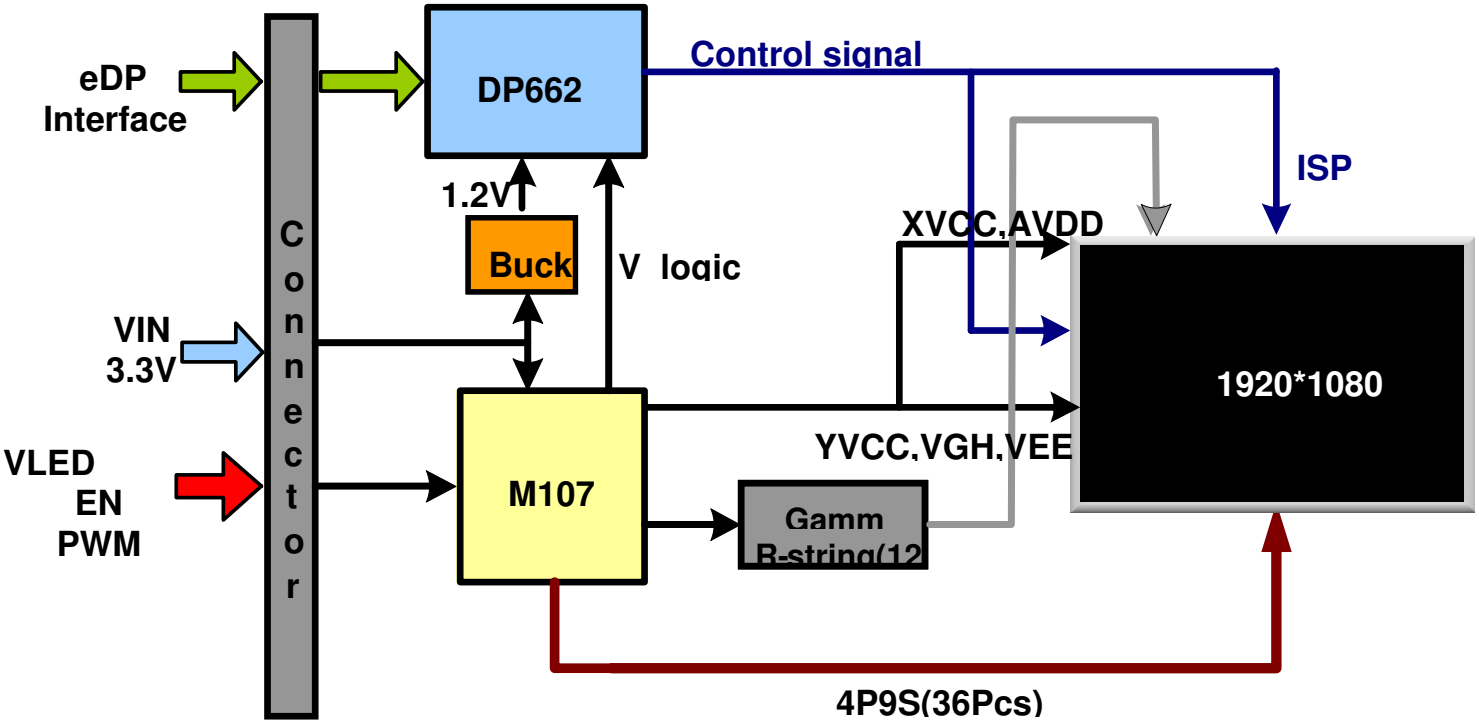
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-20	+60	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-30	+70	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

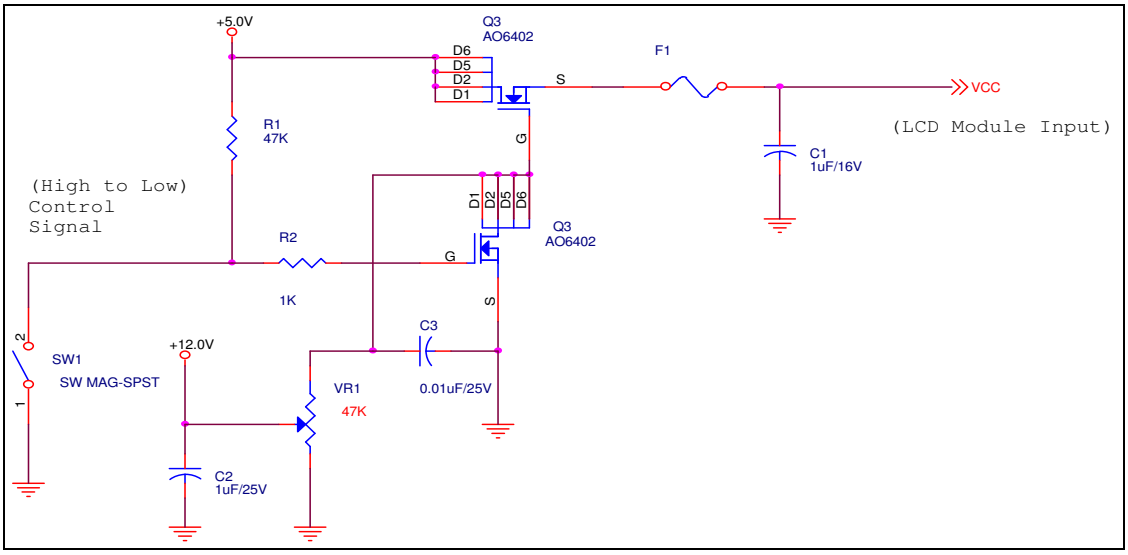
Input power specifications are as follows;

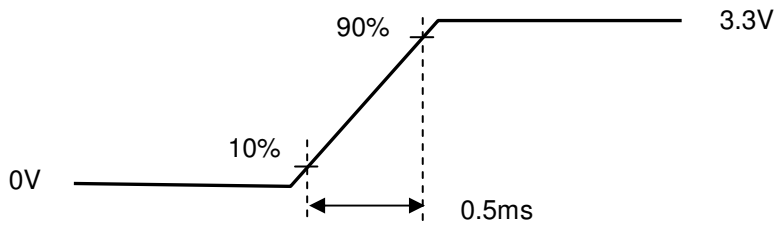
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.2	[Watt]	Note 1
IDD	IDD Current	-	-	400	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Withe Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2：Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

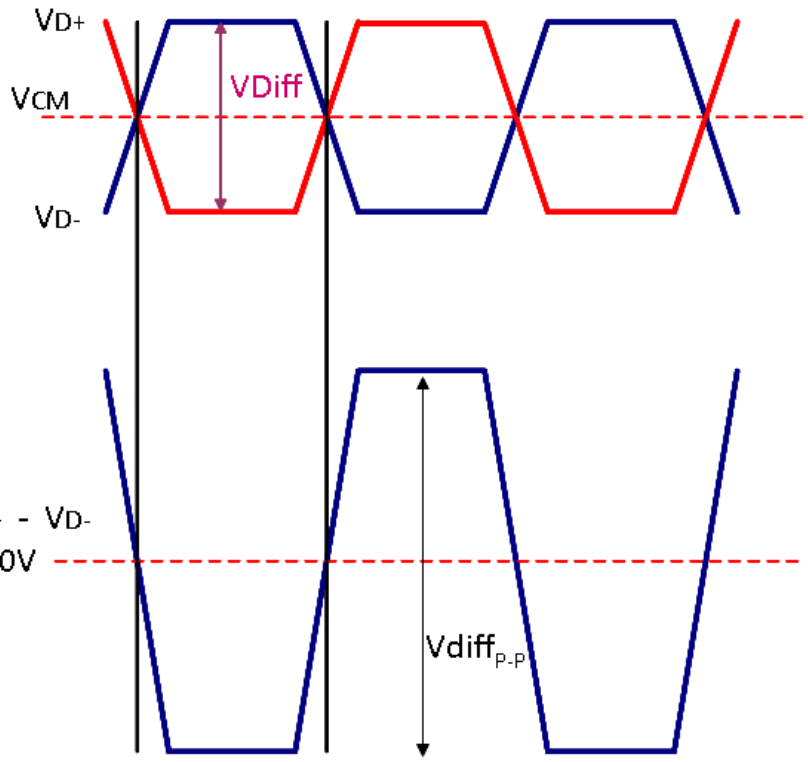
Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

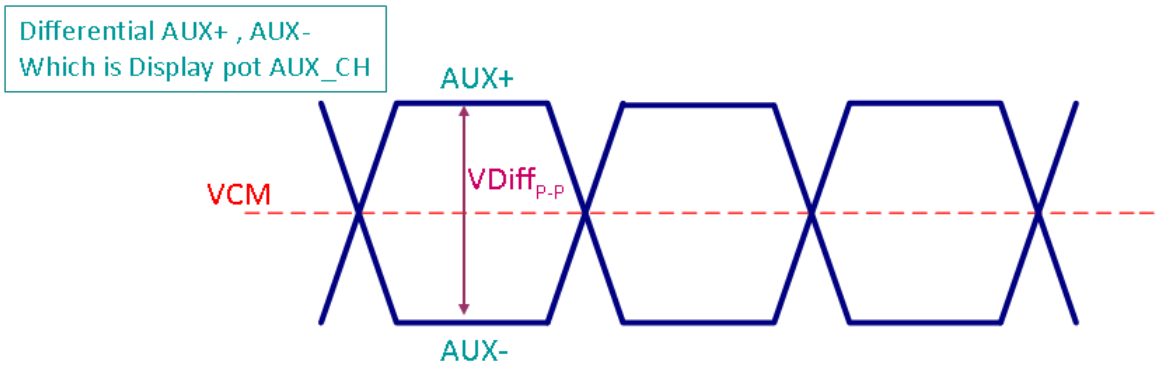


$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$

Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a.

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

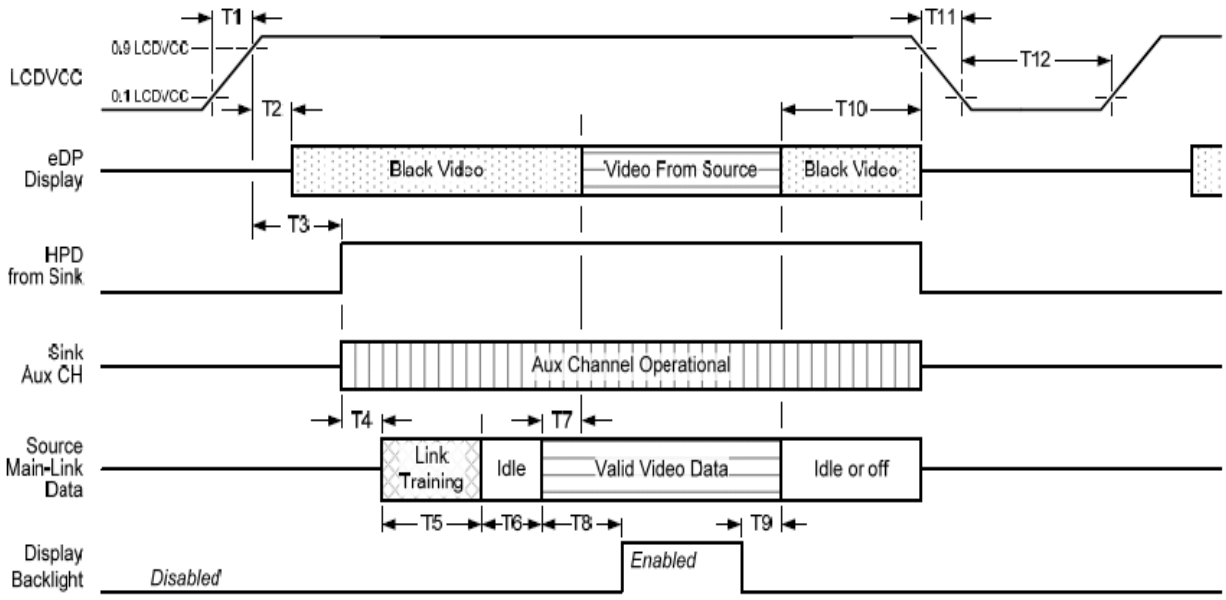
Fallow as VESA display port standard V1.1a.

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	2.25		3.6	V

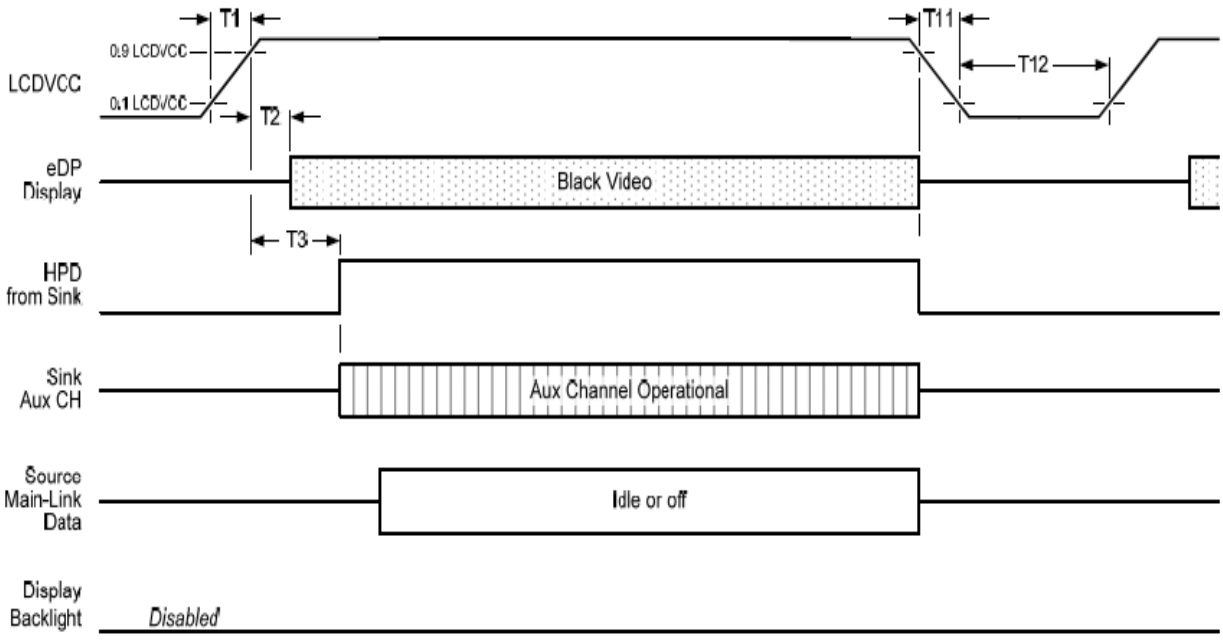
Fallow as VESA display port standard V1.1a.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

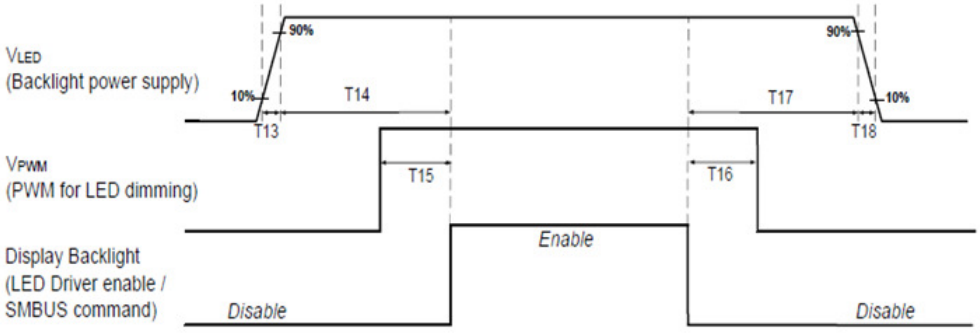
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

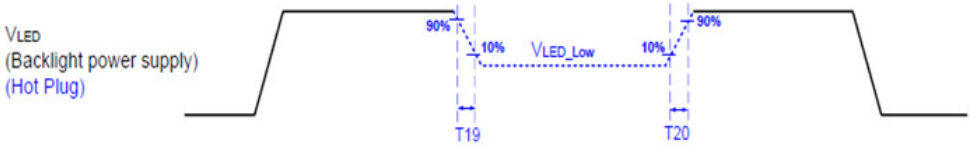


	Min (ms)	Max (ms)
T13	0.2	-
T14	0	-
T15	-	-
T16	-	-
T17	0	-
T18	0	-
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Note : If T19,T20 < 5xTPWM* , The flash display may occur. We suggest T19,T20 ≧ 5xTPWM* to realize seamless change display.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.97	[Watt]	(Ta=25℃), Note 1
LED Life-Time	N/A	12,000	-	-	Hour	(Ta=25℃ Tj≦70℃), Note 2 I_F=22mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency **(Efficiency=100%)**

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

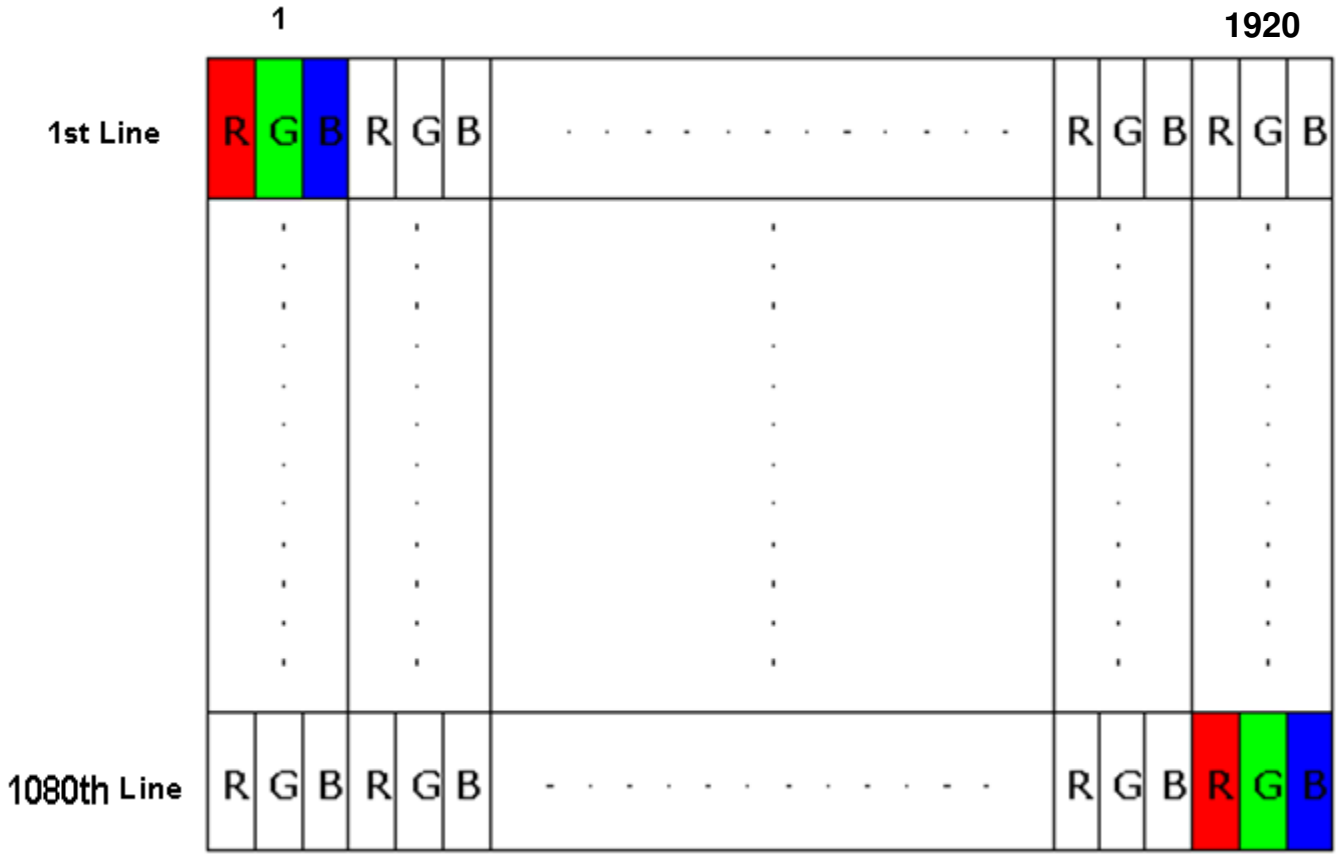
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5		9	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2	-	-	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2	-	-	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency *1	FPWM	100	-	20k	Hz	
PWM Duty Ratio	Duty	0	--	100	%	

Note1: LED Power Supply is evaluated by Lextar LED.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

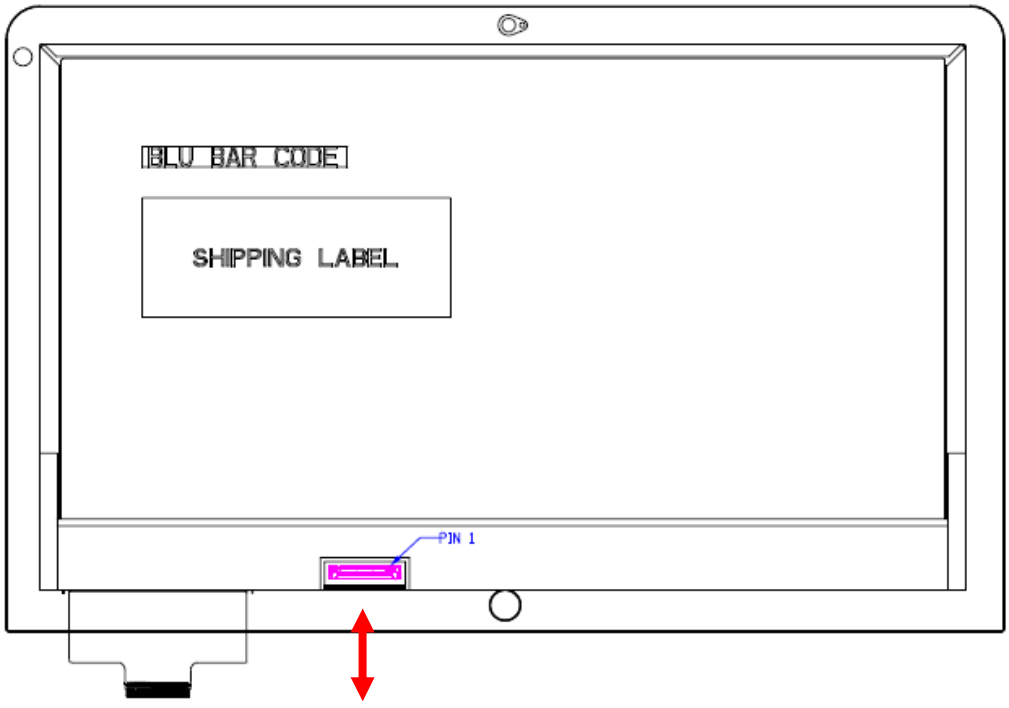
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	I-PEX 20455-030E-12 or Compatible
Mating Housing/Part Number	I-PEX 20453-030T-11 or Compatible

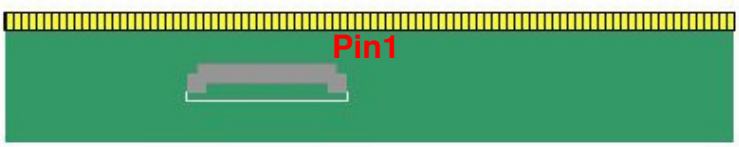
6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal Name	Description
1	NC	NC
2	GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	GND	High Speed Ground
12	VDD	LCD logic and driver power
13	VDD	LCD logic and driver power
14	Aging	LCD Panel Self Test
15	GND	LCD logic and driver ground
16	GND	LCD logic and driver ground
17	HPD_N	HPD signal pin
18	GND	Backlight ground

19	GND	Backlight ground
20	GND	Backlight ground
21	GND	Backlight ground
22	LED_EN	Backlight On/Off
23	LED_PWM	System PWM signal input for dimming
24	NC-Reserved	Reserved for LCD manufacture's use(EDID_CLK)
25	NC-Reserved	Reserved for LCD manufacture's use(EDID_DATA)
26	V_LED	Backlight power
27	V_LED	Backlight power
28	V_LED	Backlight power
29	V_LED	Backlight power
30	NC	NC





Note1:Input signals shall be low or High-impedance state when VDD is off.

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		$1/T_{Clock}$		138.5		MHz
Vertical Section	Period	T_V	1090	1111	1200	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	10	30	120	
Horizontal Section	Period	T_H	2000	2080	2320	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	80	160	400	

Note : DE mode only

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 240h	
High Temperature Operation	Ta= 60℃, Dry, 240h	
Low Temperature Operation	Ta= -20℃, 240h	
High Temperature Storage	Ta= 70℃,240h	
Low Temperature Storage	Ta= -30℃, 240h	
Thermal Shock Test	Ta=-20℃(30min) ~70℃(30min), 15 cycles condition	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

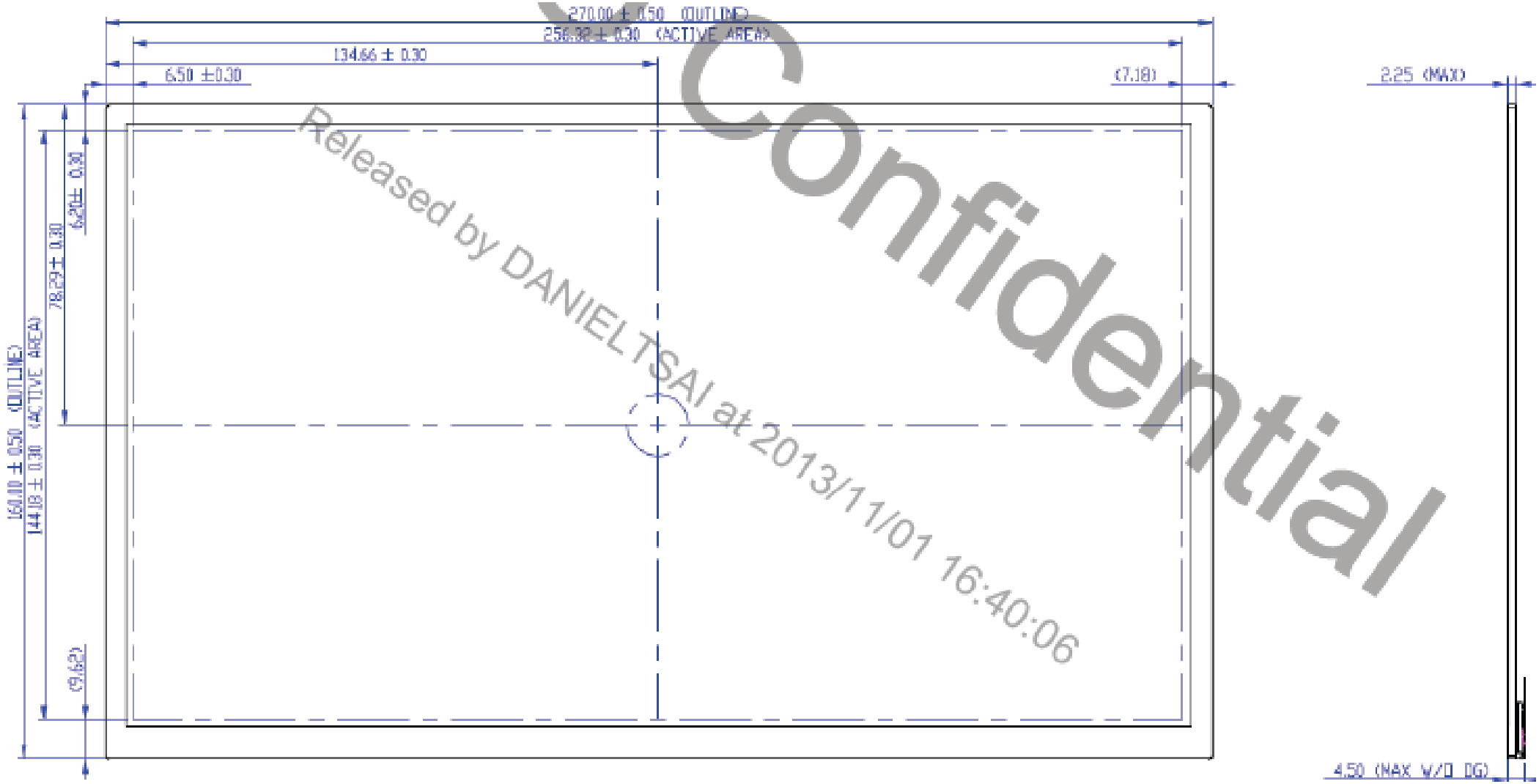
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

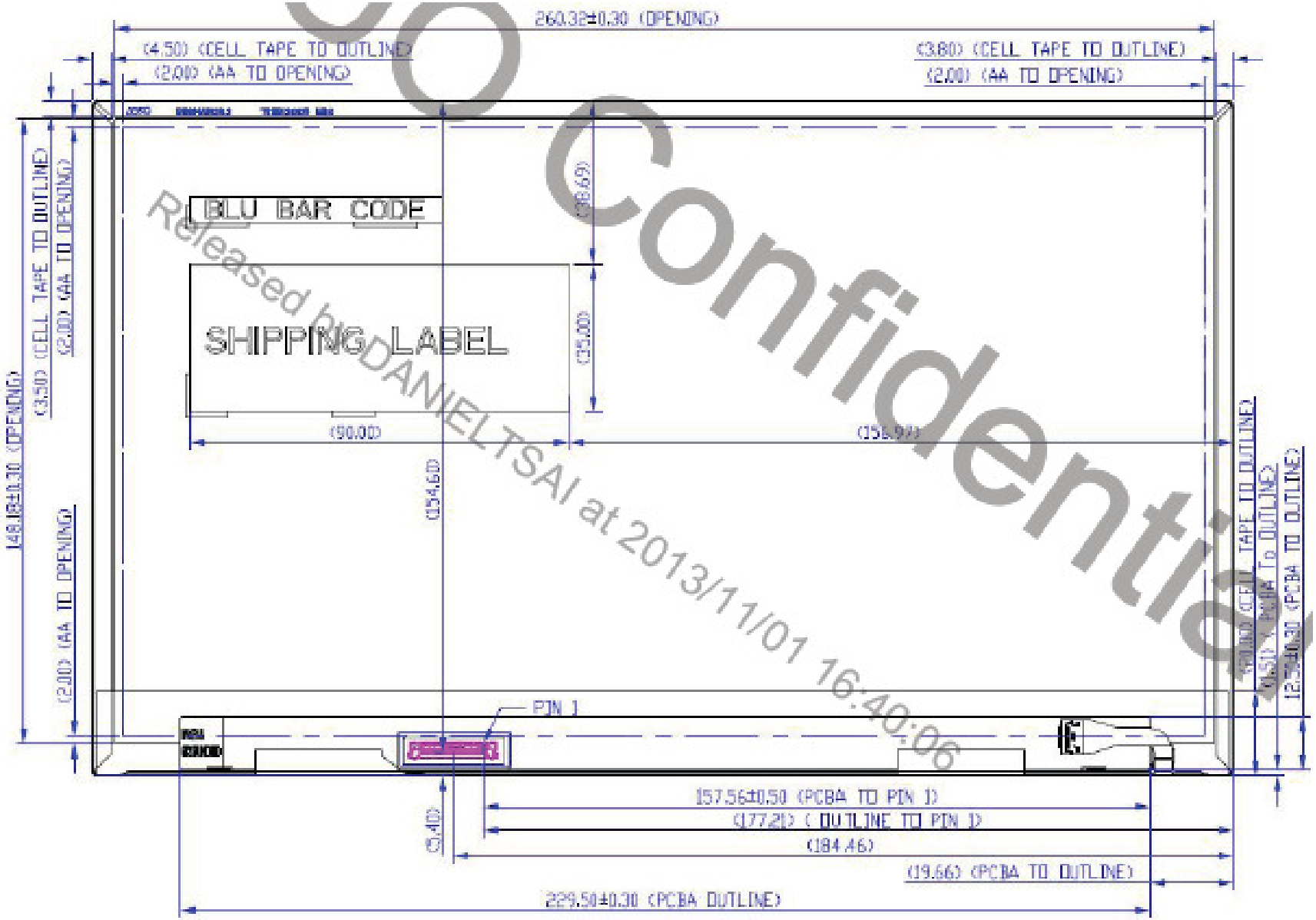
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Rear View

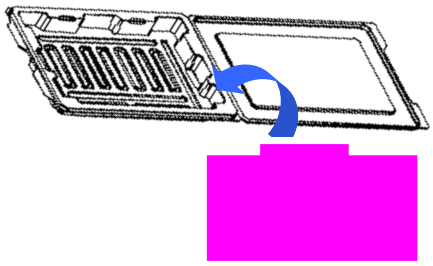


9. Shipping and Package

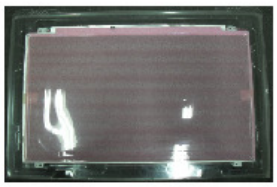
9.1 Shipping Label Format

9.2 Carton Label Format

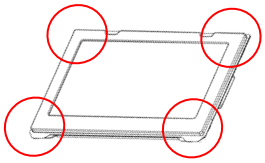
9.3 Carton Package



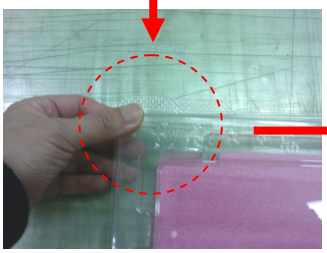
Place 1 pcs Spacer first before placing 1 panel (panel face up)
4PCS PANEL ＋4PCS SPACER

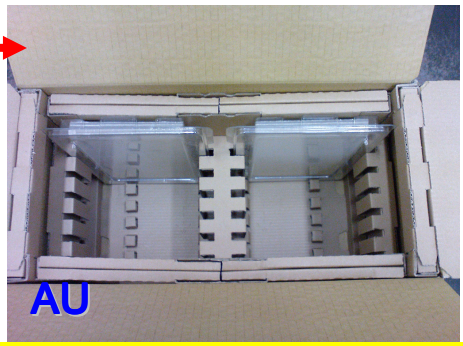


Close Tray Box



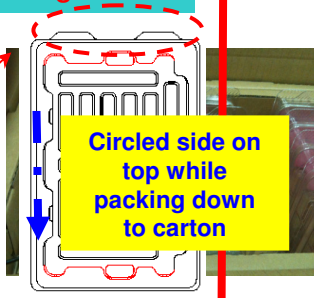
Check if the TRAY BOX corners are properly sealed





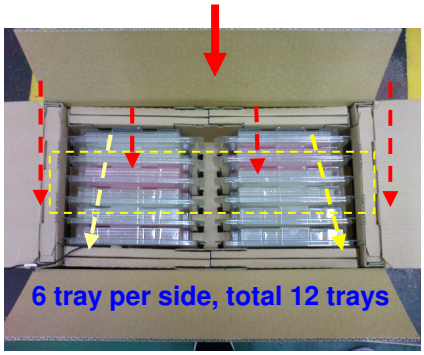
- Tray Box properly placed left and right with 4 trays each side
- LCM AA should face the direction with AUO Logo

TRAY BOX with backside facing front

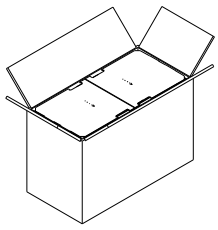


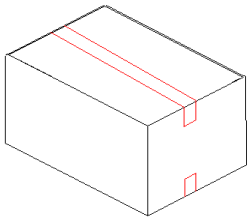
Circled side on top while packing down to carton

TRAY BOX slowly place in carton

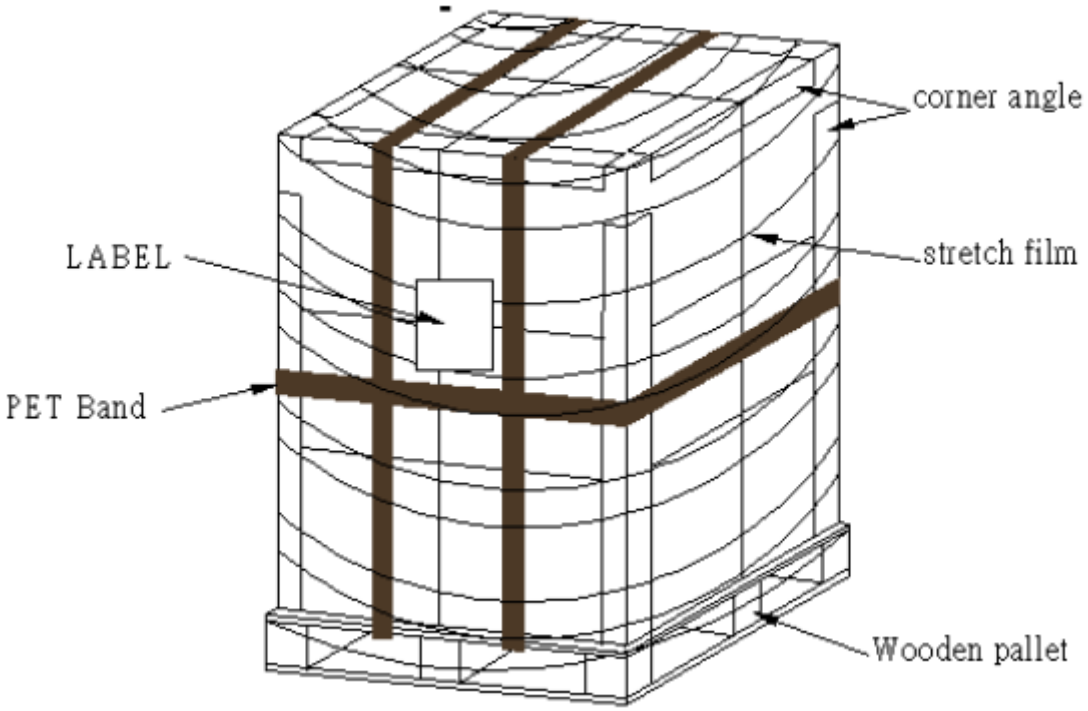


6 tray per side, total 12 trays





9.4 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01	Header	FF	11111111	255	
02	Header	FF	11111111	255	
03	Header	FF	11111111	255	
04	Header	FF	11111111	255	
05	Header	FF	11111111	255	
06	Header	FF	11111111	255	
07	Header	00	00000000	0	
08	ID Manufacturer Name	06	00000110	6	
09		AF	10101111	175	
0A	ID Product Code	D3	11010011	211	
0B		40	01000000	64	
0C	ID Serial Number (32-bit serial number)	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of Manufacture	01	00000001	1	
11	Year of Manufacture	17	00010111	23	
12	EDID Structure version	01	00000001	1	
13	EDID Revision	04	00000100	4	
14	Video Input Definition	95	10010101	149	
15	Max H Image Size(㎝)	1A	00011010	26	
16	Max V Image Size(㎝)	0E	00001110	14	
17	Display gamma (gamma x 100)-100	78	01111000	120	
18	Feature support(DPMS)	EA	11101010	234	
19	Red/Green Low Bits	D1	11010001	209	
1A	Blue/White Low Bits	15	00010101	21	
1B	Red x	9E	10011110	158	
1C	Red y	59	01011001	89	
1D	Green x	53	01010011	83	
1E	Green y	9B	10011011	155	
1F	Blue x	27	00100111	39	
20	Blue y	1E	00011110	30	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established Timing 1	00	00000000	0	
24	Established Timing 2	00	00000000	0	
25	Manufacturer's Timings	00	00000000	0	
26	Standard Timing Identification #1	01	00000001	1	
27		01	00000001	1	

28	Standard Timing Identification #2	01	00000001	1	
29		01	00000001	1	
2A	Standard Timing Identification #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard Timing Identification #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard Timing Identification #5	01	00000001	1	
2F		01	00000001	1	
30	Standard Timing Identification #6	01	00000001	1	
31		01	00000001	1	
32	Standard Timing Identification #7	01	00000001	1	
33		01	00000001	1	
34	Standard Timing Identification #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10,000 (LSB)	B0	10110000	176	
37	Pixel Clock/10,000 (MSB) /	36	00110110	54	
38	Horizontal Active	80	10000000	128	
39	Horizontal Blanking	B4	10110100	180	
3A	Horizontal Active : Horizontal Blanking	70	01110000	112	
3B	Vertical Active	38	00111000	56	
3C	Vertical Blanking	1E	00011110	30	
3D	Vertical Active : Vertical Blanking	40	01000000	64	
3E	Horizontal Sync. Offset	30	00110000	48	
3F	Horizontal Sync Pulse Width	64	01100100	100	
40	Vertical Sync Offset : Sync Width	31	00110001	49	
41	Horizontal Vertical Sync Offset/Width upper 2bits	00	00000000	0	
42	Horizontal Image Size	00	00000000	0	
43	Vertical Image Size	90	10010000	144	
44	Horizontal & Vertical Image Size	10	00010000	16	
45	Horizontal Border	00	00000000	0	
46	Vertical Border	00	00000000	0	
47	Flags	18	00011000	24	
48	Pixel Clock/10,000 (LSB) (Slow Refresh rate)	93	10010011	147	50Hz
49	Pixel Clock/10,000 (MSB) / (Slow Refresh rate)	2D	00101101	45	
4A	Horizontal Active	80	10000000	128	
4B	Horizontal Blanking	B4	10110100	180	
4C	Horizontal Active : Horizontal Blanking	70	01110000	112	
4D	Vertical Active	38	00111000	56	
4E	Vertical Blanking	1E	00011110	30	
4F	Vertical Active : Vertical Blanking	40	01000000	64	
50	Horizontal Sync. Offset	30	00110000	48	
51	Horizontal Sync Pulse Width	64	01100100	100	
52	Vertical Sync Offset : Sync Width	31	00110001	49	
53	Horizontal Vertical Sync Offset/Width upper 2bits = 0	00	00000000	0	
54	Horizontal Image Size	00	00000000	0	
55	Vertical Image Size	90	10010000	144	

56	Horizontal & Vertical Image Size	10	00010000	16	
57	Horizontal Border	00	00000000	0	
58	Vertical Border	00	00000000	0	
59	Flags	18	00011000	24	
5A	Flag	00	00000000	0	
5B	Flag	00	00000000	0	
5C	Flag	00	00000000	0	
5D	Data Type Tag	FE	11111110	254	
5E	Flag	00	00000000	0	
5F	(Horizontal active pixel /8)-31	41	01000001	65	A
60	Image Aspect Ratio	55	01010101	85	U
61	Middle Refresh Rate	4F	01001111	79	
62	(Horizontal active pixel /8)-31	5E	01011110	94	^
63	Image Aspect Ratio	20	00100000	32	
64	Low Refresh Rate	20	00100000	32	
65	Brightness(1/10nit)	20	00100000	32	
66	Feature flag	20	00100000	32	
67	Reserved	20	00100000	32	
68	LCD Supplier manufacture Code (3 character ID)	20	00100000	32	
69		20	00100000	32	
6A	LCD Supplier Product code	20	00100000	32	
6B	LCD Supplier Product code	20	00100000	32	
6C	Flag	00	00000000	0	
6D	Flag	00	00000000	0	
6E	Flag	00	00000000	0	
6F	Data Type Tag	FE	11111110	254	
70	Flag	00	00000000	0	
71	Model Name	42	01000010	66	B
72	Model Name	31	00110001	49	1
73	Model Name	31	00110001	49	1
74	Model Name	36	00110110	54	6
75	Model Name	48	01001000	72	H
76	Model Name	41	01000001	65	A
77	Model Name	4E	01001110	78	N
78	Model Name	30	00110000	48	0
79	Model Name	33	00110011	51	3
7A	Model Name	2E	00101110	46	.
7B	Model Name	33	00110011	51	3
7C	Model Name	20	00100000	32	
7D	Model Name	0A	00001010	10	
7E	Extension flag	00	00000000	0	
7F	Checksum	2C	00101100	44	
			SUM	7680	