( ) Preliminary Specifications
(V) Final Specifications

Module	**11.6”(11.58 ”) 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B116HAT03.2 (H/W:1B)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
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Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/11/19	All	First Edition for Customer		
1.0 2012/11/20	All	Final Edition for Customer		
1.1 2013/02/20	5	Weight: 260g	Weight: 266g	
	5	Thickness: 3.655(panel side)/5.655(PCBA side)	Thickness: 3.73(panel side)/5.73(PCBA side)	
	27~28	Old outline dimension	New outline dimension	
	29	Old shipping label/carton label	New shipping label/carton label	
1.2 2013/02/26	5	Length: 271.62 typ	270.62 typ	
	6	TP interface: I2C	Remove TP interface column	
	13	Absolute rating of touch sensor	remove	
	19	Old Display Port BL power sequence timing parameter	New Display Port BL power sequence timing parameter update	
	21	Connector Manufacturer: IPEX or Compatible	Connector Manufacturer: IPEX	
		Connector Type/Part Number: IPEX or Compatible	Connector Type/Part Number: IPEX	
	27~28	Old outline dimension	New outline dimension	
1.3 2013/3/6	6		Add AS coating criteria	
1.4 2013/09/10		LED Backlight without driving circuit design	LED Backlight with driving circuit design	
1.5 2013/10/15	29	Shipping label changed	Shipping label changed	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B116HAT03 V2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 , 1920(H) x1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116HAT03 V2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	294.09 (11.58W")			
Active Area	[mm]	256.32(H) x 144.18(V)			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.1335 X 0.1335			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
White Luminance (I_{LED}=19mA) **(Note: ILED is LED current)**	[cd/m^2]	Base Panel: 400 typ/.340 min. (5 points average) Total Solution: 350 typ			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.75 W(max.)			
Weight	[Grams]	160 max. (Panel only)			
		266 max. (Total Solution)			
Physical Size **(Panel only) without bracket**	[mm]		Min.	Typ.	Max.
		Length	270.12	270.62	271.12
		Width	159.26	159.76	160.26
		Thickness	--	--	2.50 (Panel Side) 4.50 (PCBA Side)
Physical Size **(Total Solution) without bracket**	[mm]		Min.	Typ.	Max.
		Length	291.7	291.8	291.9
		Width	182.9	183.0	183.1
		Thickness	--	--	3.73 (Panel Side) 5.73 (PCBA Side)
Electrical Interface		2 lane eDP			

Glass Thickness	[mm]	0.25
Surface Treatment		Glare, Hardness 3H
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -20 to +60 -20 to +70
RoHS Compliance		RoHS Compliance

2.1.1 General Touch Specification

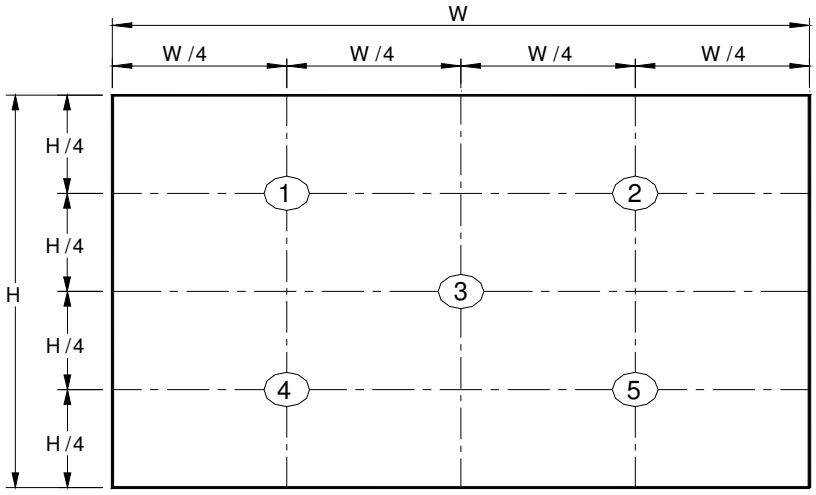
Item		Spec.	Unit
Type of Touch Panel		Projective Capacitive	
Material Type		Gorilla Glass	
Substrate thickness		0.83 mm	mm
Panel Size		11.6”	inch
Sensor Active Area		260.32 ± 0.3 x 148.18± 0.3	mm
TP Viewing Area		257.32± 0.15 x 145.18± 0.15	mm
TP Outline Dimension		291.8± 0.1 x 183.0± 0.1	mm
Total Weight		96+/-9	G
IC Driver		Atmel mXT1664S	
Channel		52*30	
Surface hardness		7	H
CS		600	Mpa
DOL		35	Um
AS coating	Contact angle Oleic acid	> 60	degree
	Contact angle Water	> 95	degree

2.2 Optical Characteristics

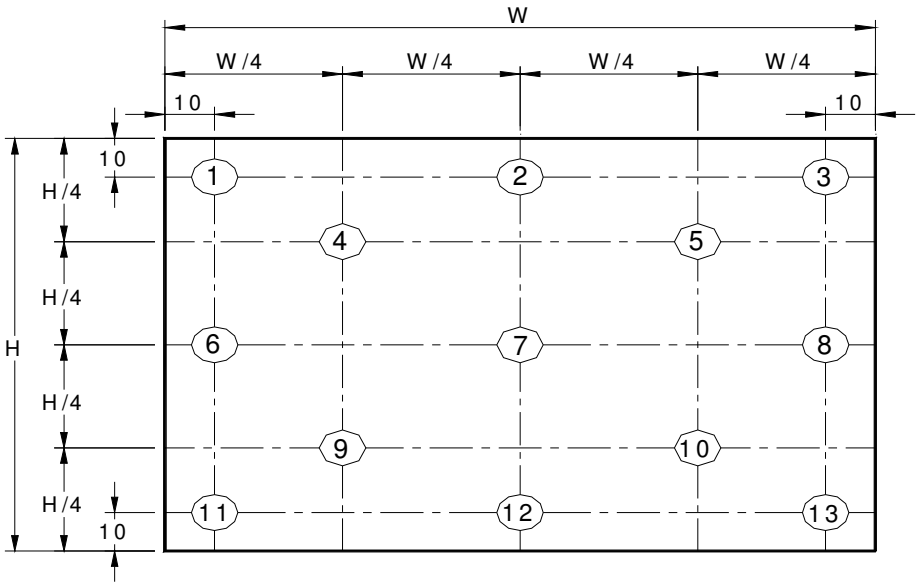
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=19mA			5 points average	297	350	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10		85	---	degree	4, 9
		θ_L	(Left)		85	---		
		ψ_H	Vertical (Upper) CR = 10		85	---		
		ψ_L	(Lower)		85	---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.50		2, 3, 4
Contrast Ratio		CR			800	-		4, 6
Cross talk		%		---	---			4, 7
Response Time		T_{RT}	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.566	0.596	0.626		4
		Ry		0.316	0.346	0.376		
	Green	Gx		0.293	0.323	0.353		
		Gy		0.552	0.582	0.612		
	Blue	Bx		0.117	0.147	0.177		
		By		0.098	0.128	0.158		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	52	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



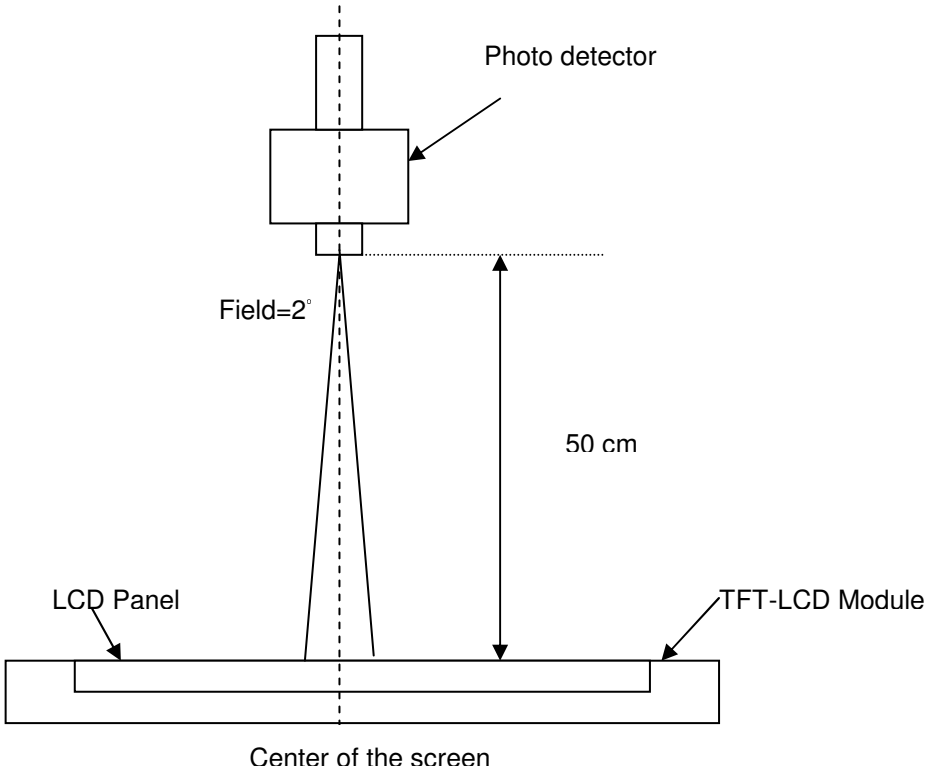
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

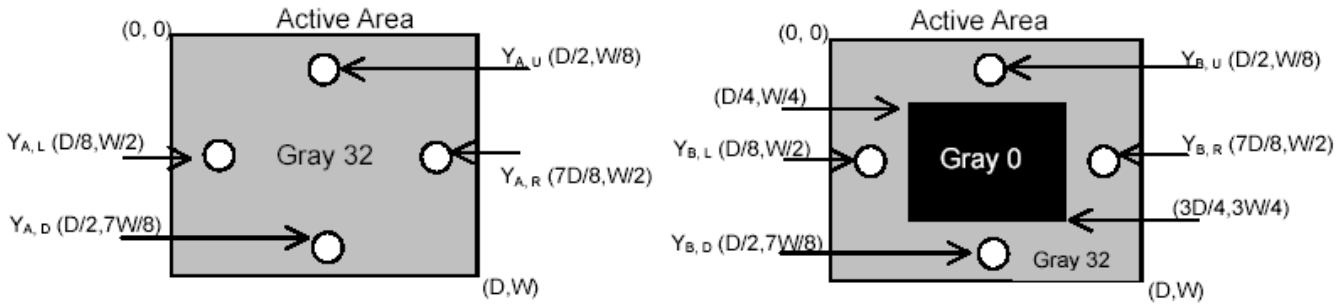
Note 7 : Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

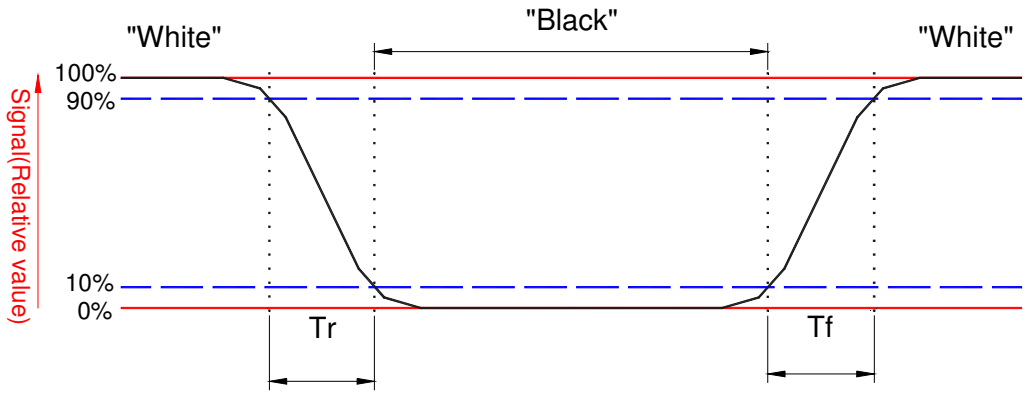
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



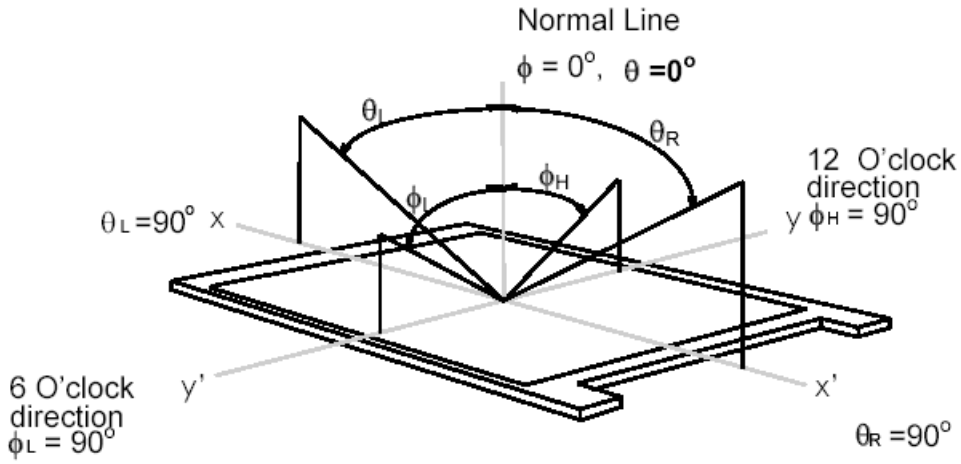
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



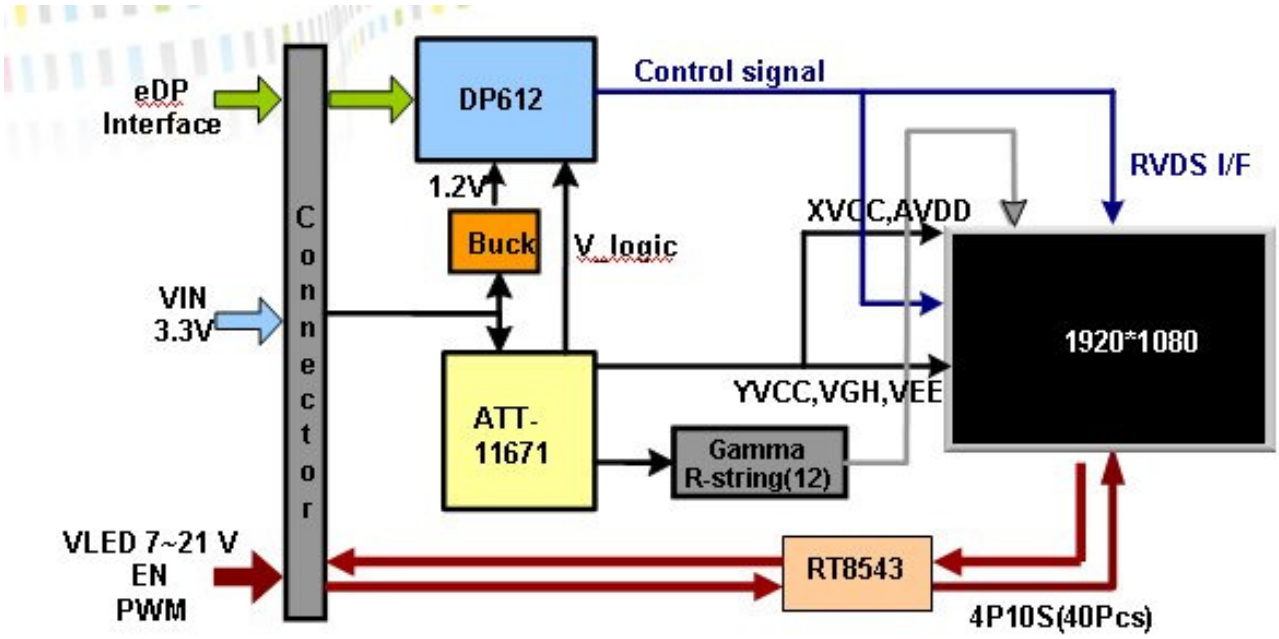
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-20	+60	[°C]	Note 4
Operation Humidity	HOP	5	90	[%RH]	Note 4
Storage Temperature	TST	-30	+70	[°C]	Note 4
Storage Humidity	HST	5	90	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

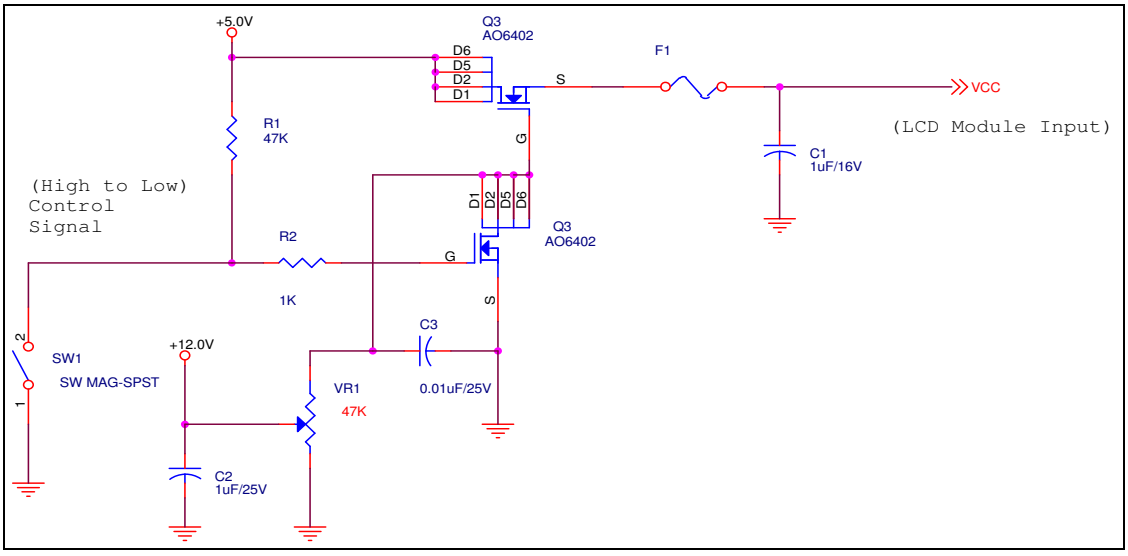
Input power specifications are as follows;

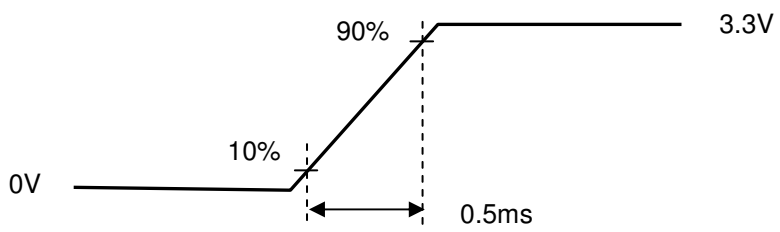
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1	[Watt]	Note 1
IDD	IDD Current	-	-	333	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Withe Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

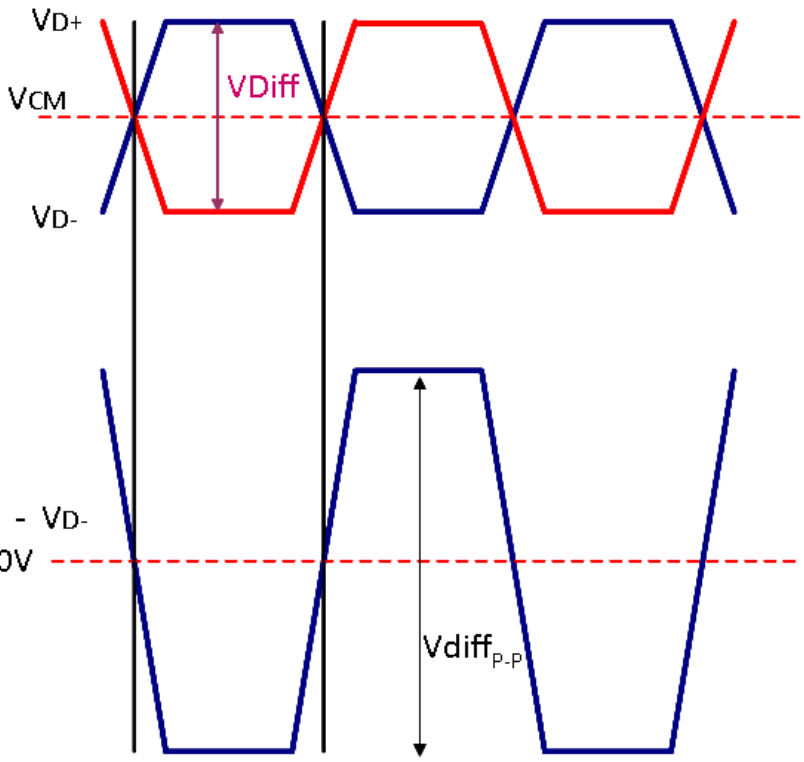
Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link

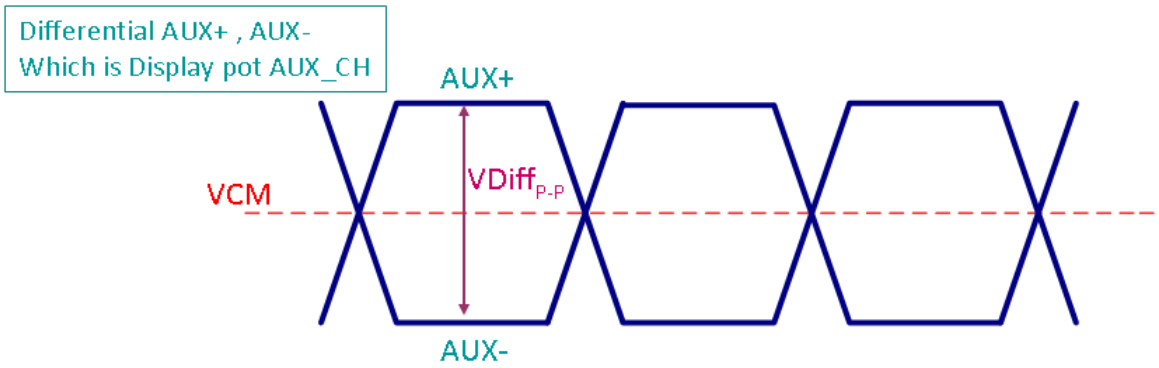


$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$

Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a.

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

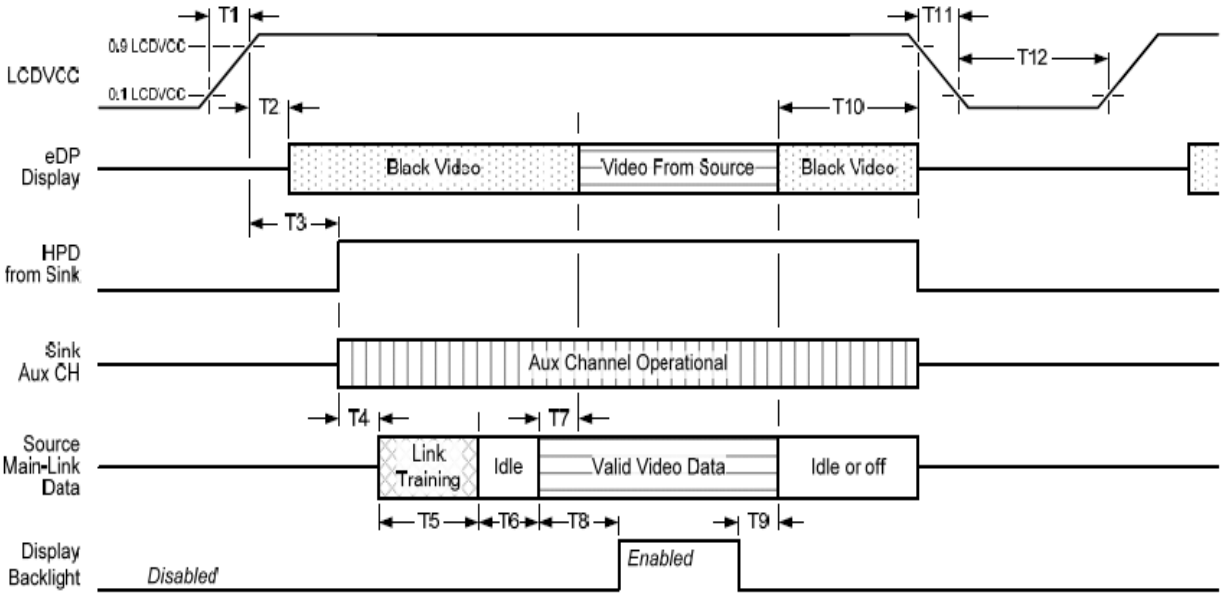
Fallow as VESA display port standard V1.1a.

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	2.25		3.6	V

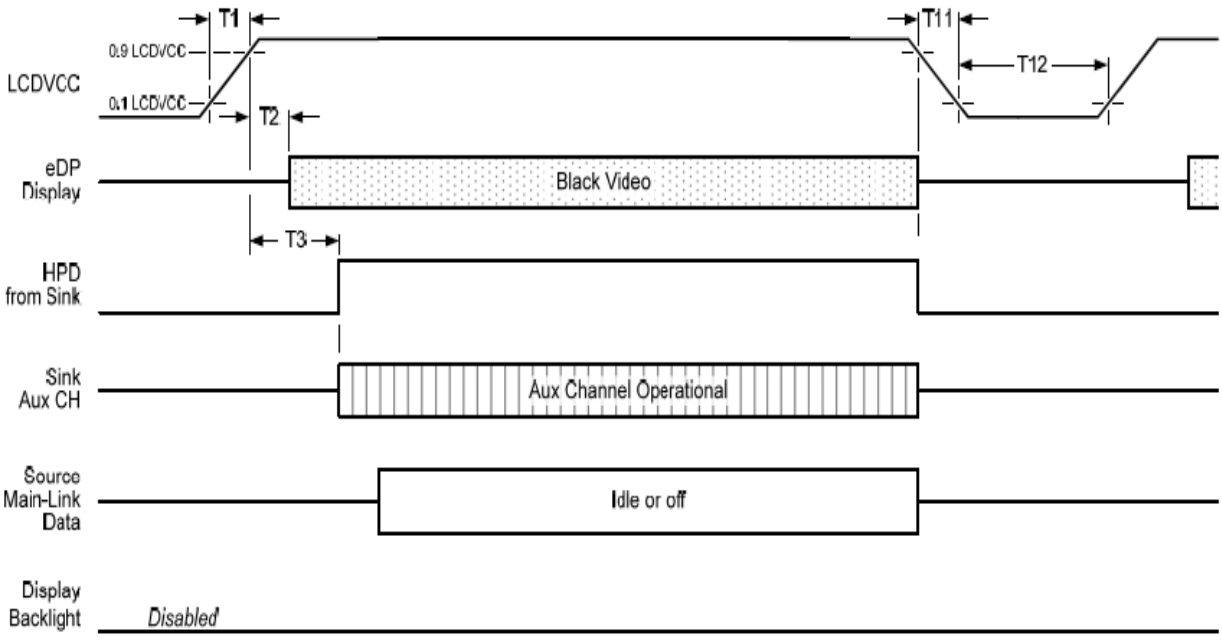
Fallow as VESA display port standard V1.1a.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

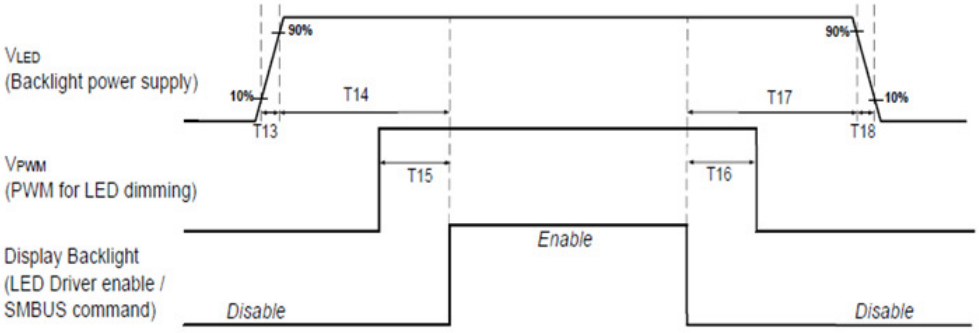
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

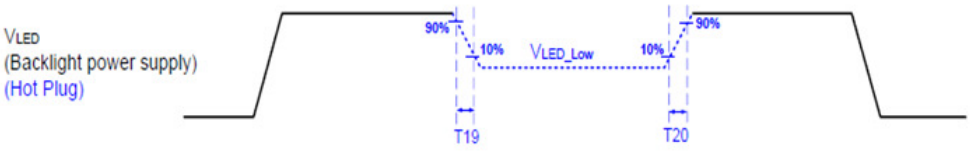


	Min (ms)	Max (ms)
T13	0.2	-
T14	0	-
T15	-	-
T16	-	-
T17	0	-
T18	0	-
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Note : If T19,T20 < 5xTPWM* , The flash display may occur. We suggest T19,T20 ≧ 5xTPWM* to realize seamless change display.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.97	[Watt]	(Ta=25℃), Note 1
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25℃), Note 2 I_F=18mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

(Efficiency=100%)

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7	12	24	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2	-	-	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	

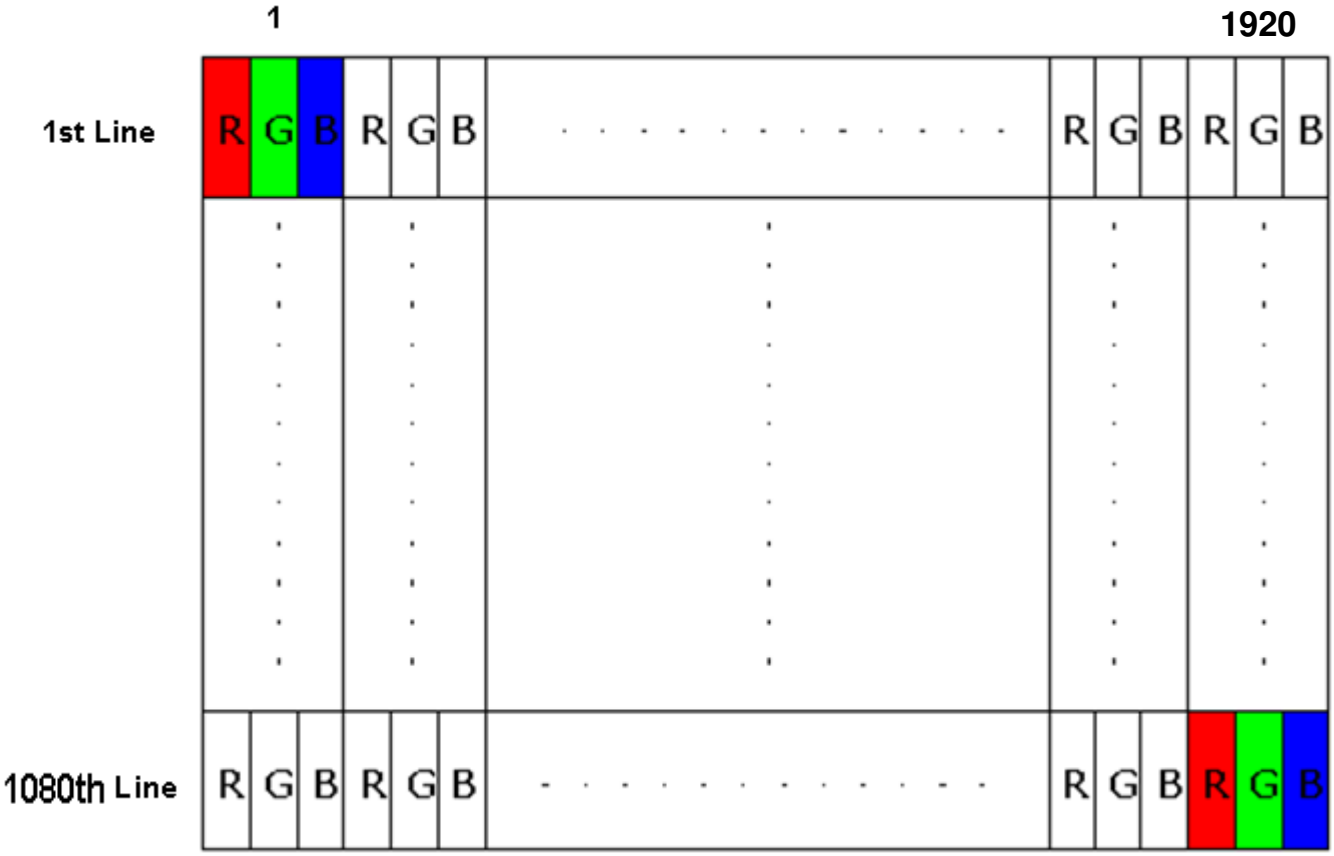
PWM Logic Input High Level	VPWM_EN	2	-	-	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency *1	FPWM	100	-	20k	Hz	
PWM Duty Ratio	Duty	0	--	100	%	

Note1: LED Power Supply is evaluated by Lextar LED.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

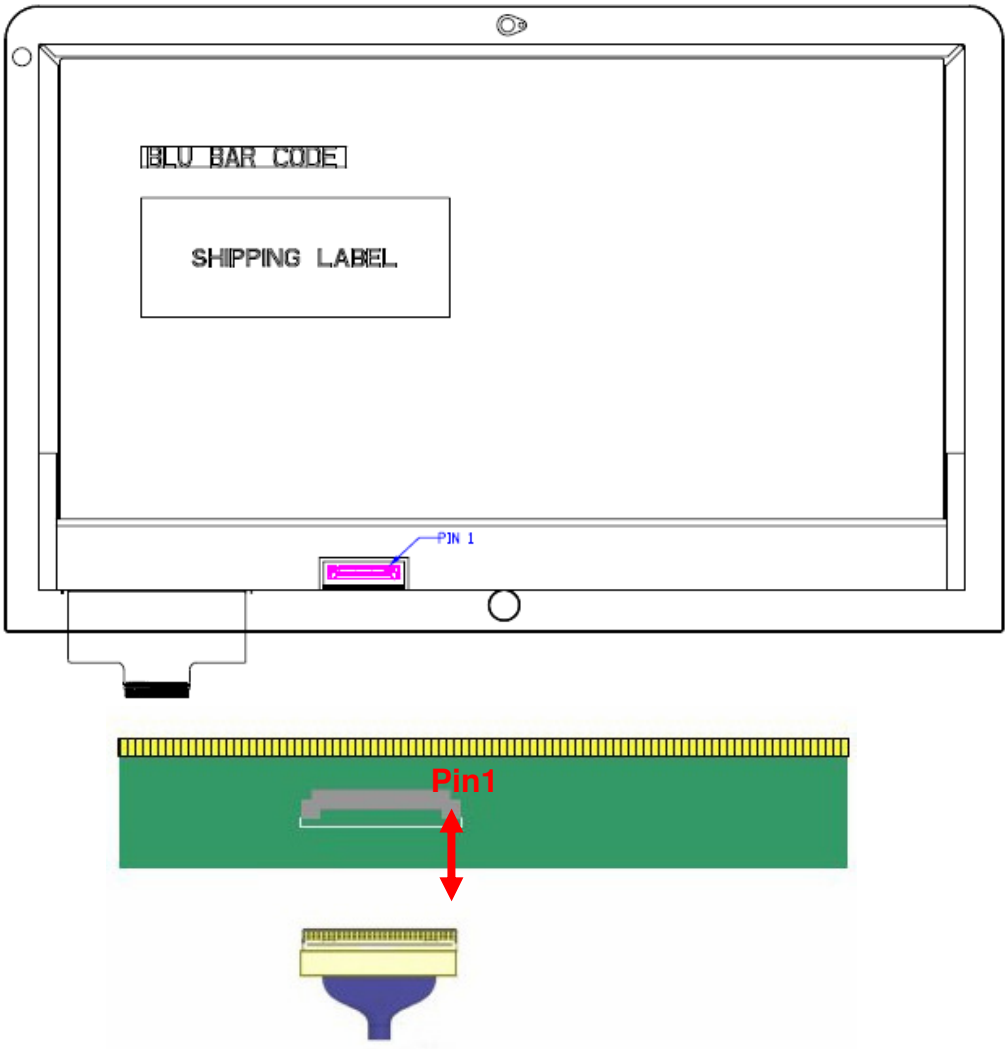
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	I-PEX 20455-030E-12
Mating Housing/Part Number	I-PEX 20453-030T-11 or Compatible

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal Name	Description
1	NC	NC
2	GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	GND	High Speed Ground
12	VDD	LCD logic and driver power
13	VDD	LCD logic and driver power
14	Aging	LCD Panel Self Test
15	GND	LCD logic and driver ground
16	GND	LCD logic and driver ground
17	HPD_N	HPD signal pin
18	GND	Backlight ground

19	GND	Backlight ground
20	GND	Backlight ground
21	GND	Backlight ground
22	LED_EN	Backlight On/Off
23	LED_PWM	System PWM signal input for dimming
24	NC-Reserved	Reserved for LCD manufacture's use(EDID_CLK)
25	NC-Reserved	Reserved for LCD manufacture's use(EDID_DATA)
26	V_LED	Backlight power
27	V_LED	Backlight power
28	V_LED	Backlight power
29	V_LED	Backlight power
30	NC	NC



Note1:Input signals shall be low or High-impedance state when VDD is off.

6.2.3 Touch Sensor Signal Description/ Pin Assignment

FPC to board side pin assignment	
PIN	Signal
1	GND
2	GND
3	GND
4	X1
5	X2
6	X3
7	X4
8	X5
9	X6
10	X7
11	X8
12	X9
13	X10
14	X11
15	X12
16	X13
17	X14
18	X15
19	X16
20	X17
21	X18
22	X19
23	X20
24	X21
25	X22
26	X23
27	X24
28	X25
29	X26
30	X27
31	X28
32	X29
33	X30
34	GND
35	GND
36	Y1
37	Y2

38	Y3
39	Y4
40	Y5
41	Y6
42	Y7
43	Y8
44	Y9
45	Y10
46	Y11
47	Y12
48	Y13
49	Y14
50	Y15
51	Y16
52	Y17
53	Y18
54	Y19
55	Y20
56	Y21
57	Y22
58	Y23
59	Y24
60	Y25
61	Y26
62	Y27
63	Y28
64	Y29
65	Y30
66	Y31
67	Y32
68	Y33
69	Y34
70	Y35
71	Y36
72	Y37
73	Y38
74	Y39
75	Y40
76	Y41
77	Y42
78	Y43

79	Y44
80	Y45
81	Y46
82	Y47
83	Y48
84	Y49
85	Y50
86	Y51
87	Y52
88	GND
89	GND
90	GND

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}		138.5		MHz
Vertical Section	Period	T_V	1084	1111	3080	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	4	30	2000	
Horizontal Section	Period	T_H	2000	2080	2320	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	80	160	400	

Note : DE mode only

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	**Ta= 40℃, 90%RH, 240h**	
High Temperature Operation	**Ta= 60℃, Dry, 240h**	
Low Temperature Operation	**Ta= -20℃, 240h**	
High Temperature Storage	**Ta= 70℃,240h**	
Low Temperature Storage	**Ta= -30℃, 240h**	
Thermal Shock Test	**Ta=-30℃(30min) ~70℃(30min), 15cycles condition**	
ESD	**Contact : ±8 KV** **Air : ±15 KV**	Note 1

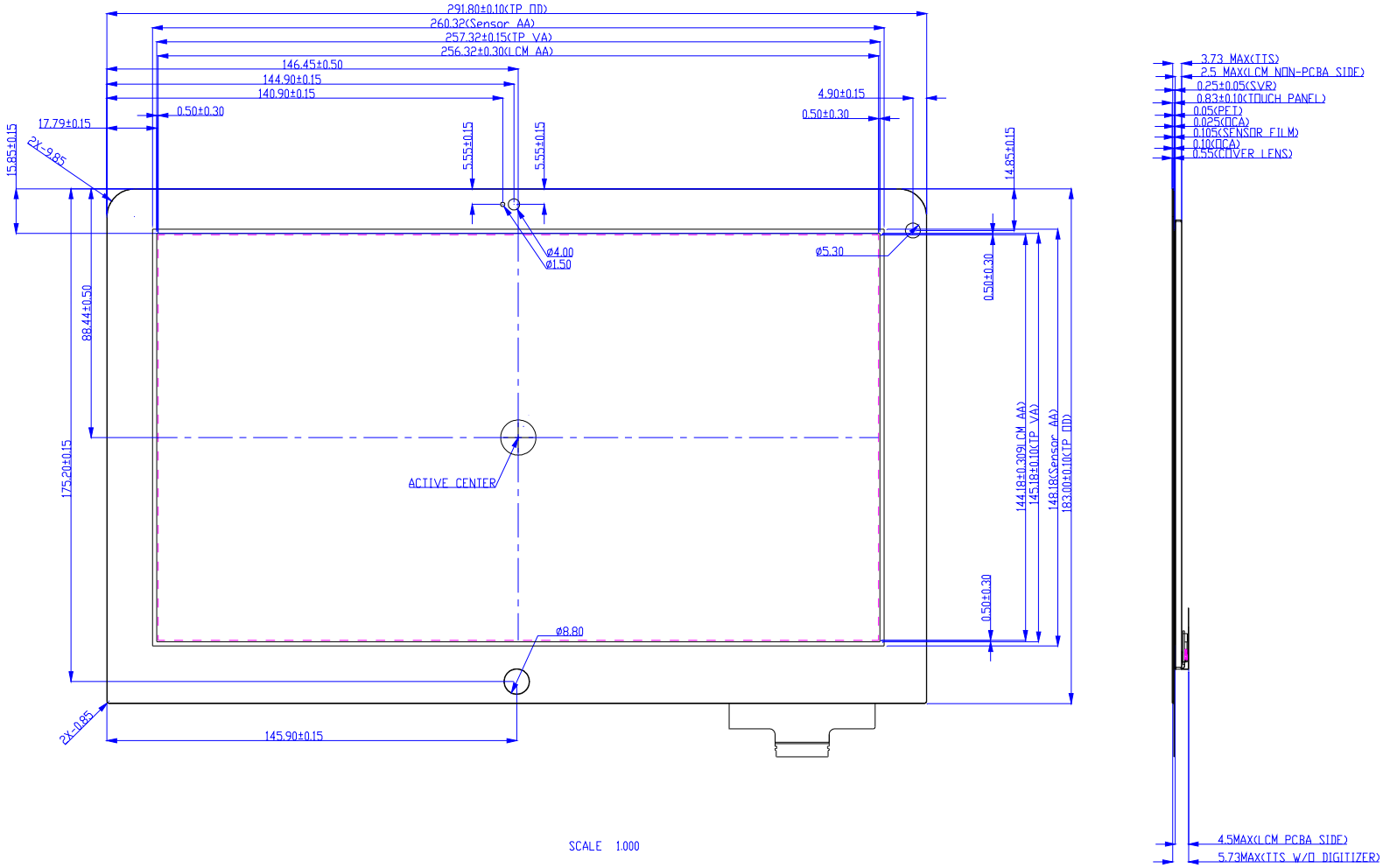
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

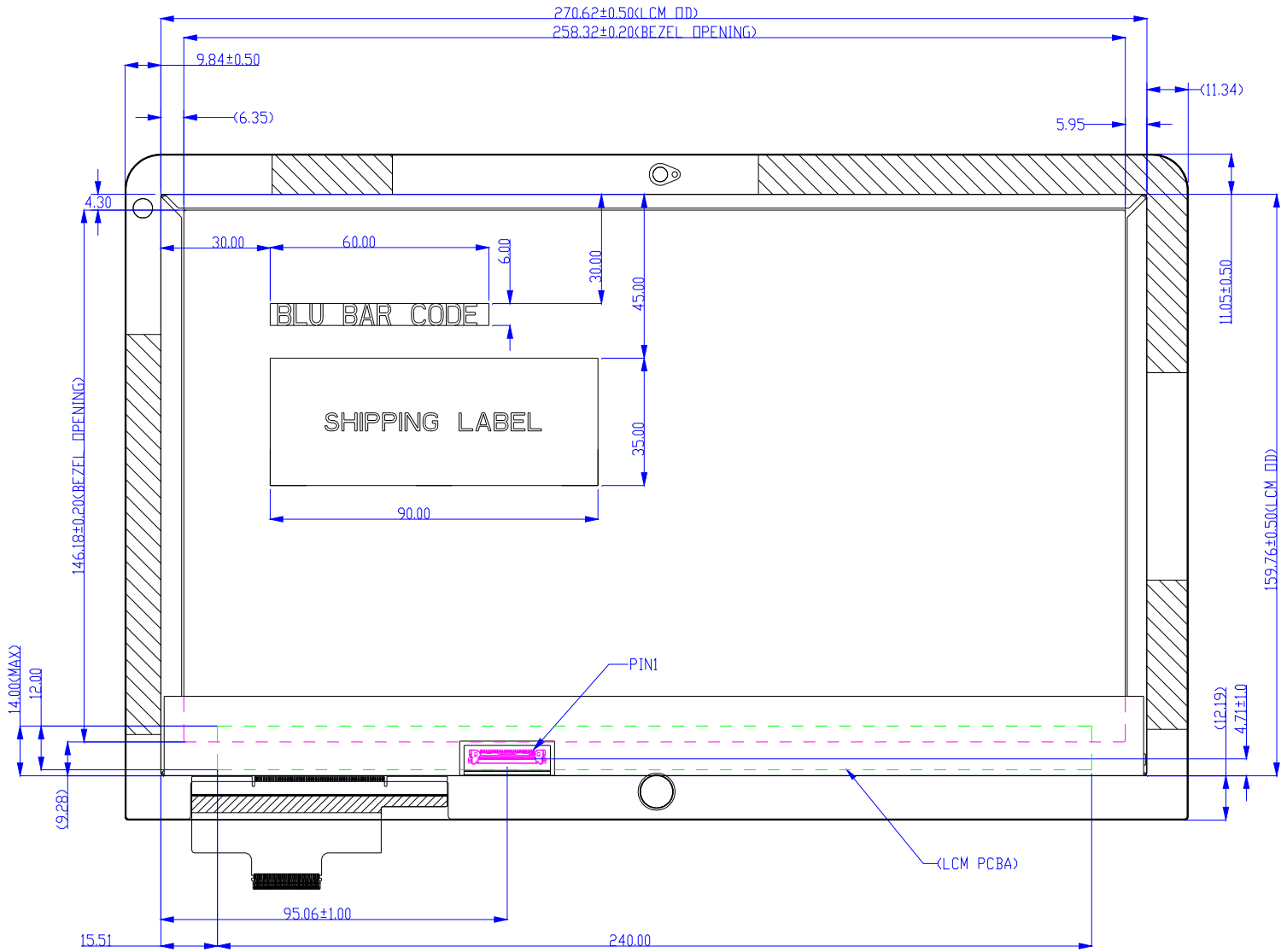
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Rear View

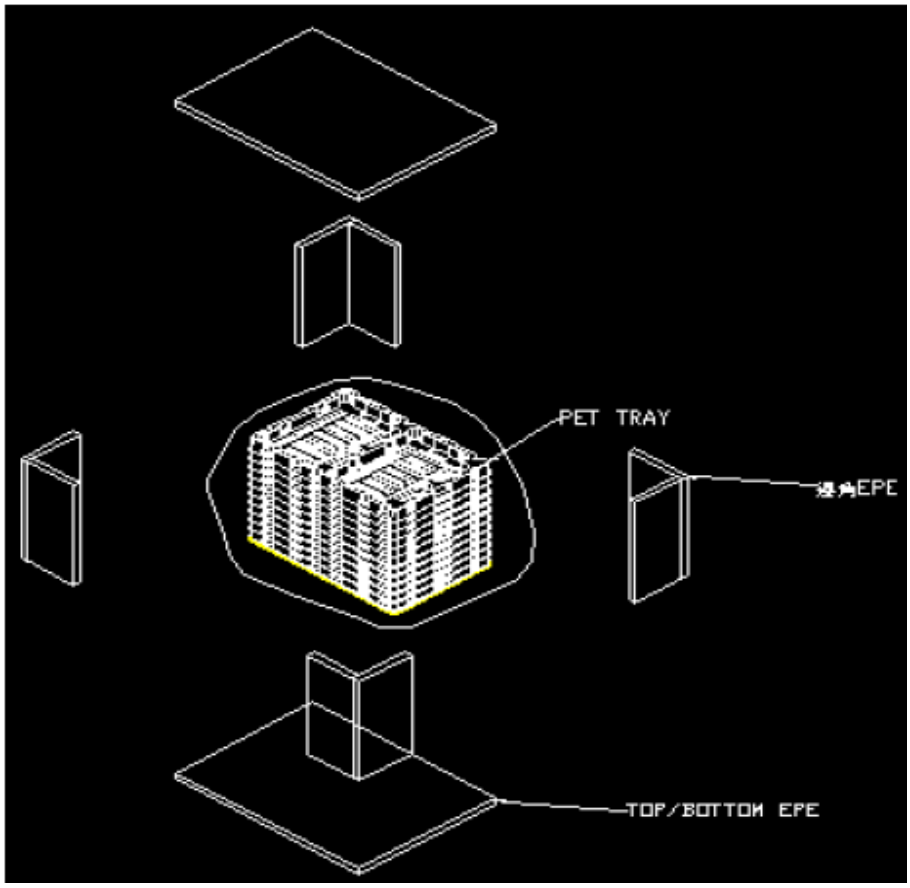


9. Shipping and Package

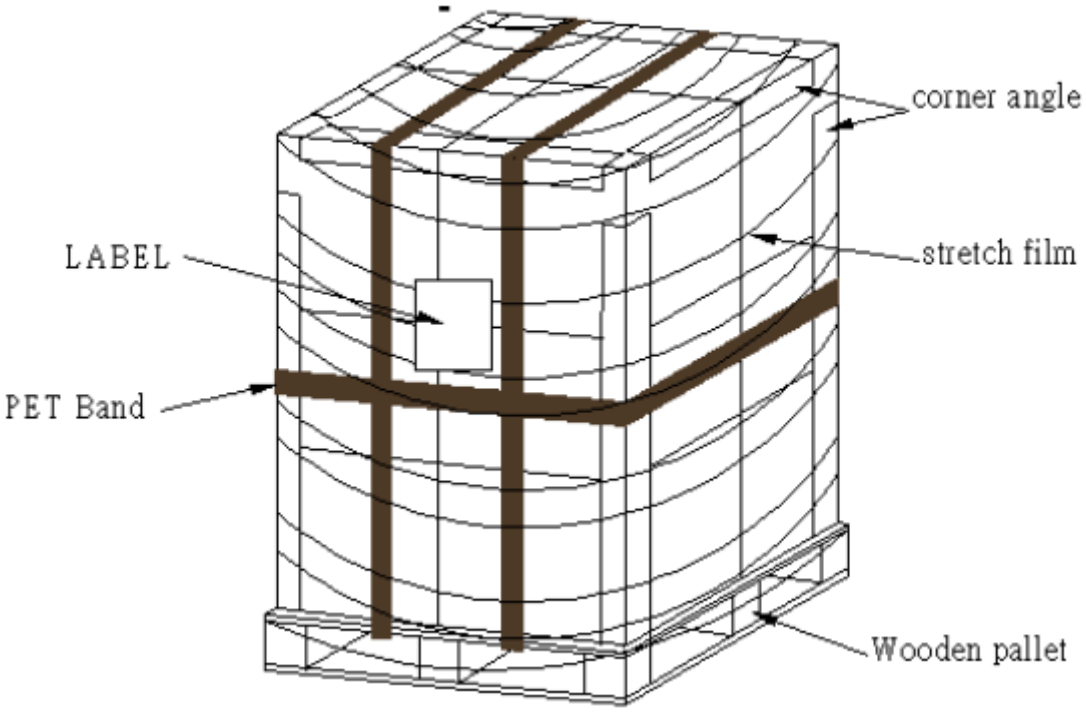
9.1 Shipping Label Format

9.2 Carton Label Format

9.3 Carton Package



9.4 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	5D	01011101	93	
0B	hex, LSB first	32	00110010	50	
0C	32-bit ser #	00	00000000	0	Color Engine Setting
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	16	00010110	22	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	95	10010101	149	
15	**Max H image size** *(rounded to cm)*	1A	00011010	26	
16	**Max V image size** *(rounded to cm)*	0E	00001110	14	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	EA	11101010	234	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	AC	10101100	172	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	F5	11110101	245	
1B	Red x **(Upper 8 bits)**	98	10011000	152	
1C	Red y/ highER 8 bits	58	01011000	88	
1D	Green x	52	01010010	82	
1E	Green y	95	10010101	149	
1F	Blue x	25	00100101	37	
20	Blue y	20	00100000	32	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	

24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	1D	00011101	29	
37	Pixel Clock/10000 USB	36	00110110	54	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	A0	10100000	160	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	38	00111000	56	
3C	Vertical Blanking **Lower 8bits**	1E	00011110	30	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	8E	10001110	142	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	00	00000000	0	
43	Vertical Image Size **Lower 8bits**	90	10010000	144	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	18	00011000	24	
49	descriptor #2	2D	00101101	45	
4A		80	10000000	128	
4B		A0	10100000	160	
4C		70	01110000	112	
4D		38	00111000	56	

4E		1E	00011110	30	
4F		40	01000000	64	
50		30	00110000	48	
51		20	00100000	32	
52		8E	10001110	142	
53		00	00000000	0	
54		00	00000000	0	
55		90	10010000	144	
56		10	00010000	16	
57		00	00000000	0	
58		00	00000000	0	
59		18	00011000	24	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		5E	01011110	94	^
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	31	00110001	49	1
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	54	01010100	84	T

78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	33	00110011	51	3
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	32	00110010	50	2
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	03	00000011	3	