Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**11.6”(11.58”) HD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B116XAN04.1(H/W:0A)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**

Approved by	**Date**
Marcus Yen	2016/07/14
Prepared by	
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Note: This Specification is subject to change without notice.

MPBU Marketing Division
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Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2014/12/10	All	First Edition for Customer		
0.2 2015/01/20	18	Connector modify		
0.3 2015/01/21	23,24	Drawing modify		
0.4 2015/05/27	5,6	16.7M colors (RGB 6bit)	262K color (RGB 6bit)	
	6	(1) Uniformity (13point) = 1.5 (2) Cross talk = 2% (3) Color: TBD	(1) Uniformity (13point) = 1.6 (2) Cross talk= 4% (3) Color: new updated	
	13	IDD= 300mA	IDD= 242mA	
	16	LED Forward Voltage=20.65typ/22.4Max	LED Forward Voltage = 29.5typ /32Max	
	18	Connector	Connector add “or compatible”	
	19	N/A	New add	
	20	Old timing table	New timing table	
	23	N/A	New add	
	24	7.3 Reliability Test (Old version)	7.3 Reliability Test (New version)	
	25	Label w/o manufacture fab	Label w/ manufacture fab	
1.0 2015/08/14	All		Final Spec	
1.1 2016/07/14	5	Normally Black	Normally Black (AHVA)	
	13	IDD Current	IDD Current (RMS)	
	34		Add Note 10.2	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B116XAN04.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262K colors (RGB 6-bits) with LED backlight driving circuit. All input signals are eDP (Embedded DisplayPort) interface compatible.

B116XAN04.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	294.09 (11.58W")			
Active Area	[mm]	256.125(H) x 144(V)			
Pixels H x V		1366 x 3(RGB) x 768			
Pixel Pitch	[mm]	0.1875 X 0.1875			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black (AHVA)			
White Luminance (I_{LED}=25mA) **(Note: ILED is LED current)**	[cd/m^2]	220typ. (5 points average) 187 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	27 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.8W @Mosaic Pattern			
Weight	[Grams]	200 max.			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	267.5	268.0	268.5
		Width	167.5	168.0	168.5
		Thickness	--	--	2.8 (Panel Side) 3.0 (PCBA Side)
Electrical Interface		1 lane eDP			
Glass Thickness	[mm]	0.4			
Surface Treatment(panel only)		Anti-Glare,Hardness 3H			

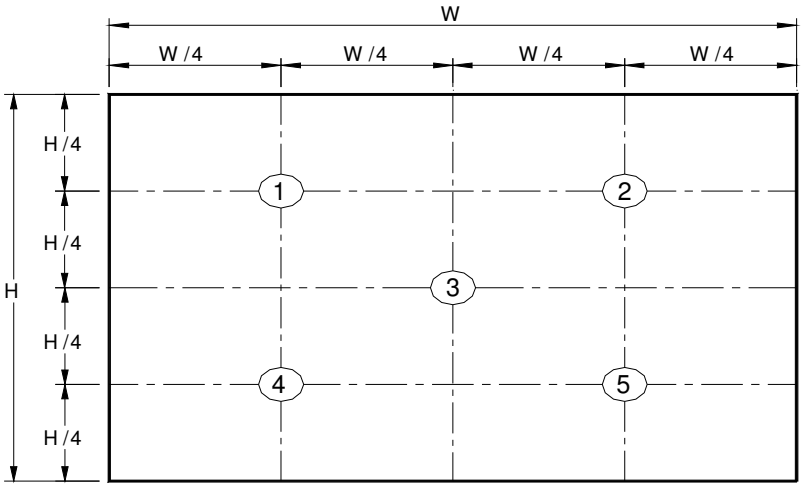
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

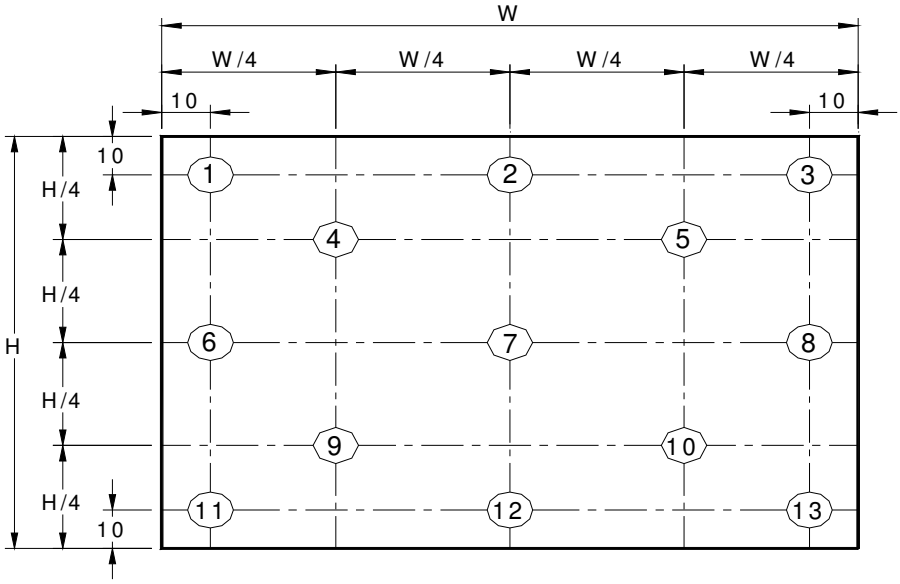
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=25mA			5 points average	187	220	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	--- ---	85 85	--- ---	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	--- ---	85 85	--- ---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	---	---	1.60		2, 3, 4
Contrast Ratio		CR		---	800	---		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	27	35	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.560	0.590	0.620		4
		Ry		0.320	0.350	0.380		
	Green	Gx		0.302	0.332	0.362		
		Gy		0.544	0.574	0.604		
	Blue	Bx		0.126	0.156	0.186		
		By		0.081	0.111	0.141		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		---	50	---		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



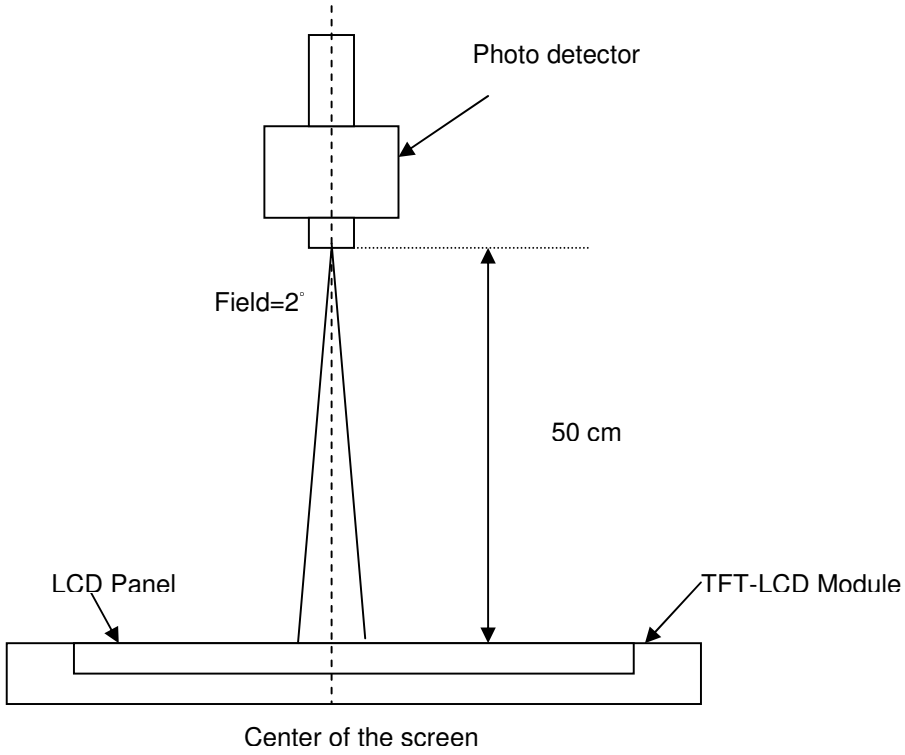
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

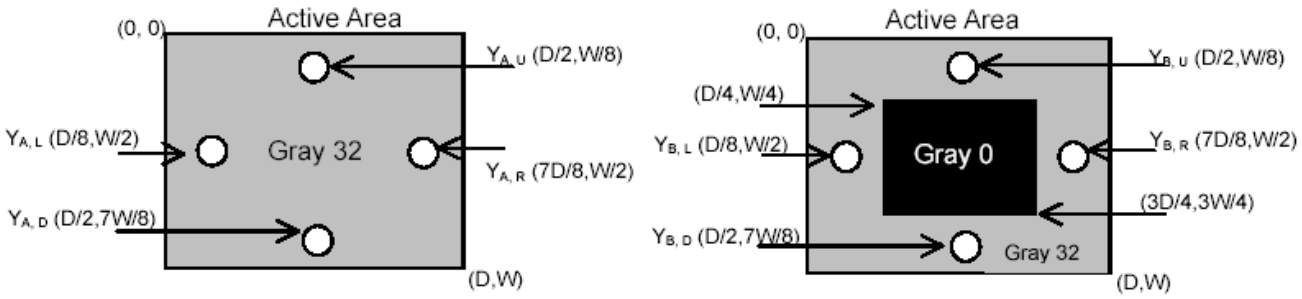
Note 7： Definition of Cross Talk (CT)

CT = | YB – YA | / YA × 100 (%)

Where

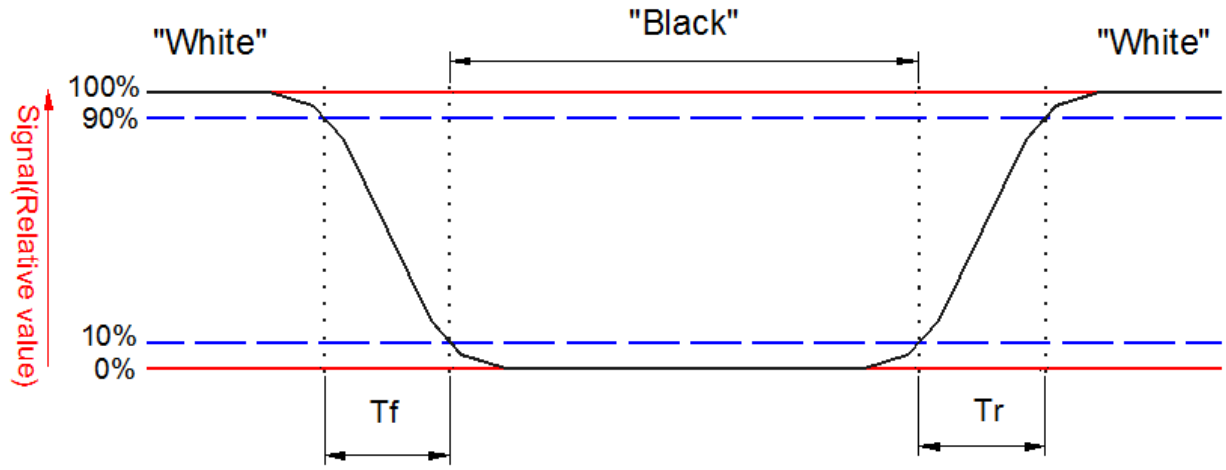
YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



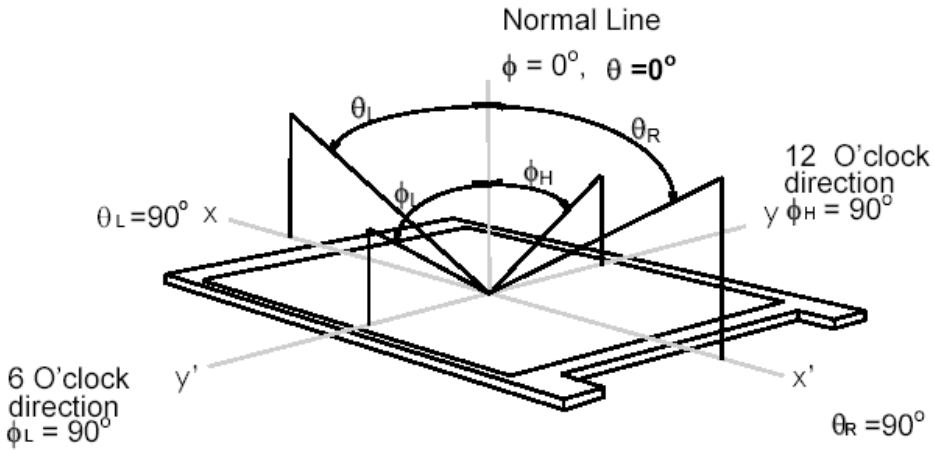
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (rising time) and from “White” to “Black” (falling time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



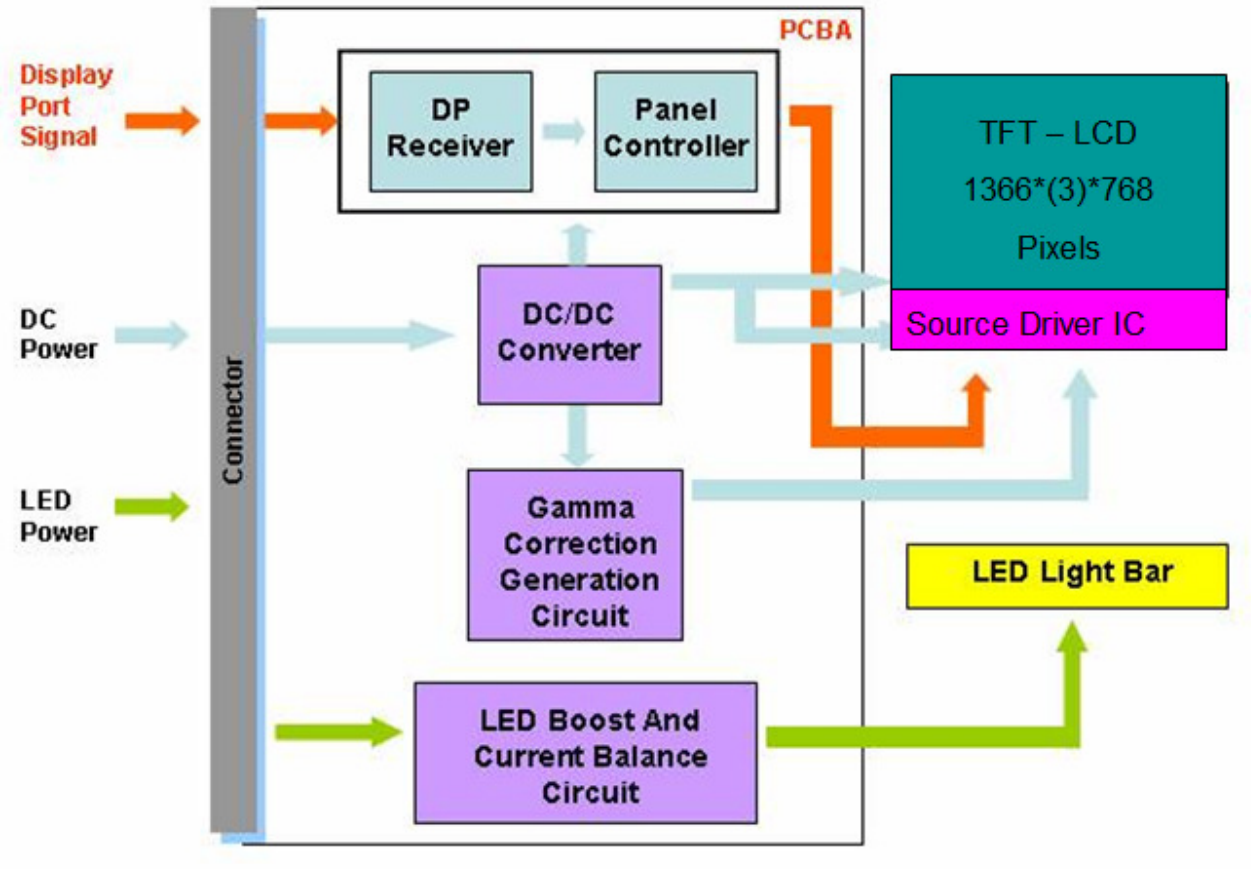
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/ LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

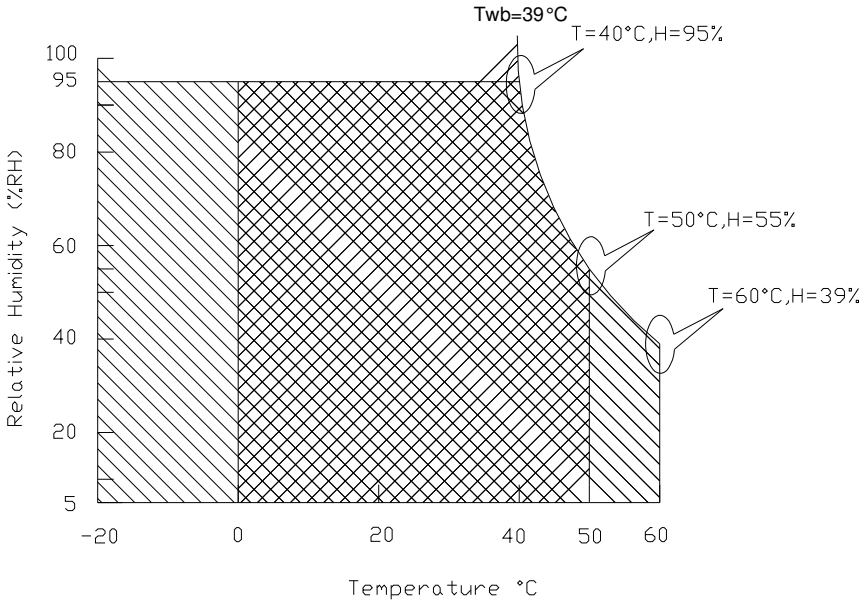
4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)
Note 2: Permanent damage to the device may occur if exceed maximum values
Note 3: LED specification refer to section 5.2
Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
Note 5: The packing material of system forbid to involve ammonium component.
Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module.
Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



Operating Range Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

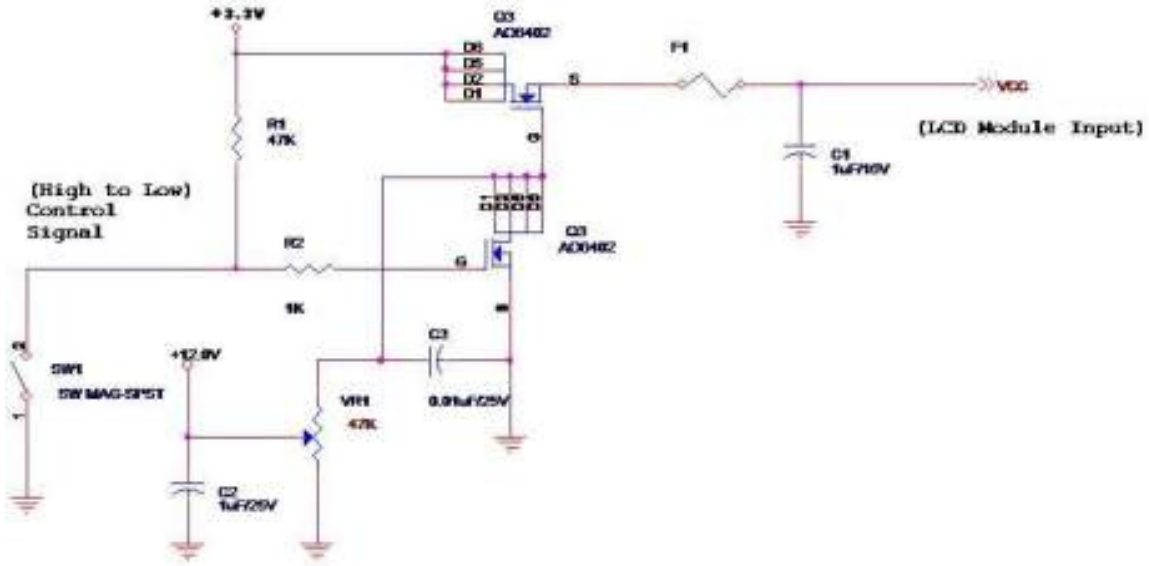
The power specification are measured under 25℃ and frame frenquency under 60Hz

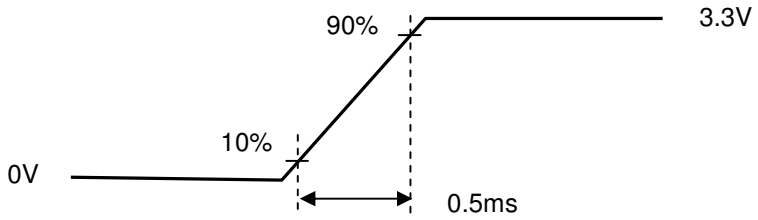
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	at Mosaic Pattern
IDD	IDD Current (RMS)	-	-	242	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Mosic Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{Mosaic}$)

Typical Measurement Condition : Mosaic Pattern

Note 2：Measure Condition





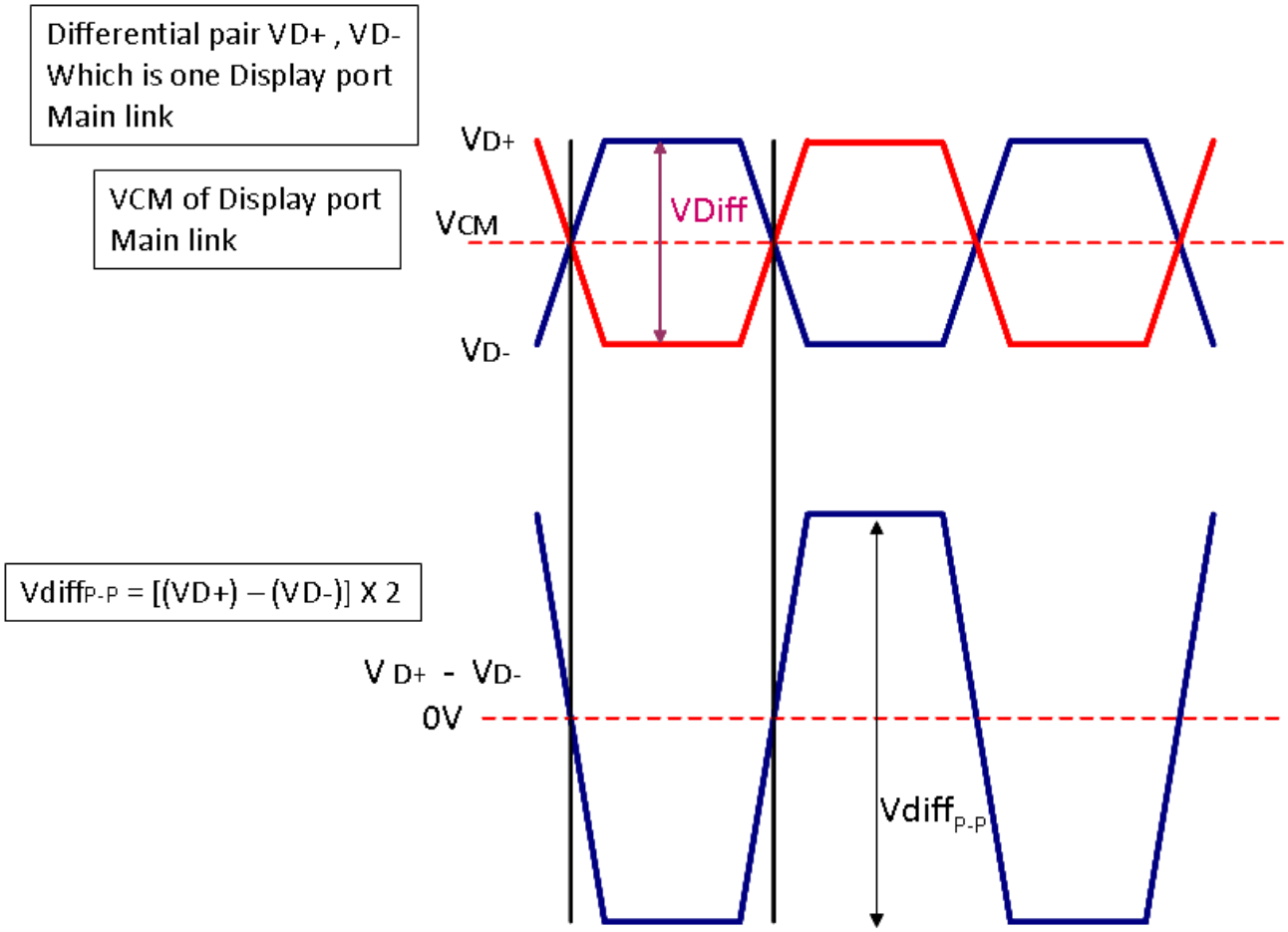
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:

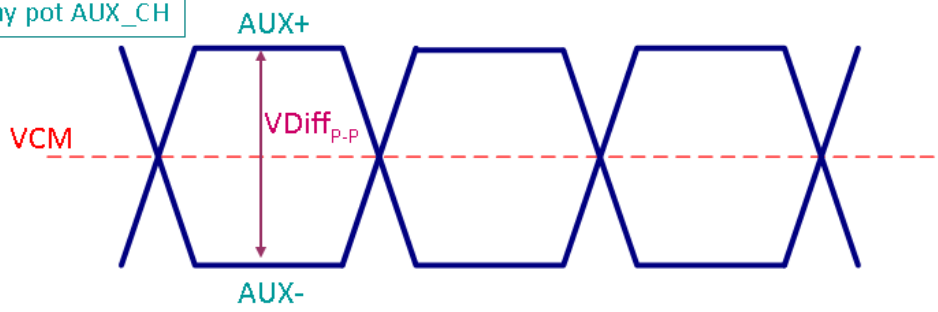


Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	120		1320	mV

Follow as VESA display port standard V1.1a.

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display pot AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display Port VHPD					
		Min	Typ	Max	unit
VHPD	HPD voltage	2.25		3.6	V

Follow as VESA display port standard V1.1a.

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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.0	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=25mA
LED Forward Voltage	VF	2.8	2.95	3.2	[Volt]	
LED Forward Voltage of every LED string	VF-string	-	29.5	32	[Volt]	
LED Forward Current	IF		25		[mA]	

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency
Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

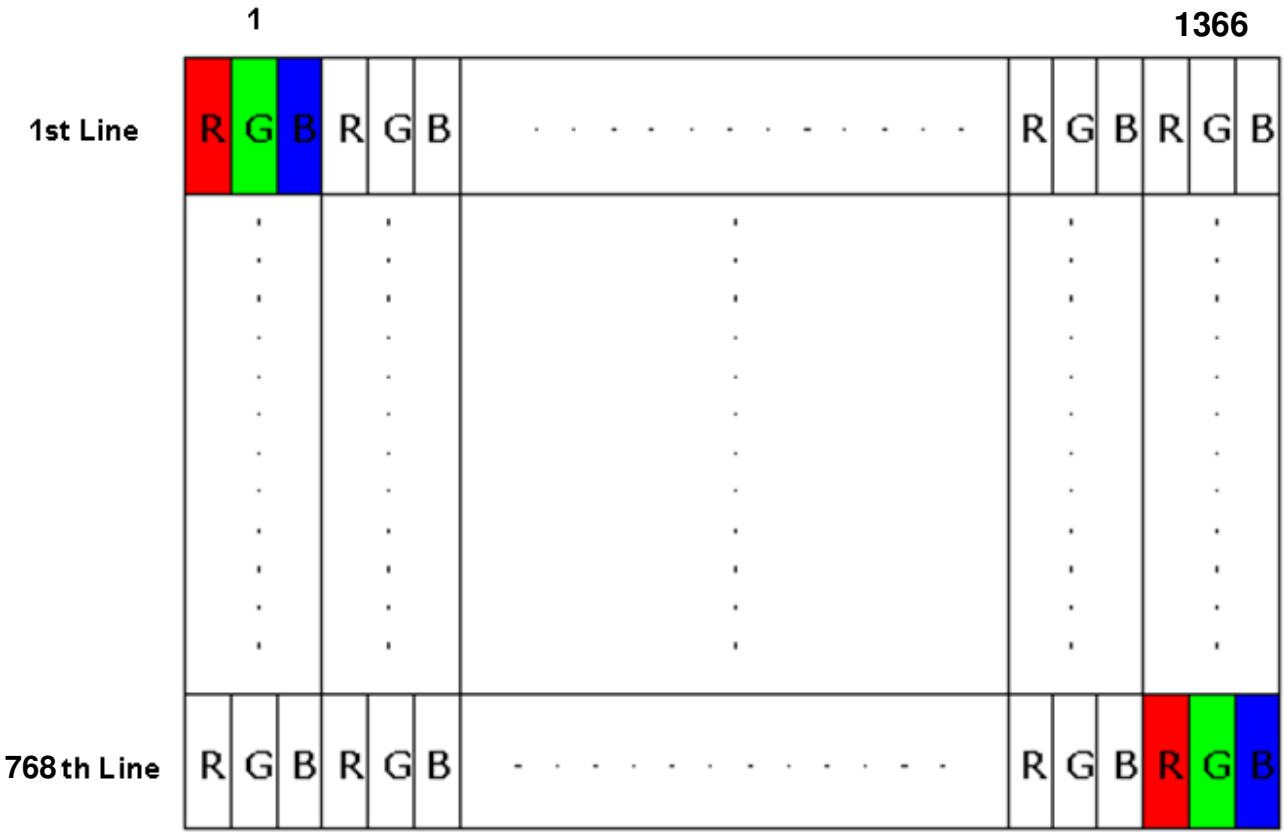
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃) **Note 1**
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	-	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6.Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX or compatible
Type / Part Number	20455-030E-12R or compatible
Mating Housing/Part Number	20453-030T or compatible

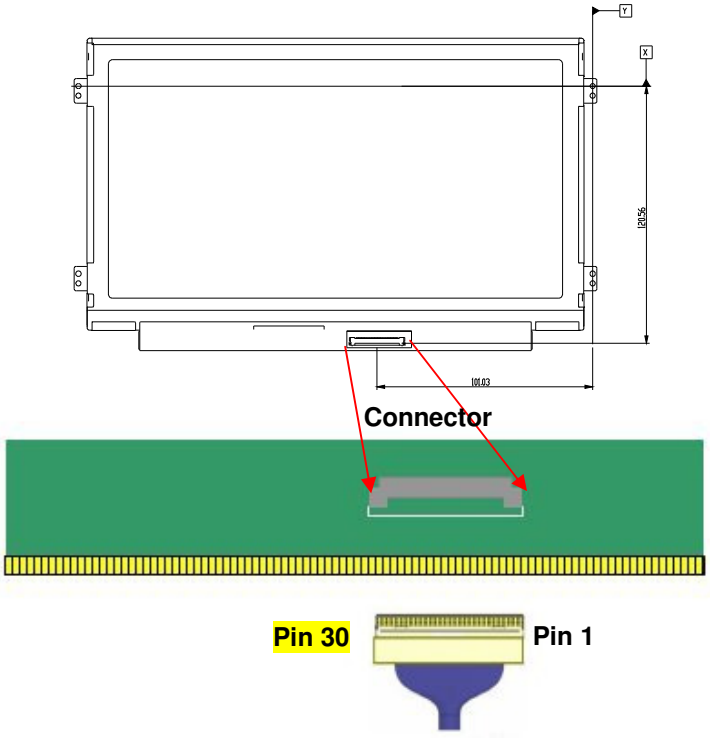
6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

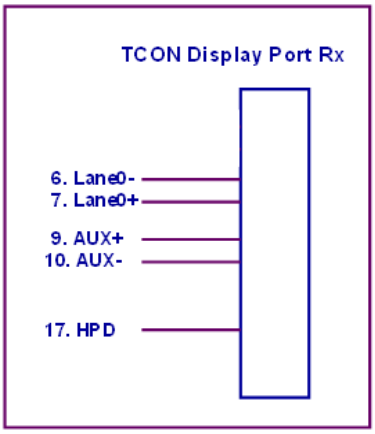
PIN#	Signal Name	Description
1	NC	NC
2	GND	Ground
3	NC	NC
4	NC	NC
5	GND	Ground
6	Lane0_N	Complement signal link lane0
7	Lane0_P	True signal link lane0
8	GND	Ground
9	AUX_CH_P	True signal Auxiliary Channel
10	AUX_CH_N	Complement signal Auxiliary Channel
11	GND	Ground
12	LCD_VCC	Logic power
13	LCD_VCC	Logic power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD_IN	HPD Signal in
18	LED_GND	Backlight_ground
19	LED_GND	Backlight_ground
20	LED_GND	Backlight_ground
21	LED_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL_PWM	System PWM signal Input

24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	V_LED	Backlight power (6V~21V)
27	V_LED	Backlight power (6V~21V)
28	V_LED	Backlight power (6V~21V)
29	V_LED	Backlight power (6V~21V)
30	NC	NC

Note1：Start from right side
Note2：Input signals shall be low or High-impedance state when VDD is off.



Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

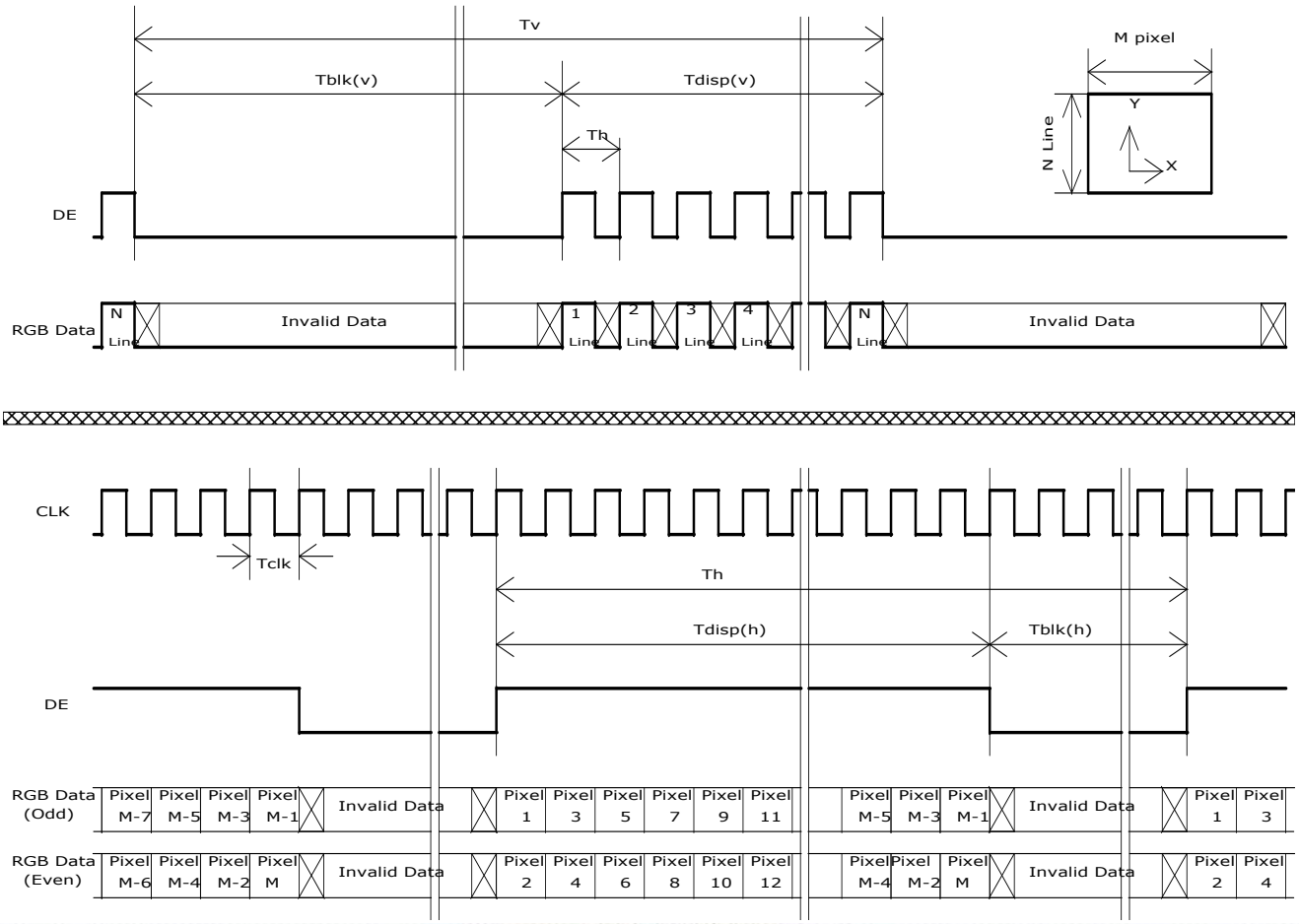
6.3.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	67	69.3	76.3	MHz
Vertical Section	Period	T_V	778	793	768+A	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	20	25	A	
Horizontal Section	Period	T_H	1416	1456	1366+B	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	50	90	B	

Note 1:The abobe is as optimized setting
Note 2:The maximum clock frequency = (1366+B)*(768+A)*60 <76.3MHz

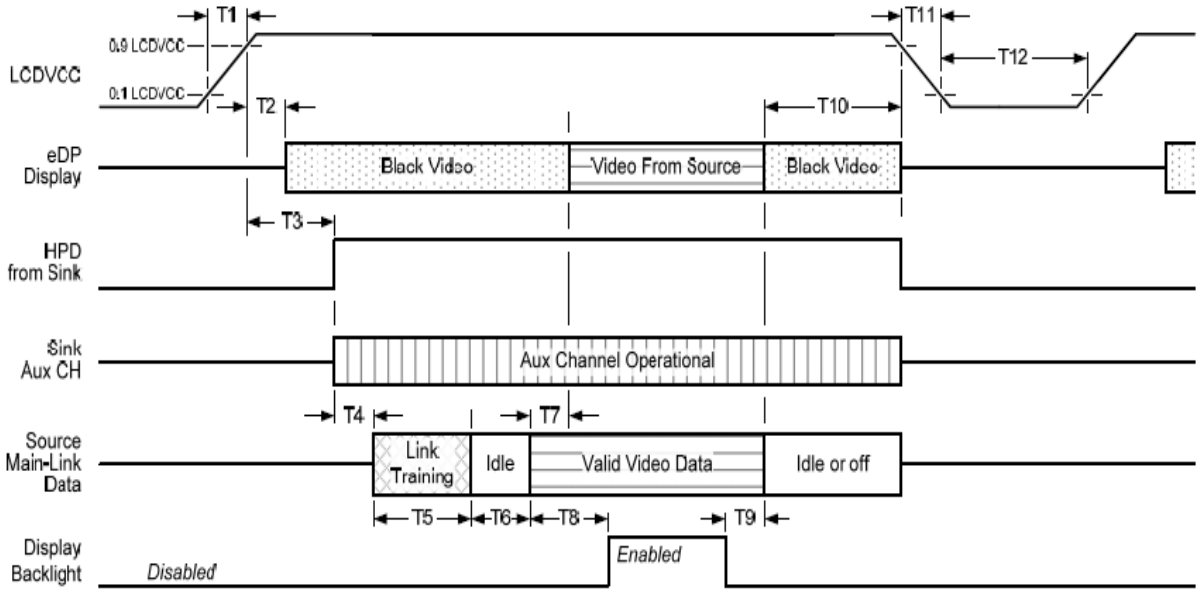
6.3.2 Timing diagram



6.4 Power On/OFF Sequence

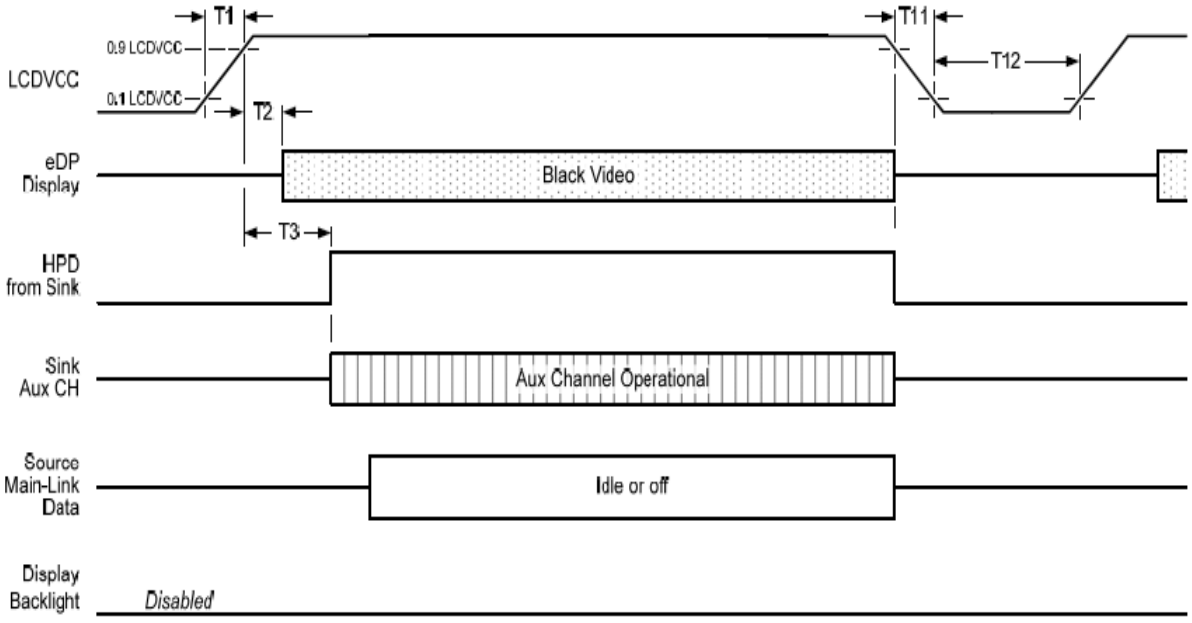
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

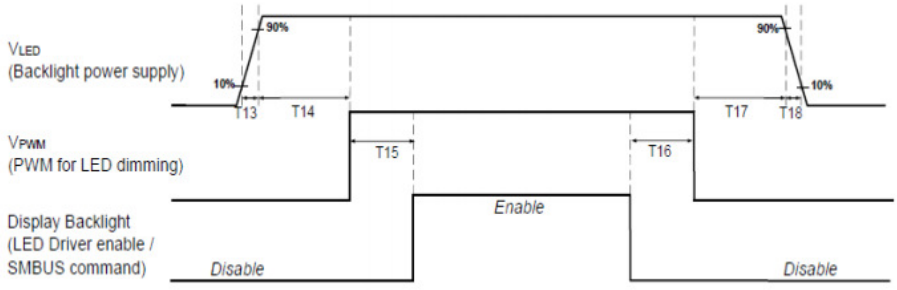
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

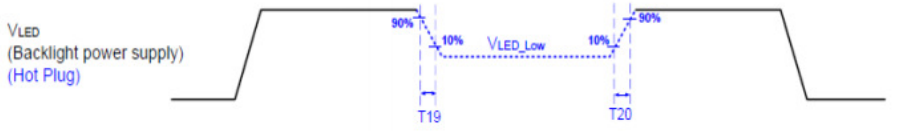
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

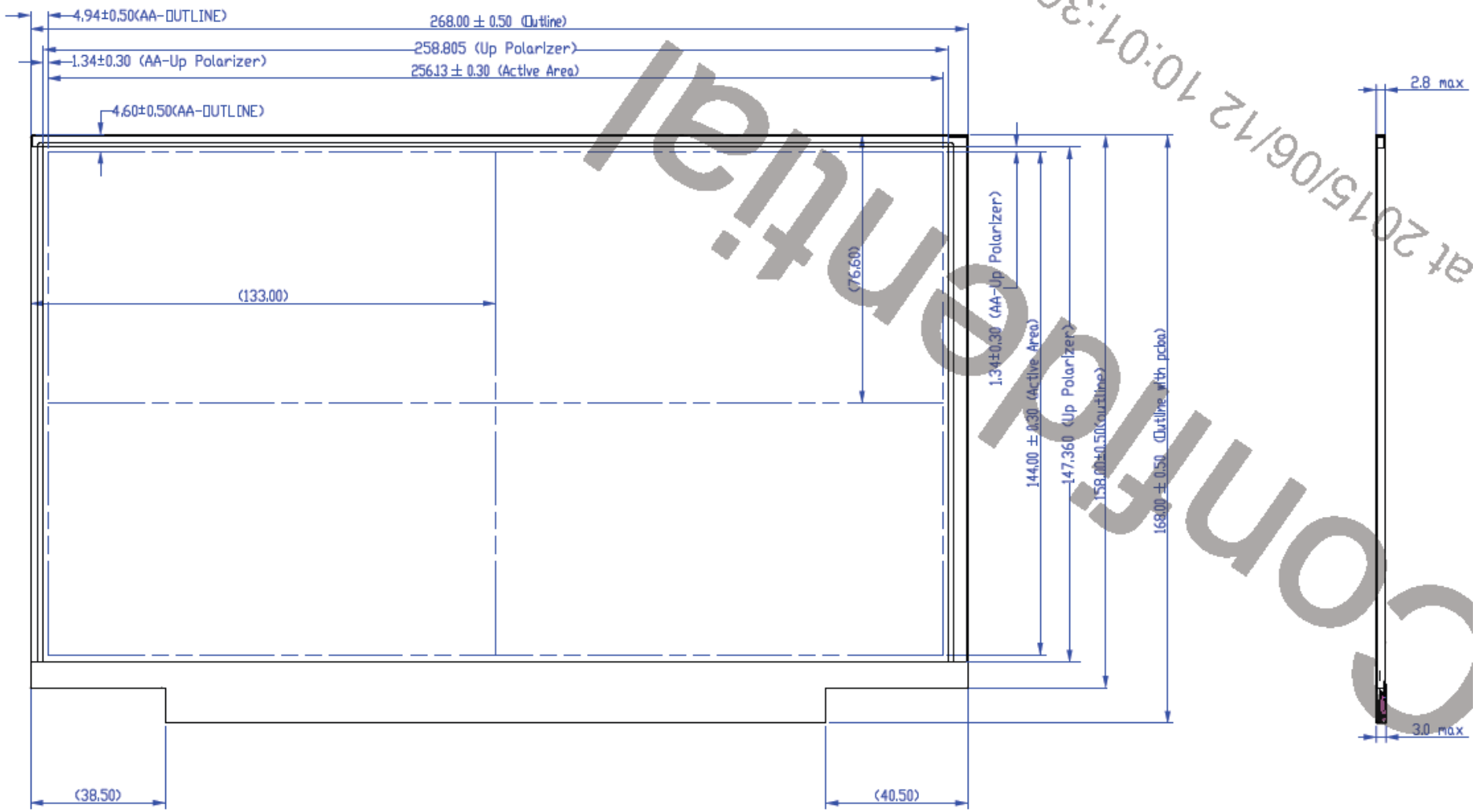
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

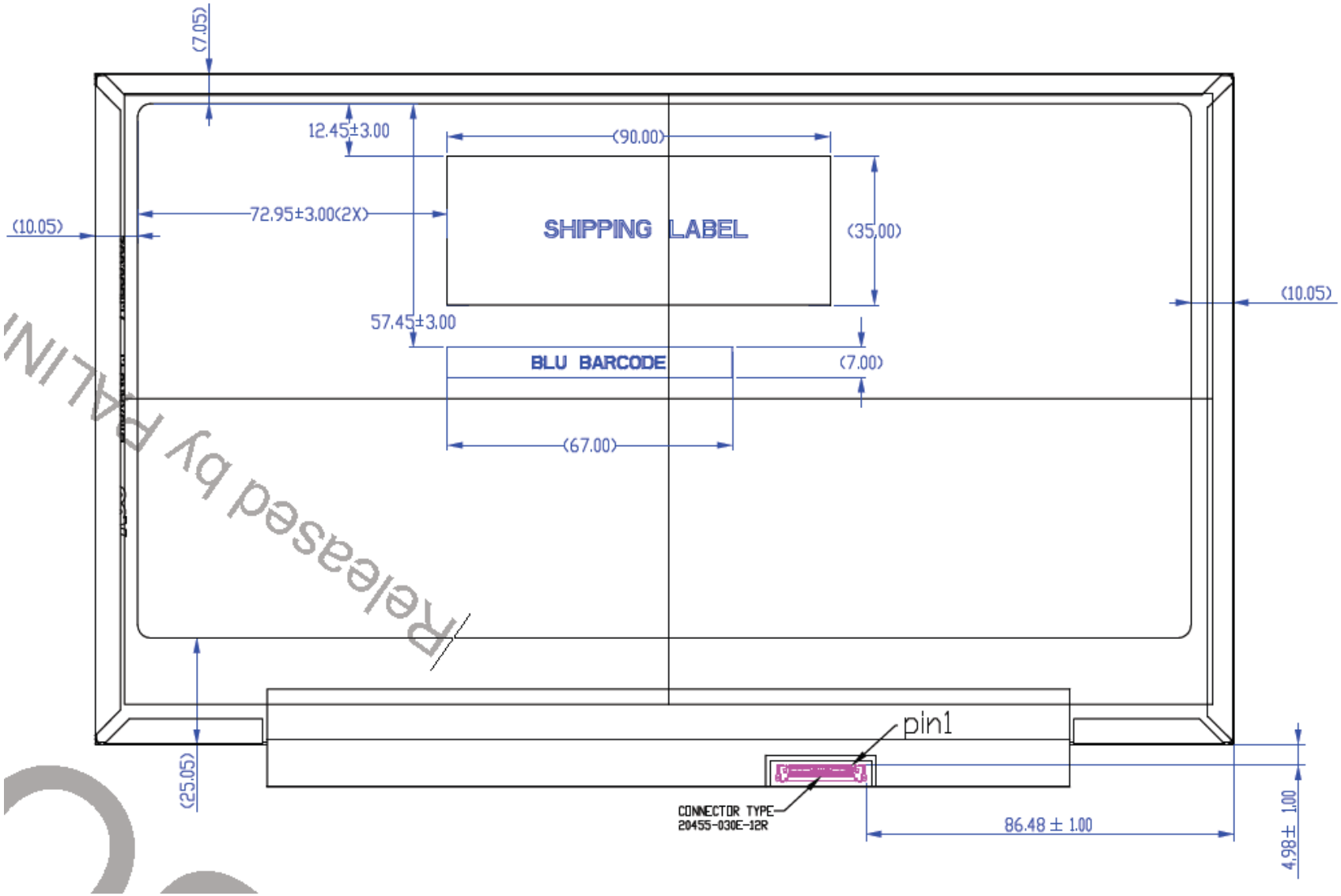
8. Mechanical Characteristics

8.1 Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Back View

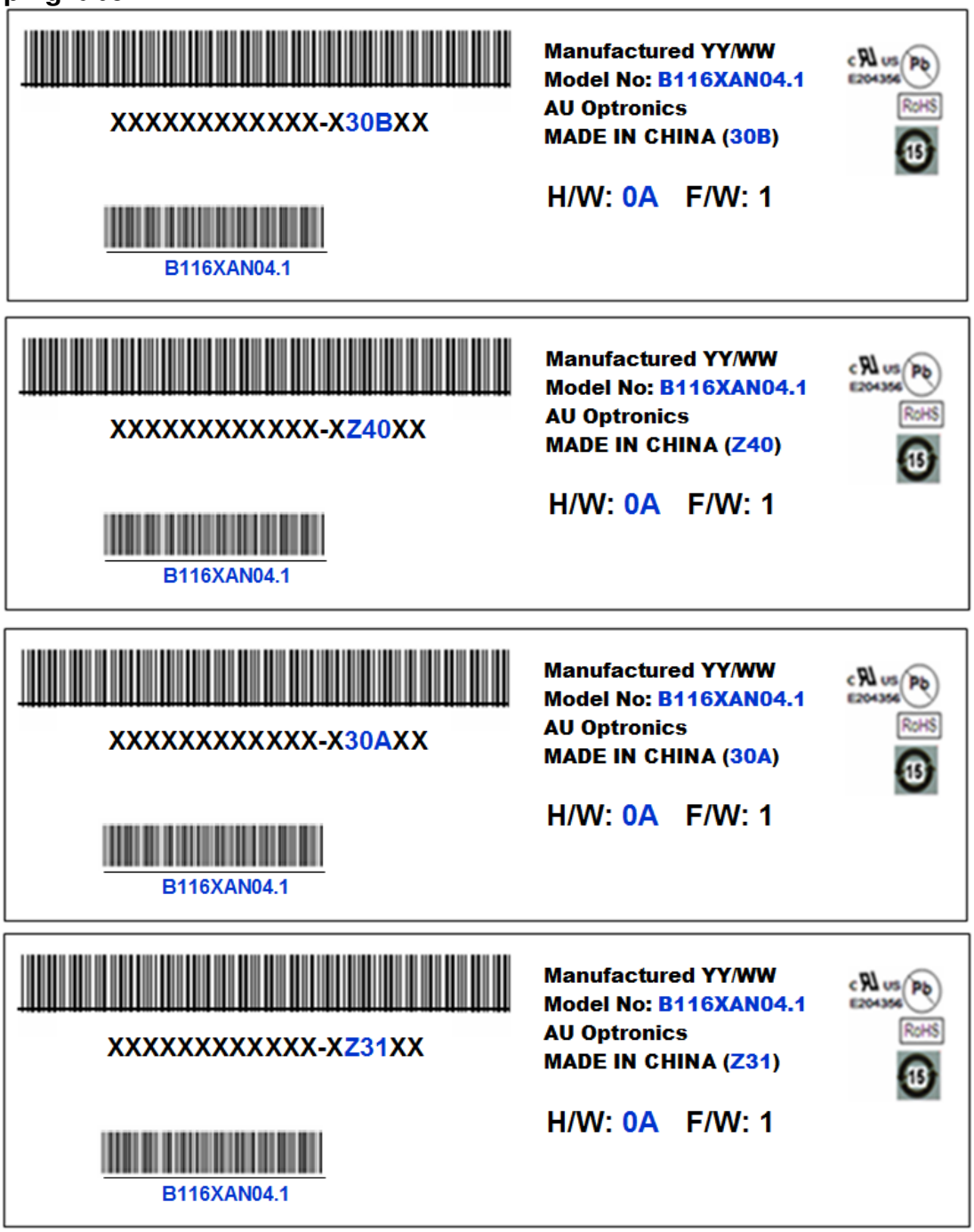


Note: AUO using caliper to measured outline dimension.

9. Shipping and Package

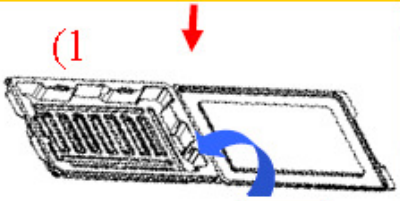
9.1 Label Format

Shipping label



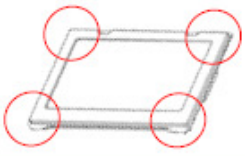
9.2 Carton Package

1.Add pull tape at the position of corner of panel's P board side, as shown in the above drawing



2. The panel mus be faceup, and place 1PCS panel first then place 1PCS Spacer, total 5PCS PANEL and 5PCS SPACER in one tray box

3. Close the tray box .



4. Check if the four corners of tray box are properly sealed.

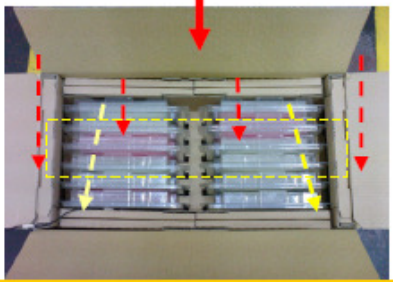
5.Tray Boxes upright placed left and right in the carton, 6 tray boxes each side.

➢LCM AA must face the direction withAUO Logo

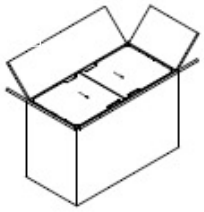
6.Tray box at both side should face front

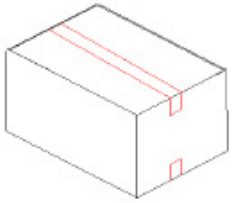
Place direction in the carton

7.Tray box opening side on top while palced in the cuhion

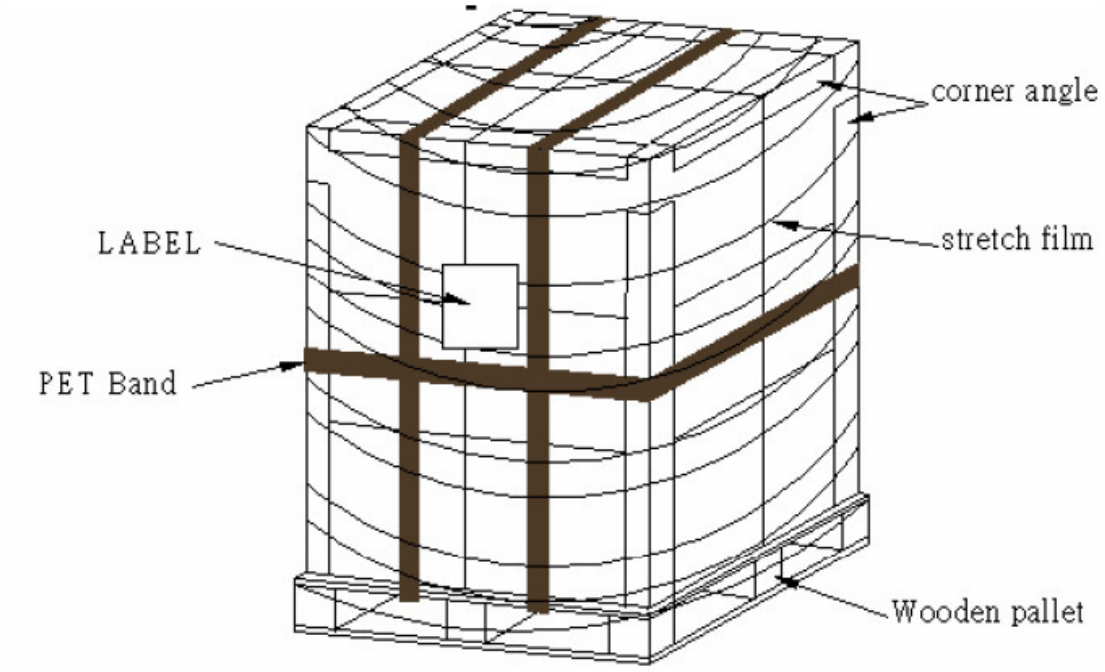


6PCS tray box per side, total 12PCS Tray box





9.3 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	5C	01011100	92	
0B	hex, LSB first	40	01000000	64	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	19	00011001	25	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	90	10010000	144	
15	**Max H image size** *(rounded to cm)*	1A	00011010	26	
16	**Max V image size** *(rounded to cm)*	0E	00001110	14	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	99	10011001	153	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	85	10000101	133	
1B	Red x **(Upper 8 bits)**	95	10010101	149	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	56	01010110	86	
1E	Green y	92	10010010	146	

1F	Blue x	28	00101000	40	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	12	00010010	18	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active **Lower 8bits**	56	01010110	86	
39	Horz blanking **Lower 8bits**	5A	01011010	90	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80	
3B	Vertical Active **Lower 8bits**	00	00000000	0	
3C	Vertical Blanking **Lower 8bits**	19	00011001	25	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	46	01000110	70	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	

42	Horizontal Image Size **Lower 8bits**	00	00000000	0	
43	Vertical Image Size **Lower 8bits**	90	10010000	144	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	

65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	31	00110001	49	1
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	58	01011000	88	X
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	34	00110100	52	4
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	CC	11001100	204	

10.2 Notes

1) The height of cell tape no higher than top polarizer 3.0mm
2) Marking DPCD version, including PSR, PSR2, MBO, VESA DSC,

DPCD Ver.	PSR	MBO	VESA DSC
1.2	Off	Off	Off

3) LED Driving Solution: Minimum change scale duty of the PWM is 0.1% @PWM frequency 200Hz.
4) When twisting or pressing LCD module, it may cause unexpected acoustic noises or sounds.
5) Maximum value of “Peak current” is as same as “Inrush current” in Electrical Characteristics (Power Specification)
6) $VDiff_{P-P}$ (Peak-to-peak Voltage at a receiving Device) follow as VESA display port standard (test point, TP3, is on panel’s PCBa)