( ) Preliminary Specifications
(v) Final Specifications

Module	**11.6”HD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B116XTT01.0 (H/W: 2A)
Note ( )	*e-TP Display* *(LCM:B116XTN02.2 +TP : I116FGT10.0)*

Customer	**Date**	**Approved by**	**Date**
		Marcus.Yen	2017/12/14
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Huiwen.Huang	2017/12/14
Note: This Specification is subject to change without notice.		**NBBU Marketing Division** **AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2017/10/03	All	First Edition for Customer		
1.0 2017/12/14	All	Final spec.		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B116XTT01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116XTT01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	**Unit**	**Specifications**			
Screen Diagonal	[mm]	293.8mm			
Active Area	[mm]	256.125 x 144.0			
Pixels H x V		1366 x 3 (RGB) x 768			
Pixel Pitch	[mm]	0.1875 x 0.1875			
Pixel Format		R.G.B Vertical stripe			
Display Mode		Normally White			
White Luminance (ILED= 20mA) **(Note: ILED is LED current)**	[cd/m^2]	220 typ. (5 points average) (Total Solution) 187 min. (5 points average) (Total Solution)			
Luminance Uniformity		1.6 max (13points)			
Contrast Ratio		500 typ.			
Response Time	[ms]	8 typ/16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.11 max. (Include Logic, TP and BLU power)			
Weight	[Grams]	280 max.			
Physical Size **Include bracket** **(Panel only)**	[mm]		Min.	Typ.	Max.
		Length	277.5	278.0	278.5
		Width	172.04	172.54	173.04
		Thickness	_	_	3.95
Physical Size **Include bracket** **(Total Solution)**	[mm]		Min.	Typ.	Max.
		Length	277.5	278.0	278.5
		Width	172.04	172.54	173.04
Electrical Interface		eDP 1.2 (1 lane)			
Glass Thickness	[mm]	0.4			
Surface Treatment		Glare, hardness 7H			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.1.1 General Touch Specification

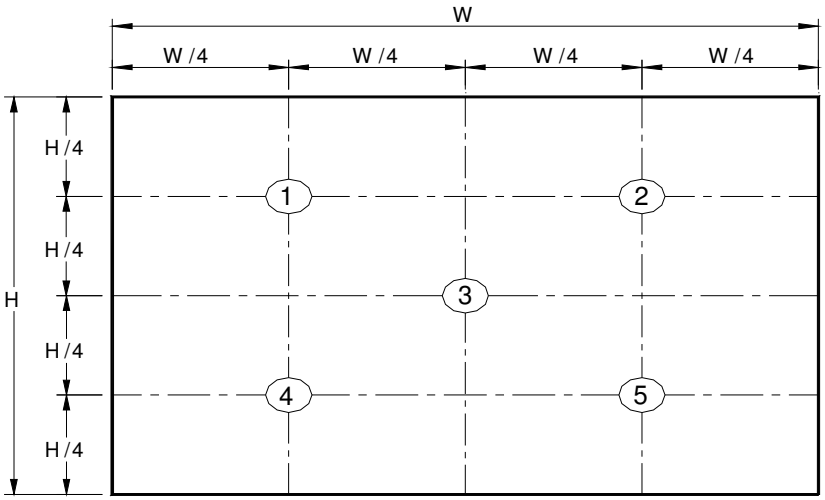
Items	Unit	Specifications
Type of Touch Sensor		Projective Capacitive (OGS)
Panel Size		11.6”
Outline Dimension	mm	265.2mm x 155.3mm
Total Thickness	mm	0.7 typ
Total Weight	g	85 max.
TP View Area	mm	257.32mm x 145.18mm
TP Active Area	mm	256.125mm x 144 mm
Interface		I2C
Report Rate	Hz	Follow Google
Multi-Touch Point		10 points
Input method		Finger
Touch panel sensor IC		5012
Channel		52 x 30
Distance between 2 point	mm	Follow Google
Surface hardness	H	7

2.2 Optical Characteristics

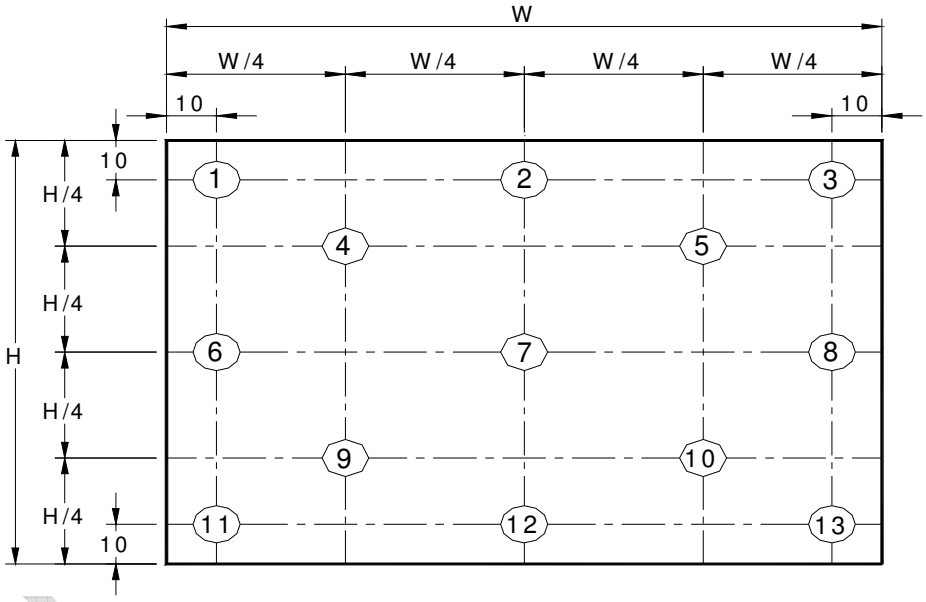
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			5 points average	187	220	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		400	500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	8	16		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.537	0.567	0.597		4
		Ry		0.305	0.335	0.365		
	Green	Gx		0.300	0.330	0.360		
		Gy		0.535	0.565	0.595		
	Blue	Bx		0.125	0.155	0.185		
		By		0.110	0.140	0.170		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	45	-		

Note 1: 5 points' position (Ref: Active area)



Note 2: 13 points' position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

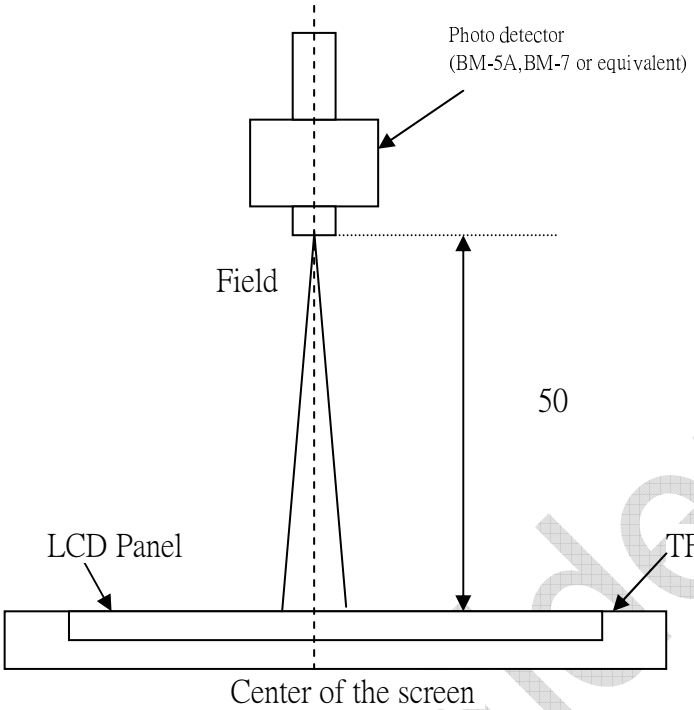
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement

should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5
L (x) is corresponding to the luminance of the point X at Figure in Note (1).

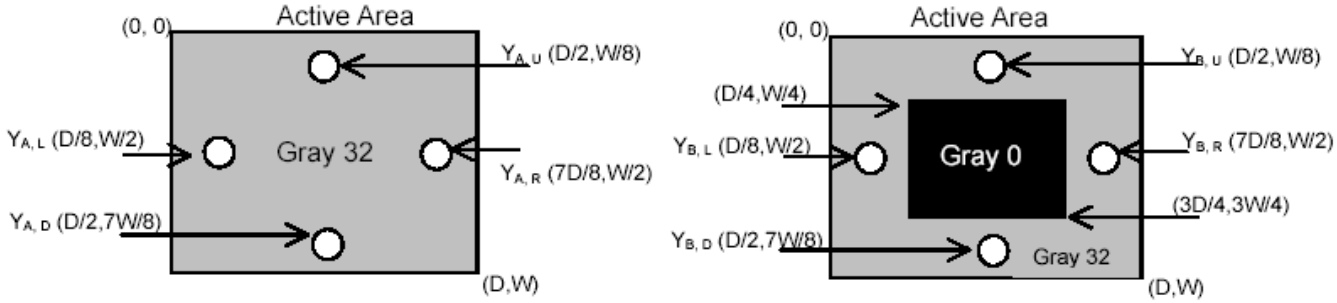
Note 6： Definition of contrast ratio:
Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7： Definition of Cross Talk (CT)
$CT = |Y_B - Y_A| / Y_A \times 100$ (%)

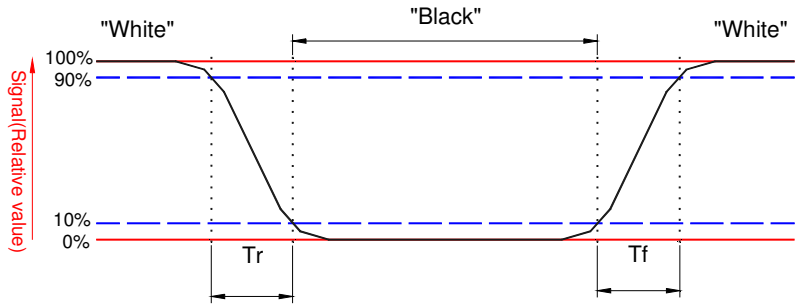
Where
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



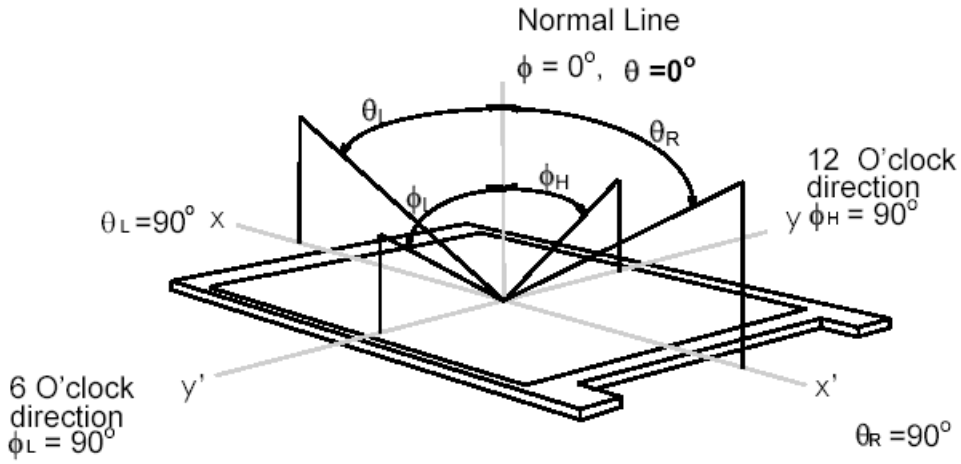
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



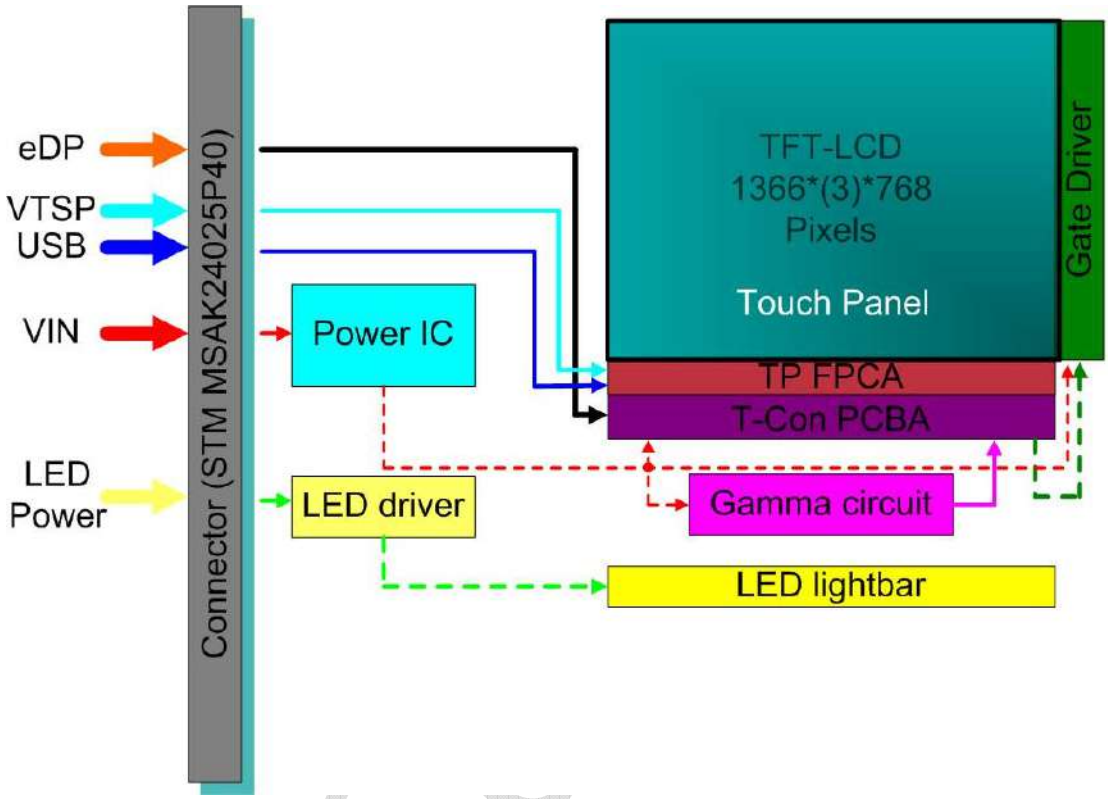
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin (One CH/connector Module)



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

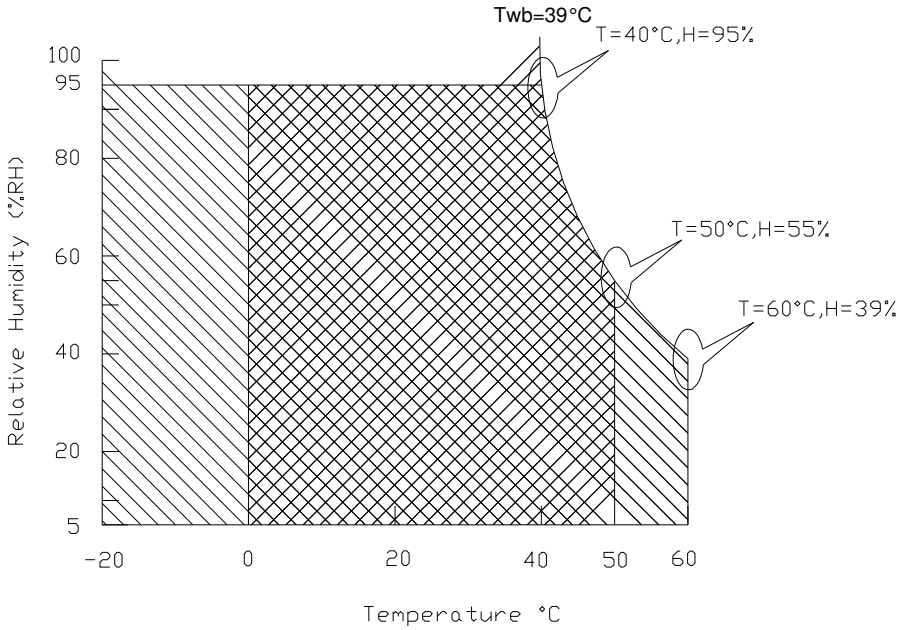
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

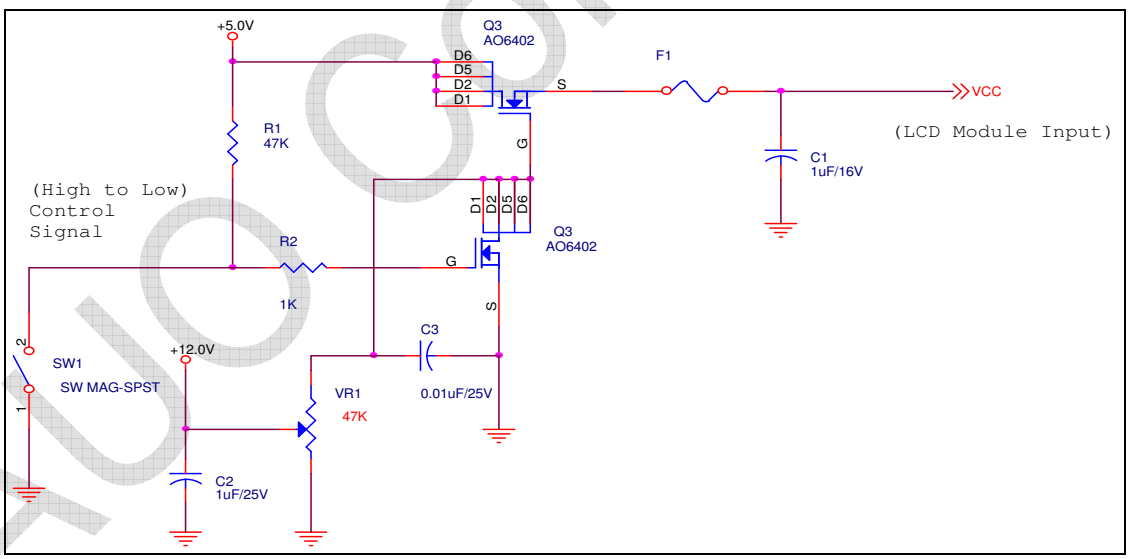
Input power specifications are as follows;

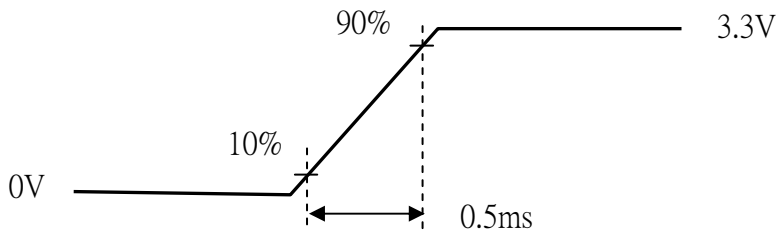
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1	[Watt]	Note 1
IDD	IDD Current	-	-	333	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.0V driving voltage. (Pmax=V3.0 x Iwhite)

Note 2 : Measure Condition





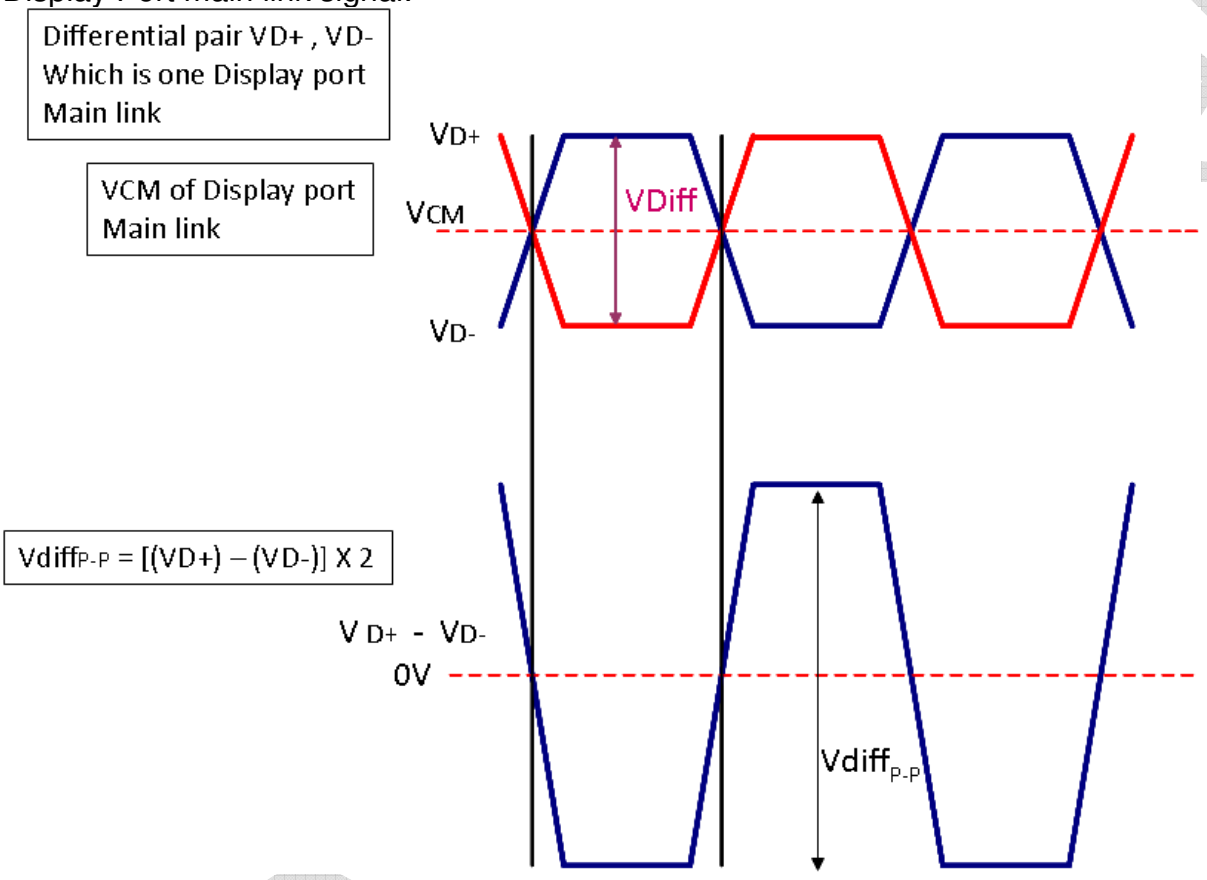
Vin rising

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

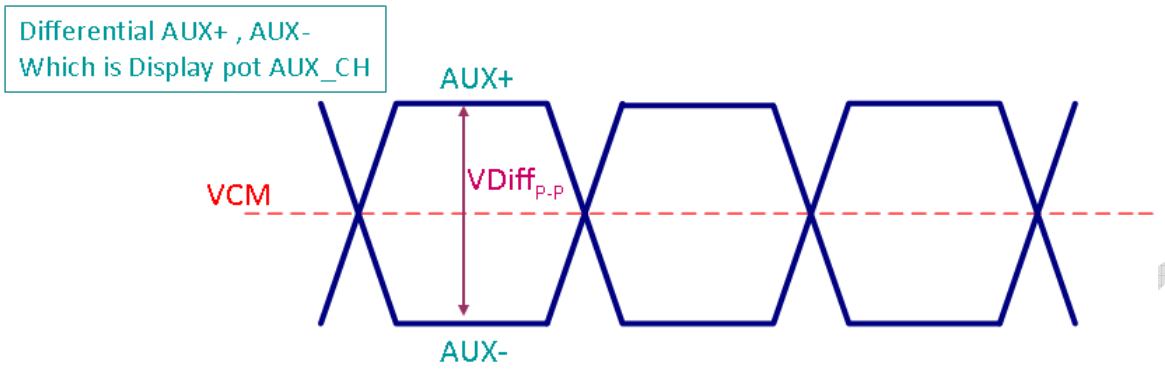
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiffP-P	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a.

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiffP-P	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

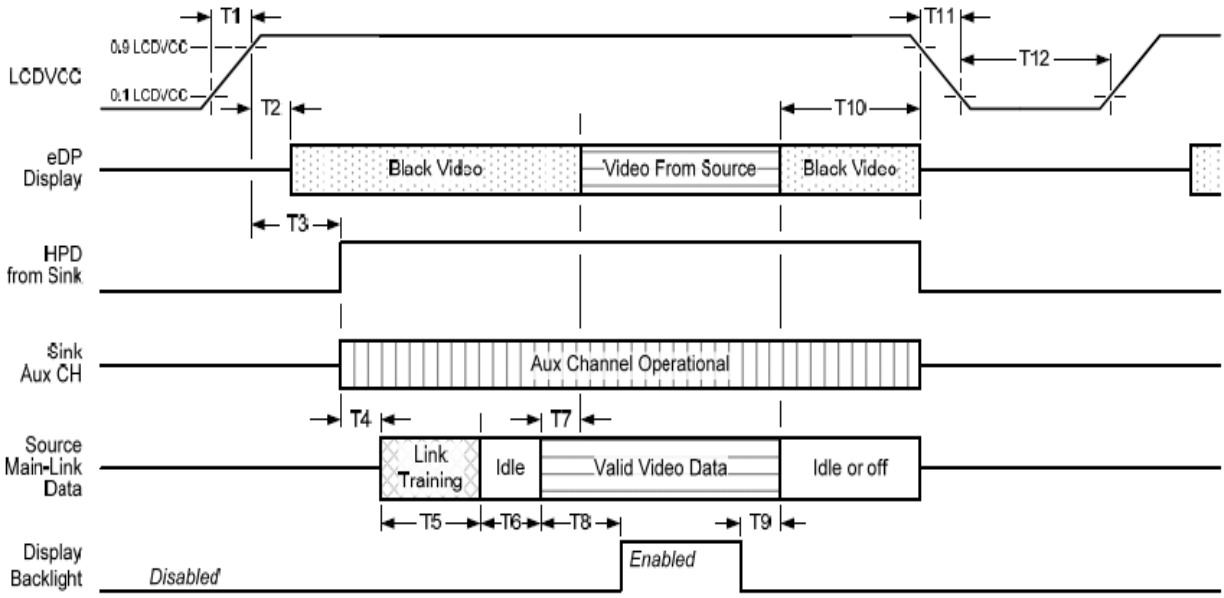
Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

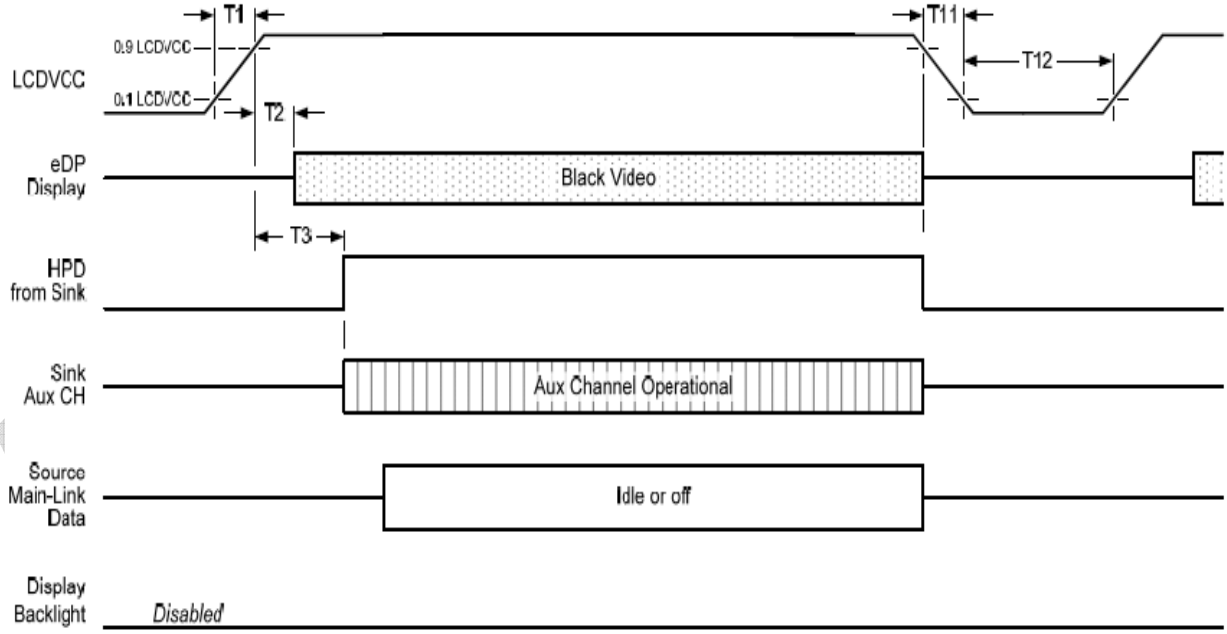
Follow as VESA display port standard V1.1a.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

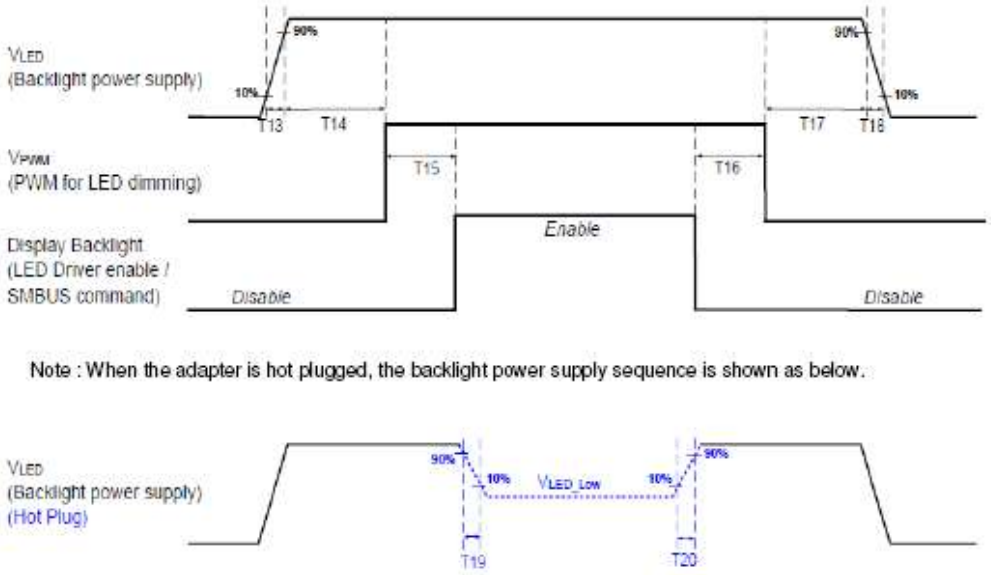
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



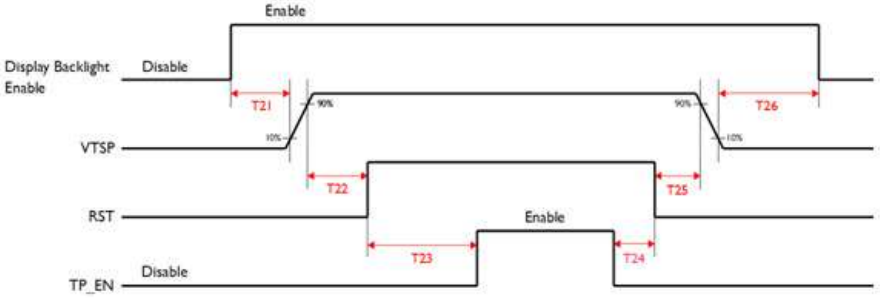
	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	0	-
T16	0	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

Display port TP power sequence timing parameter:



	Min	Max
T21	10ms	-
T22	1ms	-
T23	20ms	-
T24	2ms	-
T25	2ms	-
T26	100ms	-

5.2 Touch Sensor

5.2 Touch Sensor Power Consumption

Items	Symbol	Specifications			Unit	Notes
		Min.	Typ.	Max.		
Touch Panel Power Supply	VDD	4.5	5	5.5	V	
	Active	-	175	357.5	mW	
	Idle	-	60	82.5	mW	
	Sleep		4.25	5.5	mW	

5.3 Backlight Unit

5.3.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.75	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.3.2 Backlight input signal characteristics

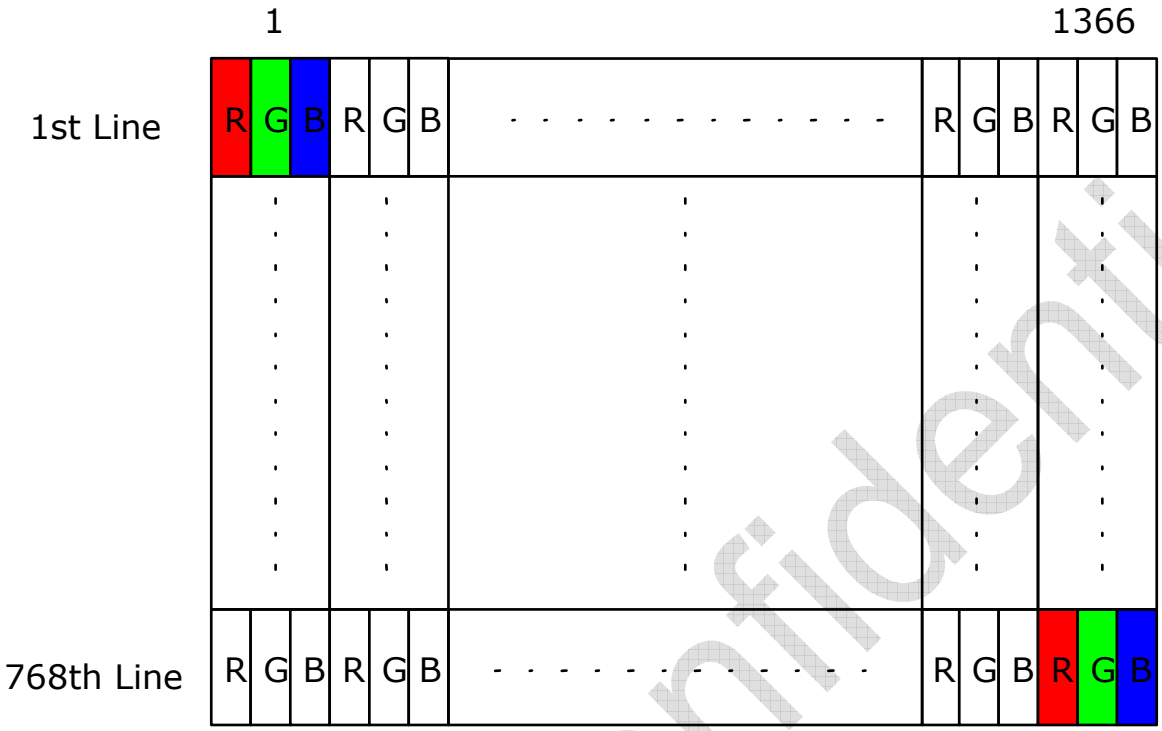
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6	12	21	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommanded system pull up/down resistor no bigger than 10kohm.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatible
Type / Part Number	I-PEX 20455-040E-12R or Compatible
Mating Housing/Part Number	20453-040T-01 or compatible

6.2.2 Pin Assignment

Display Port is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No connect
2	H_GND	High Speed Ground
3	NC	No connect
4	NC	No connect
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	No connect
25	NC	No connect

26	NC	No connect
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connect
31	NC Reserved	Reserved for USB Device port data (-)
32	NC Reserved	Reserved for USB Device port data (+)
33	GND	Ground–Shield
34	VTSP	5V power for touch
35	VTSP	5V power for touch
36	NC	No connect
37	SCL	I2C Clock for Touch
38	SDA	I2C Data for Touch
39	INT	Interrupt for Touch
40	Reset	Reset for Touch

Note1：start from right side
Note2：Input signals shall be low or High-impedance state when VDD is off.

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		$1/T_{Clock}$	66.9	72	80	MHz
Vertical Section	Period	T_V	788	824	768+A	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	20	56	A	
Horizontal Section	Period	T_H	1416	1456	1366+B	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	50	90	B	

Note 1 : The above is as optimized setting

Note 2 : DE mode only

Note 3 : The maximum clock frequency = (1366+B)*(768+A)*60<80MHz

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	**Ta= 40℃, 90%RH, 300h**	
High Temperature Operation	**Ta= 50℃, Dry, 300h**	
Low Temperature Operation	**Ta= 0℃, 300h**	
High Temperature Storage	**Ta= 60℃, 35%RH, 300h**	
Low Temperature Storage	**Ta= -20℃, 50%RH, 250h**	
Thermal Shock Test	**Ta=-20℃to 60℃, Duration at 30 min, 100 cycles**	
ESD	**Contact : ±8 KV** **Air : ±15 KV**	Note 1

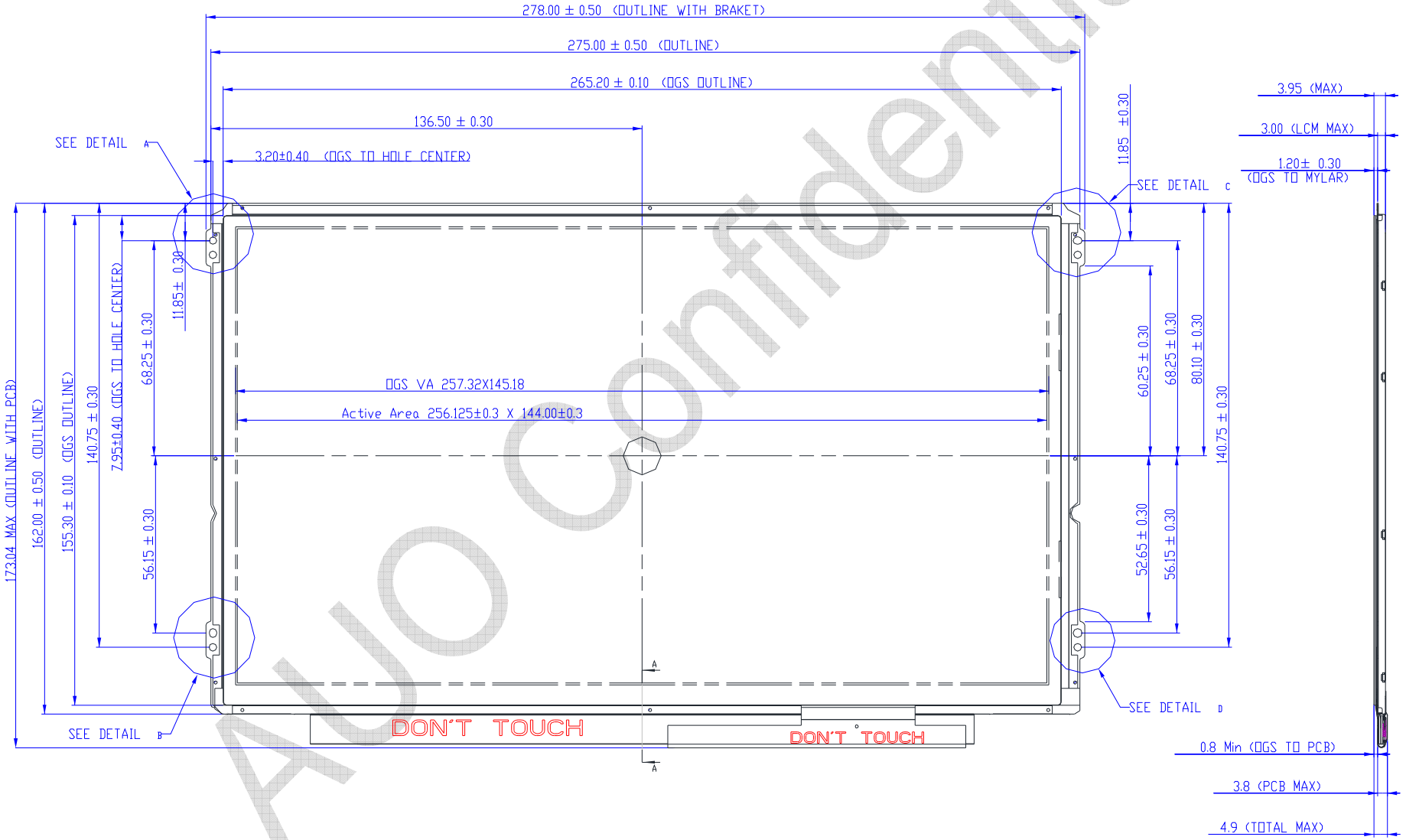
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

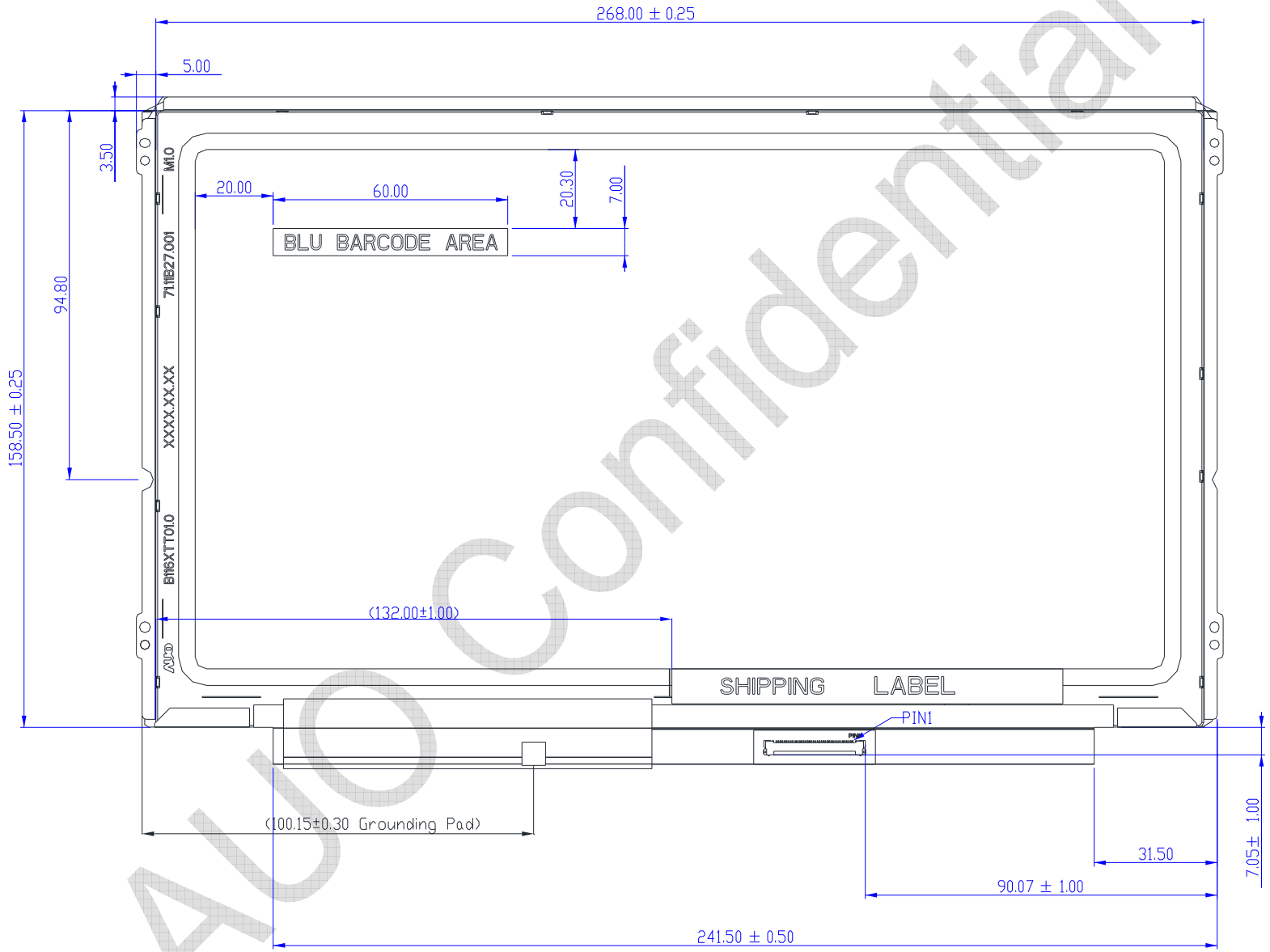
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Rear View



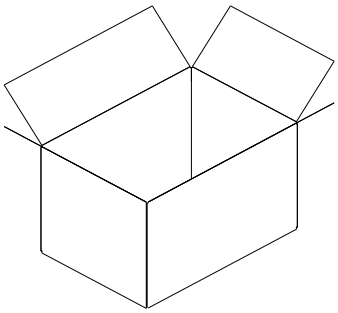
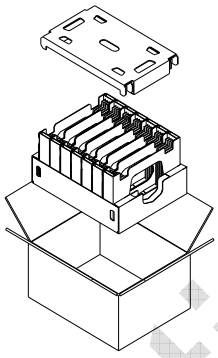
9. Shipping and Package

9.1 Shipping Label Format

9.1 Carton Label Format

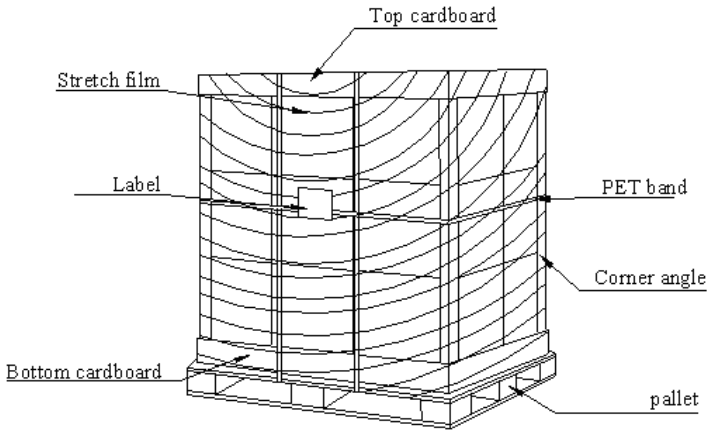
9.2 Carton Package

The outside dimension of carton is 460 (L)mm x 375 (W)mm x 268 (H)mm

	
Carton P/N：	Cushion P/N：

- Pallet : **1140**mm*__890__mm*__138__mm
- Stretch film : **500**mm (W)*__300__M (L)

9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
0		00	00000000	0
1		FF	11111111	255
2		FF	11111111	255
3		FF	11111111	255
4		FF	11111111	255
5		FF	11111111	255
6		FF	11111111	255
7	EISA Manuf. Code LSB	00	00000000	0
8	Compressed ASCII	06	00000110	6
9	Product Code	AF	10101111	175
0A	hex, LSB first	5C	01011100	92
0B	32-bit ser #	10	00010000	16
0C		00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F	Week of manufacture	00	00000000	0
10	Year of manufacture	0E	00001110	14
11	EDID Structure Ver.	19	00011001	25
12	EDID revision #	01	00000001	1
13	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	04	00000100	4
14	**Max H image size** *(rounded to cm)*	95	10010101	149
15	**Max V image size** *(rounded to cm)*	1A	00011010	26
16	**Display Gamma** *(=(gamma*100)-100)*	0E	00001110	14
17	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	78	01111000	120
18	Red/green low bits **(Lower 2:2:2:2 bits)**	02	00000010	2
19	Blue/white low bits **(Lower 2:2:2:2 bits)**	6B	01101011	107
1A	Red x **(Upper 8 bits)**	F5	11110101	245
1B	Red y/ highER 8 bits	91	10010001	145
1C	Green x	55	01010101	85
1D	Green y	54	01010100	84
1E	Blue x	91	10010001	145
1F	Blue y	27	00100111	39
20	White x	22	00100010	34
21	White y	50	01010000	80
22	Established timing 1	54	01010100	84
23	Established timing 2	00	00000000	0
24	Established timing 3	00	00000000	0
25	Standard timing #1	00	00000000	0
26		01	00000001	1
27	Standard timing #2	01	00000001	1
28		01	00000001	1
29	Standard timing #3	01	00000001	1
2A		01	00000001	1

2B	Standard timing #4	01	00000001	1
2C		01	00000001	1
2D	Standard timing #5	01	00000001	1
2E		01	00000001	1
2F	Standard timing #6	01	00000001	1
30		01	00000001	1
31	Standard timing #7	01	00000001	1
32		01	00000001	1
33	Standard timing #8	01	00000001	1
34		01	00000001	1
35	Pixel Clock/10000 LSB	01	00000001	1
36	Pixel Clock/10000 USB	A2	10100010	162
37	Horz active **Lower 8bits**	1C	00011100	28
38	Horz blanking **Lower 8bits**	56	01010110	86
39	HorzAct:HorzBlnk **Upper 4:4 bits**	A0	10100000	160
3A	Vertical Active **Lower 8bits**	50	01010000	80
3B	Vertical Blanking **Lower 8bits**	00	00000000	0
3C	Vert Act : Vertical Blanking **(upper 4:4 bit)**	20	00100000	32
3D	HorzSync. Offset	30	00110000	48
3E	HorzSync.Width	28	00101000	40
3F	VertSync.Offset : VertSync.Width	20	00100000	32
40	Horz&Vert Sync Offset/Width **Upper 2bits**	36	00110110	54
41	Horizontal Image Size **Lower 8bits**	00	00000000	0
42	Vertical Image Size **Lower 8bits**	00	00000000	0
43	Horizontal & Vertical Image Size **(upper 4:4 bits)**	90	10010000	144
44	Horizontal Border *(zero for internal LCD)*	10	00010000	16
45	Vertical Border *(zero for internal LCD)*	00	00000000	0
46	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	00	00000000	0
47	Detailed timing/monitor	1A	00011010	26
48	descriptor #2	A2	10100010	162
49		1C	00011100	28
4A		56	01010110	86
4B		1E	00011110	30
4C		52	01010010	82
4D		00	00000000	0
4E		20	00100000	32
4F		30	00110000	48
50		28	00101000	40
51		20	00100000	32
52		36	00110110	54
53		00	00000000	0
54		00	00000000	0
55		90	10010000	144
56		10	00010000	16
57		00	00000000	0
58		00	00000000	0
59	Detailed timing/monitor	1A	00011010	26

5A	descriptor #3	00	00000000	0
5B		00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E	Manufacture	00	00000000	0
5F	Manufacture	30	00110000	48
60	Manufacture	32	00110010	50
61		58	01011000	88
62		33	00110011	51
63		54	01010100	84
64		80	10000000	128
65		42	01000010	66
66		31	00110001	49
67		31	00110001	49
68		36	00110110	54
69		58	01011000	88
6A		54	01010100	84
6B	Detailed timing/monitor	54	01010100	84
6C	descriptor #4	00	00000000	0
6D		00	00000000	0
6E		00	00000000	0
6F		00	00000000	0
70	Manufacture P/N	00	00000000	0
71	Manufacture P/N	00	00000000	0
72	Manufacture P/N	41	01000001	65
73	Manufacture P/N	22	00100010	34
74	Manufacture P/N	96	10010110	150
75	Manufacture P/N	01	00000001	1
76	Manufacture P/N	11	00010001	17
77	Manufacture P/N	00	00000000	0
78	Manufacture P/N	00	00000000	0
79	Manufacture P/N	0A	00001010	10
7A	Manufacture P/N	01	00000001	1
7B		0A	00001010	10
7C		20	00100000	32
7D	Extension Flag	20	00100000	32
7E	Checksum	00	00000000	0
7F		C9	11001001	201