( ) Preliminary Specifications
(V) Final Specifications

Module	**13.3”(13.26”) FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B133HAB01.0 (HW:0A)**
Note ( )	***oTP Display***

Customer **Date**	**Approved by** **Date**
	Wen Hwa 2016/6/20
Checked & Approved by **Date**	**Prepared by** **Date**
	Tommy Chang 2016/8/12
Note: This Specification is subject to change without notice.	**AU Optronics corporation**

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2015/09/04	All	First Edition for Customer		
0.2 2015/09/18	7	Surface hardness 5H	Surface hardness 7H	
0.3 2015/09/21	21	**Table:6.2.1Connector Description** Is TBD	Modify	
0.4 2015/10/22	29~30		Add Drawing	
0.5 2016/08/12	31~35		Update EDID & Shipping Label	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B133HAB01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x1080(V) screen and 262K colors (RGB –6bits with FRC)with LED backlight driving circuit. All input signals are eDP (Embedded DisplayPort) interface compatible.

B133HAB01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	336.71			
Active Area	[mm]	293.472x165.078			
Pixels H x V		1920x3(RGB) x 1080			
Pixel Pitch	[mm]	0.1529 x 0.1529			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=24mA) (Note: ILED is LED current)	[cd/m^2]	220 typ. (5 points average) 187 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.7 max (Include Logic and Blu power)			
Weight	[Grams]	400 g max (Total Solution)[1]			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	304.85	305.35	305.85
		Width	193.21	193.71	194.21

[1] Total solution max weight includes touch sensor FPCA and OGS.

		Thickness	-	-	3.0 (Panel Side) 3.2 (PCBA Side)
Total solution [Note: OGS Touch module]	[mm]		Min.	Typ.	Max.
		Length	316.85	317	317.15
		Width	207.85	208	208.15
		Thickness	-	-	4.0 (Panel Side) 4.2 (PCBA Side) 4.2 (Total)
Electrical Interface		2 Lane eDP 1.2			
Glass Thickness	[mm]	0.4			
Surface Treatment		AS			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 General Touch Specification

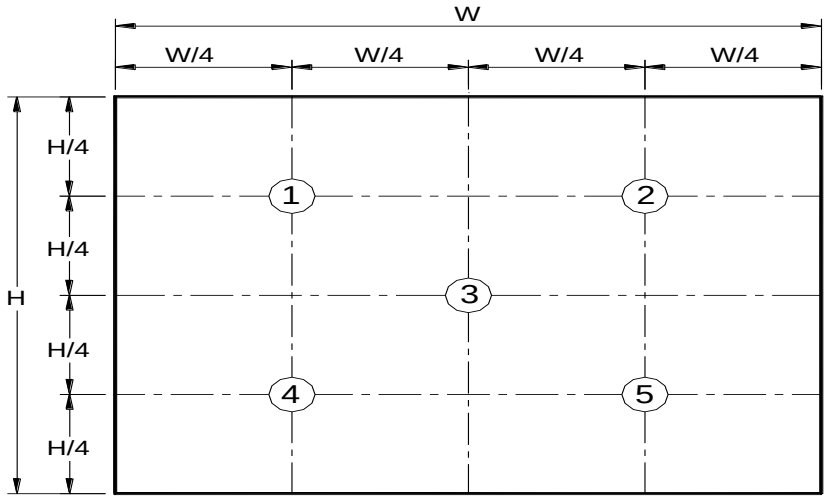
Item	Spec	Unit
Type of Touch Sensor	Projective Capacitive (On cell)	
Panel Size	13.3”	
Outline Dimension	317 X 208 typ	mm
Total Thickness	0.7 typ(Coverlens)	mm
Total Weight	400 max(Including LCM)	g
TP View Area	294.42 X 165.97 typ	mm
TP Active Area	295.872 X 167.478 typ	mm
Interface	USB	
Report Rate	Follow win10 – ≧100Hz	Hz
Multi-Touch Point	10 points	
Input method	Finger	
Touch panel sensor IC	Raydium (RM32380)	
Channel	70 x 40	
Distance between 2 point	Follow win10	mm
Surface hardness	7 (Note 1)	H
Surface treatment	AS	
TP F/W version	TBD (Version : 00)	
Support OS	Window 10	
BM ink	聯致 SBK 630A	
TP Power Consumption	0.3(Active Mode)	mW

2.3 Optical Characteristics

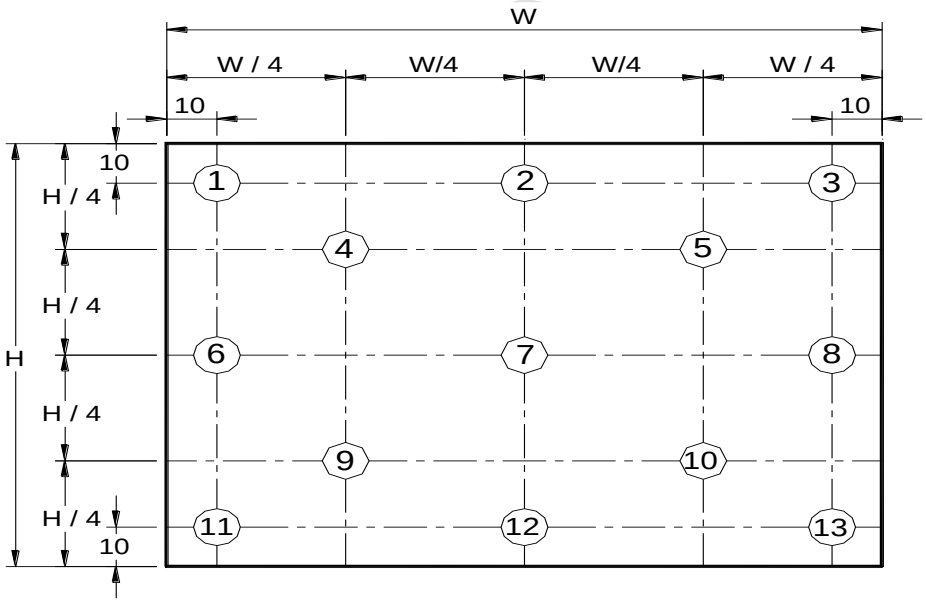
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=24mA (Base Panel Only)			5 points average	187	220	-	cd/m2	1, 4, 5.
Viewing Angle		θR θL	Horizontal (Right) CR = 10 (Left)	80 80	85 85	- -	degree	4, 9
		ψH ψL	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	- -		
Luminance Uniformity		δ5P	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ13P	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR		700	800	-		4, 6
Cross talk		%				4		4, 7
Response Time		TRT	Rising + Falling	-	25	35		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.541	0.571	0.601	-	4
		Ry		0.315	0.345	0.375	-	
	Green	Gx		0.316	0.346	0.376	-	
		Gy		0.541	0.571	0.601	-	
	Blue	Bx		0.128	0.158	0.188	-	
		By		0.086	0.116	0.146	-	
	White	Wx		0.283	0.313	0.343	-	
		Wy		0.299	0.329	0.359	-	
NTSC		%		-	45	-	-	

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

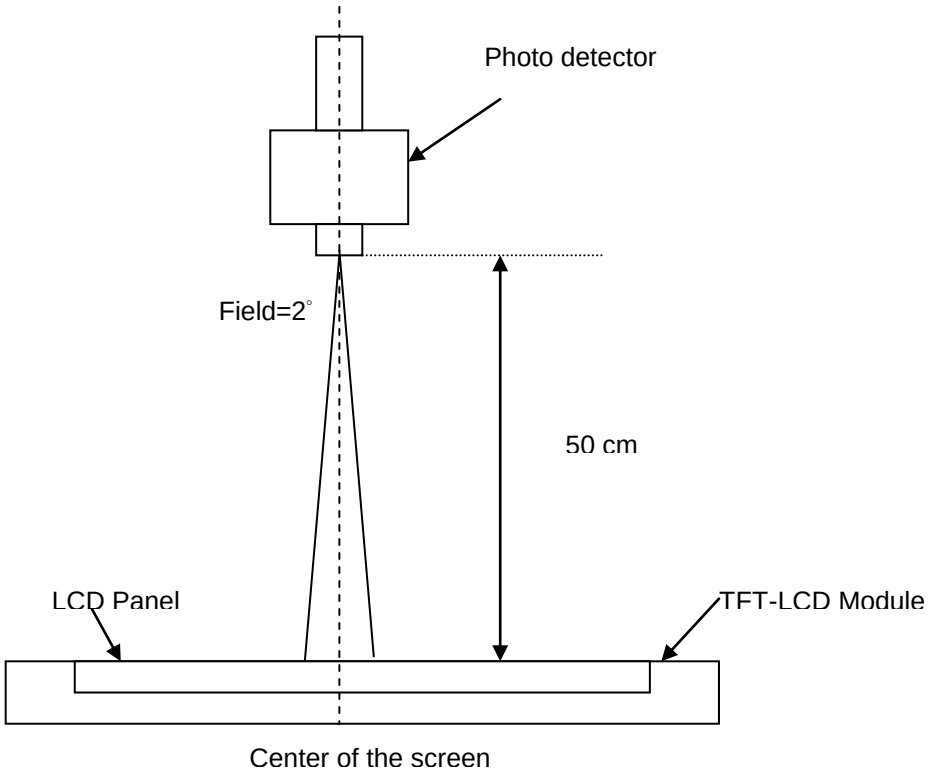
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

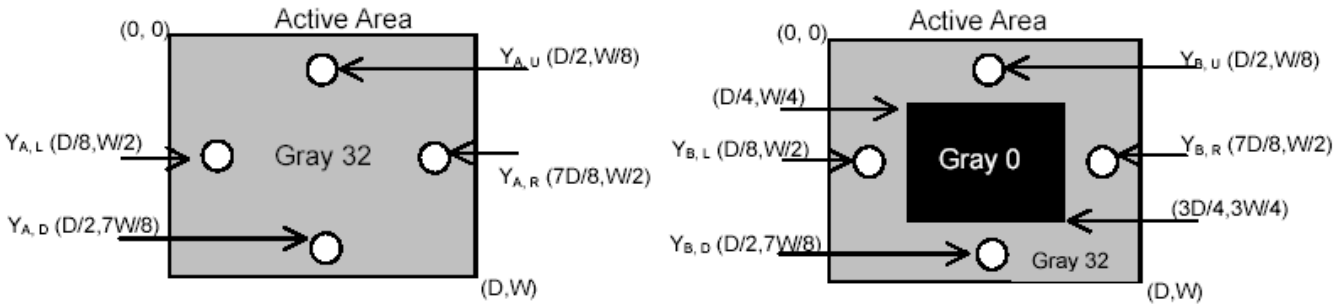
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

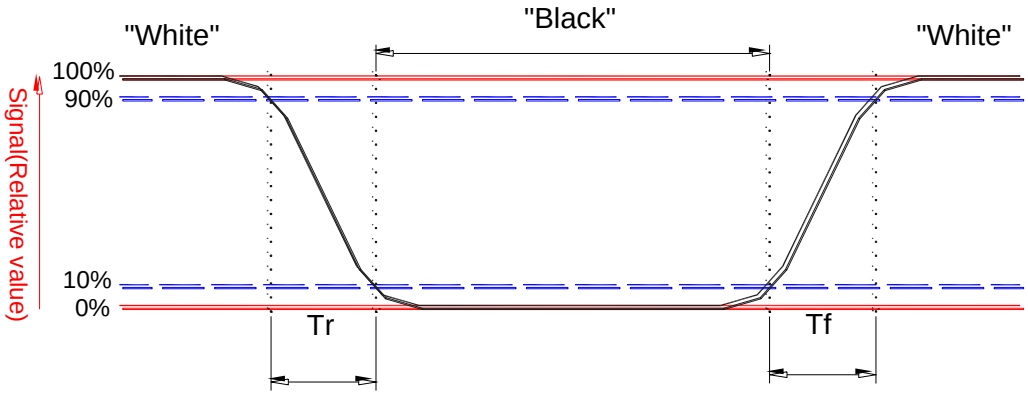
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



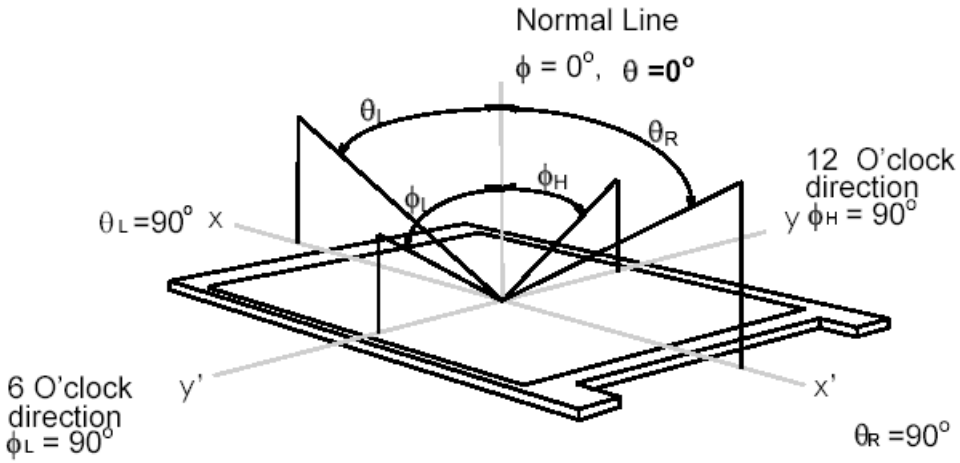
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.

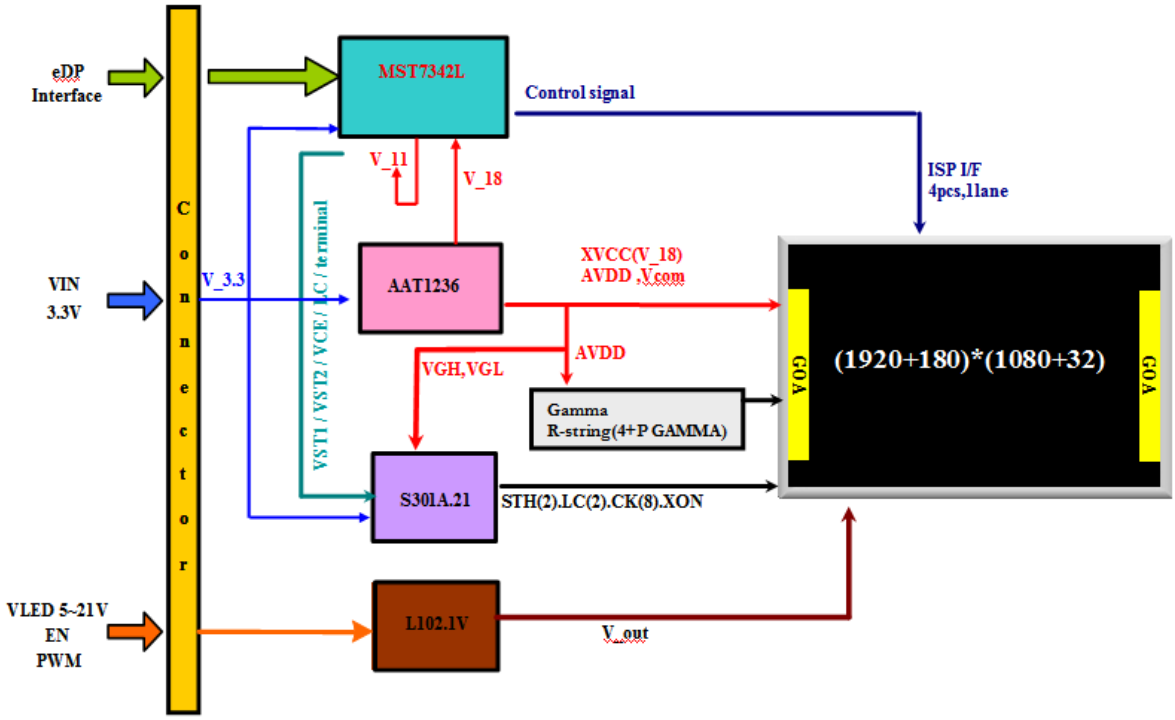


Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	4	[Volt]	Note 1,2

4.2 Absolute Ratings of Touch Sensor Module

Item	Symbol	Min	Max	Unit	Conditions
Touch Sensor Module Power Voltage	VTSP	-0.3	7	[Volt]	
Touch Sensor Module Reset Signal	RST	-0.3	3.6	[Volt]	
Touch Sensor Module enable Signal	TP_EN	-0.3	3.6	[Volt]	

4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

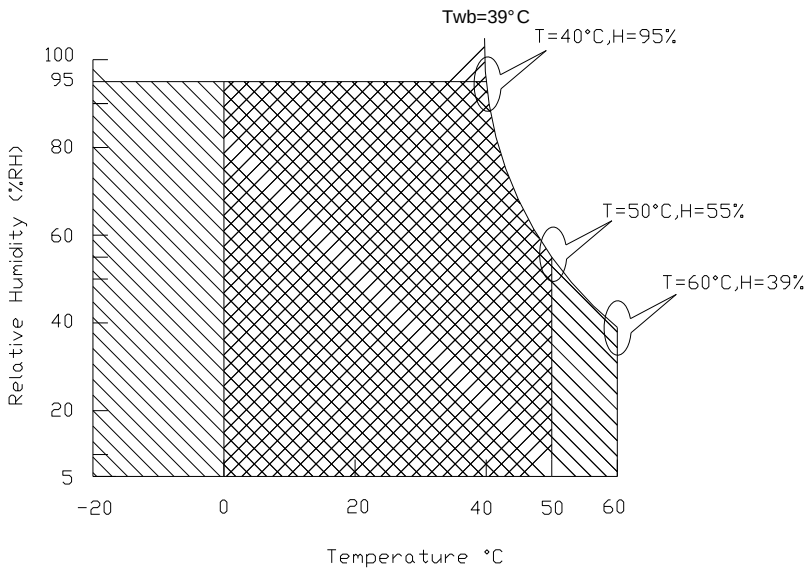
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal , for example)



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

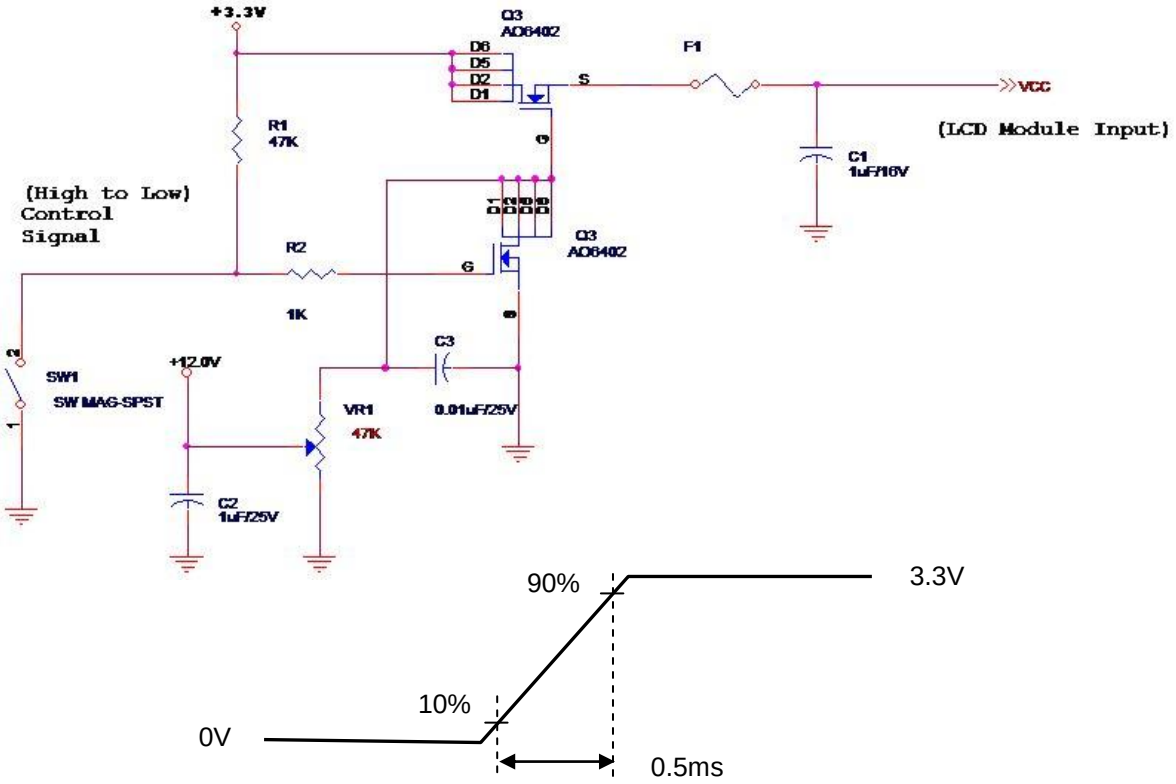
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.0	[Watt]	Note 1
IDD	IDD Current	-	-	334	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Mosaic pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2：Measure Condition

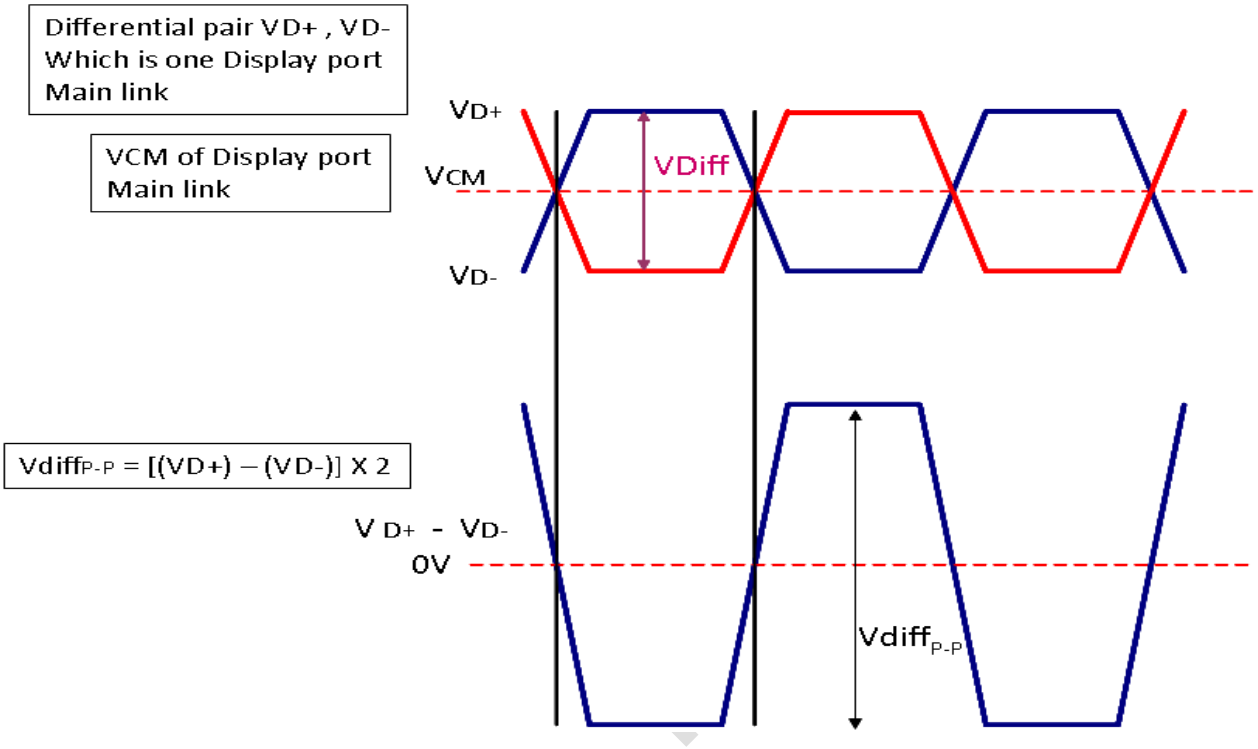


Vin rising time

5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

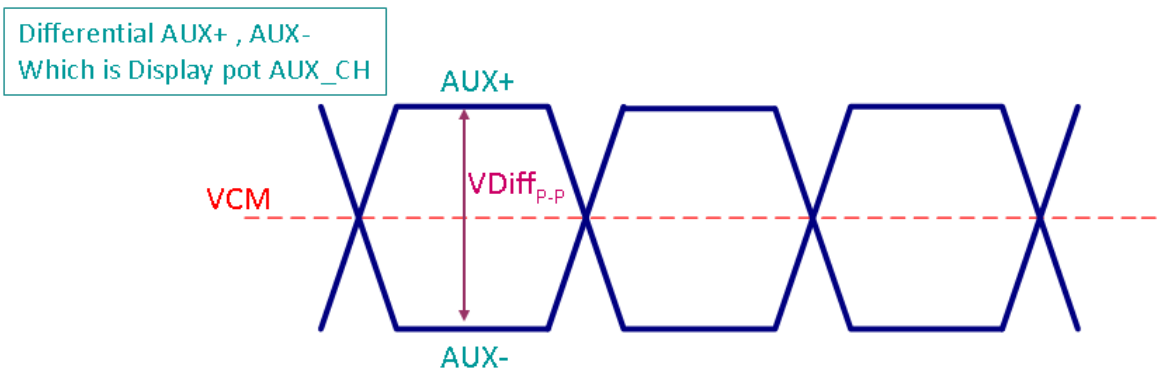
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Follow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.1a.

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	2.25	-	3.6	V

Follow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.15	[Watt]	**(Ta=25℃), Note 1**
LED Life-Time	N/A	15,000	-	-	Hour	**(Ta=25℃), Note 2** **I_F=24 mA**

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	5.0 (Note 2)	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.6	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.6	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1 (Note 3)	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

Note 2 : measured in panel VIN

Note 3 : If the PWM duty ratio(min) is set between 5% to 1%，the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

5.3 Touch Sensor Module

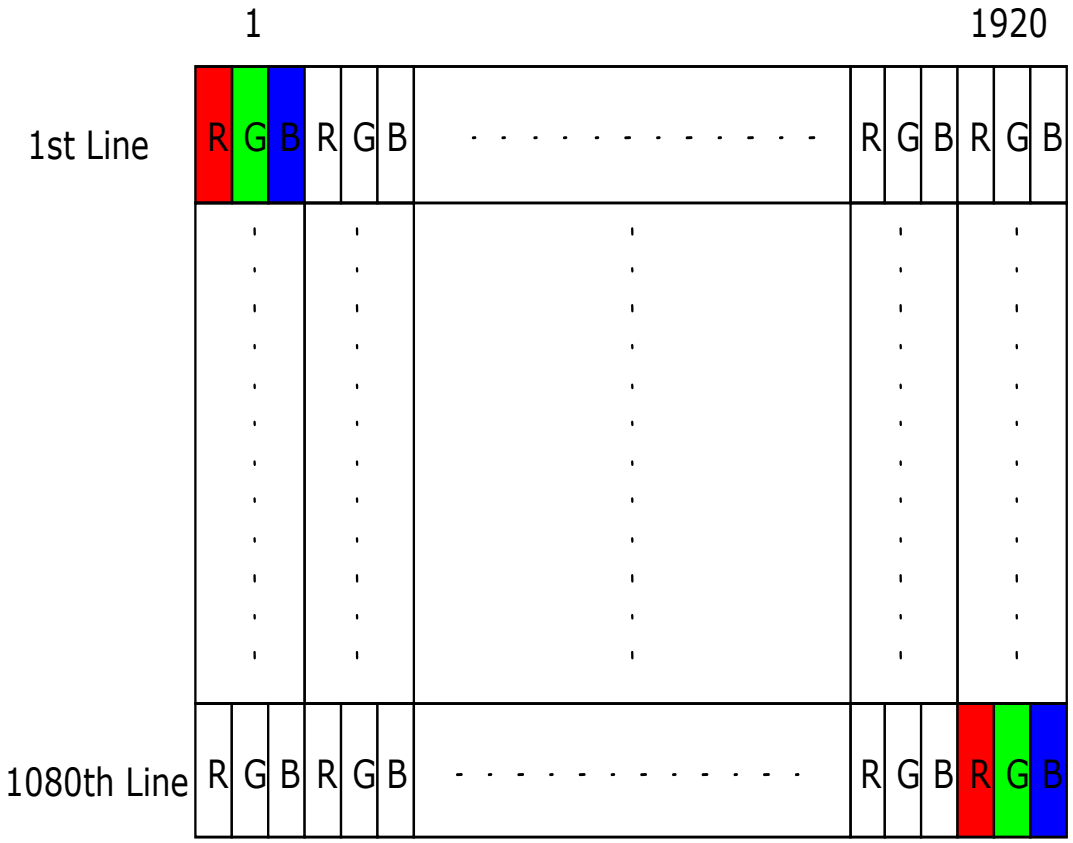
5.3.1 Power Specification

Items	Symbol		Specifications			Unit	Notes
			Min.	Typ.	Max.		
Touch sensor module Power Supply	VTSP		4.5	5	5.5	V	
Touch Sensor Module Power ripple	VTSPrp		-	-	100	mV	
Input Voltage	RST, TP_EN	VIH	2.64		3.3	V	
		VIL	0		0.66	V	
Touch sensor module Power Comsumption	P_{VTSP}				0.3	W	Active mode

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

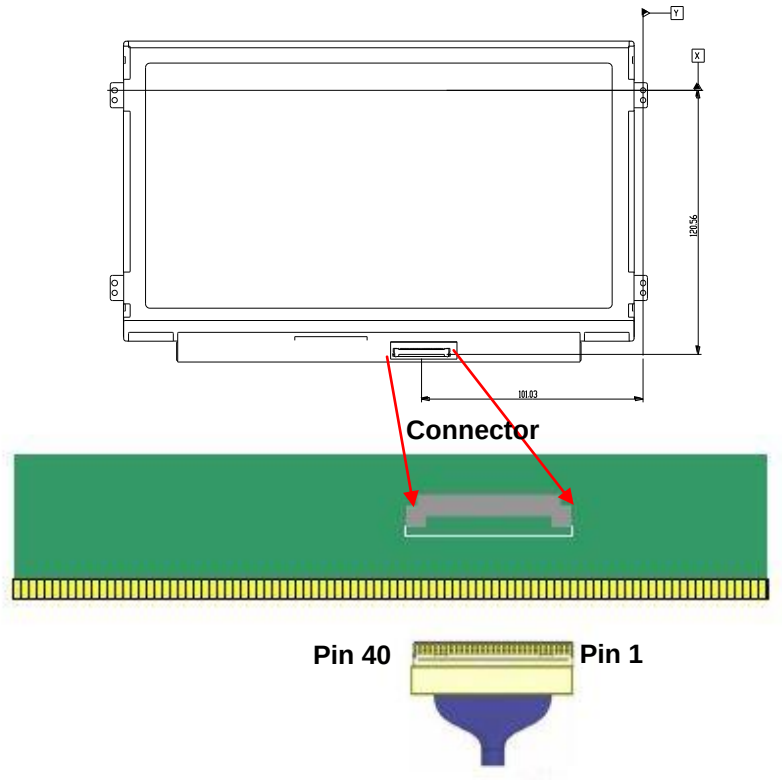
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	I-PEX 20455-040E-76B or Compatible
Mating Housing/Part Number	IPX or compatible

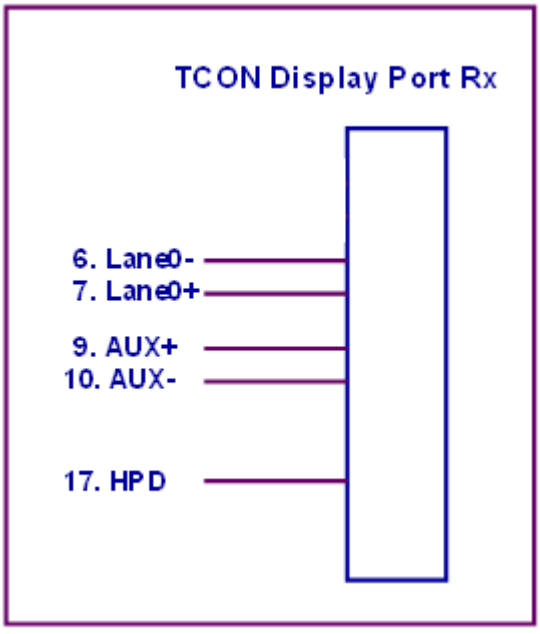
6.2.2 Pin Assignment (with Touch Sensor Pin Assignment)

Pin	Symbol	Description
1	DCR	DCR Function
2	GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	GND	High Speed Ground
12	VCC	LCD logic and driver power
13	VCC	LCD logic and driver power
14	LCD Self Test or NC	LCD Panel Self Test Enable (Optional)
15	GND	LCD logic and driver ground
16	GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	LED Backlight ground
19	BL_GND	LED Backlight ground
20	BL_GND	LED Backlight ground
21	BL_GND	LED Backlight ground
22	BL ENABLE	LED Backlight control on/off control
23	BL PWM	System PWM signal input for dimming
24	H_Sync	H_ sync function
25	NC Reserved	Reserved for LCD manufacture's use
26	VLED	LED Backlight power (12V Typical)

27	VLED	LED Backlight power (12V Typical)
28	VLED	LED Backlight power (12V Typical)
29	VLED	LED Backlight power (12V Typical)
30	NC Reserved	Reserved for LCD manufacture's use
31	**DM (USB-)**	**Touch panel USB D-**
32	**DP (USB+)**	**Touch panel USB D+**
33	**GND**	**GND**
34	**Touch Power line**	**Touch Panel Power line 5V**
35	**Touch Power line**	**Touch Panel Power line 5V**
36	**Touch_EN(Report Switch)**	**Touch_EN(Report Switch)**
37	**TP I2C-SCK**	**Touch panel I2C-SCK**
38	**TP I2C-SDA**	**Touch panel I2C-SDA**
39	**TP I2C-INT**	**Touch panel I2C-INT**
40	**TP_RST**	**Touch paenl IC reset, Low active**



Note1: Start from right side.
Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

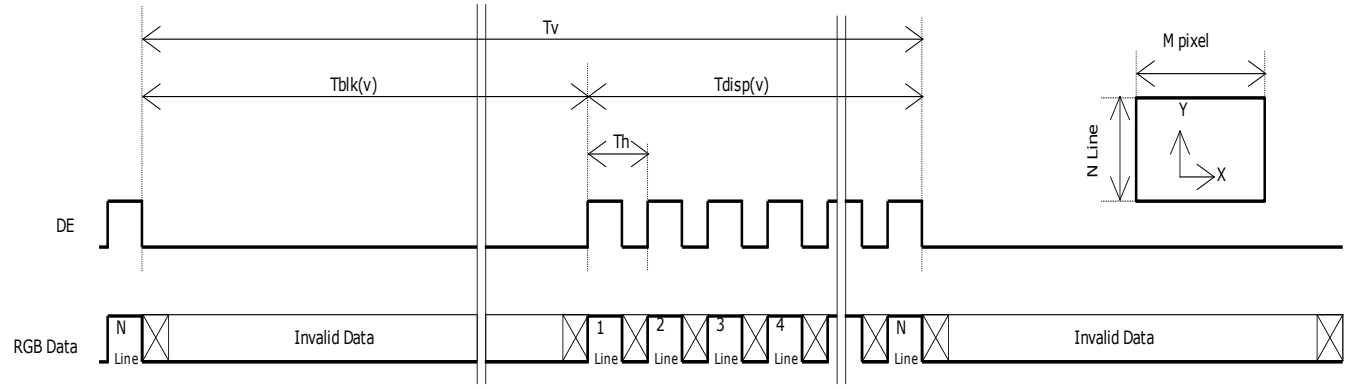
Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

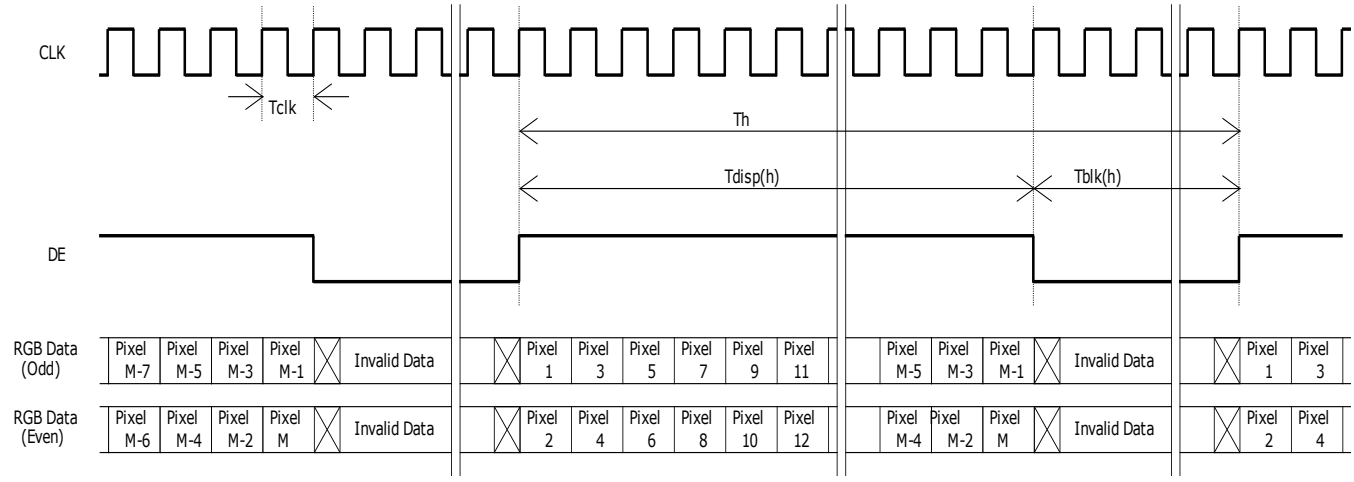
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T_{Clock}	69.4	70.5	74.55	MHz
Vertical Section	Period	T_V	1112	1116	1080+A	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	32	36	A	
Horizontal Section	Period	T_H	1040	1052	960+B	T_{Clock}
	Active	T_{HD}	960			
	Blanking	T_{HB}	80	92	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = (960+B)*2*(1080+A)*60 < 149.1 MHz

6.3.2 Timing diagram

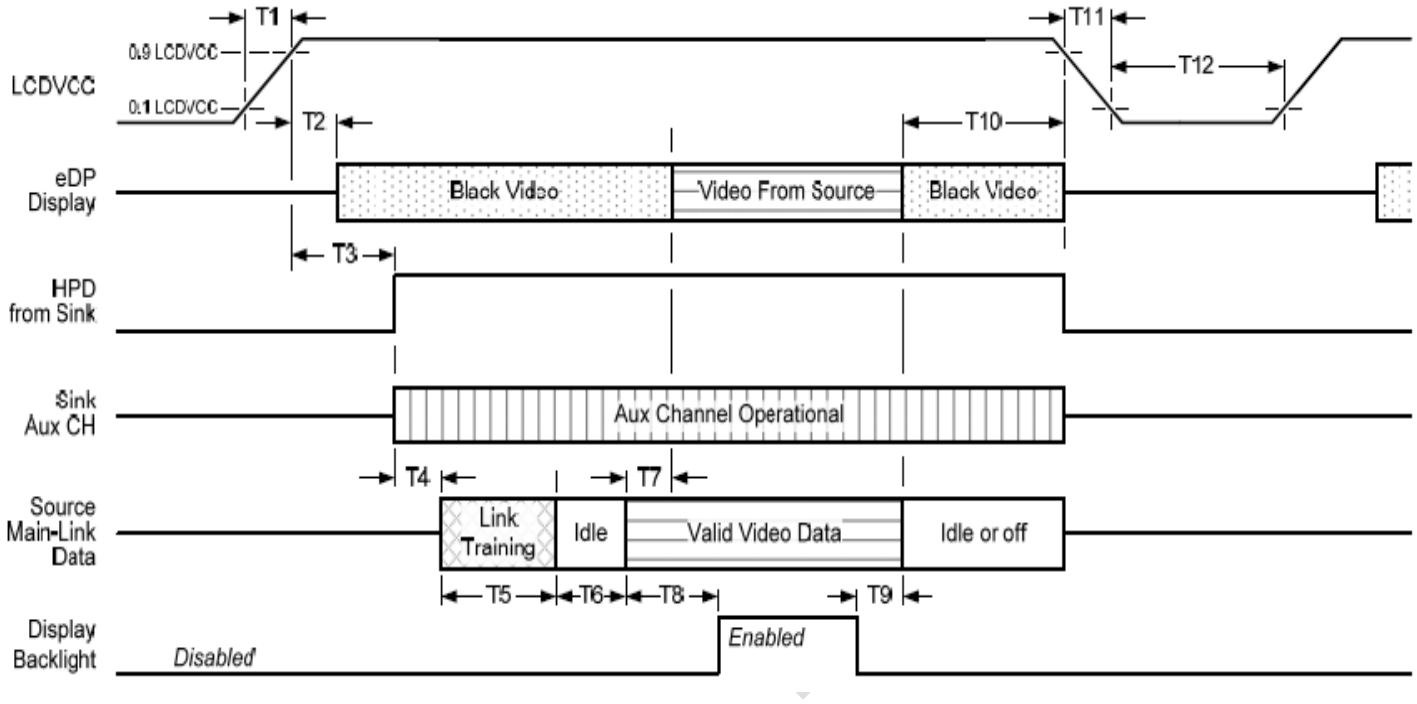




6.4 Power ON/OFF Sequence

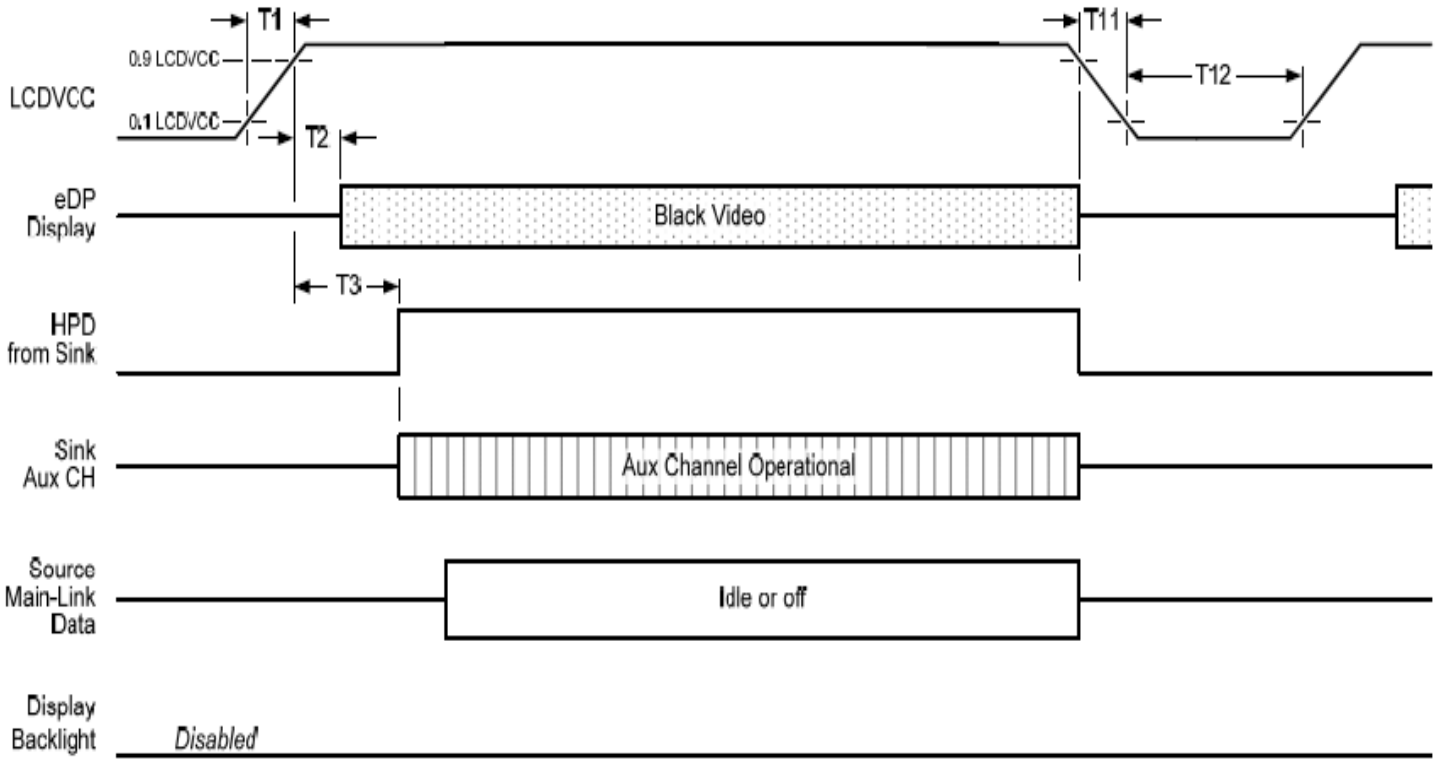
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

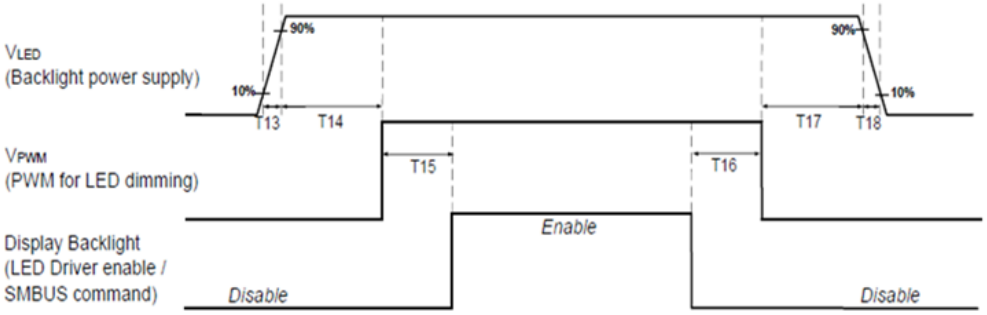
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

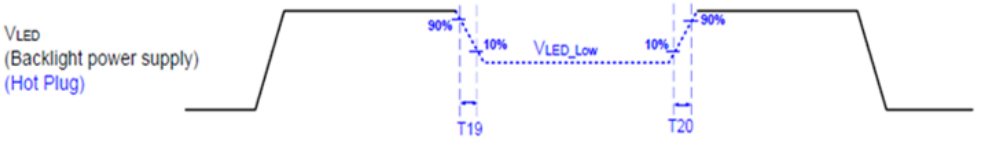


	Min (ms)	Max (ms)
T13	0.2	10
T14	0	-
T15	0	-
T16	0	-
T17	0	-
T18	0.2	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

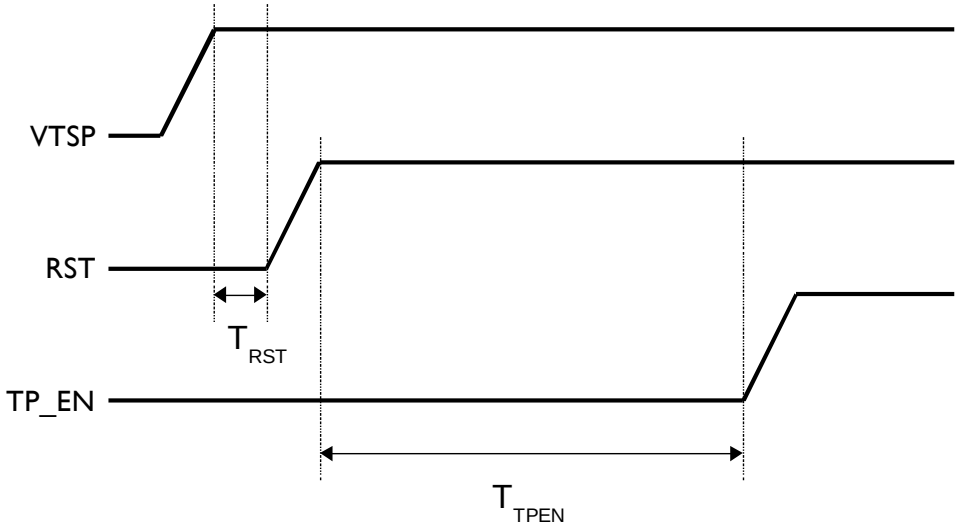
Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Note 1 : If T14,T15,T16,T17<10ms，The display garbage may occur. We suggest T14,T15,T16,T17>10ms to avoid the display garbage.

Note 2：If T13 or T18<0.5ms，the inrush current may cause the damage of fuse. If T13 or T18<0.5ms，the inrush current I^2t is under typical melt of fuse Spec.，there is no mentioned problem.

Touch Panel Power on Sequence



Timing	Description	Min (ms)
T_{RST}	Reset signal delay time from VTSP (TP power)	1
T_{TPEN}	TP enable signal delay time from reset signal	20

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

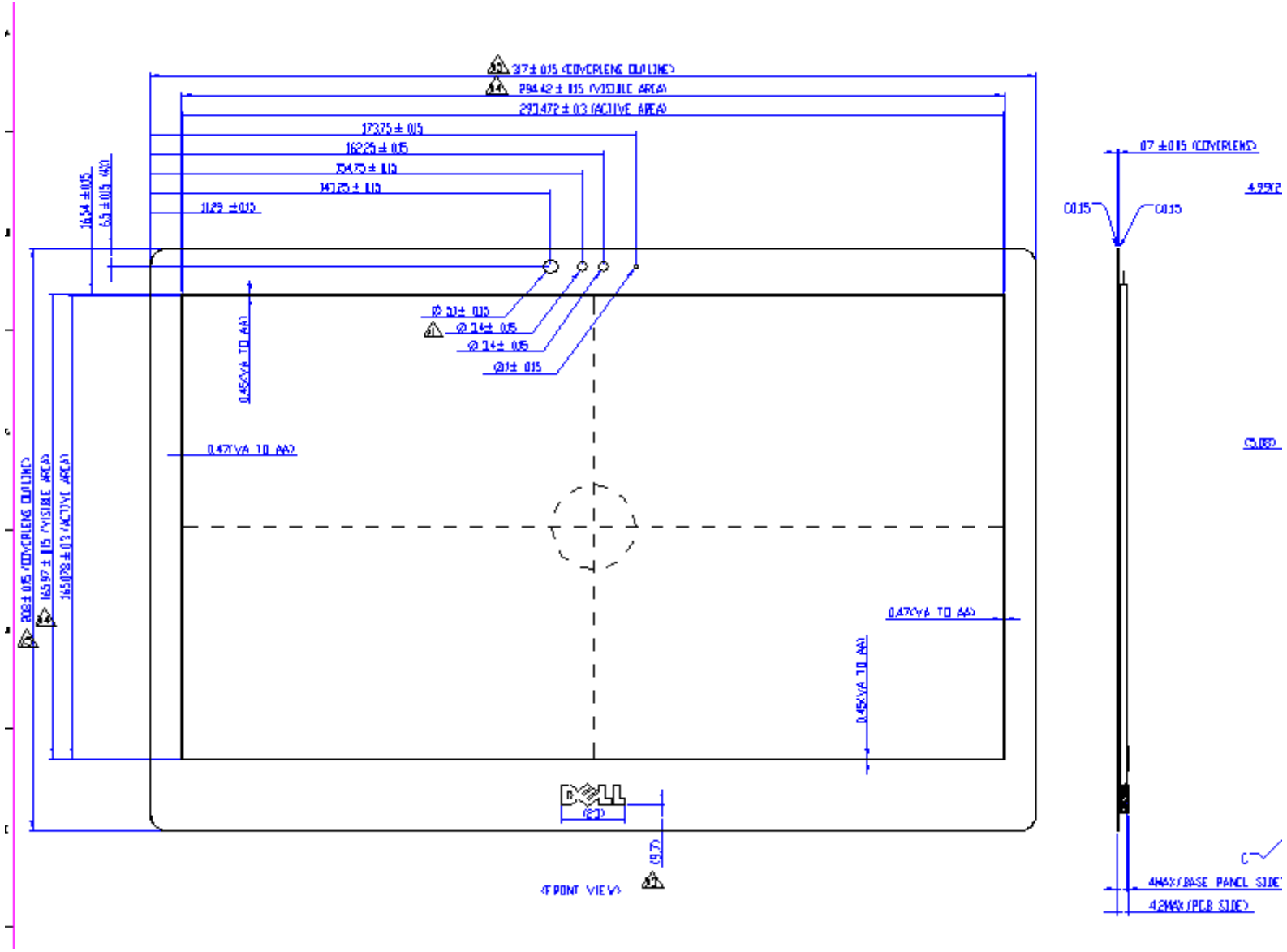
Items	Required Condition	Note
Temperature Humidity Bias	**Ta= 40℃, 90%RH, 300h**	
High Temperature Operation	**Ta= 50℃, Dry, 300h**	
Low Temperature Operation	**Ta=0℃, 300h**	
High Temperature Storage	**Ta= 60℃, 300h**	
Low Temperature Storage	**Ta= -20℃, 250h**	
Thermal Shock Test	**Ta=-20℃(30min) ~60℃(30min), 100cycles condition.**	
ESD	**Contact : ±8 KV** **Air : ±15 KV**	**Note 1**

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

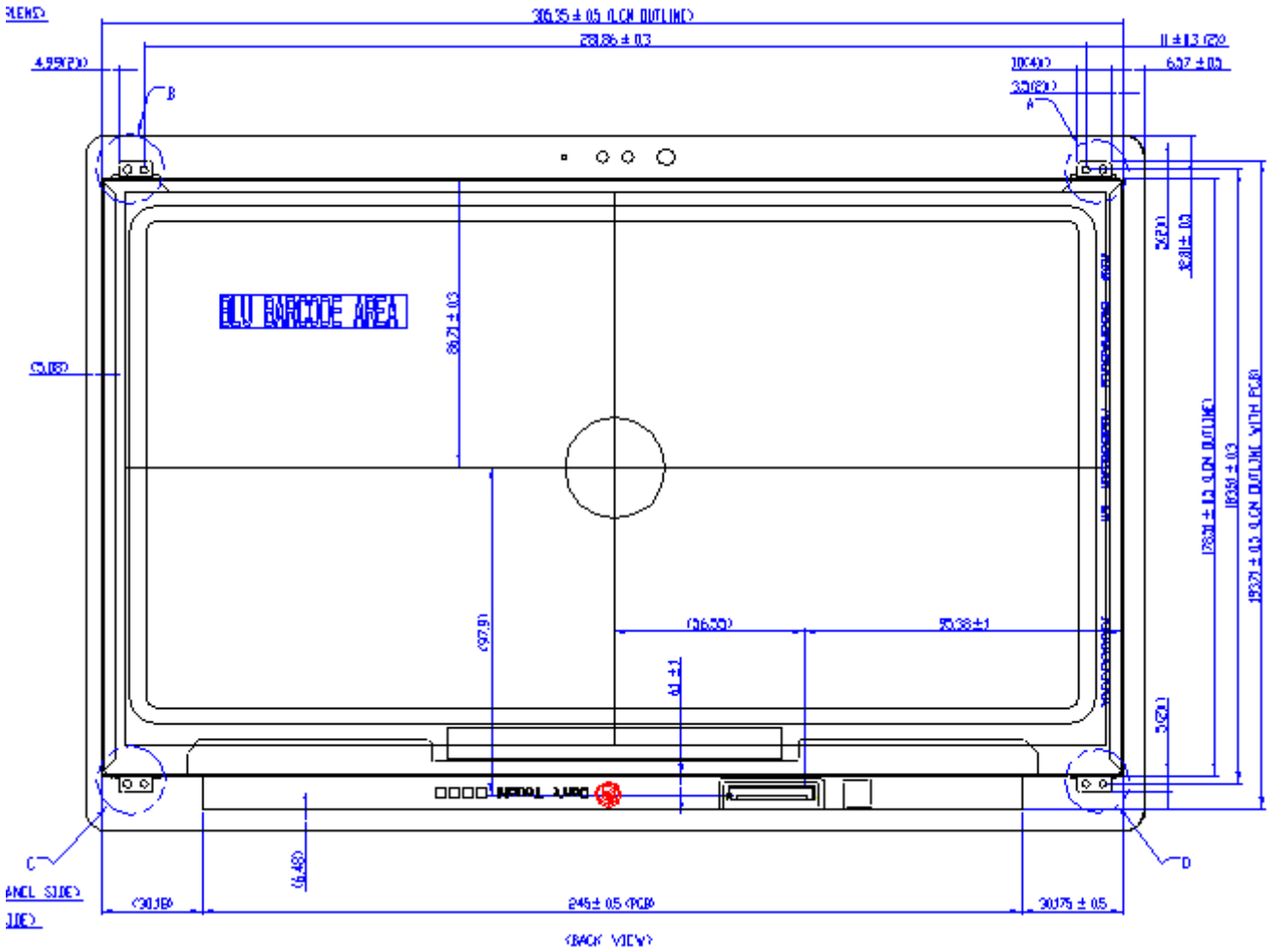
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 Total Solution Outline Dimension



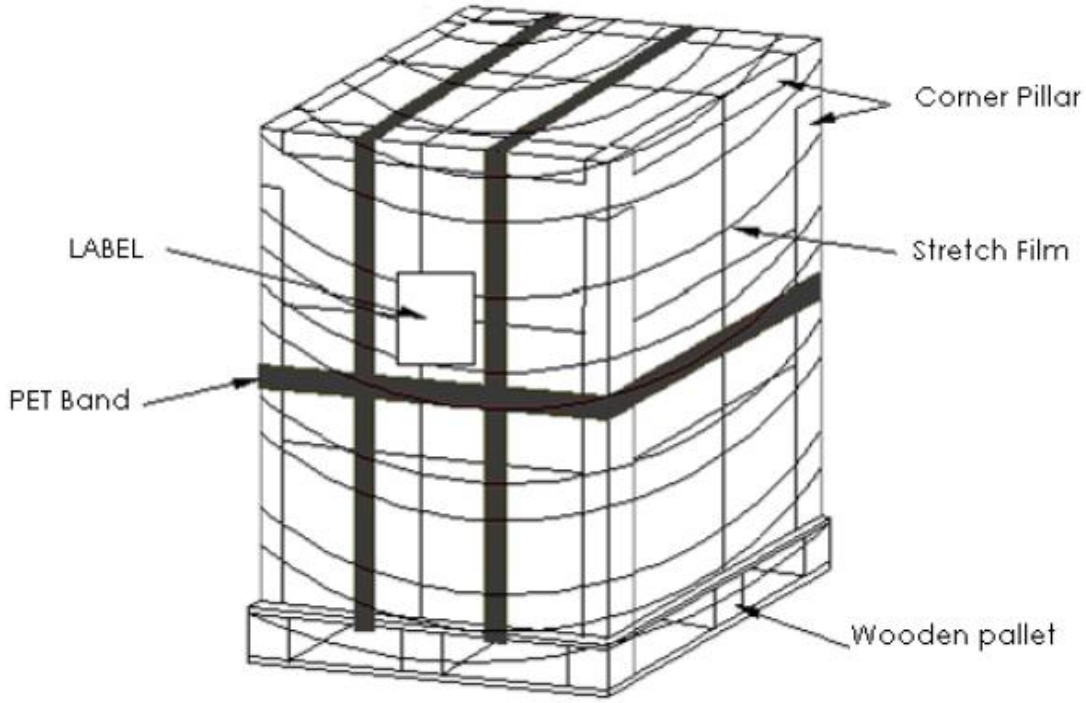
Note: “Z” 方向為最大變形量,已含變異量,此 panel 不允許外力進行扭曲


BLU BARCODE AREA
(BACK VIEW)

9. Shipping and Package

9.1 Shipping Label Format

9.2 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

	Byte (hex)	Field Name and Comments	Value (hex)
Header	0	Header	00
	1	Header	FF
	2	Header	FF
	3	Header	FF
	4	Header	FF
	5	Header	FF
	6	Header	FF
	7	Header	00
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06
	9	EISA manufacture code (Compressed ASCII)	AF
	0A	Panel Supplier Reserved – Product Code	2D
	0B	Panel Supplier Reserved – Product Code	10
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	10	Week of manufacture	00
	11	Year of manufacture	1A
	12	EDID structure version # = 1	01
	13	EDID revision # = 4	04
Display Parameters	14	Video I/P definition	95
	15	Max H image size = ?? cm (Rounded to cm)	1D
	16	Max V image size = ?? cm (Rounded to cm)	11
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78
	18	Feature support	02
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	C3
	1A	Blue/White Low bit (BxBy/WxWy)	14
	1B	Red X Rx = 0.???	93
	1C	Red Y Ry = 0.???	58
	1D	Green X Rx = 0.???	59
	1E	Green Y Ry = 0.???	92
	1F	Blue X Rx = 0.???	29
	20	Blue Y Ry = 0.???	22
	21	White X Rx = 0.???	51
	22	White Y Ry = 0.???	57
Established Timings	23	Established timings 1 (00h if not used)	00
	24	Established timings 2 (00h if not used)	00
	25	Manufacturer’s timings (00h if not used)	00
Standard Timing	26	Standard timing ID1 (01h if not used)	01

	27	Standard timing ID1 (01h if not used)	01
	28	Standard timing ID2 (01h if not used)	01
	29	Standard timing ID2 (01h if not used)	01
	2A	Standard timing ID3 (01h if not used)	01
	2B	Standard timing ID3 (01h if not used)	01
	2C	Standard timing ID4 (01h if not used)	01
	2D	Standard timing ID4 (01h if not used)	01
	2E	Standard timing ID5 (01h if not used)	01
	2F	Standard timing ID5 (01h if not used)	01
	30	Standard timing ID6 (01h if not used)	01
	31	Standard timing ID6 (01h if not used)	01
	32	Standard timing ID7 (01h if not used)	01
	33	Standard timing ID7 (01h if not used)	01
	34	Standard timing ID8 (01h if not used)	01
	35	Standard timing ID8 (01h if not used)	01
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	14
	37	Pixel Clock/10,000 (MSB)	37
	38	Horizontal Active = ???? pixels (lower 8 bits)	80
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	B8
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70
	3B	Vertical Active = ??? lines	38
	3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	24
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40
	3E	Horizontal Sync, Offset (Thfp) = ?? pixels	10
	3F	Horizontal Sync, Pulse Width = ??? pixels	10
	40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	3E
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	42	Horizontal Image Size =??? mm	25
	43	Vertical image Size = ??? mm	A5
	44	Horizontal Image Size / Vertical image size	10
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00
	46	Vertical Border = 0 (Zero for Notebook LCD)	00

	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A
Timing Descripter #2 (=Timing Descripter #1)	48	Pixel Clock/10,000 (LSB)	24
	49	Pixel Clock/10,000 (MSB)	2C
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	80
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	B8
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70
	4D	Vertical Active = xxxx lines	38
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	24
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	10
	51	Horizontal Sync, Pulse Width = xxxx pixels	10
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	3E
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	54	Horizontal Image Size =xxx mm	25
	55	Vertical image Size = xxx mm	A5
	56	Horizontal Image Size / Vertical image size	10
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00
	58	Vertical Border = 0 (Zero for Notebook LCD)	00
	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A
Timing Descripter #3 Dell specific information	5A	Flag	00
	5B	Flag	00
	5C	Flag	00
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE
	5E	Flag	00
	5F	Dell P/N 1st Character	46
	60	Dell P/N 2nd Character	43

	61	Dell P/N 3rd Character	54
	62	Dell P/N 4th Character	47
	63	Dell P/N 5th Character	38
	64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	83
	65	Manufacturer P/N	42
	66	Manufacturer P/N	31
	67	Manufacturer P/N	33
	68	Manufacturer P/N	33
	69	Manufacturer P/N	48
	6A	Manufacturer P/N	41
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	42
Timing Descripter #4	6C	Flag	00
	6D	Flag	00
	6E	Flag	00
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00
	70	Flag	00
	71	Color Management	00
	72	Panel Structure	41
	73	Frame Rate	22
	74	Light Controller Interface and Luminance	96
	75	Outdoor Features	00
	76	Multi-Media Features	11
	77	Multi-Media Features	00
	78	Special Features #1	00
	79	Special Features #2	0A
	7A	Special Features #3	01
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	61