( ) Preliminary Specifications
(V) Final Specifications

Module	**13.3”(13.26”) UHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B133ZAN02.2 (H/W:0A)**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**

Approved by	**Date**
Marcus Yen	2018/06/06
Prepared by	**Date**
Katrina Chen	2018/06/06

Note: This Specification is subject to change without notice.

NBBU Marketing Division
AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2017/06/12	All	First edition for customer		
0.2 2017/09/18	25	Update label information		
0.3 2017/09/20	28	Revise EDID		
1.0 2018/05/24	12	Update Power Specification		
1.1 2018/06/06	5	Update Power Specification		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B133ZAN02.2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 UHD, 3840(H) x2160(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B133ZAN02.2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	13.26”			
Active Area	[mm]	293.76 (H) x 165.24(V)			
Pixels H x V		3840 x 3 (RGB) x 2160			
Pixel Pitch	[mm]	0.0765 x 0.0765			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance **(Note: ILED is LED current)**	[cd/m^2]	500 typ. (5 points average)			
Luminance Uniformity		1.4 max. (13 points) 1.6 max. (13 points)			
Contrast Ratio		1400 typ			
Response Time	[ms]	30 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ			
Power Consumption	[Watt]	5.95 W max. (Include Logic and BLU)			
Weight	[Grams]	190 max			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	298.66	298.96	299.26
		Width (w/o FPCa)	176.91	177.21	177.51
		Thickness	--	--	2.0/4.0
Electrical Interface		4Lane eDP 1.4a			
Glass Thickness	[mm]	0.2			
Surface Treatment		Glare,			
Support Color		16.7M colors (RGB 8-bit)			

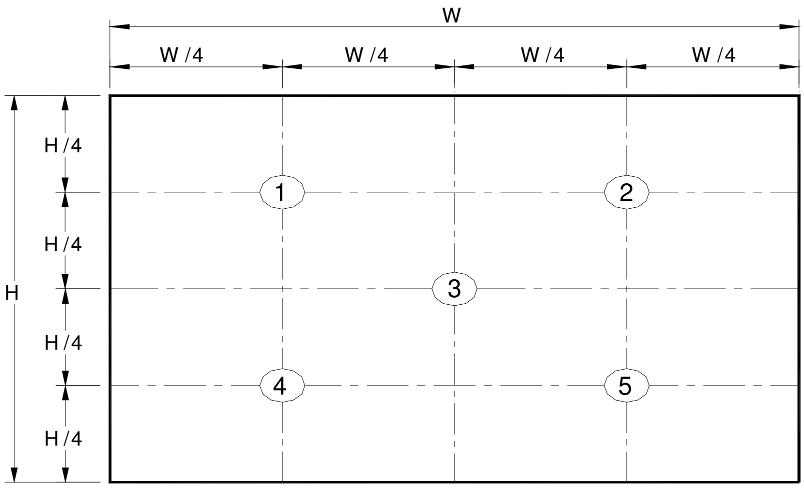
Temperature Range Operating Storage (Non-Operating)	 [^oC] [^oC]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

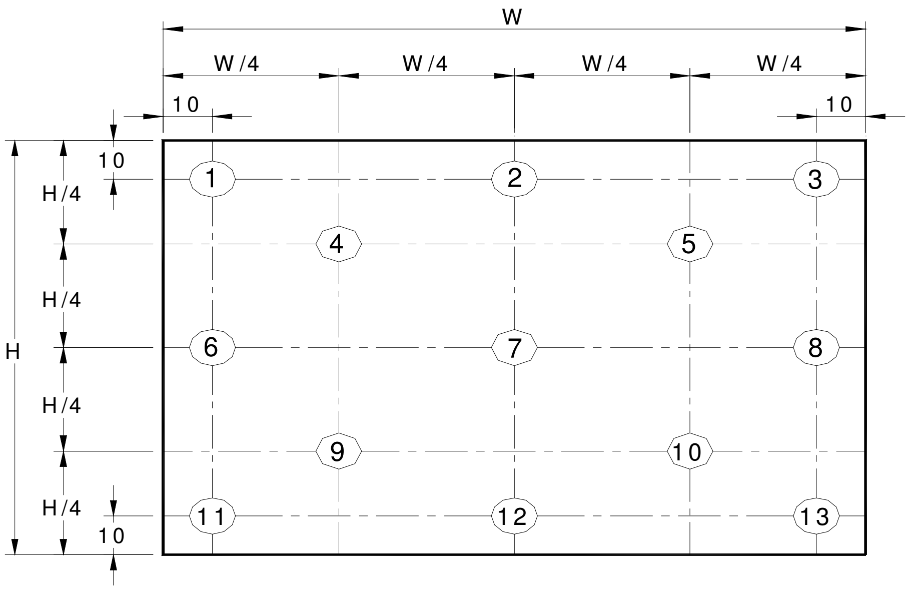
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=21mA			5 points average		500	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	80	85	-	degree	4, 9
		θ_L	(Left)	80	85	-		
		ϕ_H	Vertical (Upper) CR = 10	80	85	-		
		ϕ_L	(Lower)	80	85	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.4		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.6		2, 3, 4
Contrast Ratio		CR			1400	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	30		msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.610	0.640	0.670		4
		Ry		0.300	0.330	0.360		
	Green	Gx		0.270	0.300	0.330		
		Gy		0.570	0.600	0.630		
	Blue	Bx		0.120	0.150	0.180		
		By		0.030	0.060	0.090		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	72	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



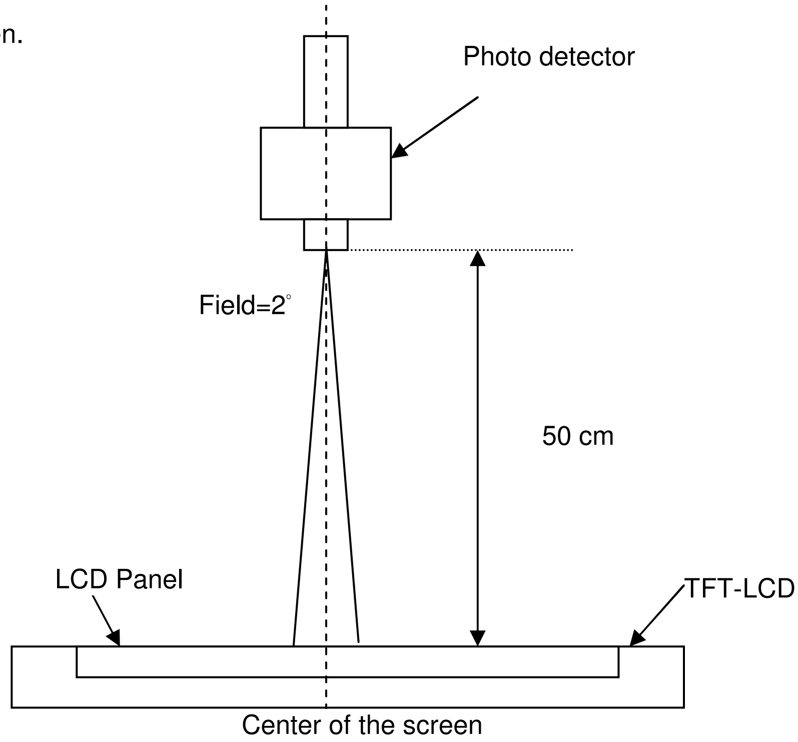
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，$Y_L = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

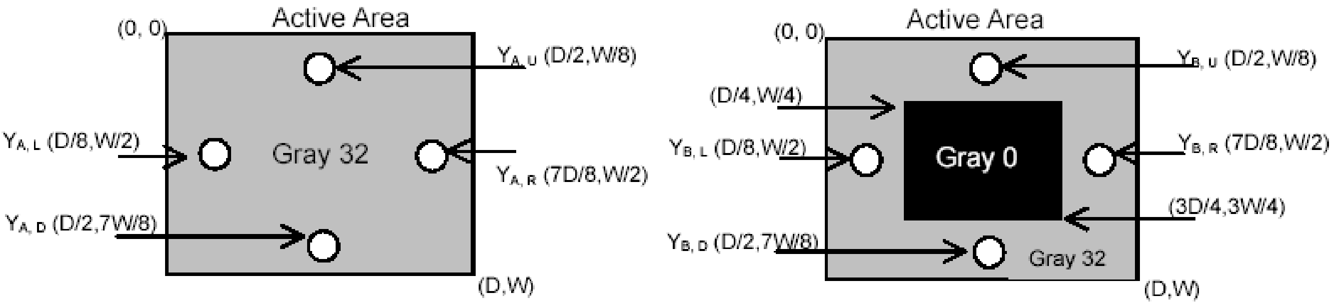
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

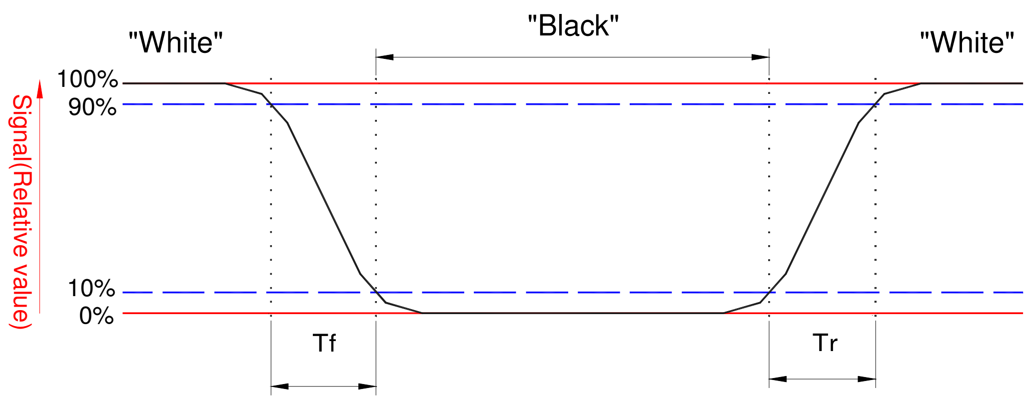
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



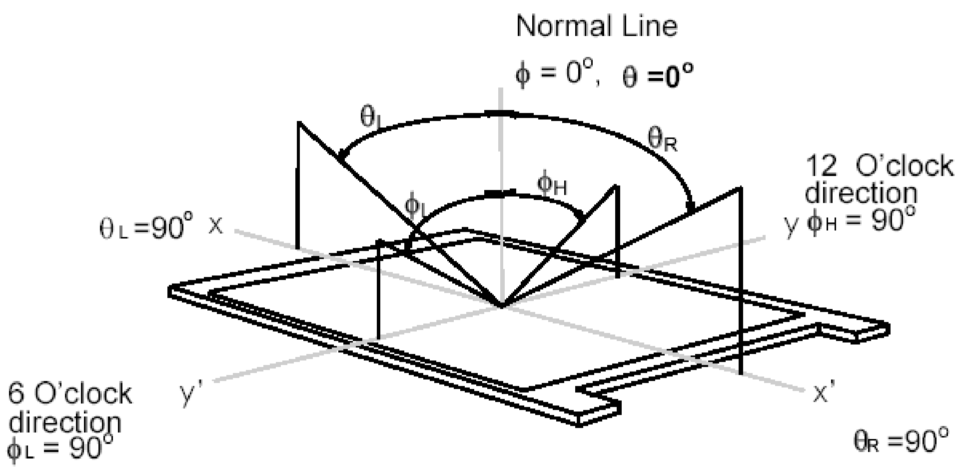
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



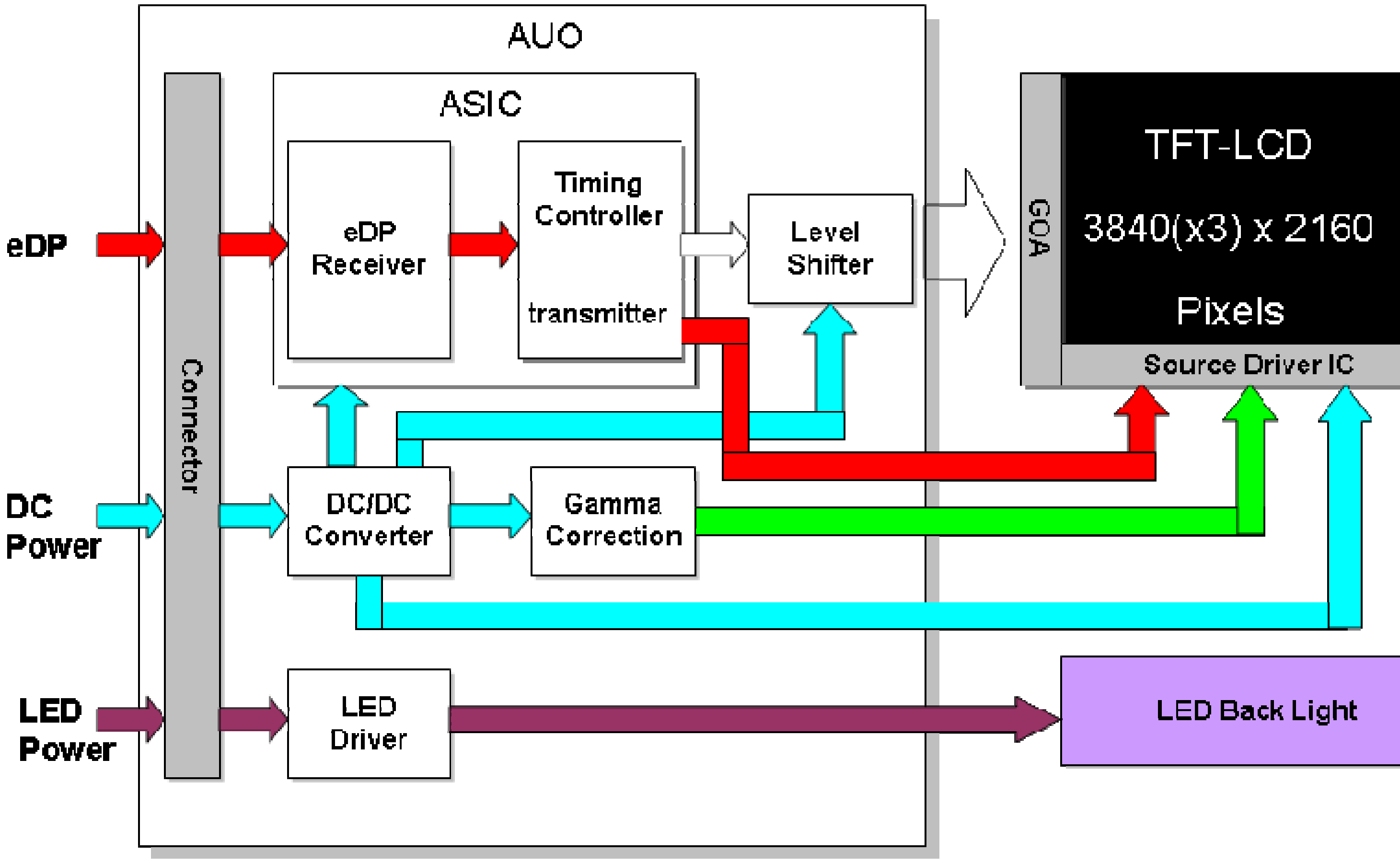
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD 40 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

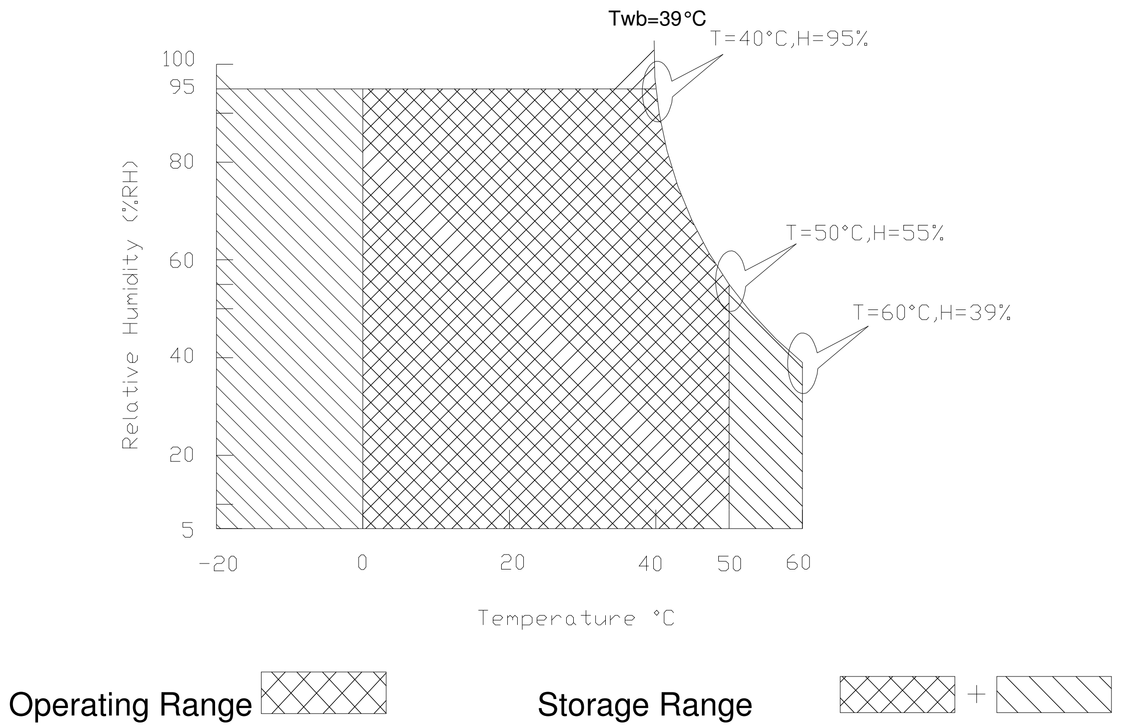
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[^{o}C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

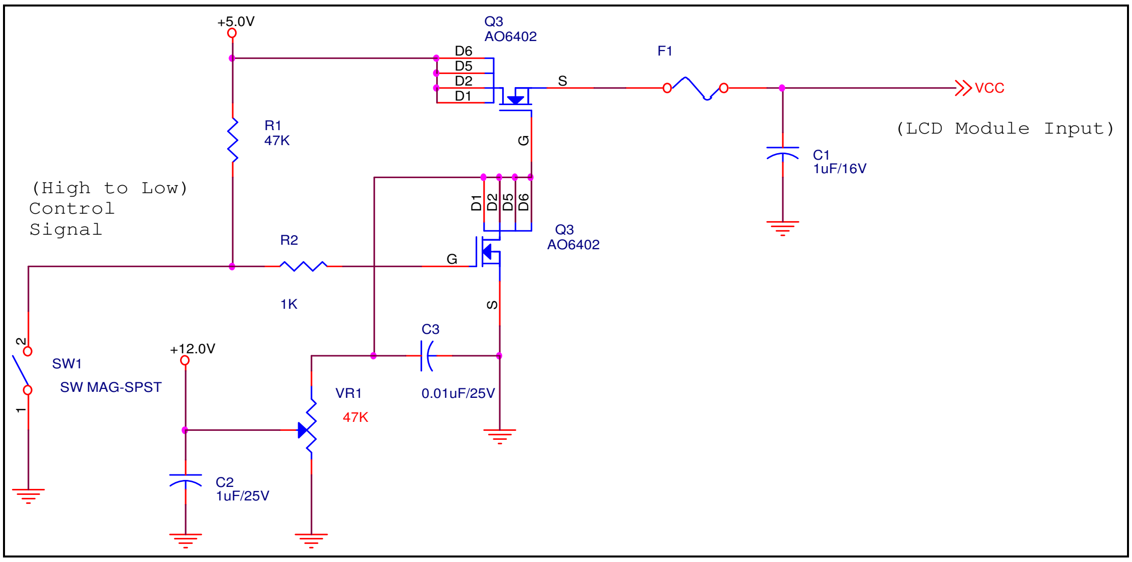
The power specification are measured under 25℃ and frame frenquency under 60Hz

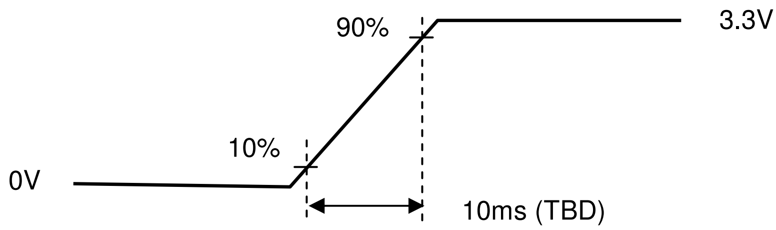
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	1.65	2.5	[Watt]	Note 1
IDD	IDD Current	-		833	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power; PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)

Note 2：Measure Condition





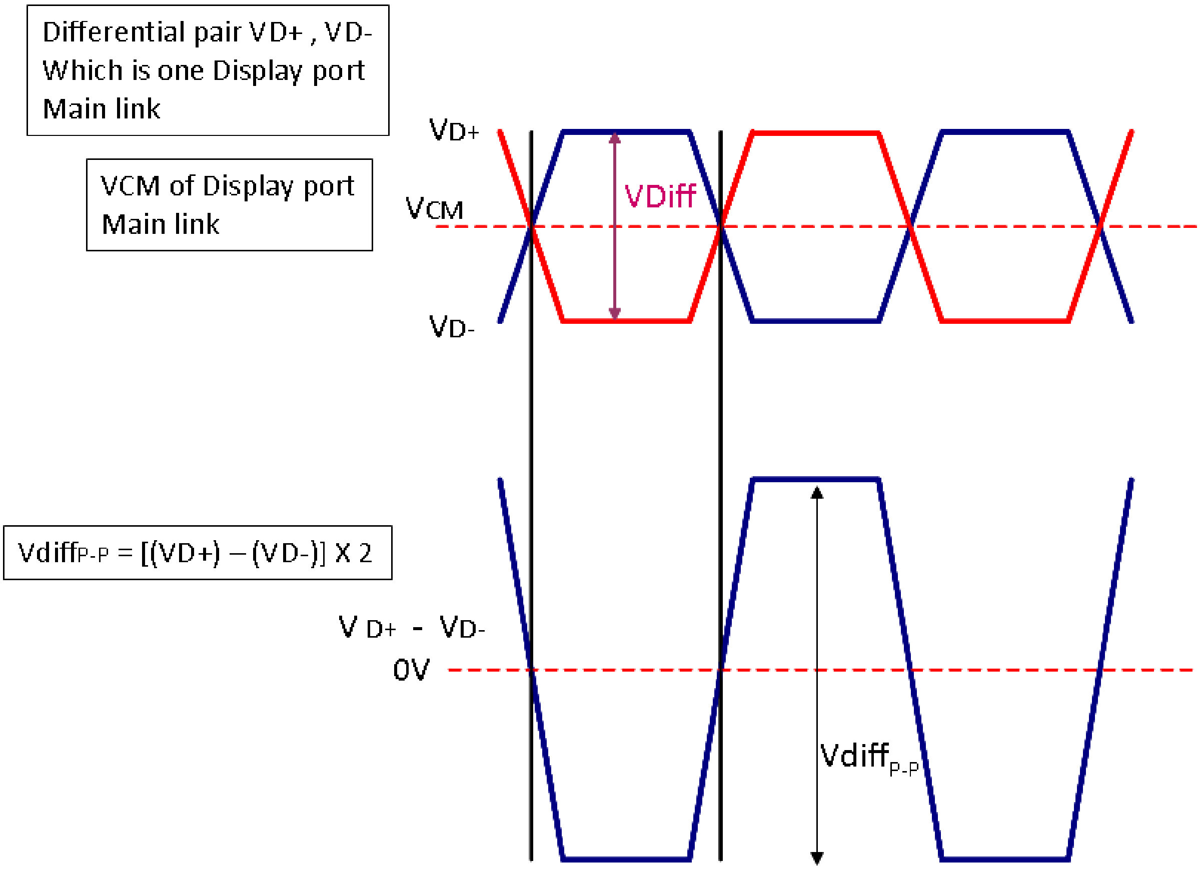
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

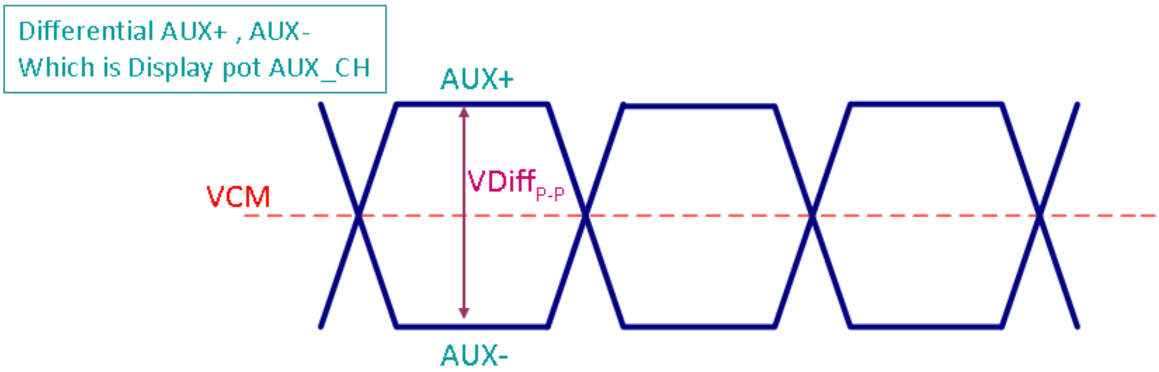
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage	--	0	--	V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100	--	1320	mV

Follow as VESA display port standard V1.4a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	--	0	--	V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.4a

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	--	3.6	V

Follow as VESA display port standard V1.4a

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	4.3	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5	12	21	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	3.0	3.3	3.6	[Volt]	
LED Enable Input Low Level		0	0	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	3.0	3.3	3.6	[Volt]	
PWM Logic Input Low Level		0	0	0.5	[Volt]	
PWM Input Frequency	FPWM	200	--	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10KOhm

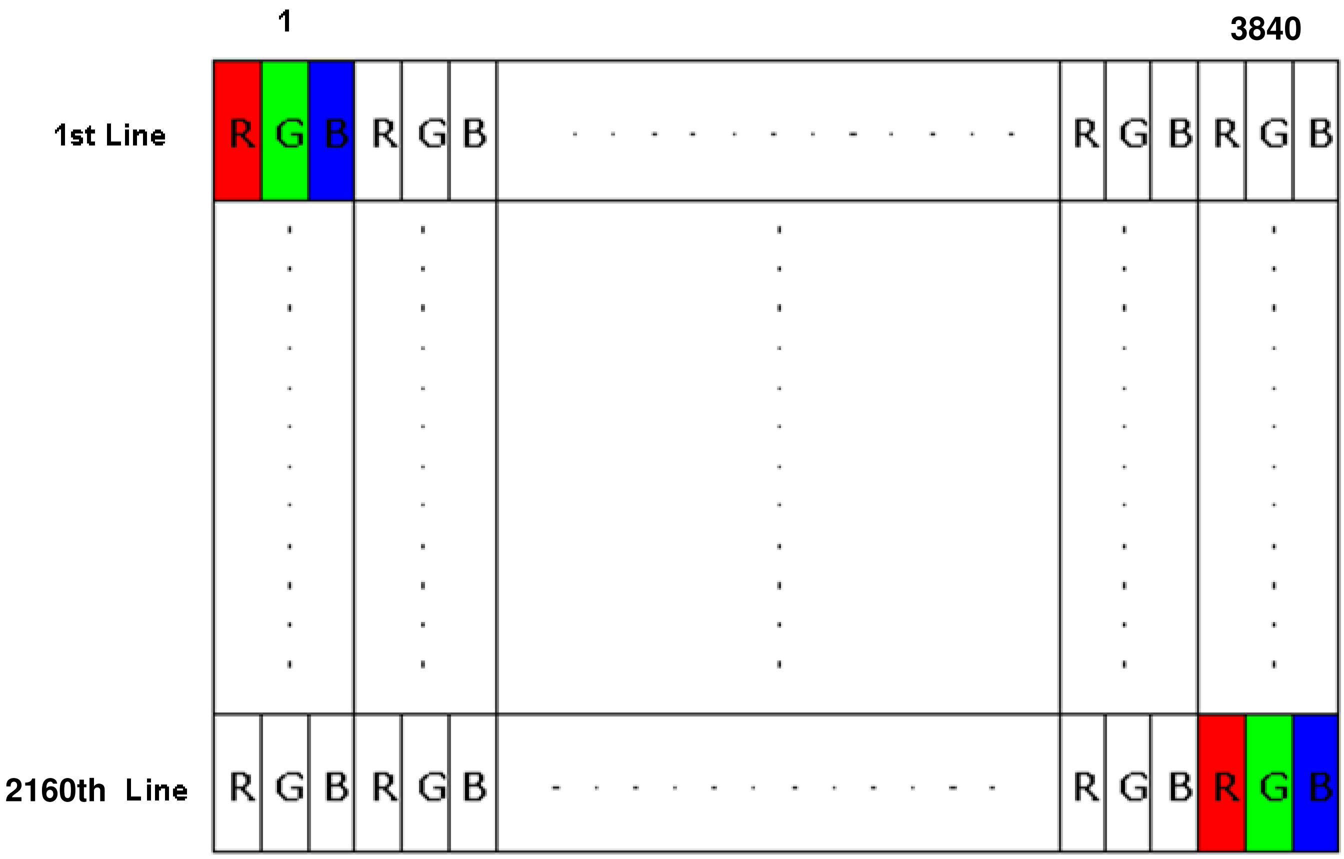
Note 2 : measured in panel VIN

Note 3 : If the PWM duty ratio(min) is set between 5% to 1%，the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX
Type / Part Number	IPEX 20455-040E-76B or compatible
Mating Housing/Part Number	IPEX 20453-040T-01 or compatible

6.2.2 Pin Assignment (4 Lane)

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin No.	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	Lane3_N	Comp Signal Link Lane3
4	Lane3_P	True Signal Link Lane3
5	H_GND	High Speed Ground
6	Lane2_N	Comp Signal Link Lane2
7	Lane2_P	True Signal Link Lane2
8	H_GND	High Speed Ground
9	Lane1_N	Comp Signal Link Lane1
10	Lane1_P	True Signal Link Lane1
11	H_GND	High Speed Ground
12	Lane0_N	Comp Signal Link Lane0
13	Lane0_P	True Signal Link Lane0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Ch
16	AUX_CH_N	Comp Signal Auxiliary Ch
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test	LCD Panel Self Test Enable
23	LCD GND	LCD logic and driver ground
24	LCD GND	LCD logic and driver ground
25	LCD GND	LCD logic and driver ground
26	LCD GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight_ground
29	BL_GND	Backlight_ground
30	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On/Off enable
33	BL_PWM_DIM	Backlight PWM Signal Input
34	NC	No connect
35	NC	No connect
36	BL_PWR	Backlight Power
37	BL_PWR	Backlight Power
38	BL_PWR	Backlight Power
39	BL_PWR	Backlight Power
40	NC	No connect

Note1: Start from right side

Note2: Input signals shall be low or High-impedance state when VDD is off. Internal circuit of **eDP inputs** are as following.

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 3840x2160 /60Hz manufacturing guide line timing.

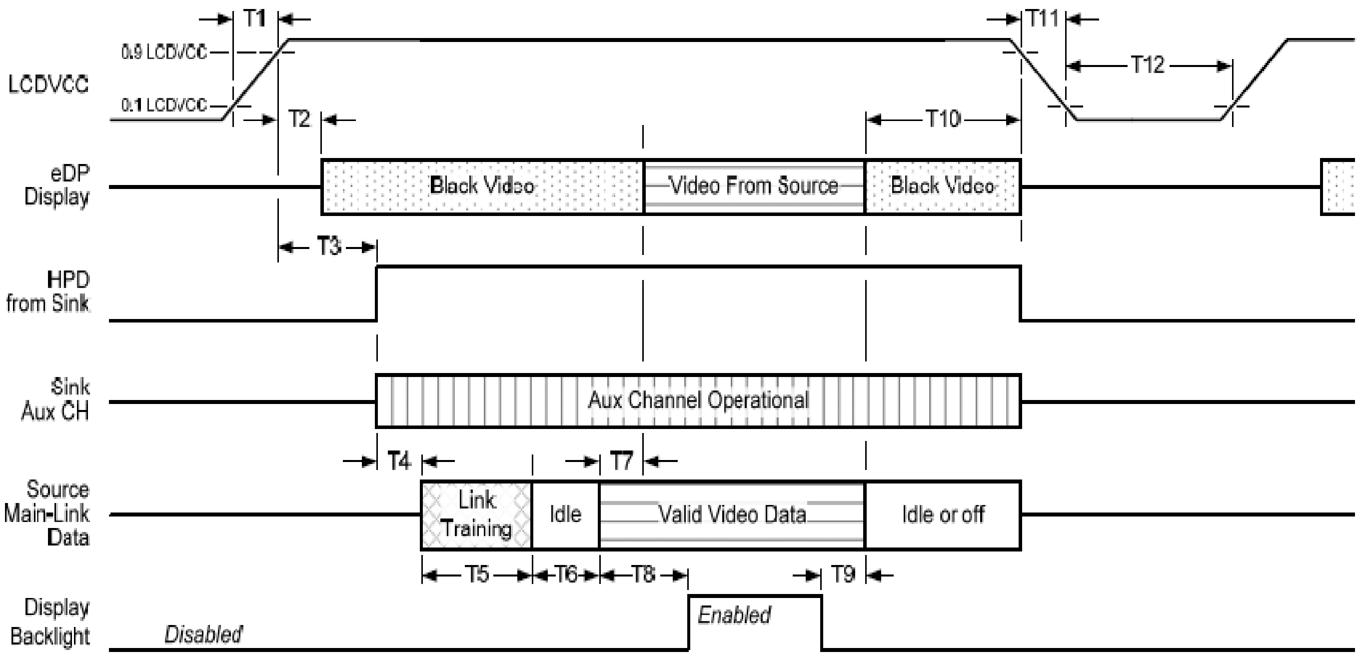
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	59.94	59.97	60	Hz
Clock frequency		$1/T_{Clock}$	--	533.01	--	MHz
Vertical Section	Period	T_V	--	2222	--	T_{Line}
	Active	T_{VD}		2160		
	Blanking	T_{VB}	--	62	--	
Horizontal Section	Period	T_H	--	4000	--	T_{Clock}
	Active	T_{HD}		3840		
	Blanking	T_{HB}	--	160	--	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency

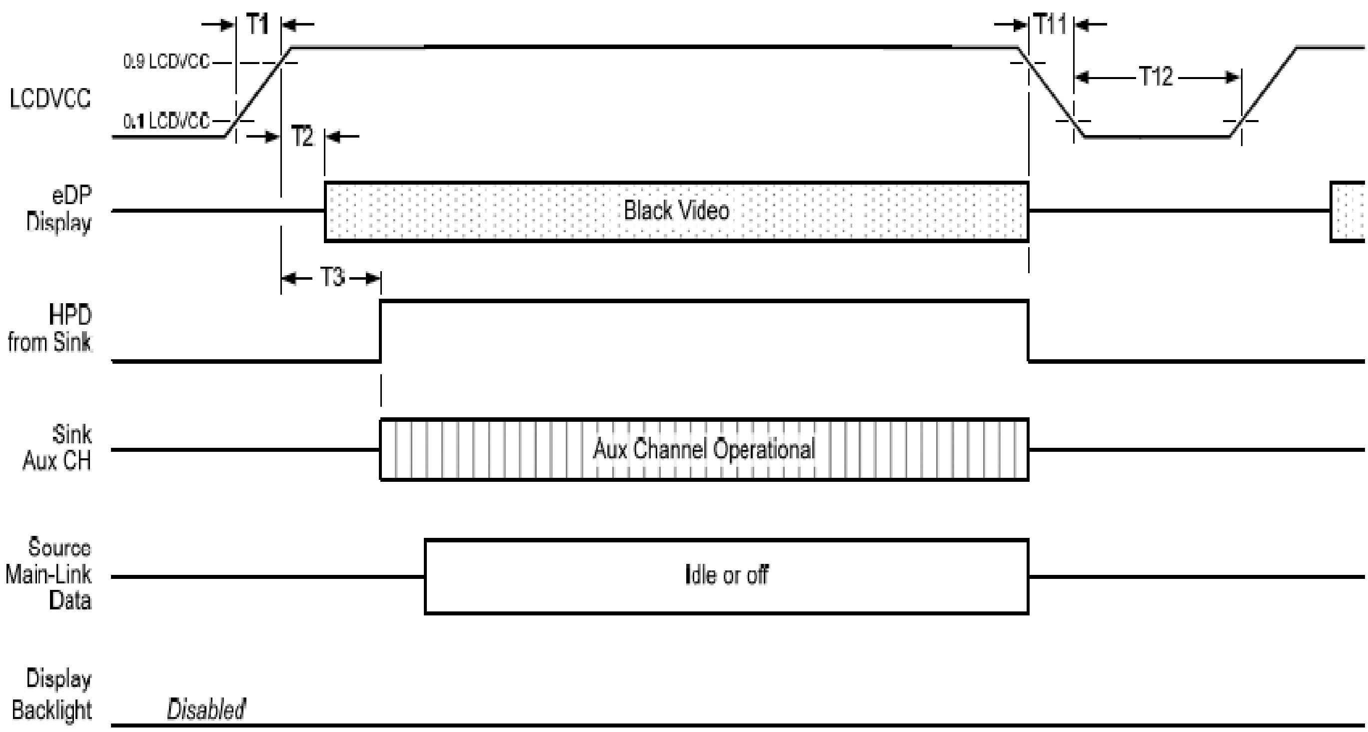
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

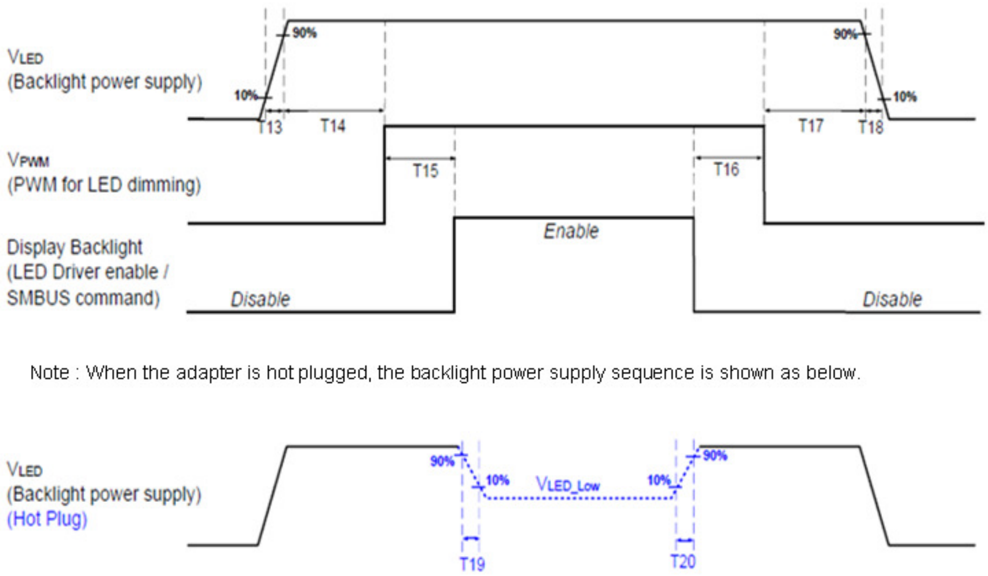
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	150ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.2	10
T14	0	-
T15	0	-
T16	0	-
T17	0	-
T18	0.2	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note 1 : If T14,T15,T16,T17<10ms，The display garbage may occur. We suggest T14,T15,T16,T17>10ms to avoid the display garbage.

Note 2：If T13 or T18<0.5ms，the inrush current may cause the damage of fuse. If T13 or T18<0.5ms，the inrush current I^2t is under typical melt of fuse Spec.，there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

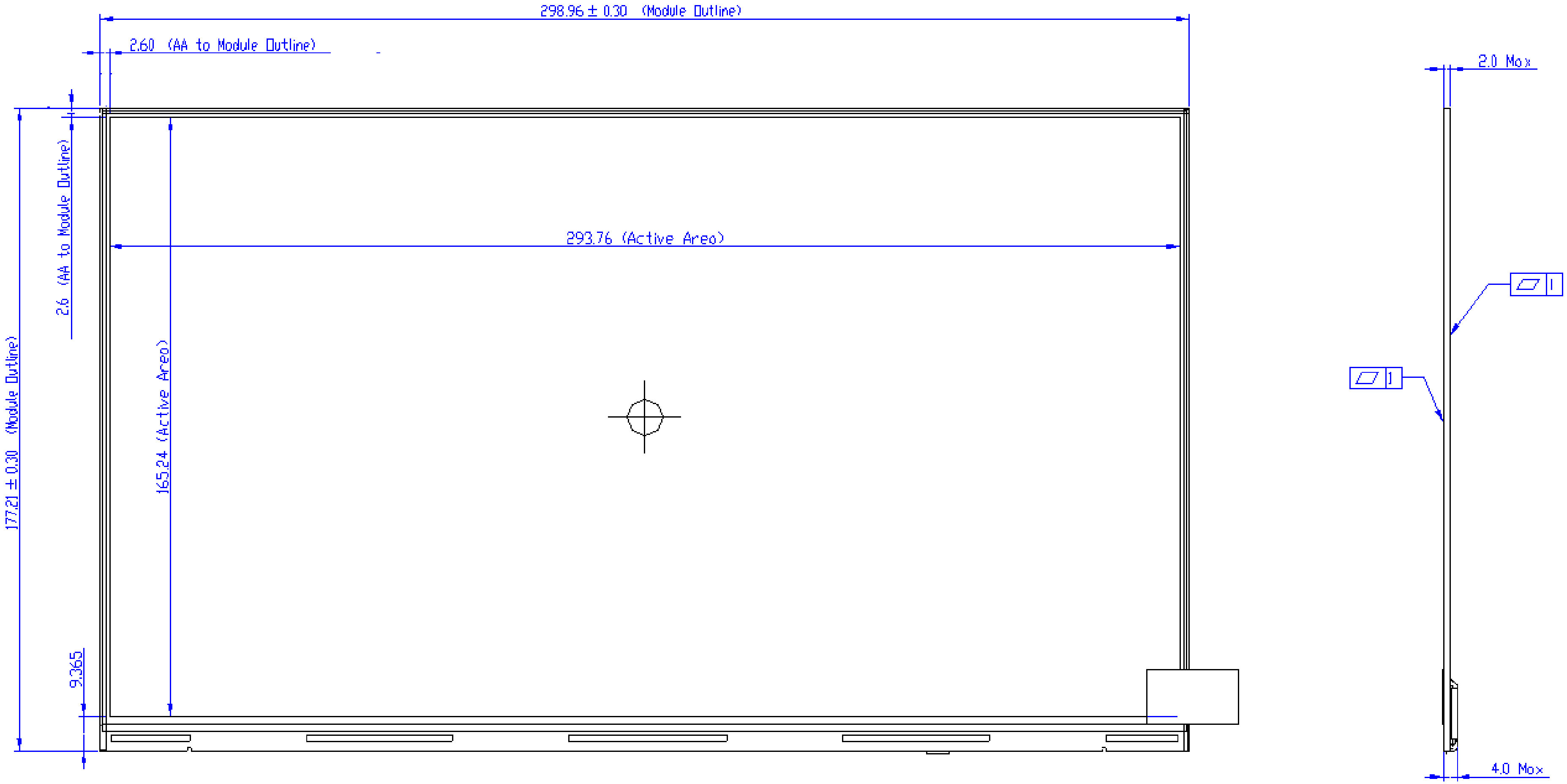
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

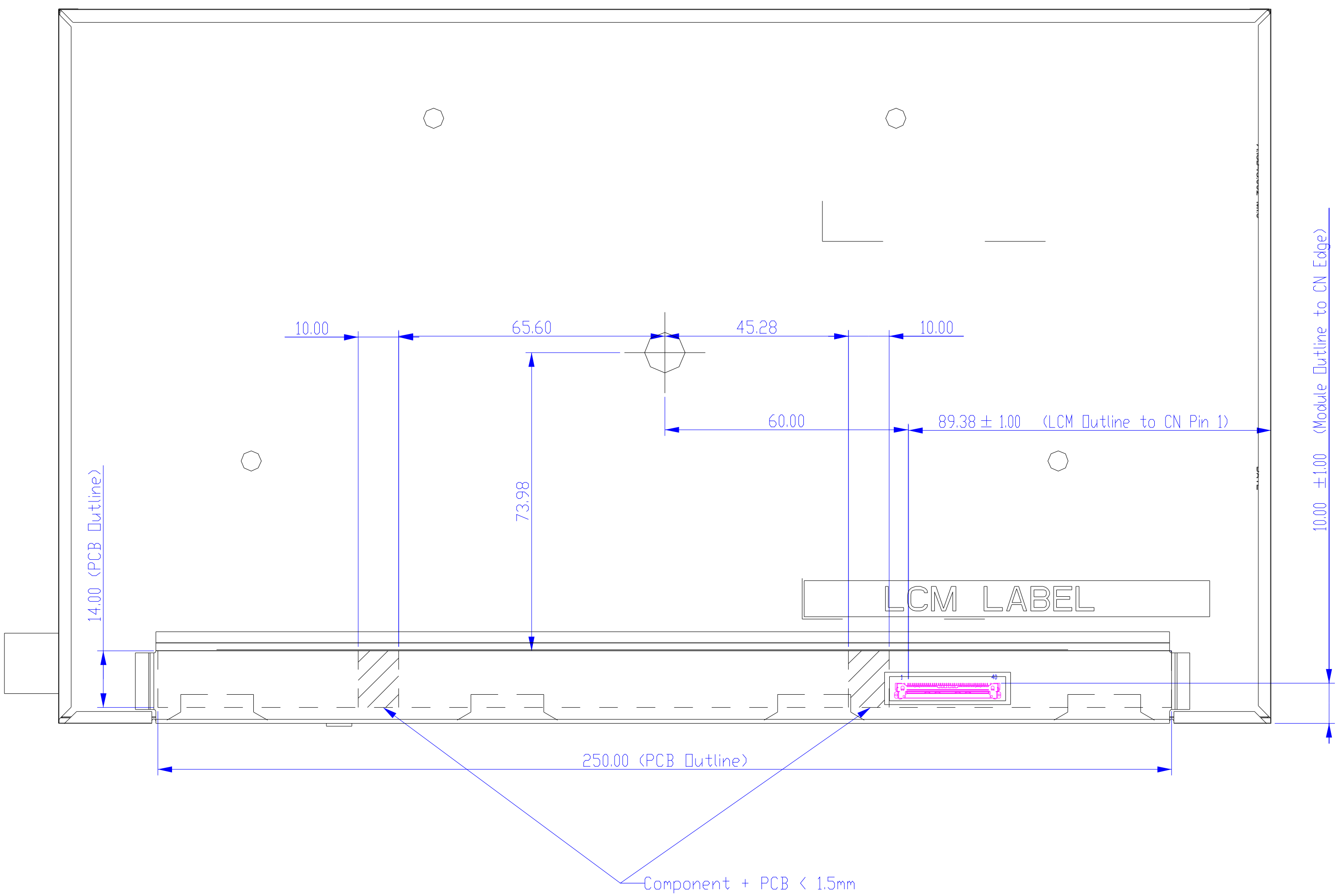
8.1 LCM Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Rear View & Key components remark and remind

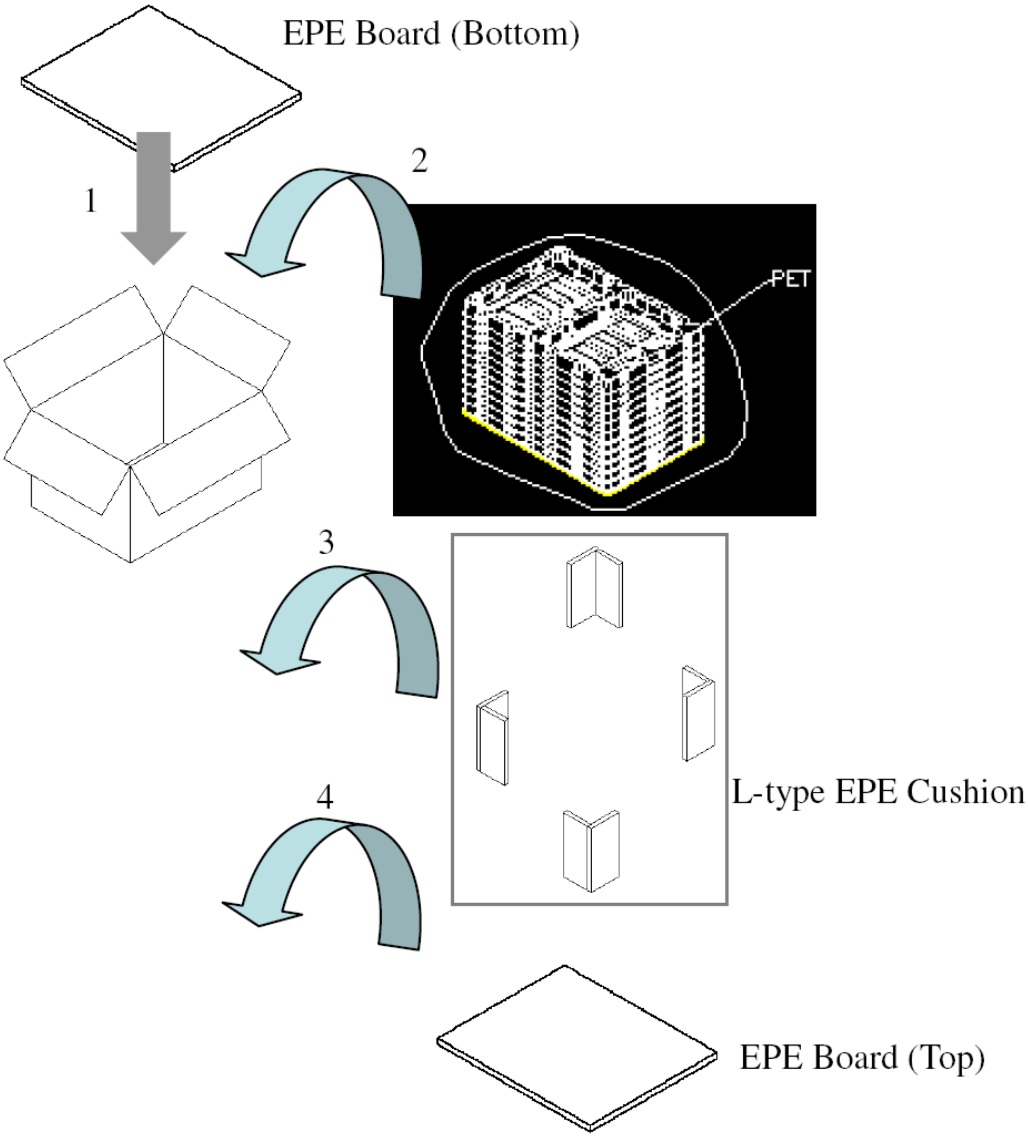
Prevention damage the IC, connector, Capacitor…., we recommend your design (Ex: cable, rib, hardness parts) far away those section those have remarked at this drawing.



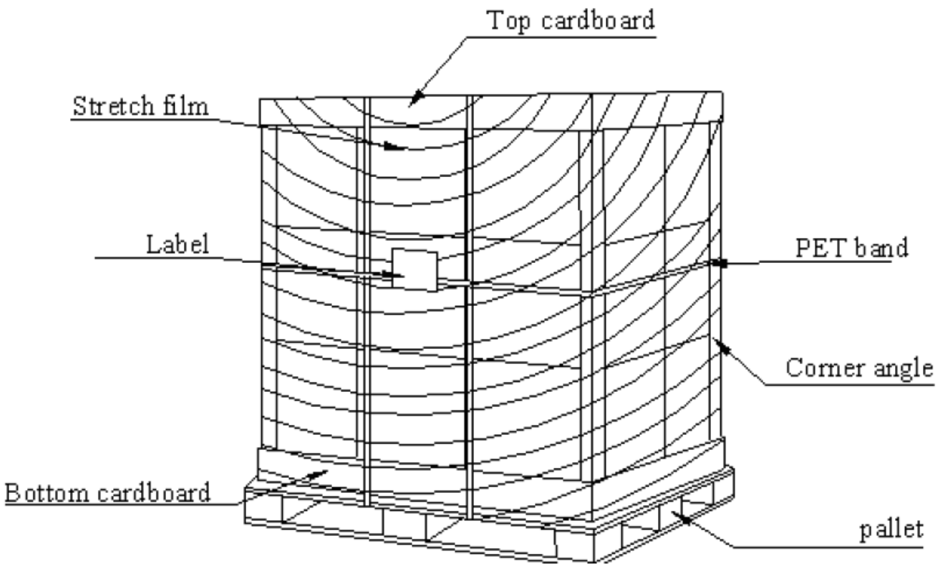
9. Shipping and Package

9.1 Shipping Label Format

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	2B	00101011	43
0B	hex, LSB first	22	00100010	34
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	10	00010000	16
11	Year of manufacture	1B	00011011	27
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A5	10100101	165
15	**Max H image size** *(rounded to cm)*	1D	00011101	29
16	**Max V image size** *(rounded to cm)*	11	00010001	17
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2
19	Red/green low bits **(Lower 2:2:2:2 bits)**	EE	11101110	238
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	95	10010101	149
1B	Red x **(Upper 8 bits)**	A3	10100011	163
1C	Red y/ highER 8 bits	54	01010100	84
1D	Green x	4C	01001100	76
1E	Green y	99	10011001	153
1F	Blue x	26	00100110	38
20	Blue y	0F	00001111	15
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0

25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	52	01010010	82
37	Pixel Clock/10000 USB	D0	11010000	208
38	Horz active **Lower 8bits**	00	00000000	0
39	Horz blanking **Lower 8bits**	A0	10100000	160
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	F0	11110000	240
3B	Vertical Active **Lower 8bits**	70	01110000	112
3C	Vertical Blanking **Lower 8bits**	3E	00111110	62
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	80	10000000	128
3E	HorzSync. Offset	30	00110000	48
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	35	00110101	53
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0
42	Horizontal Image Size **Lower 8bits**	25	00100101	37
43	Vertical Image Size **Lower 8bits**	A5	10100101	165
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
46	Vertical Border *(zero for internal LCD)*	00	00000000	0
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
48	Pixel Clock/10,000 (LSB)	52	01010010	82
49	Pixel Clock/10,000 (MSB)	D0	11010000	208
4A	Horizontal Addressable Pixels, lower 8 bits	00	00000000	0
4B	Horizontal Blanking Pixels, lower 8 bits	A0	10100000	160
4C	H Pixels, upper nibble : H Blanking, upper nibble	F0	11110000	240
4D	Vertical Addressable Lines, lower 8 bits	70	01110000	112
4E	Vertical Blanking Lines, lower 8 bits	95	10010101	149
4F	V lines, upper nibble : V blanking, upper nibble	84	10000100	132

50	Horizontal Front Porch, lower 8 bits	30	00110000	48
51	Horizontal Sync Pulse, lower 8 bits	20	00100000	32
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	35	00110101	53
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0
54	Horizontal Image Size in mm, lower 8 bits	25	00100101	37
55	Vertical Image Size in mm, lower 8 bits	A5	10100101	165
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16
57	Horizontal Border	00	00000000	0
58	Vertical Border	00	00000000	0
59	Bit Encode Sync Information	18	00011000	24
5A	DC	00	00000000	0
5B	HTOTAL	00	00000000	0
5C	HA	00	00000000	0
5D	HBL	00	00000000	0
5E	HFP	00	00000000	0
5F	HFPe	00	00000000	0
60	HBP	00	00000000	0
61	HB	00	00000000	0
62	HSO	00	00000000	0
63	HS	00	00000000	0
64	VTOTAL	00	00000000	0
65	VA	00	00000000	0
66	VBL	00	00000000	0
67	VFP	00	00000000	0
68	VBP	00	00000000	0
69	VB	00	00000000	0
6A	VSO	00	00000000	0
6B	VS	00	00000000	0
6C	Detail Timing Description #4	00	00000000	0
6D	Flag	00	00000000	0
6E	Reserved	00	00000000	0
6F	For Brightness Table and Power Consumption	02	00000010	2
70	Flag	00	00000000	0
71	PWM % [7:0] @ Step 0	14	00010100	20
72	PWM % [7:0] @ Step 5	26	00100110	38
73	PWM % [7:0] @ Step 10	FF	11111111	255
74	Nits [7:0] @ Step 0	12	00010010	18
75	Nits [7:0] @ Step 5	3C	00111100	60
76	Nits [7:0] @ Step 10	FA	11111010	250
77	Panel Electronics Power @ 32x32 Chess Pattern =	29	00101001	41
78	Backlight Power @ 60 nits =	36	00110110	54
79	Backlight Power @ Step 10 =	35	00110101	53

7A	Nits @ 100% PWM Duty =	FA	11111010	250
7B	Flag	20	00100000	32
7C	Flag	20	00100000	32
7D	Flag	20	00100000	32
7E	Extension Flag	00	00000000	0
7F	Checksum	C5	11000101	197