( ) Preliminary Specifications
(V) Final Specifications

Module	**14.0" (13.98") HD+ 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**B140RTN02.1 (H/W:0A)**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**
Dell	03/06/2012
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Claire Yu	03/06/2012
Prepared by	**Date**
Jovin Chan	03/06/2012
NBBU Marketing Division AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2011/10/14	All	First Edition for Customer		
0.2 2011/12/13			Modified label information	
0.3 2012/01/30			Modified Color coodinates/CR/EDID	
1.0 2012/03/06			Update A00 Label/EDID for X-build	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B140RTN02.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1600(H) x900(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B140RTN02.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	14.0” (13.98”)			
Active Area	[mm]	309.60 X 174.15			
Pixels H x V		1600x3(RGB) x 900			
Pixel Pitch	[mm]	0.1935X0.1935			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance **(Note: ILED is LED current)**	[cd/m^2]	300 typ. (5 points average) 255 min			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		600 (typ)			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.0 max. (Include Logic and Blu power)			
Weight	[Grams]	350 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	319.9	320.4	320.9
		Width	204.6	205.1	205.6
		Thickness			3.60
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 3H, Reflection 4.3%			
Support Color		262K colors (RGB 6-bit)			

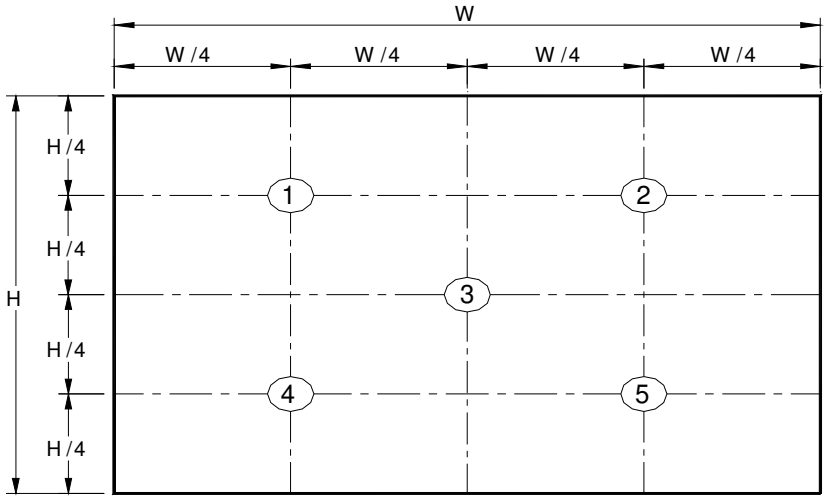
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

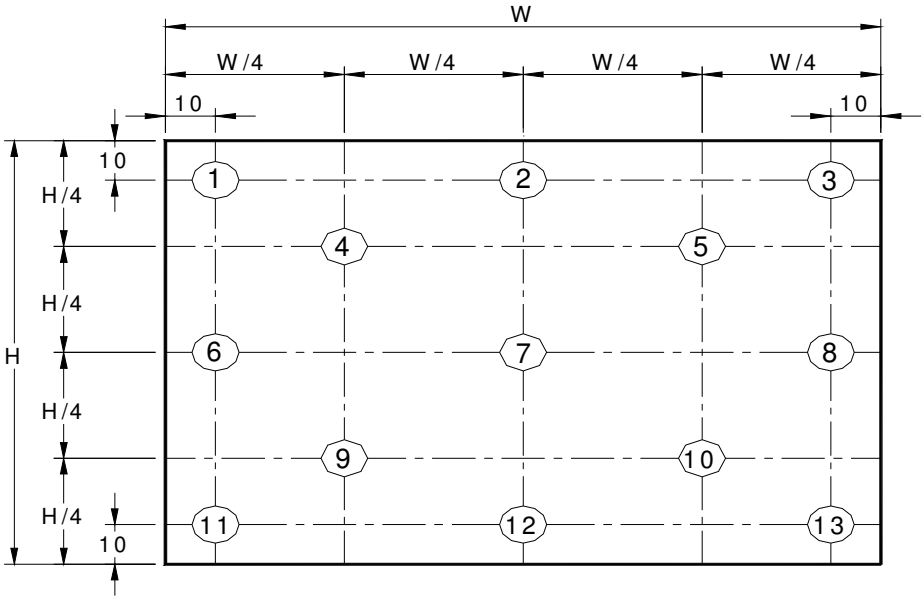
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=22mA			5 points average	255	300	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	60 60	70 70	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	50 50	60 60	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.53		2, 3, 4
Contrast Ratio		CR		500	600	-		4, 6
Cross talk		%				4		4, 7
Resoponse time		T_{RT}	Rising + Falling	-	8	16	msec	
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.57	0.60	0.63	-	4
		Ry		0.32	0.35	0.38		
	Green	Gx		0.29	0.32	0.35		
		Gy		0.55	0.58	0.61		
	Blue	Bx		0.12	0.15	0.18		
		By		0.10	0.13	0.16		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%			45			

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

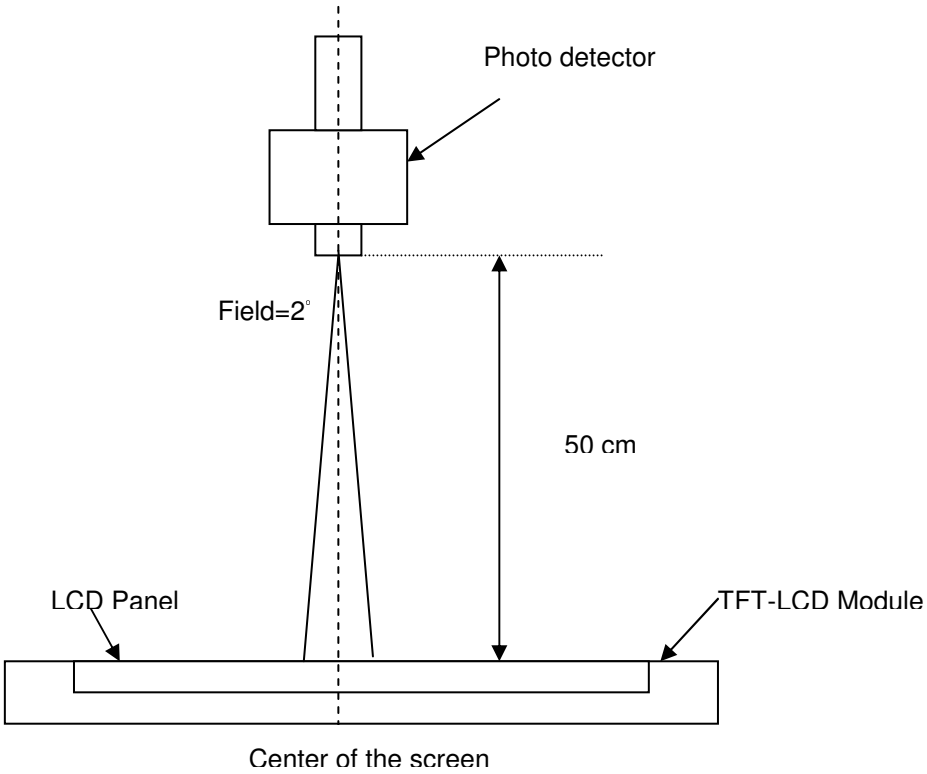
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

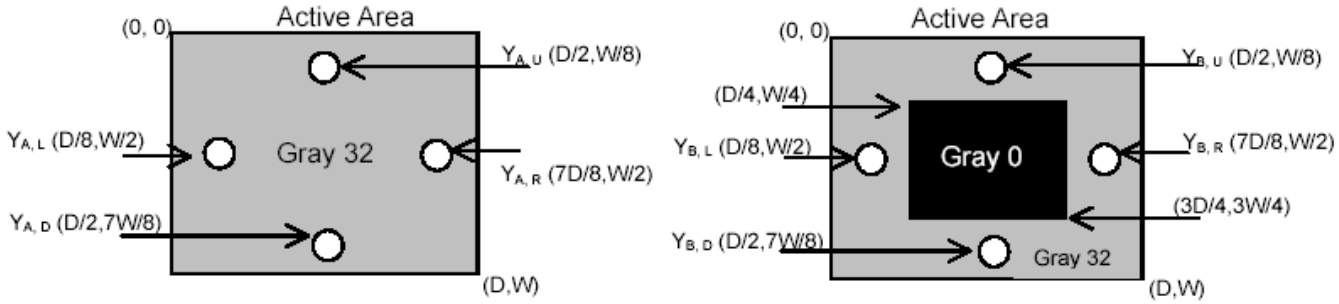
Note 7 : Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

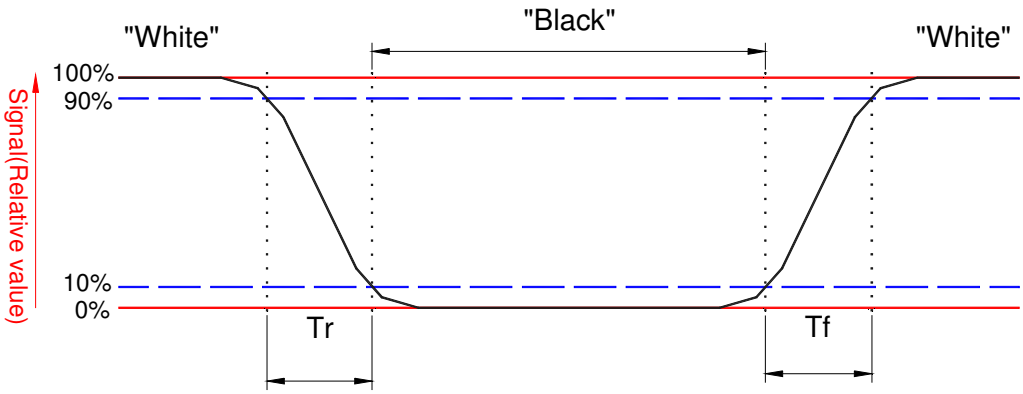
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



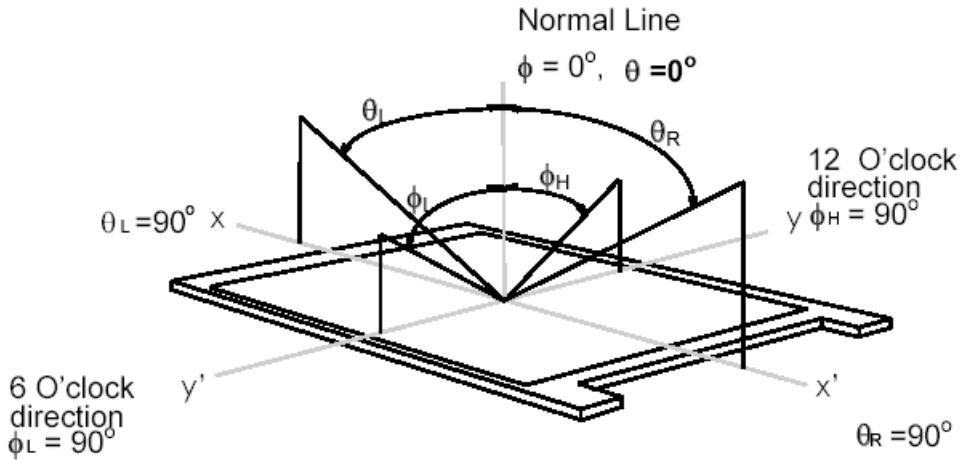
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



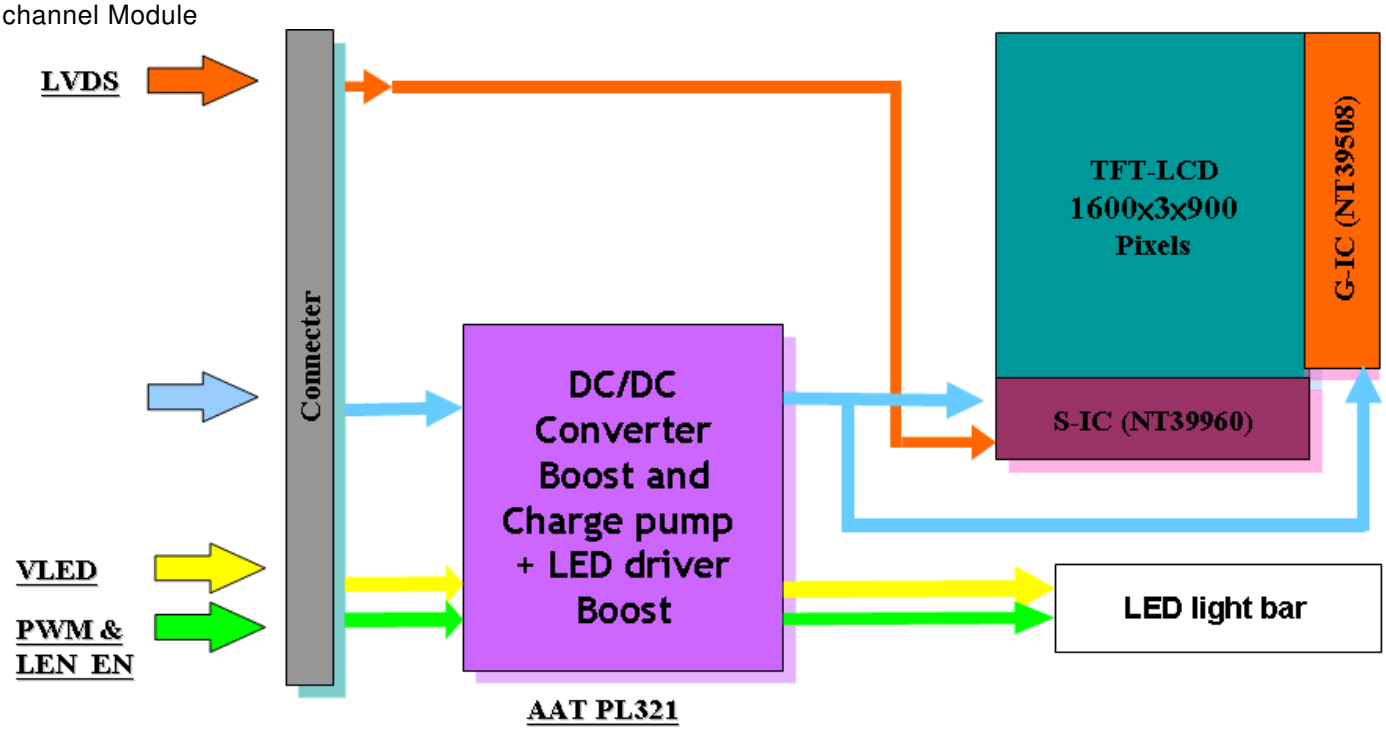
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 40 Pin two channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

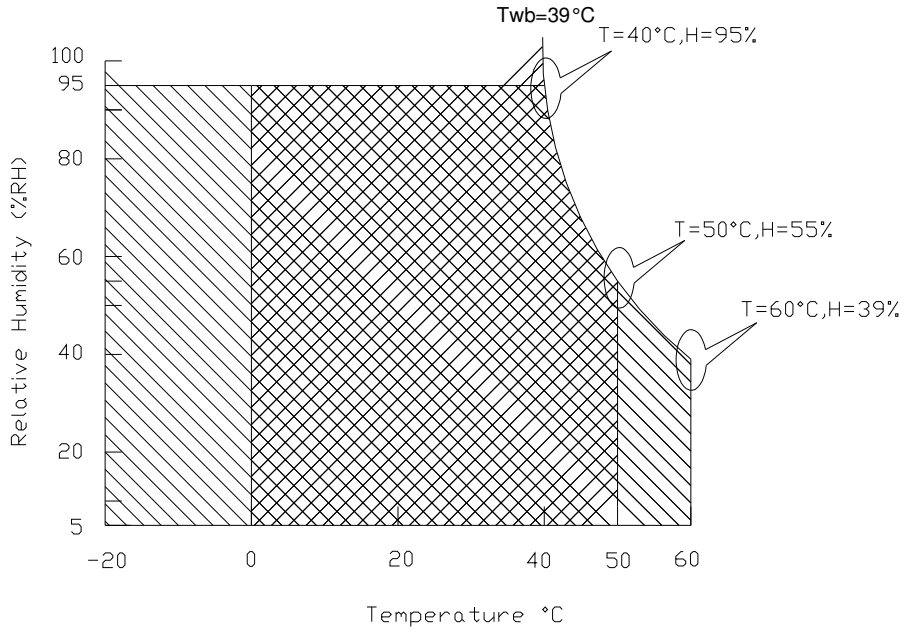
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

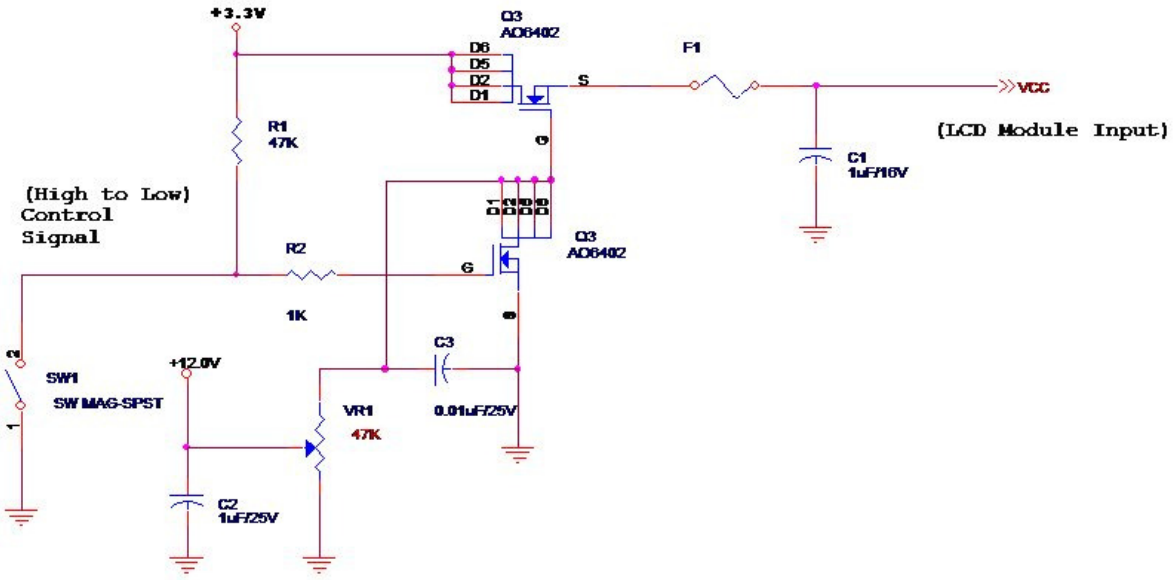
Input power specifications are as follows;

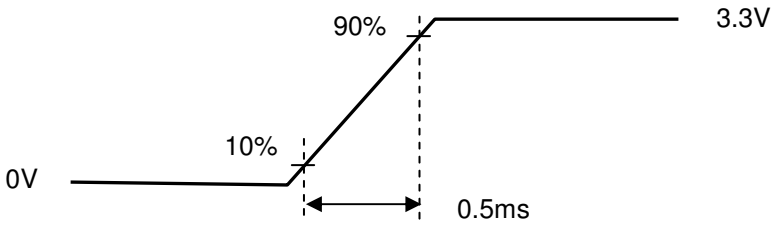
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.3	[Watt]	Note 1
IDD	IDD Current	-	-	360	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition





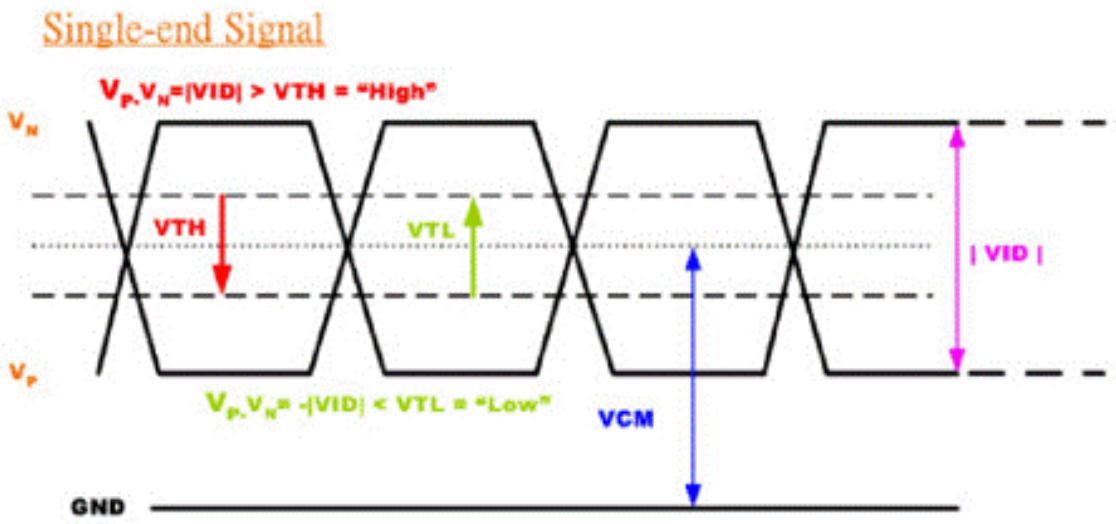
Vin rising time

5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
$\|V_{ID}\|$	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.1.3 Dynamic contrast ratio Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
Dynamic contrast ratio(DCR) Input High Level	DCR_EN	3.0	-	5.5	[Volt]	Define as Connector Interface (Ta=25℃)
Dynamic contrast ratio(DCR) Input Low Level		-	-	0.8	[Volt]	
DCR Mode Duty Index	Duty	70	-	100	%	Note 1
L0 Gray level	Power	0.45P	0.55P	0.65P	Watt	Note 2
L63 Gray level	Power	0.75P	0.85P	0.95P	Watt	

Note 1: The minimums dynamic contrast ratio is setting at darkness, and a maximum is setting at brightness.

Note 2: The power saving capability refer to original Backlight power consumption (P)

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.7	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

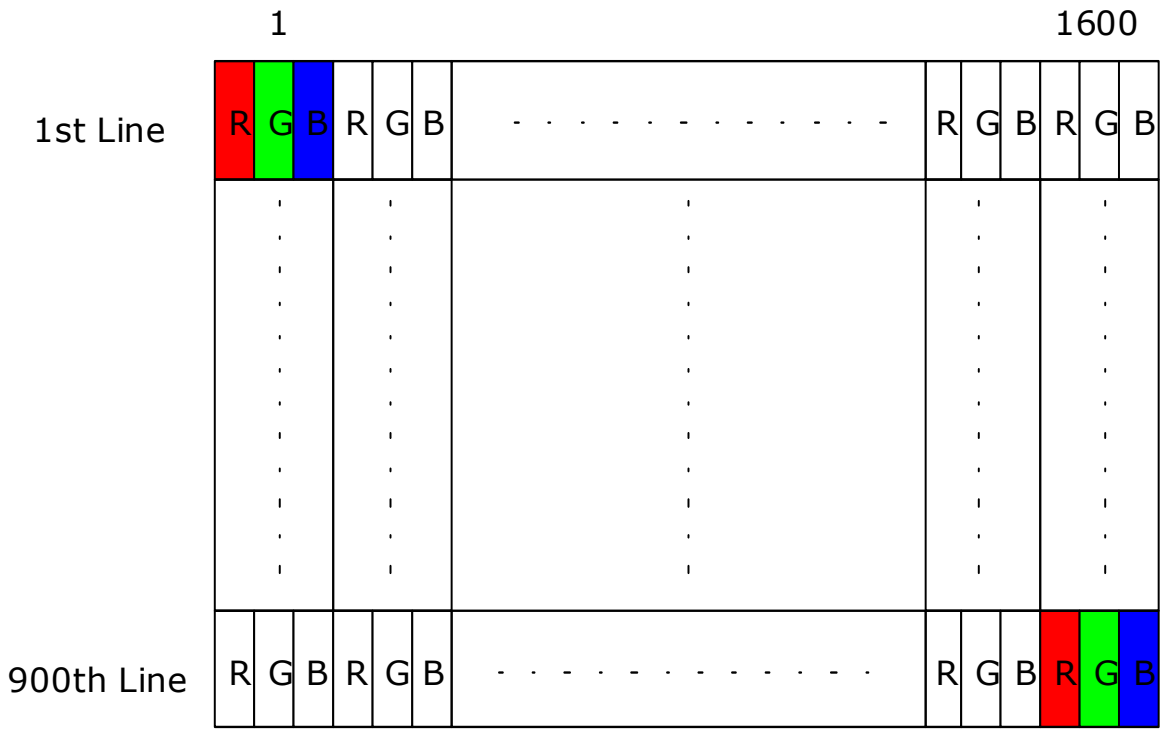
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1: Recommend system pull up/down resistor no bigger than 10kohm

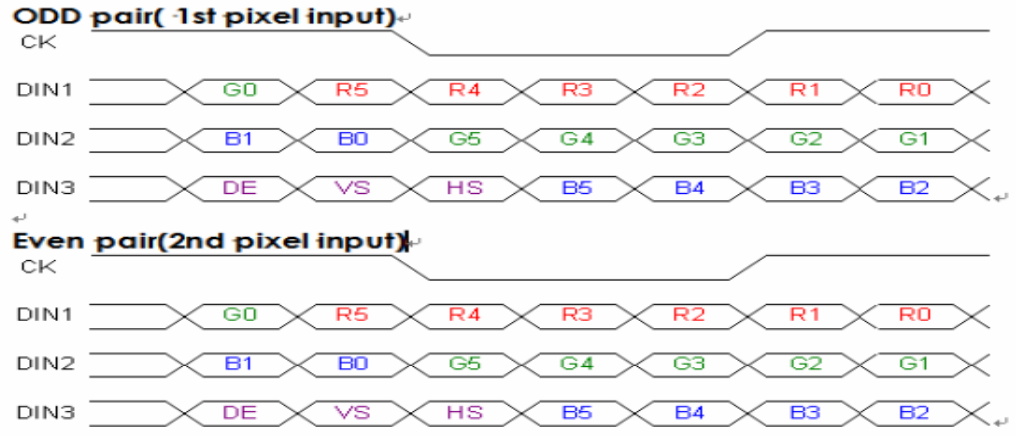
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	**IPEX or Compatiable**
Type / Part Number	**IPEX 20455-040E-12R or Compatiable**
Mating Housing/Part Number	**IPEX 20453-040T-11 or Compatiable**

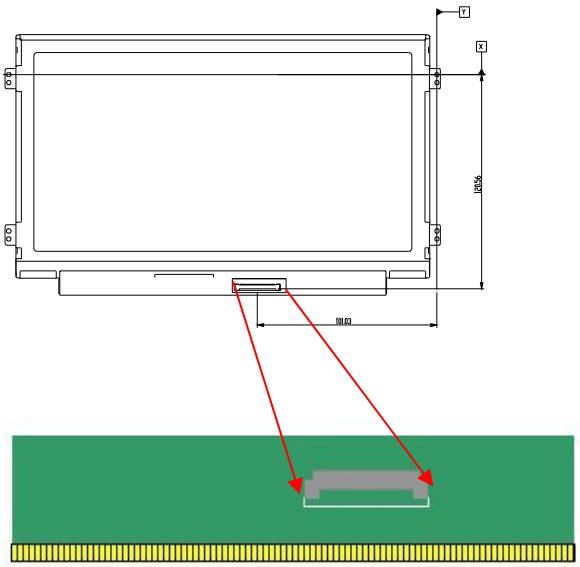
6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN #	SIGNAL NAME	DESCRIPTION
1	NC	No Connection (Reserve)
2	VDD	+ 3.3V Power Supply
3	VDD	+ 3.3V Power Supply
4	VEDID	+ 3.3V EDID Power
5	Test	Panel Self Test
6	CLKEDID	EDID Clock Input
7	DATAEDID	EDID Data Input
8	Odd_Rin0-	-LVDS Differential Data Input
9	Odd_Rin0+	+LVDS Differential Data Input
10	VSS	Power Ground
11	Odd_Rin1-	-LVDS Differential Data Input
12	Odd_Rin1+	+LVDS Differential Data Input
13	VSS	Power Ground
14	Odd_Rin2-	-LVDS Differential Data Input
15	Odd_Rin2+	+LVDS Differential Data Input
16	VSS	Power Ground
17	Odd_ClkIN-	-LVDS Differential Clock Input
18	Odd_ClkIN+	+LVDS Differential Clock Input
19	VSS	Ground
20	Even_Rin0-	-LVDS Differential Data Input

21	Even_Rin0+	+LVDS Differential Data Input
22	VSS	Power Ground
23	Even_Rin1-	-LVDS Differential Data Input
24	Even_Rin1+	+LVDS Differential Data Input
25	VSS	Power Ground
26	Even_Rin2-	-LVDS Differential Data Input
27	Even_Rin2+	+LVDS Differential Data Input
28	VSS	Power Ground
29	Even_ClkIN-	-LVDS Differential Clock Input
30	Even_ClkIN+	+LVDS Differential Clock Input
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	PWM logic input level
36	VLED_EN	LED enable input level
37	DCR_EN	Dynamic B/L Control enable(High enable)
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply

Note1: Input signals shall be low or High-impedance state when VDD is off.



Pin 40 **Pin 1**

6.4 Interface Timing

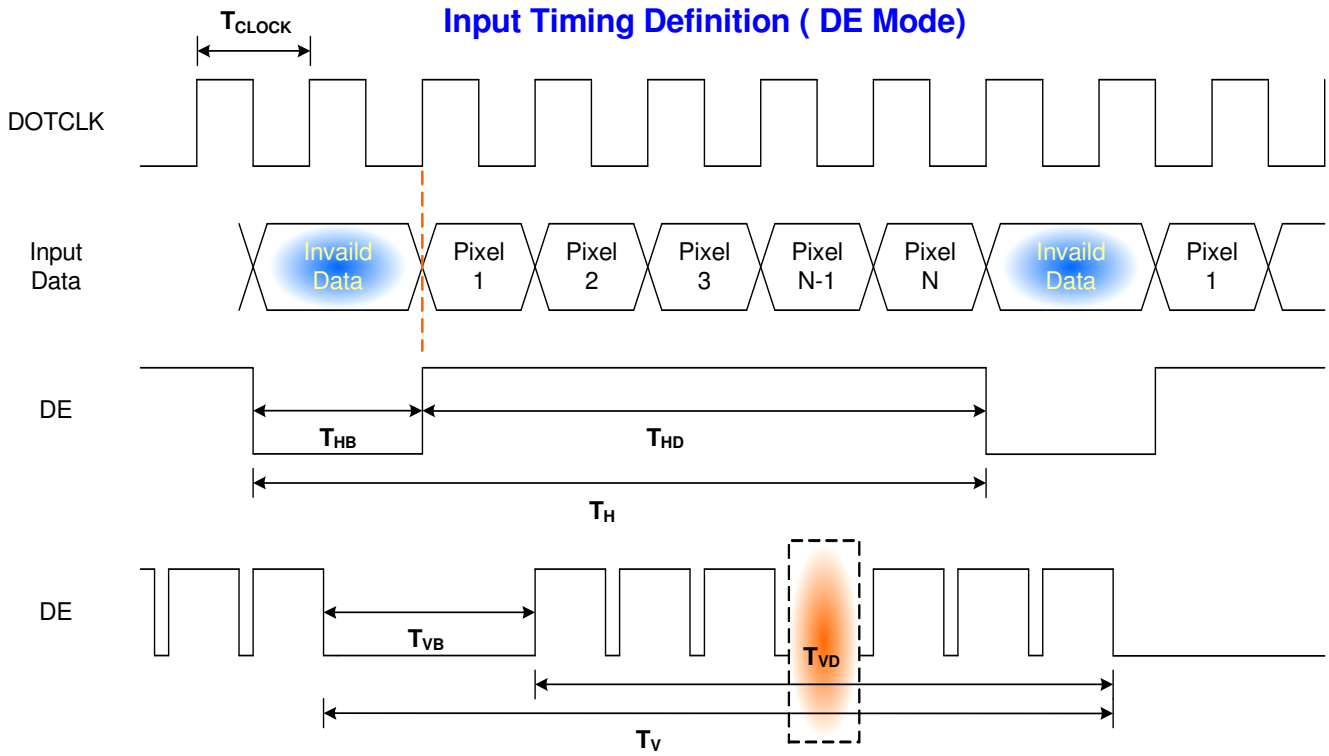
6.4.1 Timing Characteristics

Basically, interface timings should match the 1600x900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T_{Clock}		55		MHz
Vertical Section	Period	T_V	908	916	2047	T_{Line}
	Active	T_{VD}		900		
	Blanking	T_{VB}	8	16	1147	
Horizontal Section	Period	T_H	850	1080	2047	T_{Clock}
	Active	T_{HD}		800		
	Blanking	T_{HB}	50	280	1247	

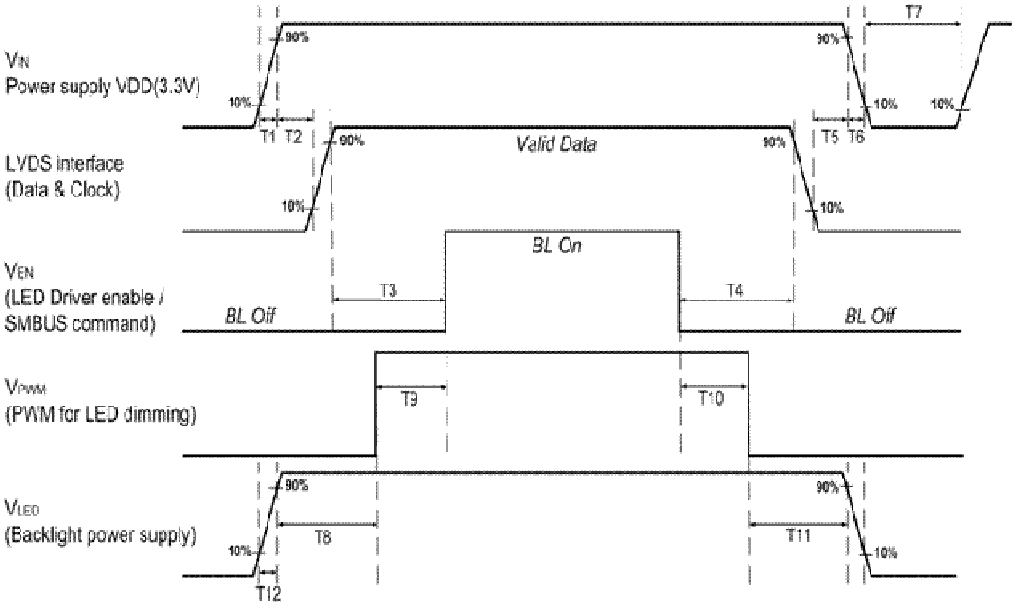
Note : DE mode only

6.4.2 Timing diagram

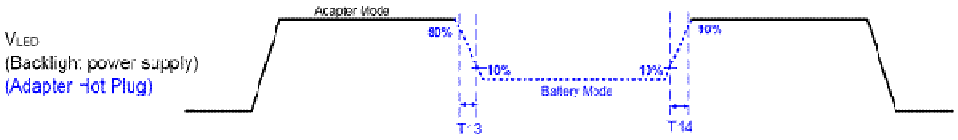


6.5 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below:



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	50	
T3	200	-	
T4	200	-	
T5	0	50	
T6	0	10	
T7	500	-	
T8	10	-	
T9	10	-	
T10	10	-	
T11	10	-	
T12	0.5	10	
T13	1	-	
T14	1	-	

Seamless change: T13/T14 = 5xT_{PWM}

T_{PWM}= 1/PWM Frequency

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	**Ta= 40℃, 90%RH, 300h**	
High Temperature Operation	**Ta= 50℃, Dry, 300h**	
Low Temperature Operation	**Ta= 0℃, 300h**	
High Temperature Storage	**Ta= 60℃, 35%RH, 300h**	
Low Temperature Storage	**Ta= -20℃, 50%RH, 250h**	
Thermal Shock Test	**Ta=-20℃to 60℃, Duration at 30 min, 100 cycles**	
ESD	**Contact : ±8 KV** **Air : ±15 KV**	Note 1

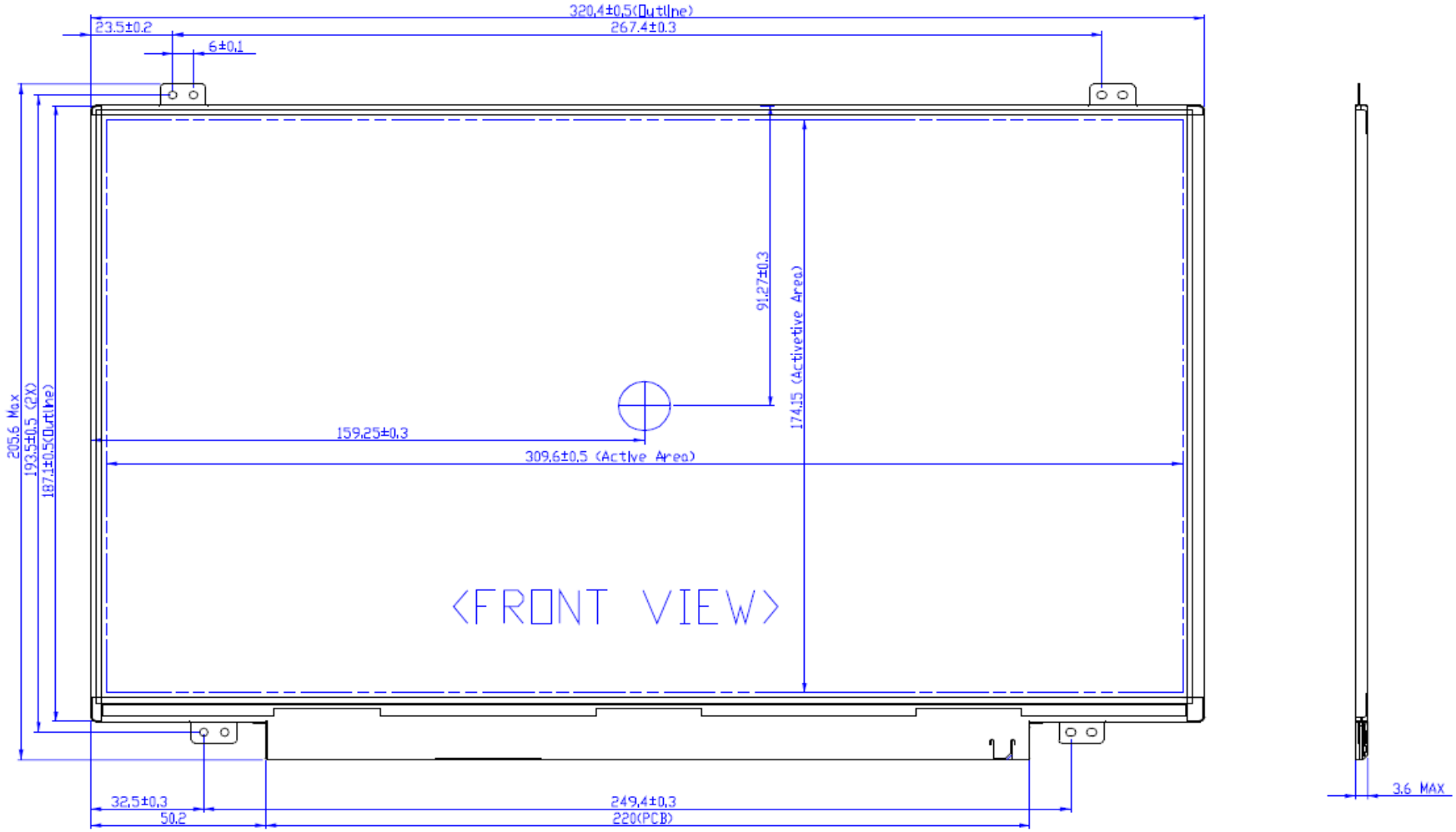
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

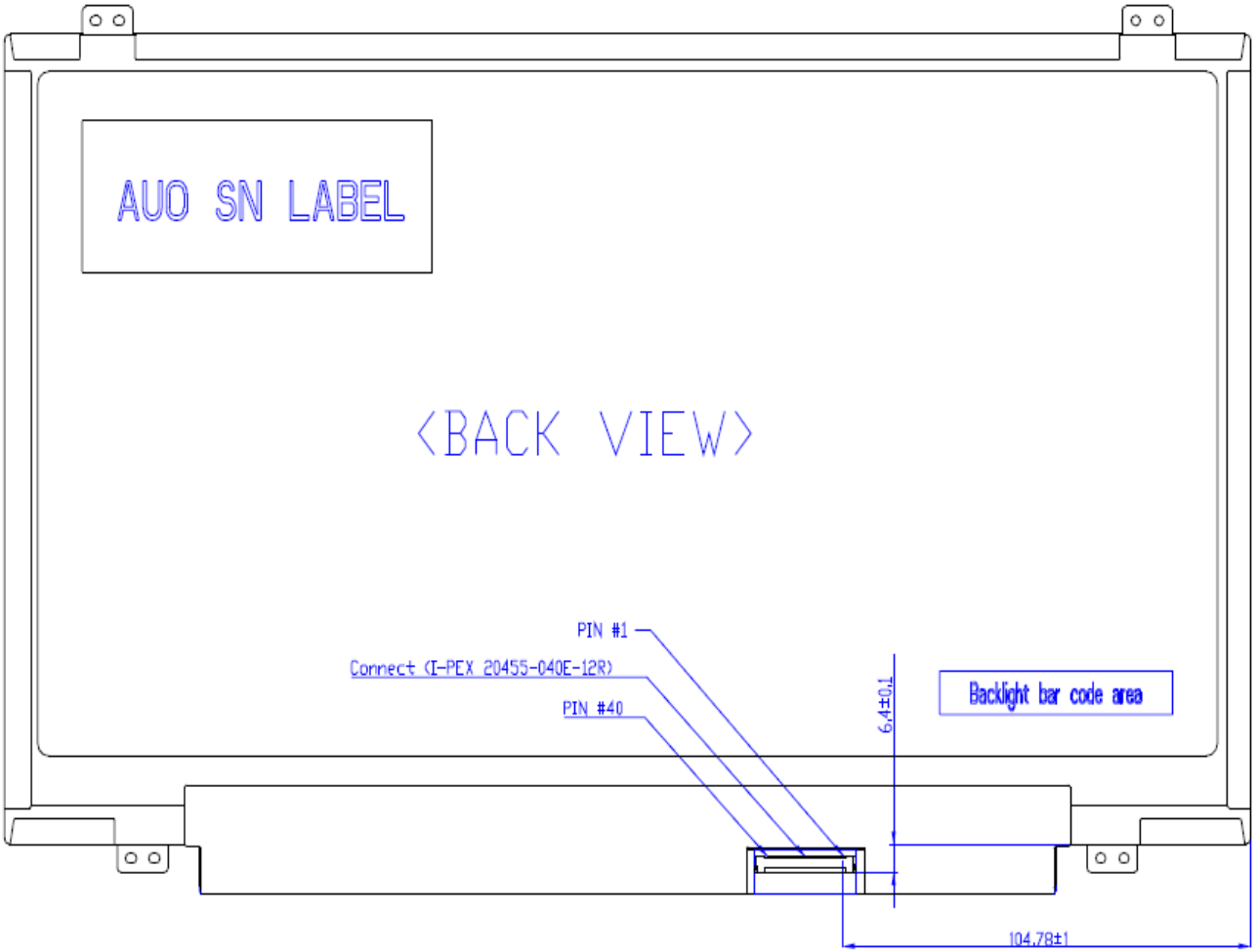
8. Mechanical Characteristics

8.1 LCM Outline Dimension

Front View



Back View



Note: Prevention IC damage, IC positions not allowed any overlap over these area

9. Shipping and Package

9.1 Shipping /Carton Label Format

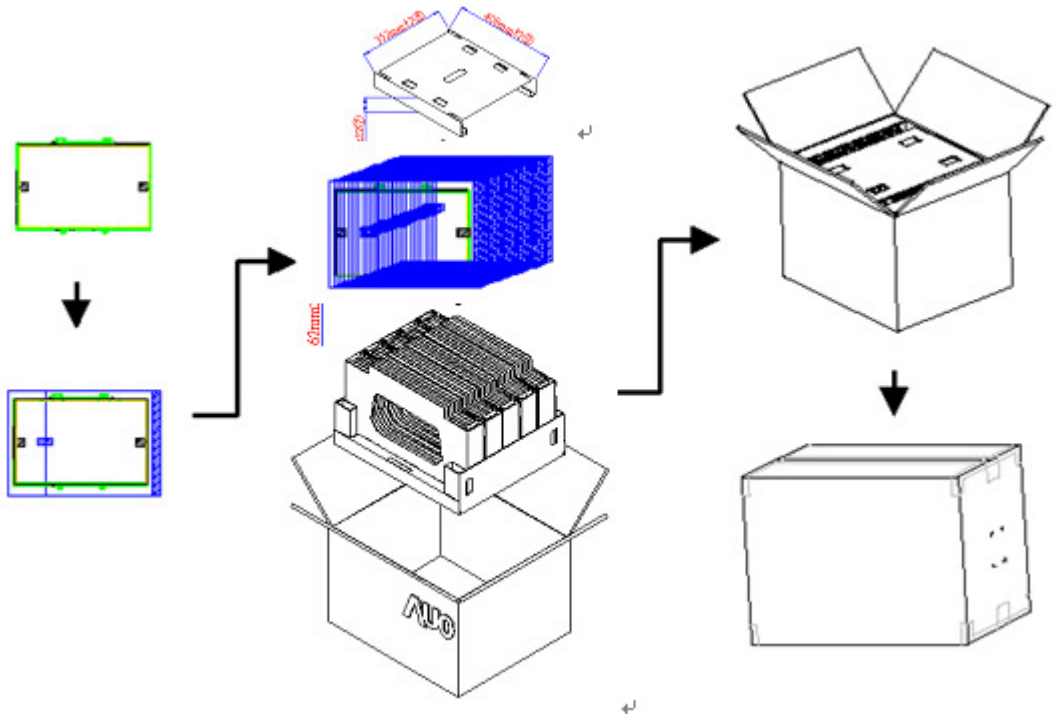
9.2 Definition of customer PPID Label and Revision Code

Please refer to the Dell Part identification Label Specification, Number:13190

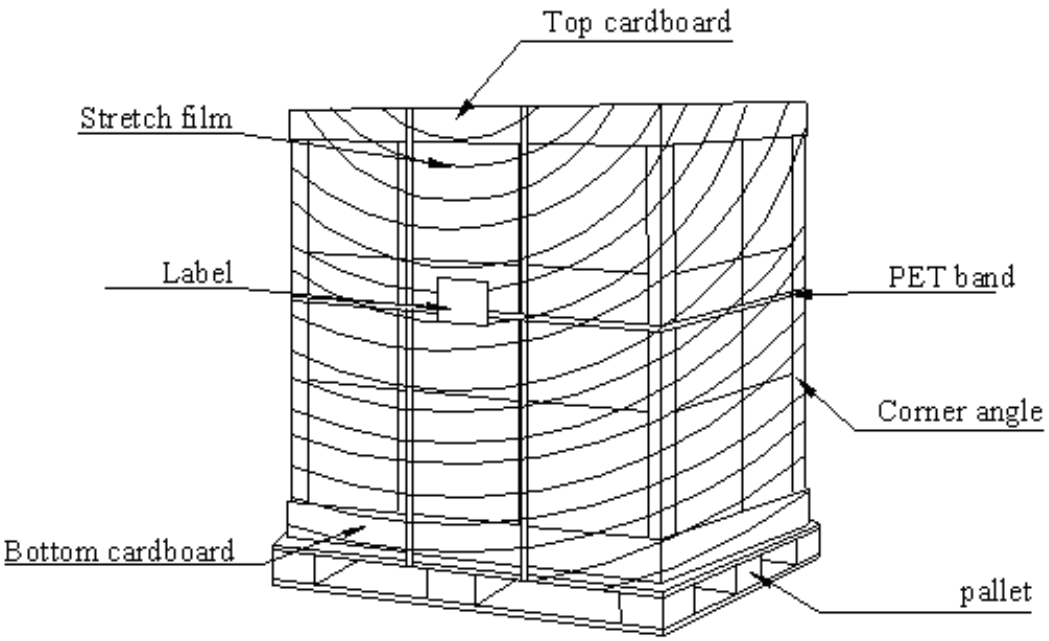
Build Name(s):	PPID Revision Code(s):
Sub System Test (SST) Working Sample (WS) ENG 2	X00, X01, X02, …, X0n
Product Test (PT) Engineering Sample (ES) ENG 3	X10, X11, X12, …, X1n
System Test (ST) Customer Sample (CS) ENG 4	X20, X21, X22, … X2n
X-Build (XB) Mass Production (MP) ENG 5	A00, A01, A02, … A0n

9.2 Carton Package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
0	Header	00	00000000	0
1	Header	FF	11111111	255
2	Header	FF	11111111	255
3	Header	FF	11111111	255
4	Header	FF	11111111	255
5	Header	FF	11111111	255
6	Header	FF	11111111	255
7	Header	00	00000000	0
8	EISA manufacture code = 3 Character ID	06	00000110	6
9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
0A	Panel Supplier Reserved – Product Code	3E	00111110	62
0B	Panel Supplier Reserved – Product Code	21	00100001	33
0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	15	00010101	21
12	EDID structure version # = 1	01	00000001	1
13	EDID revision # = 4	04	00000100	4
14	Video I/P definition	90	10010000	144
15	Max H image size (Rounded to cm)	1F	00011111	31
16	Max V image size (Rounded to cm)	11	00010001	17
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
18	Feature support	02	00000010	2
19	Red/Green Low bit (RxRy/GxGy)	61	01100001	97
1A	Blue/White Low bit (BxBy/WxWy)	95	10010101	149
1B	Red X	9C	10011100	156
1C	Red Y	59	01011001	89
1D	Green X	52	01010010	82
1E	Green Y	8F	10001111	143
1F	Blue X	26	00100110	38
20	Blue Y	21	00100001	33
21	White X	50	01010000	80
22	White Y	54	01010100	84
23	Established timings 1 (00h if not used)	00	00000000	0
24	Established timings 2 (00h if not used)	00	00000000	0

25	Manufacturer's timings (00h if not used)	00	00000000	0
26	Standard timing ID1 (01h if not used)	01	00000001	1
27	Standard timing ID1 (01h if not used)	01	00000001	1
28	Standard timing ID2 (01h if not used)	01	00000001	1
29	Standard timing ID2 (01h if not used)	01	00000001	1
2A	Standard timing ID3 (01h if not used)	01	00000001	1
2B	Standard timing ID3 (01h if not used)	01	00000001	1
2C	Standard timing ID4 (01h if not used)	01	00000001	1
2D	Standard timing ID4 (01h if not used)	01	00000001	1
2E	Standard timing ID5 (01h if not used)	01	00000001	1
2F	Standard timing ID5 (01h if not used)	01	00000001	1
30	Standard timing ID6 (01h if not used)	01	00000001	1
31	Standard timing ID6 (01h if not used)	01	00000001	1
32	Standard timing ID7 (01h if not used)	01	00000001	1
33	Standard timing ID7 (01h if not used)	01	00000001	1
34	Standard timing ID8 (01h if not used)	01	00000001	1
35	Standard timing ID8 (01h if not used)	01	00000001	1
36	Pixel Clock/10,000 (LSB)	F8	11111000	248
37	Pixel Clock/10,000 (MSB)	2A	00101010	42
38	Horizontal Active (lower 8 bits)	40	01000000	64
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	76	01110110	118
3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	61	01100001	97
3B	Vertical Active	84	10000100	132
3C	Vertical Blanking (Tvbp) (DE Blanking typ. for DE only panels)	1C	00011100	28
3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
3E	Horizontal Sync, Offset (Thfp)	40	01000000	64
3F	Horizontal Sync, Pulse Width	2A	00101010	42
40	Vertical Sync, Offset (Tvfp) Sync Width	33	00110011	51
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
42	Horizontal Image Size	35	00110101	53
43	Vertical image Size	AE	10101110	174
44	Horizontal Image Size / Vertical image size	10	00010000	16
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	1A	00011010	26
48	Pixel Clock/10,000 (LSB)	A5	10100101	165
49	Pixel Clock/10,000 (MSB)	1C	00011100	28
4A	Horizontal Active = xxxx pixels (lower 8 bits)	40	01000000	64

4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	76	01110110	118
4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	61	01100001	97
4D	Vertical Active = xxxx lines	84	10000100	132
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	1C	00011100	28
4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	40	01000000	64
51	Horizontal Sync, Pulse Width = xxxx pixels	2A	00101010	42
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	33	00110011	51
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
54	Horizontal Image Size =xxx mm	35	00110101	53
55	Vertical image Size = xxx mm	AE	10101110	174
56	Horizontal Image Size / Vertical image size	10	00010000	16
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
5A	Flag	00	00000000	0
5B	Flag	00	00000000	0
5C	Flag	00	00000000	0
5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
5E	Flag	00	00000000	0
5F	Dell P/N 1st Character	56	01010110	86
60	Dell P/N 2nd Character	33	00110011	51
61	Dell P/N 3rd Character	59	01011001	89
62	Dell P/N 4th Character	48	01001000	72
63	Dell P/N 5th Character	46	01000110	70
64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	80	10000000	128
65	Manufacturer P/N	42	01000010	66
66	Manufacturer P/N	31	00110001	49
67	Manufacturer P/N	34	00110100	52
68	Manufacturer P/N	30	00110000	48
69	Manufacturer P/N	52	01010010	82
6A	Manufacturer P/N	54	01010100	84

6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	4E	01001110	78
6C	Flag	00	00000000	0
6D	Flag	00	00000000	0
6E	Flag	00	00000000	0
6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
70	Flag	00	00000000	0
71	Color Management	00	00000000	0
72	Panel Structure	41	01000001	65
73	Frame Rate	21	00100001	33
74	Light Controller Interface and Luminance	9E	10011110	158
75	Outdoor Features	01	00000001	1
76	Multi-Media Features	10	00010000	16
77	Multi-Media Features	00	00000000	0
78	Special Features #1	00	00000000	0
79	Special Features #2	02	00000010	2
7A	Special Features #3	01	00000001	1
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	BB	10111011	187