(✓) Preliminary Specifications
( ) Final Specifications

Module	**15.6" (15.55") FHD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B156HAN09.0 (H/W:0A)
Note ( )	*LED Backlight with driving circuit design*

Customer	**Date**	**Approved by**	**Date**
Checked & Approved by	**Date**	**Prepared by**	**Date**
			2018/11/02
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2018/06/14	All	First Edition for Customer		
0.2 2018/08/13	P.5	Surface Treatment: Anti Glare	Glare	
	P.18	Update CN type :IPEX 20765-030E-02	IPEX 20765-030E-11A	
	P.25 ,26		Update Drawing	
0.3 2018/11/02	P.5	Electrical Interface eDP1.4	Electrical Interface eDP1.4	
	P.25 ,26		Update Drawing	
	P.27		Update Label	
	P.30		Update EDID	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B156HAN09.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B156HAN09.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

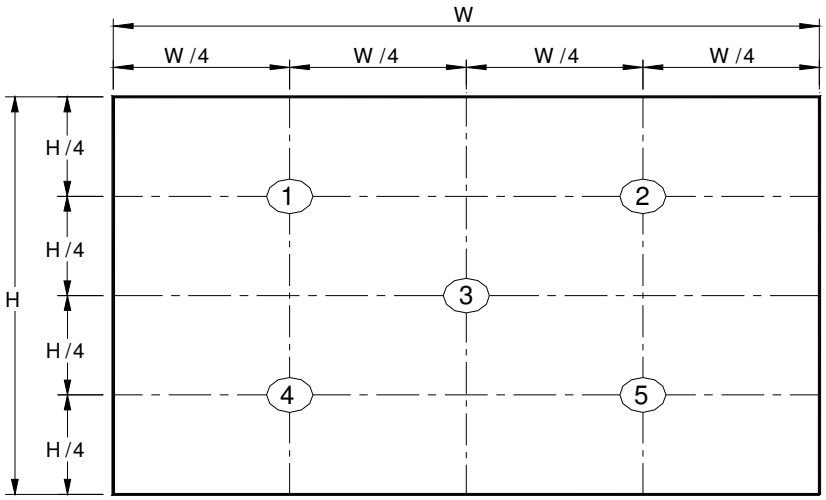
Items	**Unit**	**Specifications**			
Screen Diagonal	[mm]	394.9			
Active Area	[mm]	344.16 x 193.59			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.17925 x 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (ILED= TBDmA) **(Note: ILED is LED current)**	[cd/m^2]	400 typ. (5 points average) 340 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1200:1 typ			
Response Time	[ms]	30 Typ			
Nominal Input Voltage VDD	[Volt]	+3.3 min			
Power Consumption	[Watt]	2.45 W			
Weight	[Grams]	310 max.			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	348.86	349.16	349.46
		Width	214.90	215.40	215.90
Thicknessss		Thicknessss	2.6 max(Panel side)		
Electrical Interface		2 Lane eDP1.4			
Glass Thickness	[mm]	0.3			
Surface Treatment		Glare			
Support Color		16.7M colors (RGB 8-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

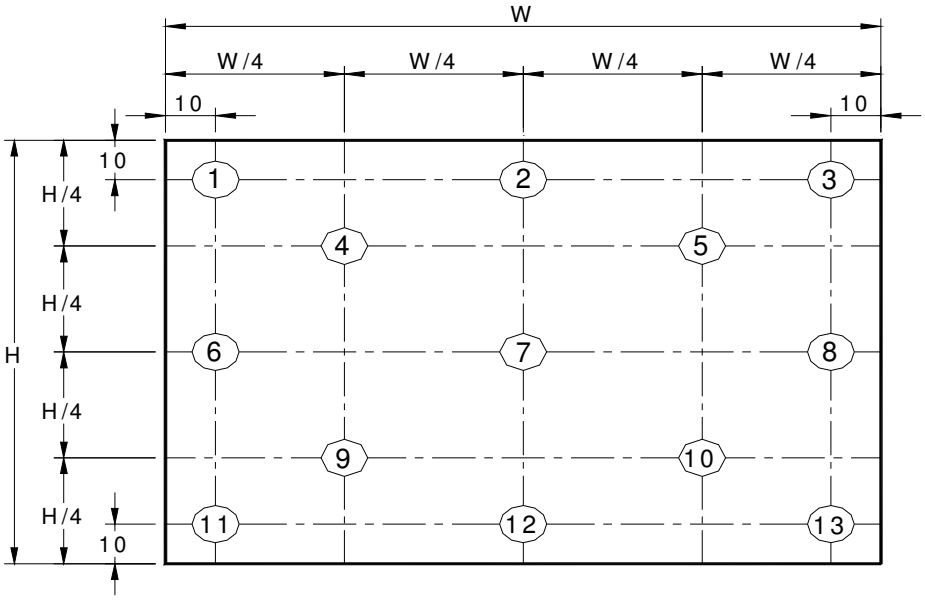
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=TBDmA			5 points average	340	400	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80 80	85 85	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio		CR		-	1200	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	30	35		4,8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	TBD	TBD	TBD		4
		Ry		TBD	TBD	TBD		
	Green	Gx		TBD	TBD	TBD		
		Gy		TBD	TBD	TBD		
	Blue	Bx		TBD	TBD	TBD		
		By		TBD	TBD	TBD		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
sRGB		%		-	100	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

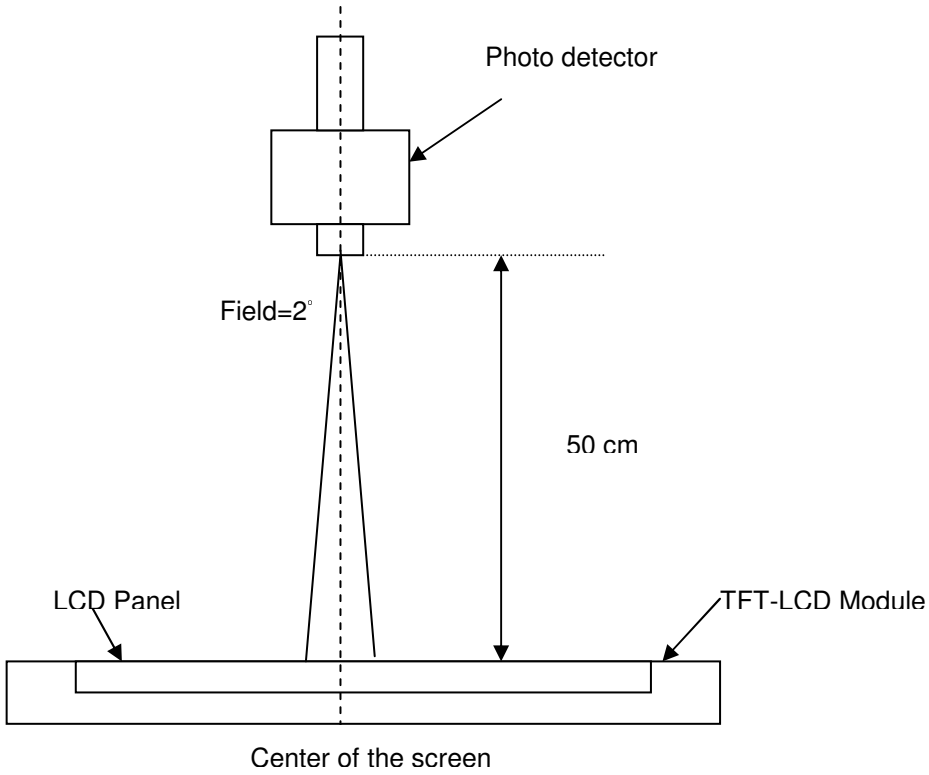
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the

center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

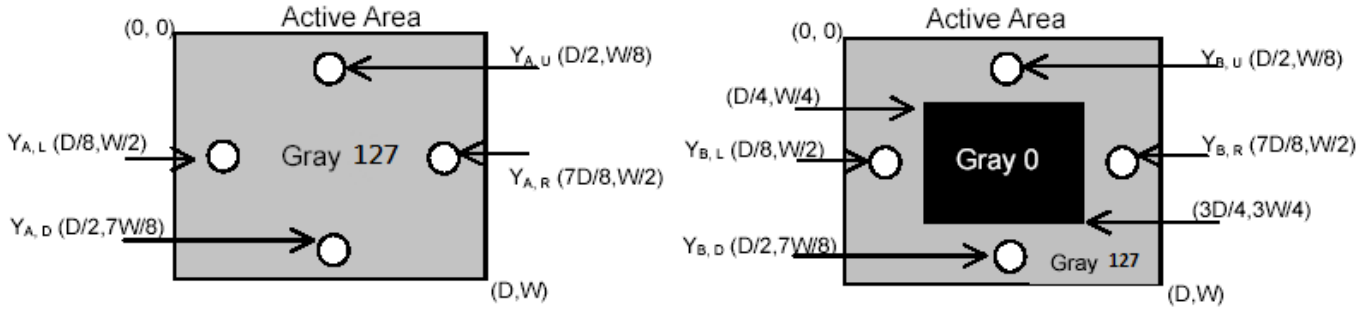
Note 7： Definition of Cross Talk (CT)

CT = | YB – YA | / YA × 100 (%)

Where

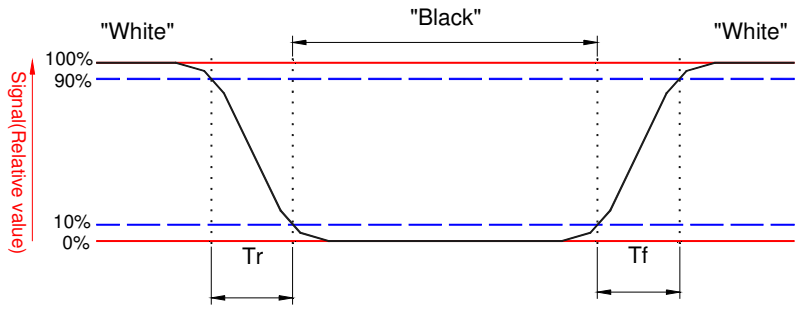
YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



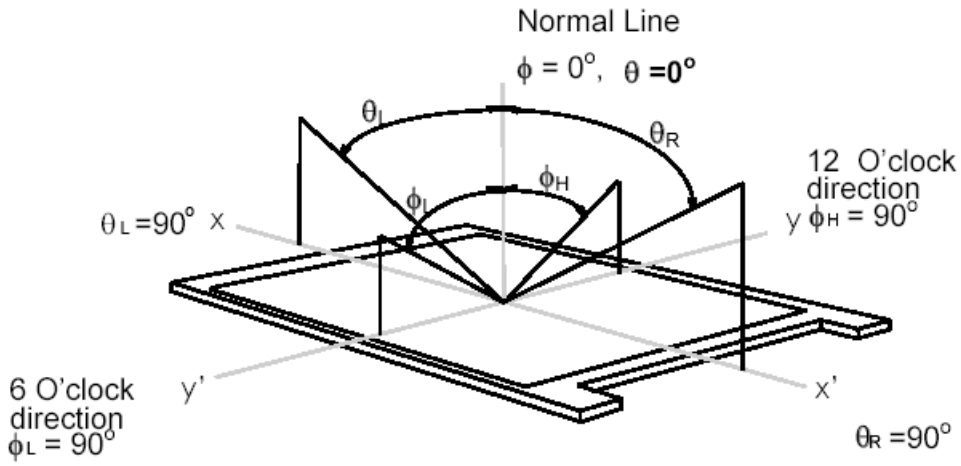
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



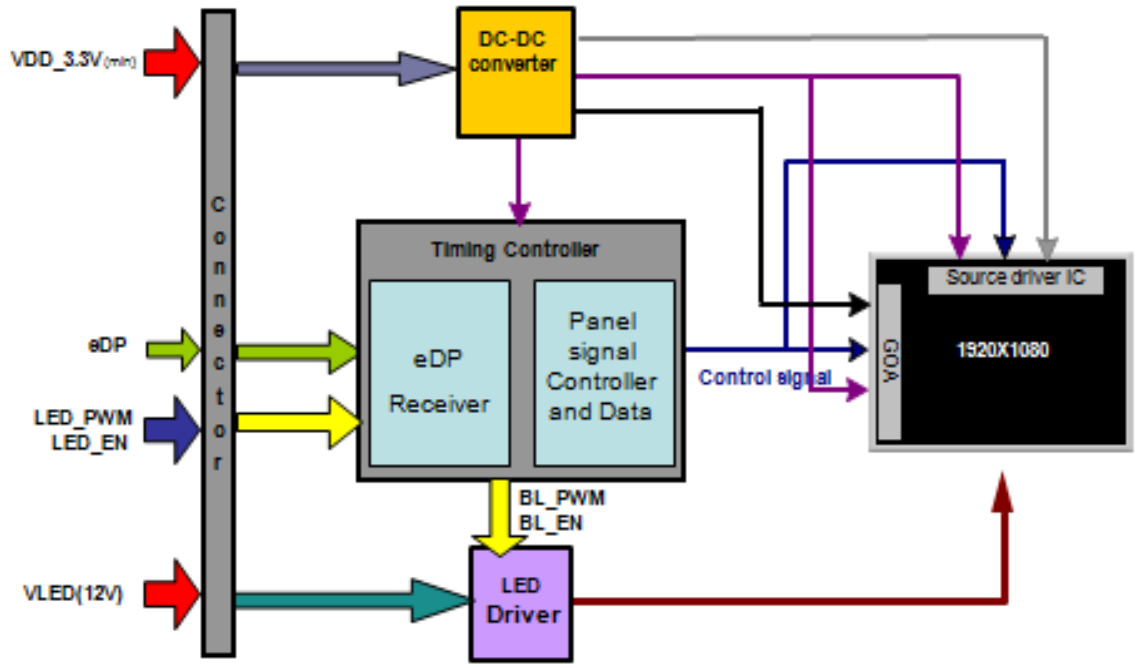
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 30 Pin (One CH/connector Module)



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

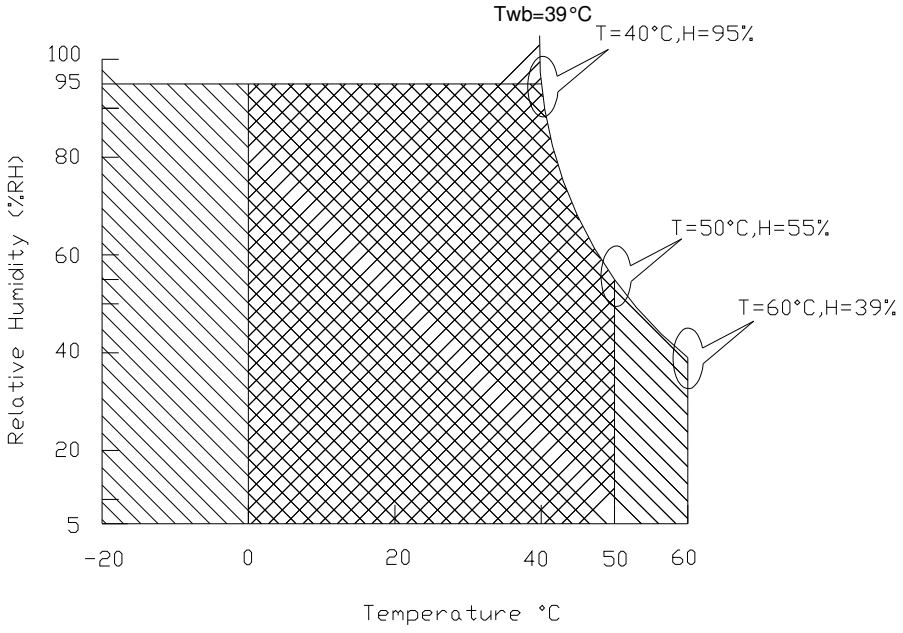
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

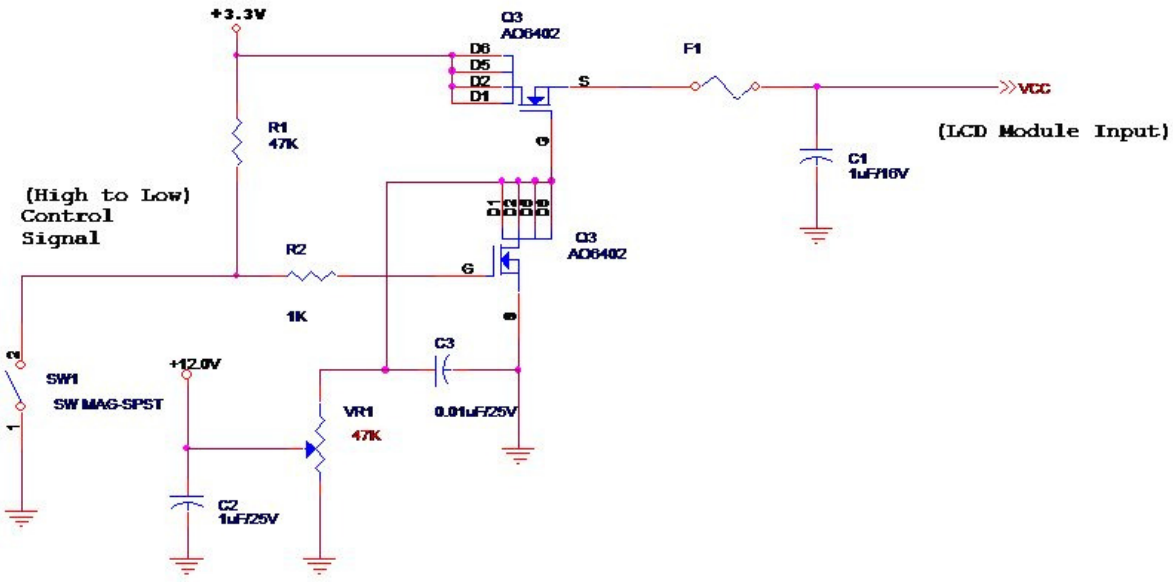
The power specification are measured under 25℃ and frame frenquency under 60Hz.

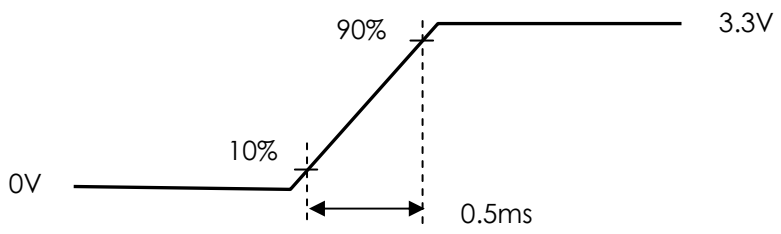
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.45	2.1	[Watt]	Note 1
IDD	IDD Current	-	-	700	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : PDD(typ)@ mosaic pattern Maximum Power; PDD(Max)@ R/G/B pattern Maximum Power

IDD(Max)=PDD(Max) / VDD(Min)

Note 2 : Measure Condition





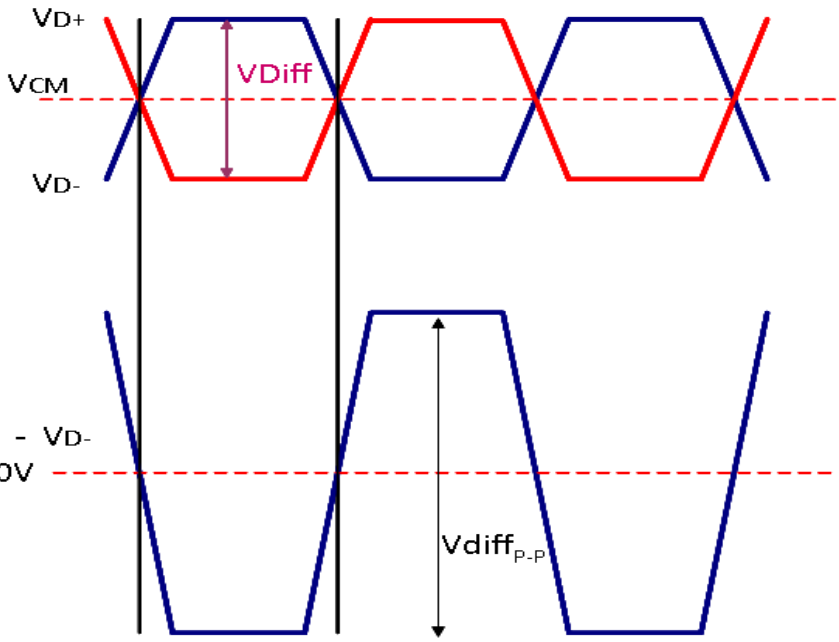
5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

Display Port main link signal:

Differential pair VD+ , VD-
Which is one Display port
Main link

VCM of Display port
Main link



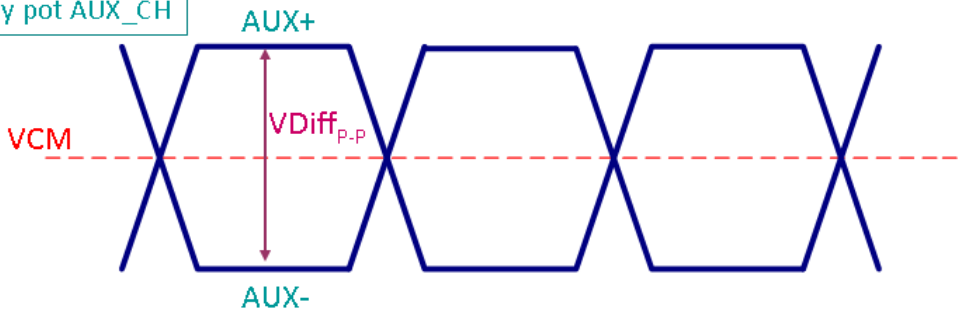
$Vdiff_{P-P} = [(VD+) - (VD-)] \times 2$

Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	75		1320	mV

Follow as VESA display port standard V1.4

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display pot AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Follow as VESA display port standard V1.3

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	V

Follow as VESA display port standard V1.3

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.0	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=TBD mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

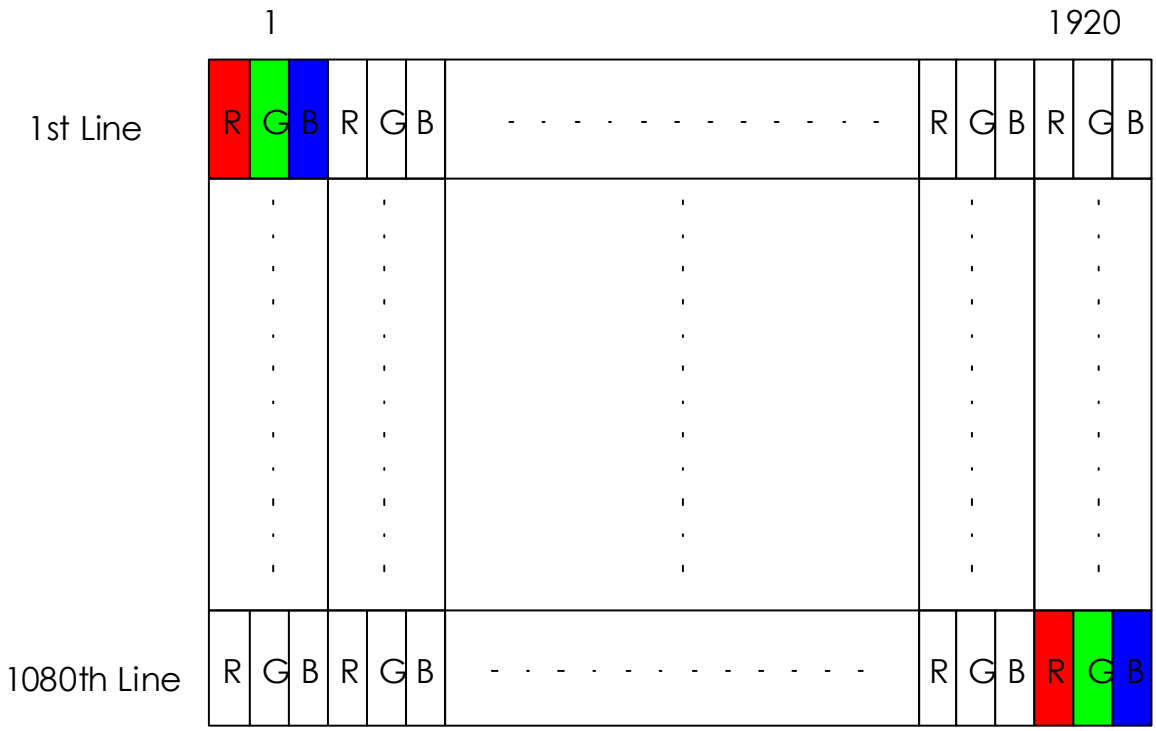
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20765-030E-11A or compatible
Mating Housing/Part Number	IPEX 20453-030T-01 or compatible

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Symbol	Function
1	NC	No Connect (Reserved)
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signale pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	No Connect (Reserved)
25	NC	No connect (Reserved)

26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No Connect (Reserved)

Note1：start from right side
Note2：Input signals shall be low or High-impedance state when VDD is off.

6.3 Interface Timing

For normal display, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

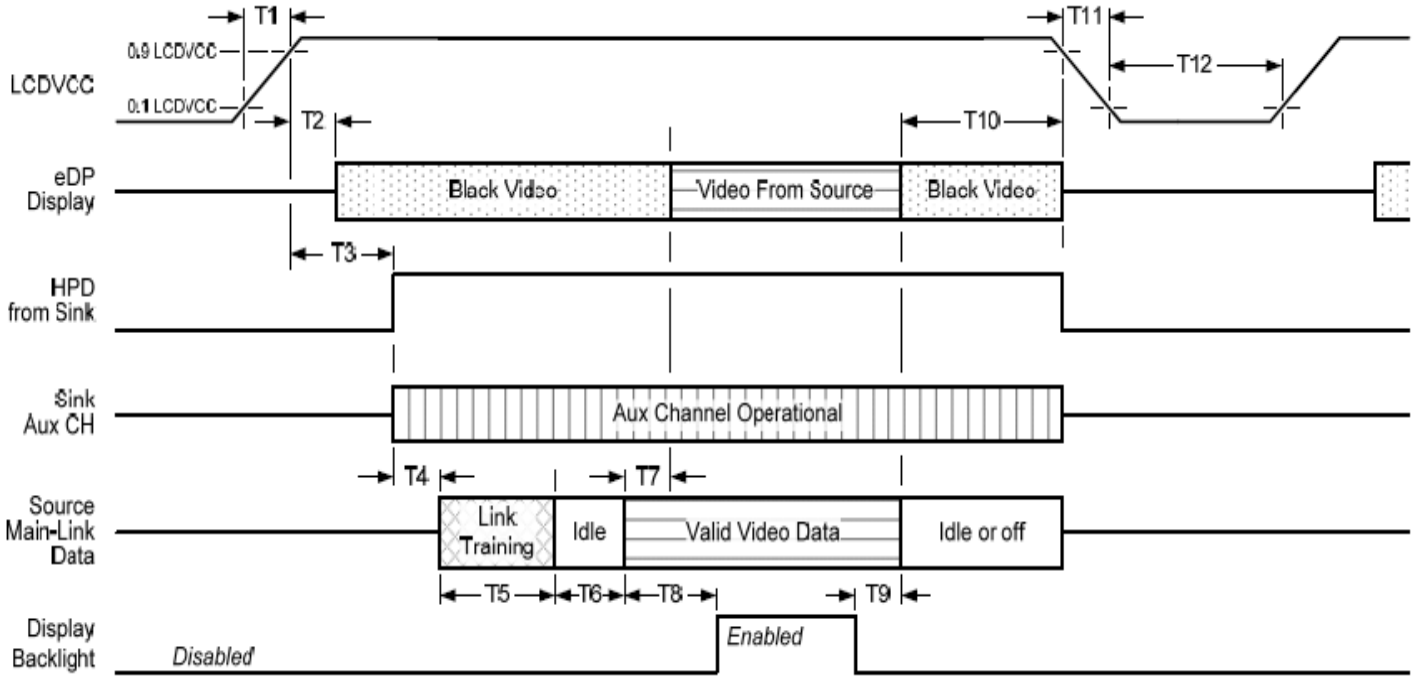
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	140	141	150	MHz
Vertical Section	Period	T_V	1110	1118	1080+A	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	30	38	A	
Horizontal Section	Period	T_H	2072	2100	1920+B	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	180	180	B	

Note 1 : The above is as optimized setting
Note 2 : The maximum clock frequency =(1920+B)*(1080+A)*60=75MHz

6.4 Power ON/OFF Sequence

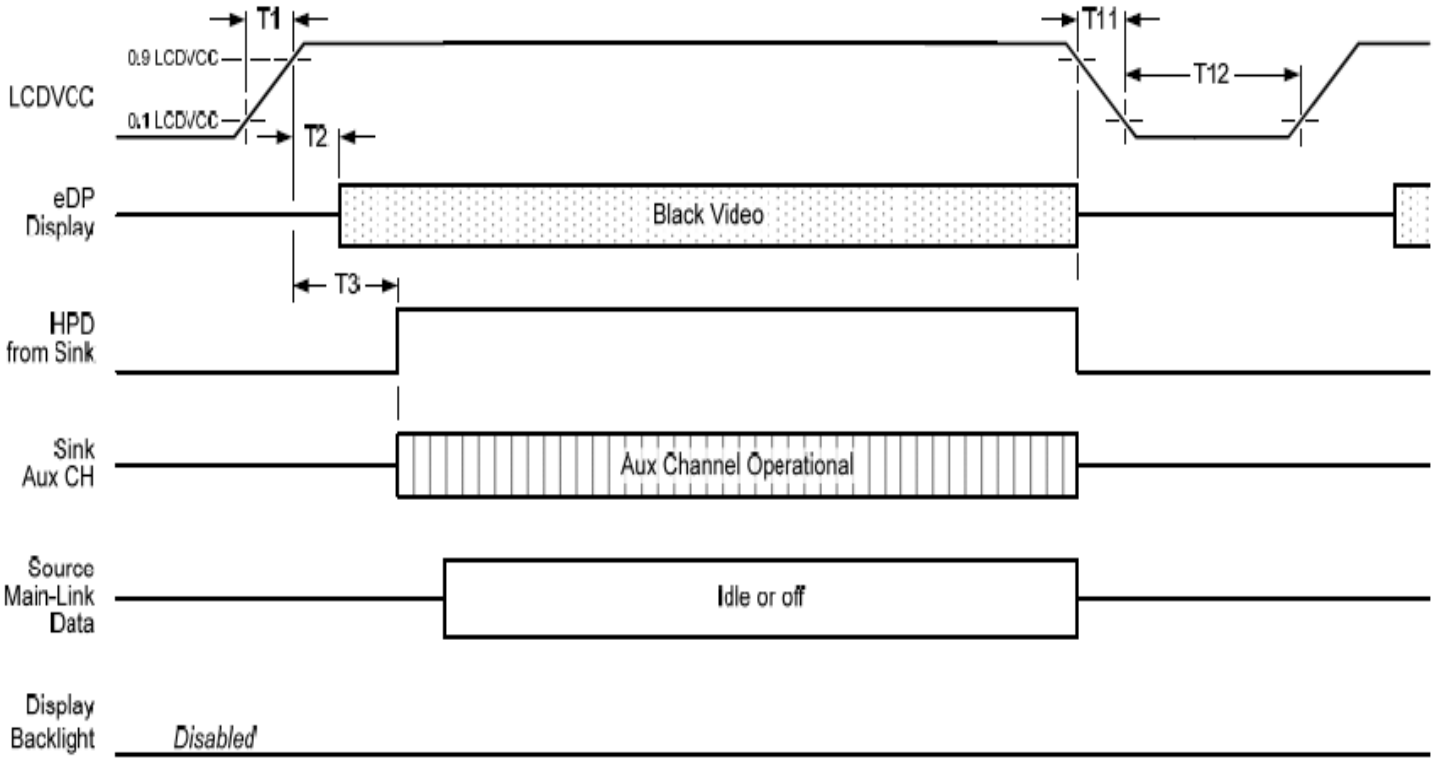
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

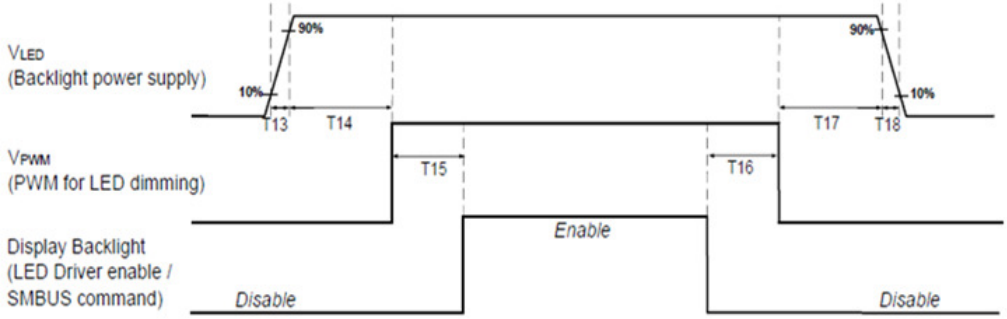
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

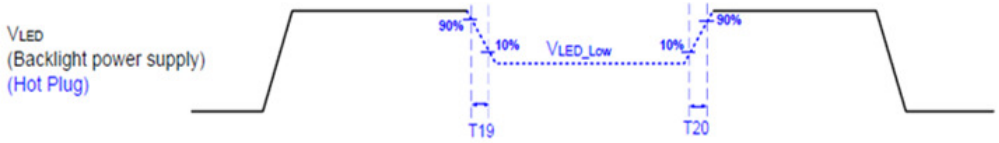


	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta=0℃, 300h	
High Temperature Storage	Ta= 60℃, 300h	
Low Temperature Storage	Ta= -20℃, 250h	
Thermal Shock Test	Ta=-20℃(30min) ~60℃(30min), 100cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

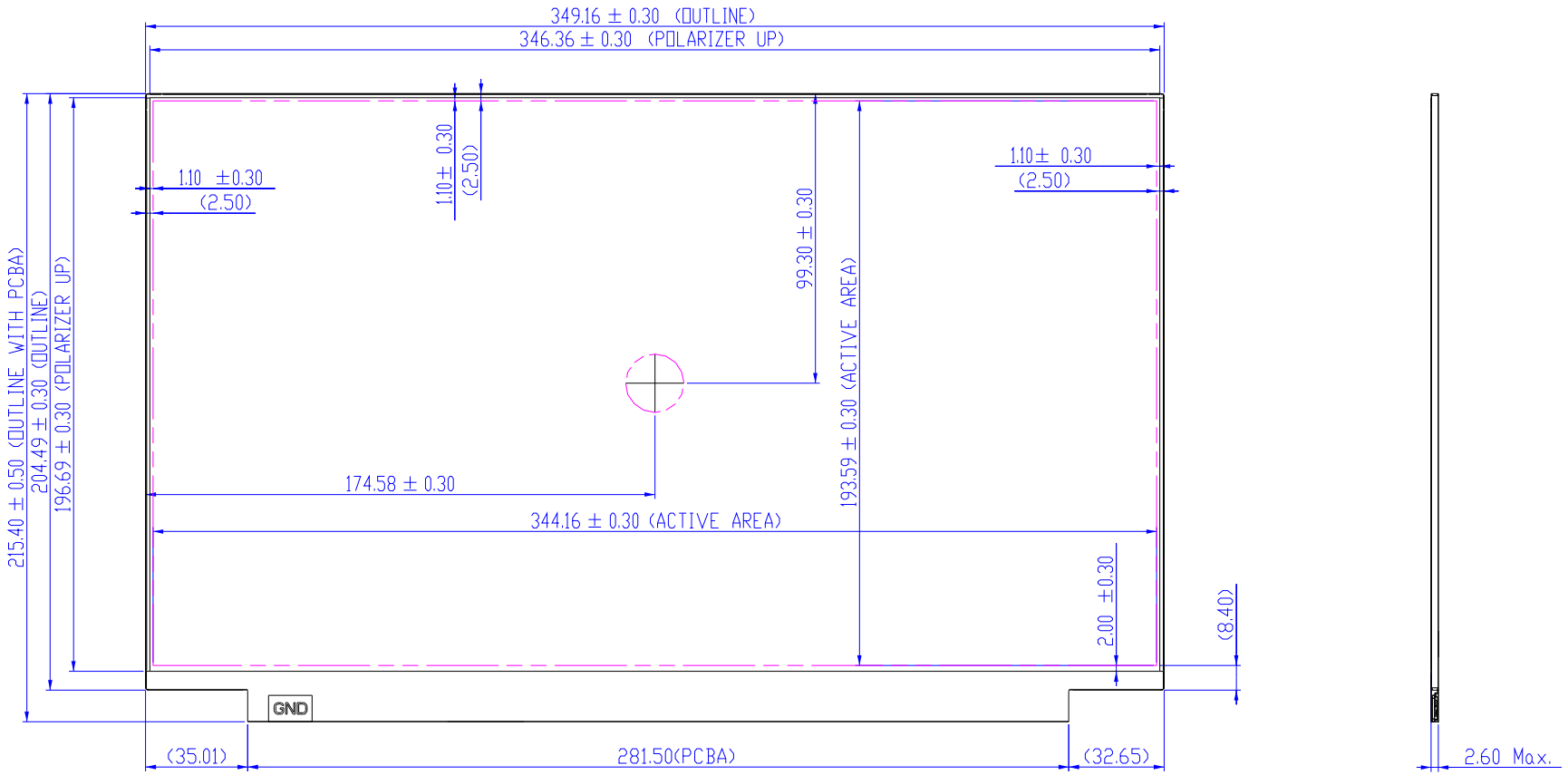
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

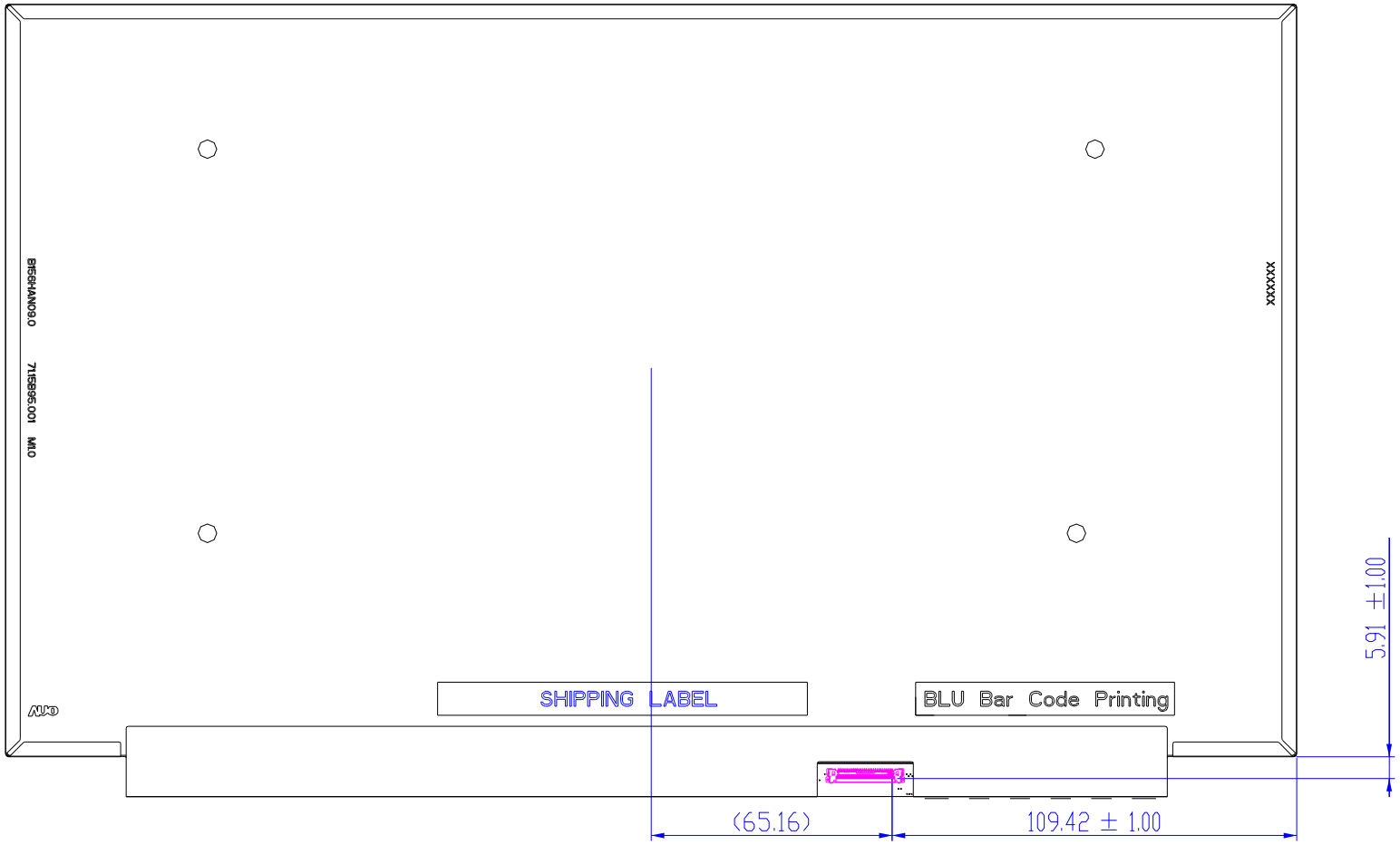
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Rear View

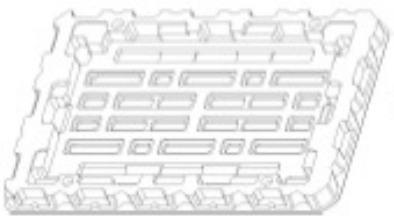


9. Shipping and Package

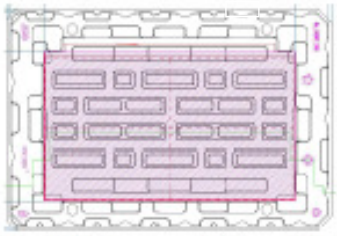
9.1 Shipping Label Format

9.2 Carton Package

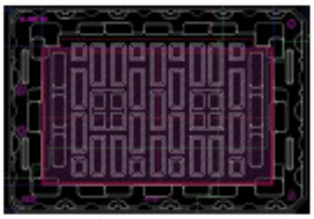
1、取出 PP 瓦楞



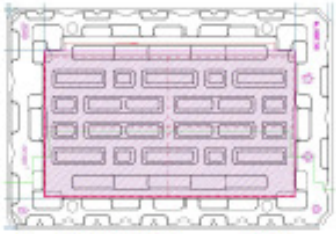
2、Tray 置放於 PP 瓦楞板上



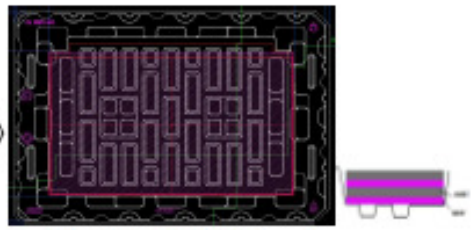
3、第一层 EPE spacer 放於 tray 盤上



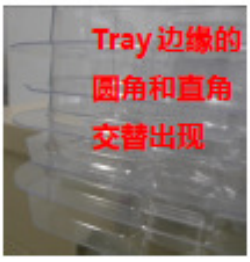
4、第一层 Panel 放於 Spacer 上, CF 面朝上



5、第二层 EPE spacer 放於第一层 Panel 上



6、第二层 Panel 放於 Spacer 上, CF 面朝上

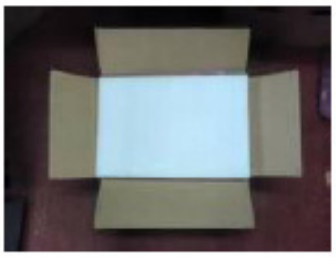


7、Tray 旋转堆叠
(Panel 共 26 片,最上面第 14 個 tray 是空的)

8、完成堆疊的 tray 放入靜電袋中, 並使用 tape 封口

9、EPE cushion 放入紙箱

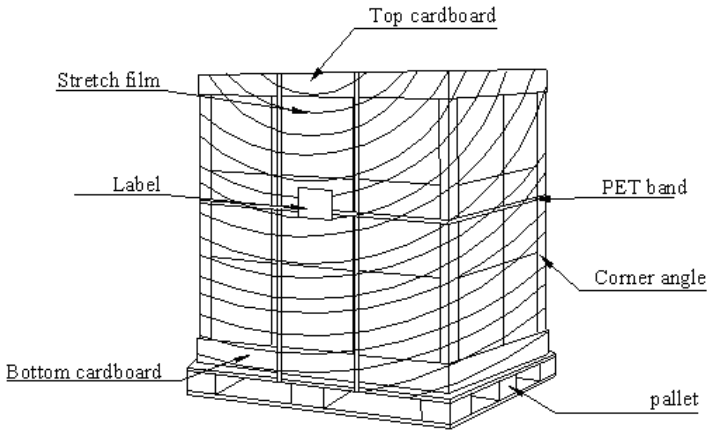
10、將包好靜電袋的 tray 整落放入紙箱中



11、放入 EPE cushion

12、Tape 封紙箱

9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	ED	11101101	237	
0B	hex, LSB first	90	10010000	144	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	1C	00011100	28	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A5	10100101	165	
15	**Max H image size** *(rounded to cm)*	22	00100010	34	
16	**Max V image size** *(rounded to cm)*	13	00010011	19	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	03	00000011	3	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	3E	00111110	62	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	85	10000101	133	
1B	Red x **(Upper 8 bits)**	91	10010001	145	
1C	Red y/ highER 8 bits	56	01010110	86	
1D	Green x	59	01011001	89	
1E	Green y	91	10010001	145	
1F	Blue x	28	00101000	40	
20	Blue y	1F	00011111	31	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	

29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	14	00010100	20	
37	Pixel Clock/10000 USB	37	00110111	55	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	B4	10110100	180	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	38	00111000	56	
3C	Vertical Blanking **Lower 8bits**	24	00100100	36	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	6C	01101100	108	
3F	HorzSync.Width	30	00110000	48	
40	VertSync.Offset : VertSync.Width	AA	10101010	170	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	58	01011000	88	
43	Vertical Image Size **Lower 8bits**	C1	11000001	193	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Pixel Clock/10,000 (LSB)	B8	10111000	184	40Hz or 48Hz frame rate
49	Pixel Clock/10,000 (MSB)	24	00100100	36	
4A	Horizontal Addressable Pixels, lower 8 bits	80	10000000	128	
4B	Horizontal Blanking Pixels, lower 8 bits	B4	10110100	180	
4C	H Pixels, upper nibble : H Blanking, upper nibble	70	01110000	112	
4D	Vertical Addressable Lines, lower 8 bits	38	00111000	56	

4E	Vertical Blanking Lines, lower 8 bits	24	00100100	36	
4F	V lines, upper nibble : V blanking, upper nibble	40	01000000	64	
50	Horizontal Front Porch, lower 8 bits	6C	01101100	108	
51	Horizontal Sync Pulse, lower 8 bits	30	00110000	48	
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	AA	10101010	170	
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0	
54	Horizontal Image Size in mm, lower 8 bits	58	01011000	88	
55	Vertical Image Size in mm, lower 8 bits	C1	11000001	193	
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16	
57	Horizontal Border	00	00000000	0	
58	Vertical Border	00	00000000	0	
59	Bit Encode Sync Information	18	00011000	24	
5A	DC	00	00000000	0	nVDPS Reserved 00
5B	HTOTAL	00	00000000	0	
5C	HA	00	00000000	0	
5D	HBL	00	00000000	0	
5E	HFP	00	00000000	0	
5F	HFPe	00	00000000	0	
60	HBP	00	00000000	0	
61	HB	00	00000000	0	
62	HSO	00	00000000	0	
63	HS	00	00000000	0	
64	VTOTAL	00	00000000	0	
65	VA	00	00000000	0	
66	VBL	00	00000000	0	
67	VFP	00	00000000	0	
68	VBP	00	00000000	0	
69	VB	00	00000000	0	
6A	VSO	00	00000000	0	
6B	VS	00	00000000	0	
6C	Detail Timing Description #4	00	00000000	0	Header
6D	Flag	00	00000000	0	
6E	Reserved	00	00000000	0	
6F	For Brightness Table and Power Consumption	02	00000010	2	
70	Flag	00	00000000	0	
71	PWM % [7:0] @ Step 0	14	00010100	20	Brightness Table
72	PWM % [7:0] @ Step 5	30	00110000	48	
73	PWM % [7:0] @ Step 10	FF	11111111	255	
74	Nits [7:0] @ Step 0	12	00010010	18	
75	Nits [7:0] @ Step 5	3C	00111100	60	
76	Nits [7:0] @ Step 10	C8	11001000	200	

77	Panel Electronics Power @ 32x32 Chess Pattern =	0B	00001011	11	Power Consumption
78	Backlight Power @ 60 nits =	07	00000111	7	
79	Backlight Power @ Step 10 =	19	00011001	25	
7A	Nits [7:0] @ 100% PWM Duty =	C8	11001000	200	
7B	Flag	20	00100000	32	Flag (if EDID Address 6F = 0x02) Nits [15:8] @ Step 10 (if EDID Address 6F = 0x03)
7C	Flag	20	00100000	32	Flag (if EDID Address 6F = 0x02) Nits [15:8] @ 100% PWM Duty (if EDID Address 6F = 0x03)
7D	Flag	20	00100000	32	
7E	Extension Flag	00	00000000	0	
7F	Checksum	6C	01101100	108	