() Preliminary Specifications
(V) Final Specifications

Module	**10.1” 2.5K Color TFT-LCD with LED Backlight design**
Model Name	**G101QAN01.1**

Customer	**Date**	**Approved by**	**Date**
		_____	2019/5/20
Checked & Approved by		**Prepared by**	
_____	_____	_____	2019/5/20
		General Display Business Unit / AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description
1.0 2019/05/20	All		-

1. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any direction.
9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
15) The data on this specification sheet is applicable when LCD module is placed in landscape position.
16) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.

2. General Description

G101QAN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel and LED backlight system. The screen format is intended to support the 16:10 1600(H) x2560(V) screen and 16.7M. All input signals are MIPI interface compatible.

2.1 Display Characteristics

The following items are characteristics summary under 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[inch]	10.1”
Active Area	[mm]	135.36 (H) x 216.576 (V)
Pixels H x V		1600 x 2560
Pixel Pitch	[mm]	0.0846 x 0.0846
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		AHVA
Nominal Input Voltage LCD VCC	[Volt]	+3.3V (Typ.)
Power Consumption	[Watt]	Logic power 0.5 max BLU power 2.03 max (w/o LED Driver)
Weight	[Grams]	120g
Physical Size	[mm]	<table><tr><td></td><td>Min.</td><td>Typ.</td><td>Max.</td></tr><tr><td>Length</td><td>142.76</td><td>142.96</td><td>143.16</td></tr><tr><td>Width</td><td>227.84</td><td>228.04</td><td>228.24</td></tr><tr><td>Thickness</td><td></td><td></td><td>4.05</td></tr></table>
Electrical Interface		8 channel MIPI
Surface Treatment		Glare
Support Color		16.7M Colors
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0℃~50℃ -20℃~60℃
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m2]		340	400		
Uniformity	%	9 points	70			
Contrast Ratio			800	1000		
Response Time	[msec]	Rising + Falling		25	35	
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	80	85		
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	80	85		
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.592	0.642	0.692	
		Red y	0.283	0.333	0.383	
		Green x	0.257	0.307	0.357	
		Green y	0.551	0.601	0.651	
		Blue x	0.100	0.150	0.200	
		Blue y	0.025	0.075	0.125	
		White x	0.263	0.313	0.363	
		White y	0.279	0.329	0.379	
Color Gamut	%			65		

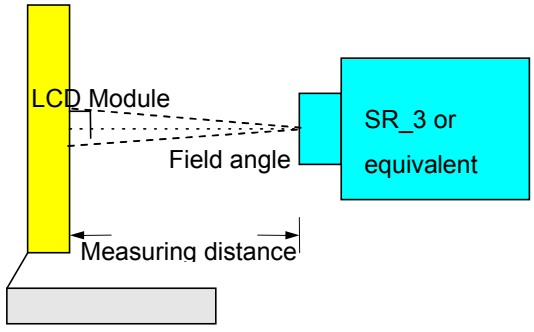
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

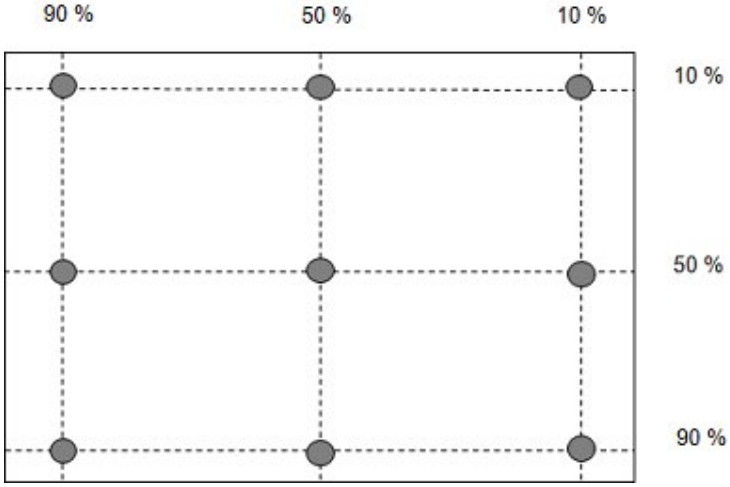
Aperture Field angle 2□with 50cm measuring distance

Test Point Follow Note 2 position

Environment *< 1 lux*



Note 2: Definition of 9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the minimum luminance values by the maximum test point luminance

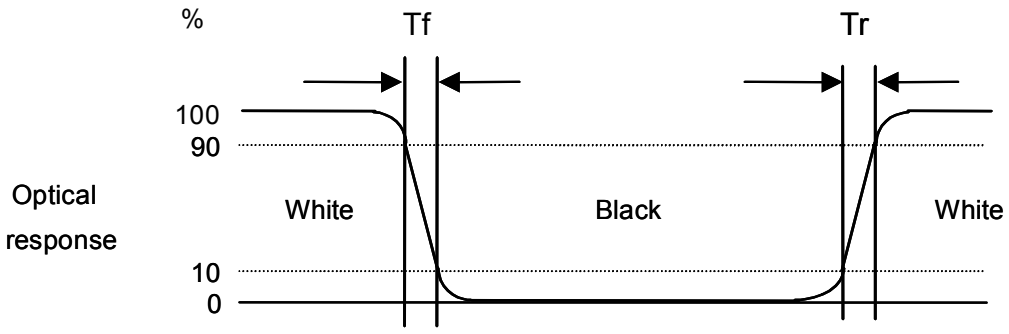
$$\delta_{W9} = \frac{\text{Minimum Brightness of nine points}}{\text{Maximum Brightness of nine points}}$$

Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

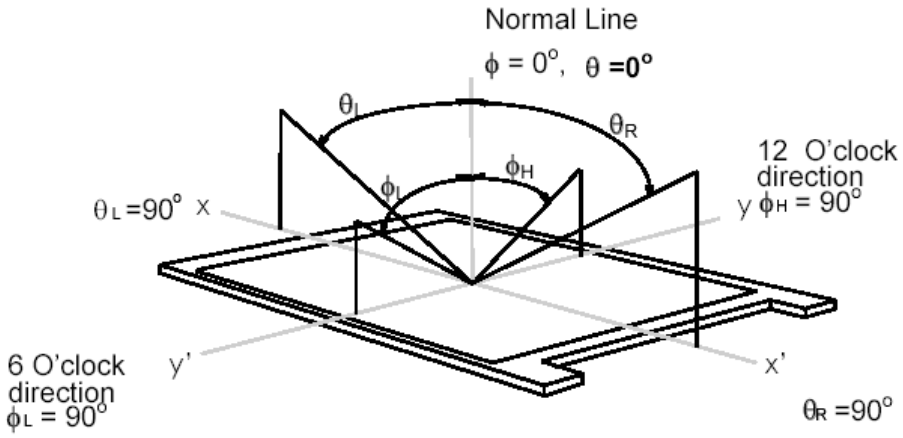
Note 5: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.



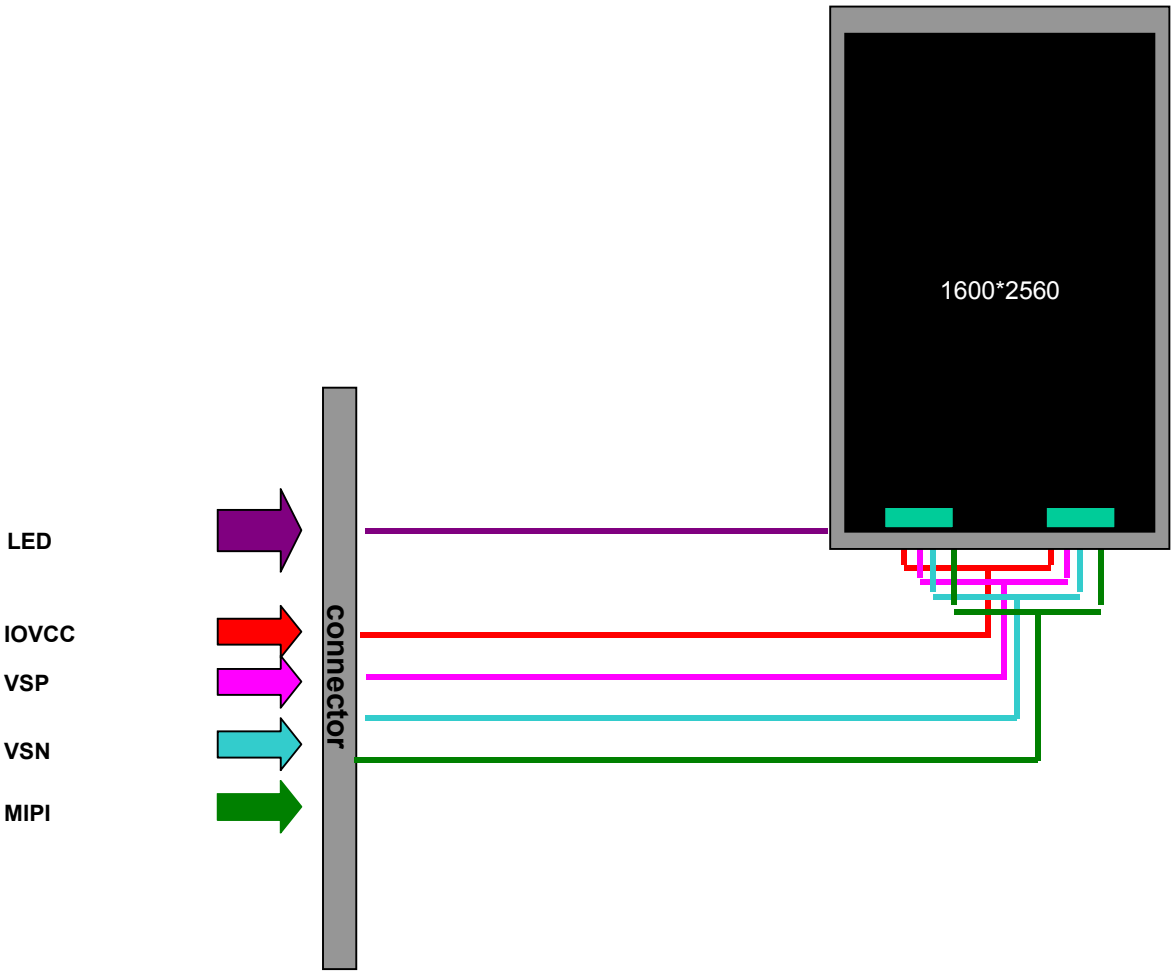
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio □10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inch color TFT/LCD module:



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD drive Voltage	IOVCC	-0.3	+3.3	[Volt]	Note 1,2
	VSP	-0.3	+6.6		
	VSN	-6.6	+0.3		

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit
Operating Temperature	TOP	0	50	[°C]
Operation Humidity	HOP	5	90	[%RH]
Storage Temperature	TST	-20	60	[°C]
Storage Humidity	HST	5	90	[%RH]

Note 1: At Ta (25□)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: Maximum wet-bulb temperature is less than 39°C and no condensation

Note 4: Operating temperature means “Front and rear surface” of panel

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25□ and frame frenquency under 60Hz

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
LCD Input Analog Voltage		IOVCC	1.7	1.8	1.9	V	
LCD Input Analog Voltage		VSP	5.3	5.6	5.9	V	
LCD Input Analog Voltage		VSN	-5.9	-5.6	-5.3	V	
"H" Level Input Voltage		VIH	0.7 IOVCC		IOVCC	V	Applicable Pin： LCD_RST
"L" Level Input Voltage		VIL	0		0.3 IOVCC	V	Applicable Pin： LCD_RST
Input high level leakage current		I IH			1	μA	For the digital, I/O circuit (Not include thepull-up/down)
Input low level leakage current		PN	-1			uA	
LCD	Normal	PD			500	mW	Note1

Notes:

(1) The specified current and power consumption are under the conditions at IOVCC = 1.8V, T = 25°C, and fv = 60 Hz, at white pattern

5.1.2 Logic Power Consumption

The power specification are measured under 25℃ and frame frenquency under 60Hz

Parameter	Symbol	Values		Units	Notes
		Typ	Max		
Normal Mode	IIOVCC		45	mA	White Pattern
	IVSP		30	mA	White Pattern
	IVSN		30	mA	White Pattern
Sleep Mode	IIOVCC		300	uA	
	IVSP		15	uA	
	IVSN		15	uA	

5.1.3 MIPI DC Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
MIPI digital operation current	IMVDDA	MVDDA=1.5V, Data Rate=1000Mbps	-	10		mA
MIPI digital stand-by current	IMVDDAST	MVDDA input current. All input signal are stopped.	-	100	-	uA
MIPI Characteristics for High Speed Receiver						
Single-endedl input low voltage	VILHS		-40	-	-	mV
Single-endedl input high voltage	VIHHS		-	-	460	mV
Common-mode voltage	VCMRXDC		70	-	330	mV
Differential input impedance	ZID		80	100	125	ohm
Differential input high threshold	VIDTH			-	70	mV
Differential input low threshold	VIDTL		-70	-	-	mV
MIPI Characteristics for Low Power Mode						
Pad signal voltage range	VI		-50	-	1350	mV
Ground shift	VGNDSH		-50	-	50	mV
Output low level	VOL		-50		50	mV
Output high level	VOH		1.1	1.2	1.3	V

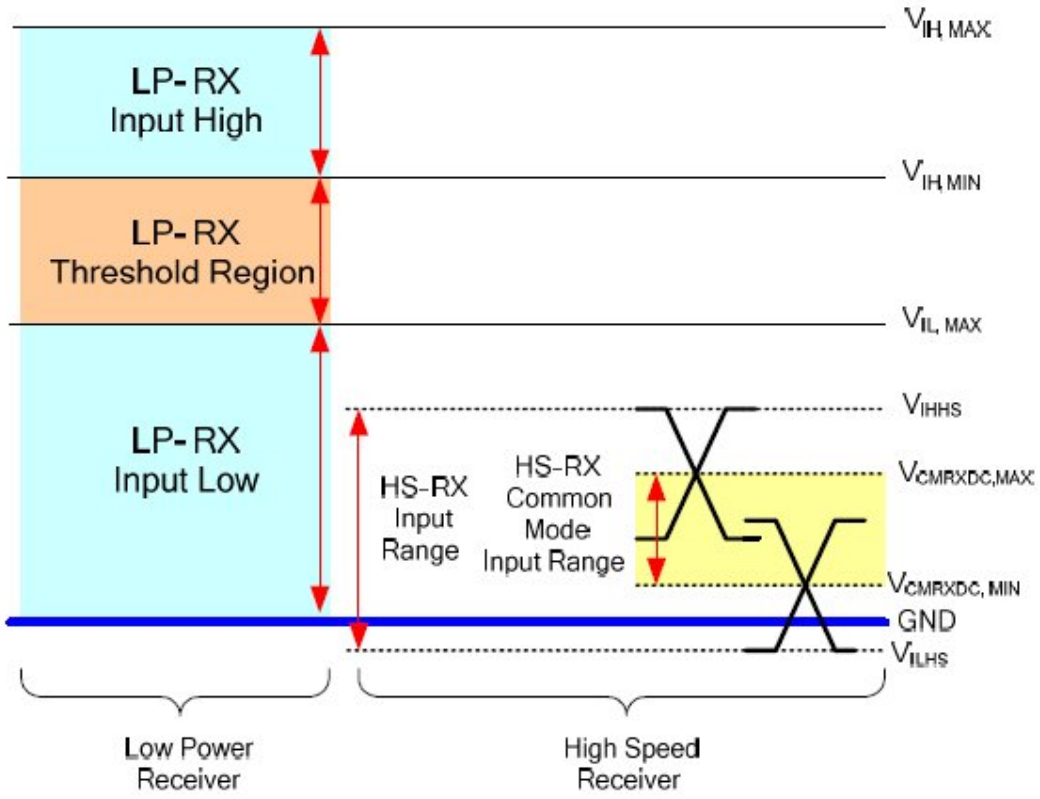


Figure: MIPI DC Diagram

5.1.4 MIPI AC Characteristics

5.1.4.1 LP Transmission

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
15%-85% rise time and fall time	TRLP / TFLP	-	-	25	ns
Pulse width of the LP exclusive-OR clock	TLP-PULSE-TX	50	-	75	ns
Period of the LP exclusive-OR clock	TLP-PER-TX	100	-	150	ns

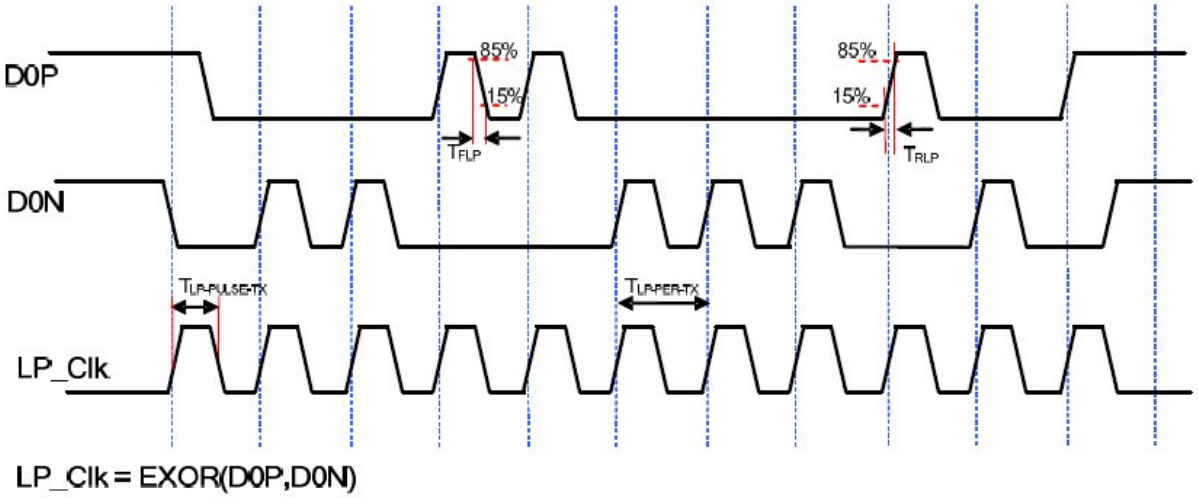


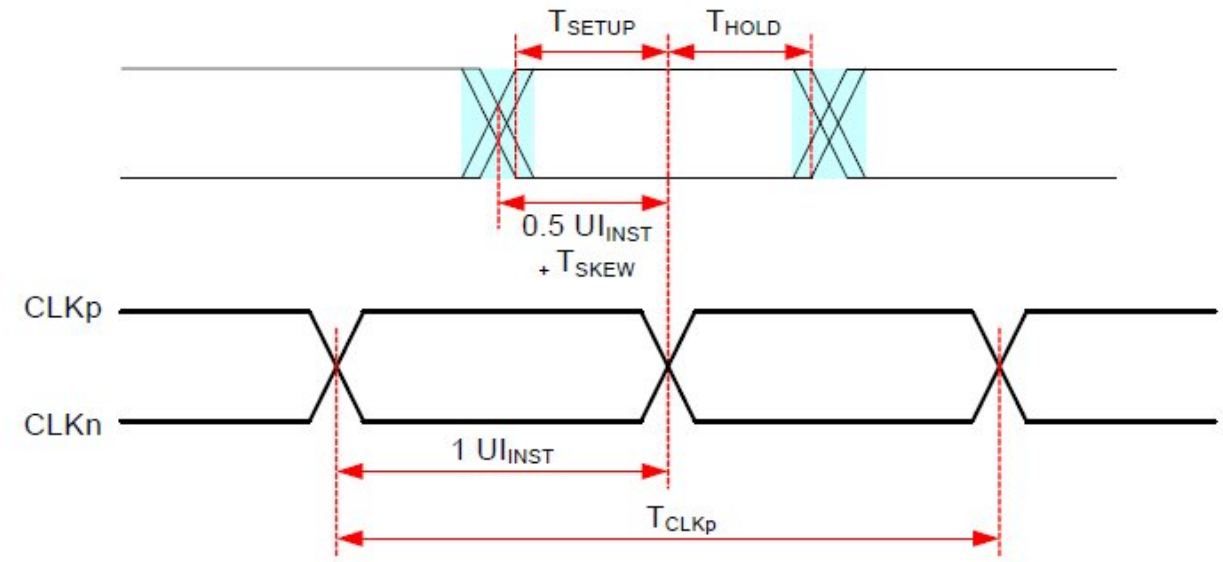
Figure: LP Transmitter Timing Definitions

5.1.4.2 High Speed Transmission

Data-Clock Timing Specifications

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
UI instantaneous	UIINST	1	-	2.5	ns
Data to Clock Setup Time	TSETUP	0.15	-	-	UIINST
Data to Clock Hold Time	THOLD	0.15	-	-	UIINST



5.1.5 High-Speed Data Transmission in Bursts

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time to drive LP-00 to prepare for HS transmission	THS-PREPARE	40+4*UI	-	85+6*UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	TEOT			105 ns +	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	THS-TERM-EN	-	-	35+4*UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	THS-TRAIL	60+4*UI	-	-	ns
Time-out at RX to ignore transition period of EoT	THS-SKIP	40	-	55+4*UI	ns
Time to drive LP-11 after HS burst	THS-EXIT	100	-	-	ns
Length of any Low-Power state period	TLPX	50	-		ns
Sync sequence period	THS-SYNC	145 ns + 10*UI			ns
Minimum lead HS-0 drive period before the Sync sequence	THS-ZERO	105ns+ 6*UI		60ns+ 4*UI	ns

Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

2. UI means Unit Interval, equal to one half HS clock period on the Clock Lane.

3. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

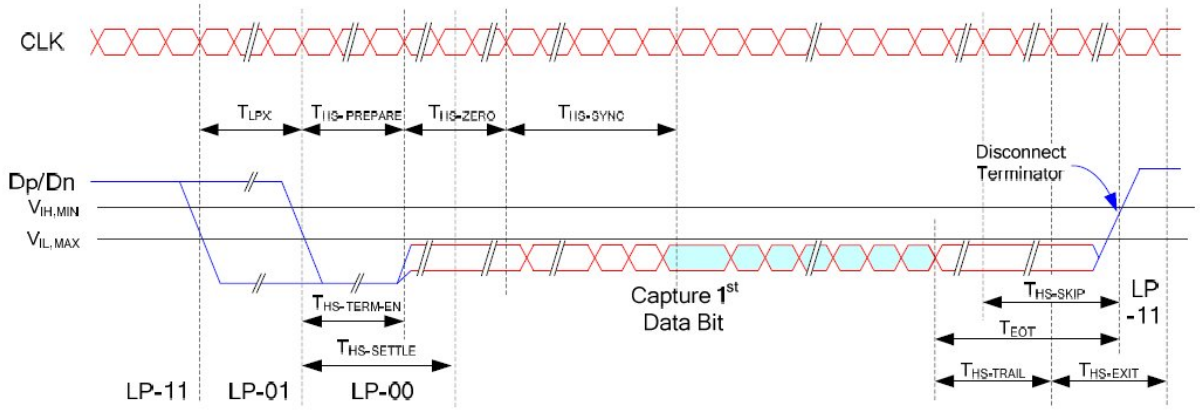


Figure : High-Speed Data Transmission in Bursts

5.1.6 High-Speed Clock Transmission

Switching the Clock Lane Operation Timing Parameters

(IOVCC= 1.7V to 1.9V, GND=DGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52*UI	-	-	ns
Detection time that the clock has stopped toggling	TCLK-MISS			60	ns
Time to drive LP-00 to prepare for HS clock transmission	TCLK-PREPARE	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	TCLK-PREPARE +TCLK-ZERO	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	THS-TERM-EN	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	TCLK-PRE	8*UI	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns

Note:

The DSI host processor shall support continuous clock on the Clock Lane for NT chip that require it, so the host processor needs to keep the HS serial clock running.

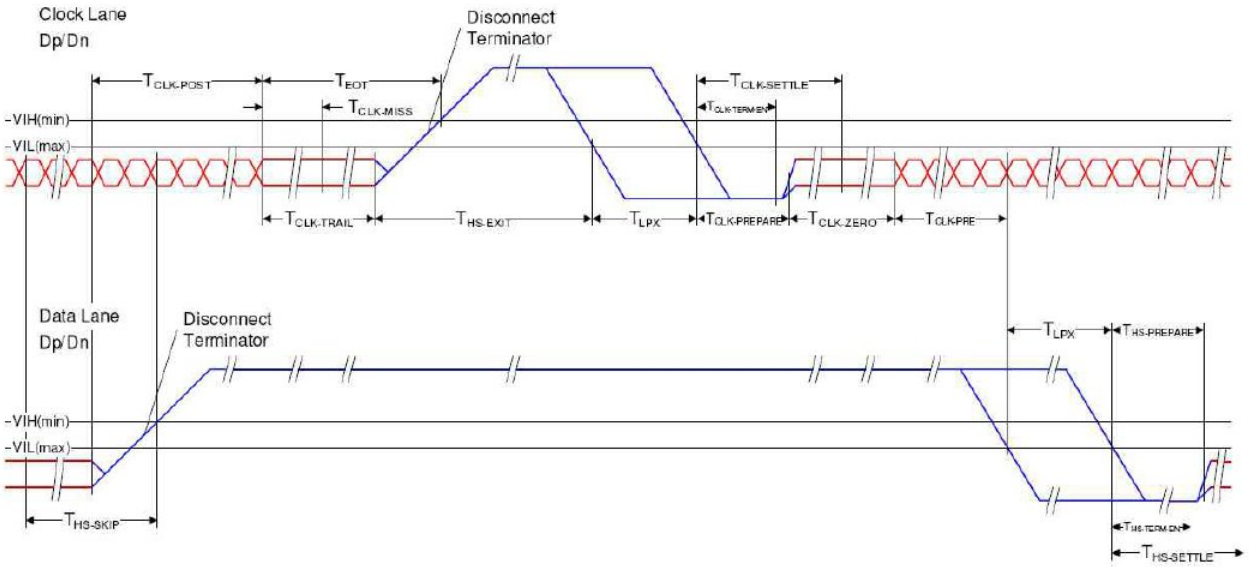


Figure: Switching the Clock Lane between Clock Transmission and Low-Power Mode

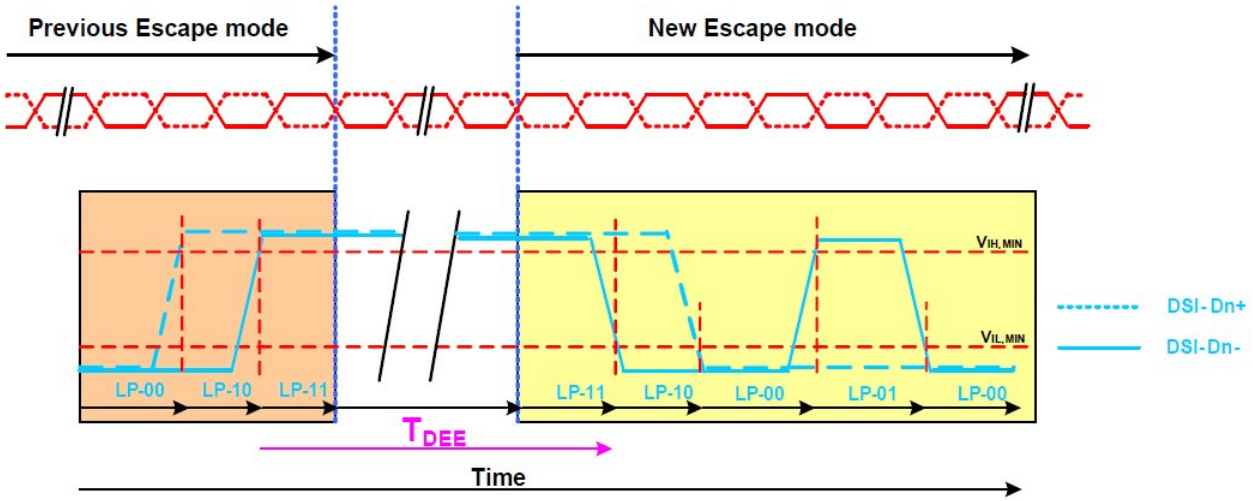
5.1.7 LP11 timing request between data transformation

When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Lowpower mode.

If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode.

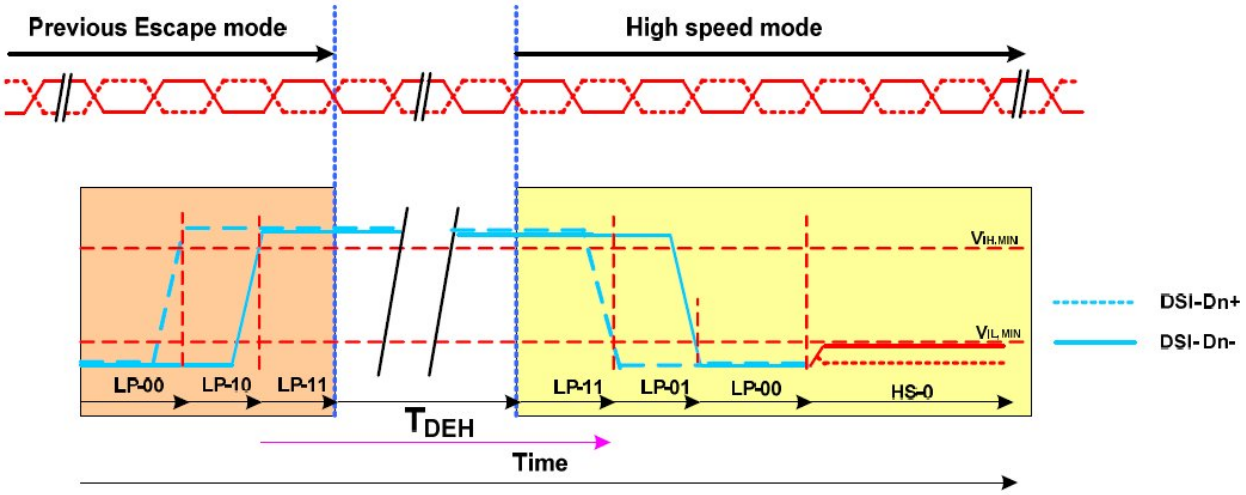
The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP - LP, LP - HS, HS - LP, and HS – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP - LP command



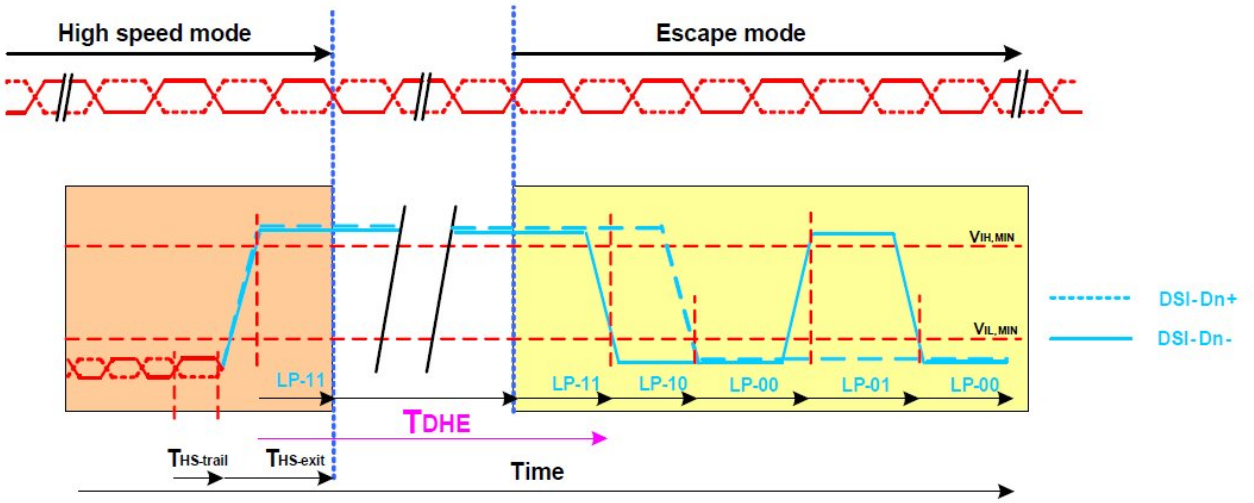
Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the new Escape Mode Entry	TDEE	100			ns

(2)Timing between LP - HS command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Entering High Speed Mode	TDEH	100			ns

(3)Timing between HS - LP command



Parameter	Symbol	Specification			UNIT
		MIN	TYP	MAX	
LP-11 delay to a start of the Escape Mode Entry	TDHE	100			ns

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED light bar Voltage per string	V_L		28.25	29	V	(Ta=25℃)
Current of Each string	I_{LED}		14		mA	(Ta=25℃)
Power Consumption (5P5S, W/O efficiency)	P_{BL}			2.03	W	(Ta=25℃) Note1.
LED Life Time	L_L	15000			Hr	(Ta=25℃) Note2.

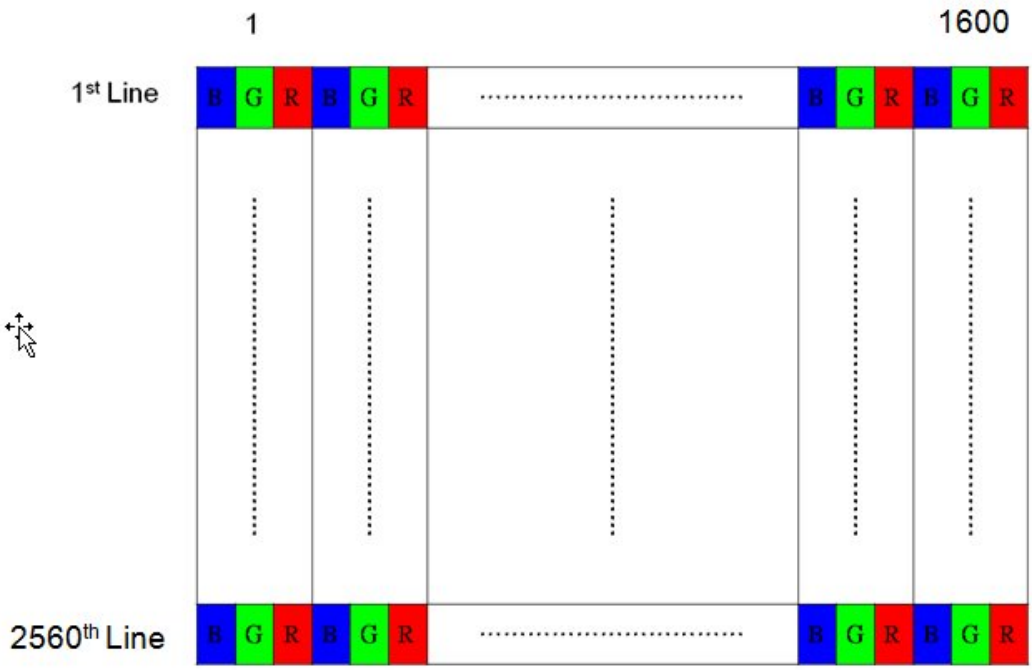
Note 1: Calculator value for reference P_{BL} = VF (Normal Distribution) * IF (Normal Distribution) . W/O Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	FH26W-61S-0.3SHW(60)
Mating Housing/Part Number	FPC

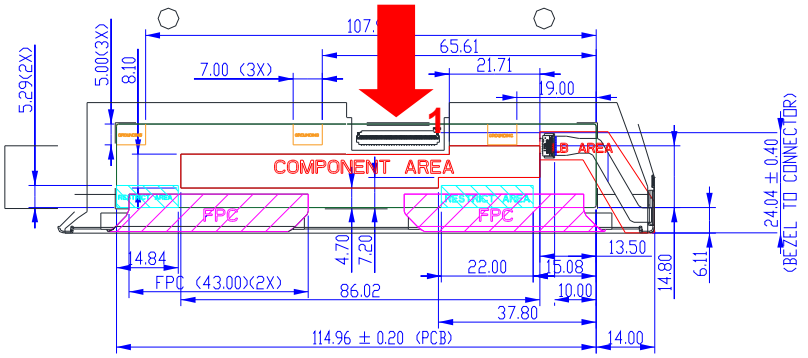
6.2.2 Pin Assignment

MIPI lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Symbol	I/O	Description
1	GND		AGND
2	GND		AGND
3	NC		
4	NC		
5	FB5	I	LED-
6	FB4	I	LED-
7	FB3	I	LED-
8	FB2	I	LED-
9	FB1	I	LED-
10	NC		
11	VLED2	I	LED+
12	VLED1	I	LED+
13	NC		
14	VSP	I	+5.6V
15	VSP	I	+5.6V
16	NC		
17	VSN	I	-5.6V
18	VSN	I	-5.6V
19	NC		
20	IOVCC	I	+1.8V
21	IOVCC	I	+1.8V

22	NC		for AUO internal use
23	LCD_RST	I	Reset +1.8V
24	NC		For AUO internal use
25	NC		For AUO internal use
26	ID	O	connect 10k ohm to GND
27	NC		For AUO internal use
28	GND		DGND
29	GND		DGND
30	D0PA	I	MIPI input Data pair
31	D0NA	I	MIPI input Data pair
32	GND		DGND
33	D1PA	I	MIPI input Data pair
34	D1NA	I	MIPI input Data pair
35	GND		DGND
36	CLKPA	I	MIPI input CLK pair
37	CLKNA	I	MIPI input CLK pair
38	GND		DGND
39	D2PA	I	MIPI input Data pair
40	D2NA	I	MIPI input Data pair
41	GND		DGND
42	D3PA	I	MIPI input Data pair
43	D3NA	I	MIPI input Data pair
44	GND		DGND
45	D0PB	I	MIPI input Data pair
46	D0NB	I	MIPI input Data pair
47	GND		DGND
48	D1PB	I	MIPI input Data pair
49	D1NB	I	MIPI input Data pair
50	GND		DGND
51	CLKPB	I	MIPI input CLK pair
52	CLKNB	I	MIPI input CLK pair
53	GND		DGND
54	D2PB	I	MIPI input Data pair
55	D2NB	I	MIPI input Data pair
56	GND		DGND
57	D3PB	I	MIPI input Data pair

58	D3NB	I	MIPI input Data pair
59	GND		DGND
60	GND		DGND
61	GND		DGND



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1600x2560 manufacturing guide line timing.

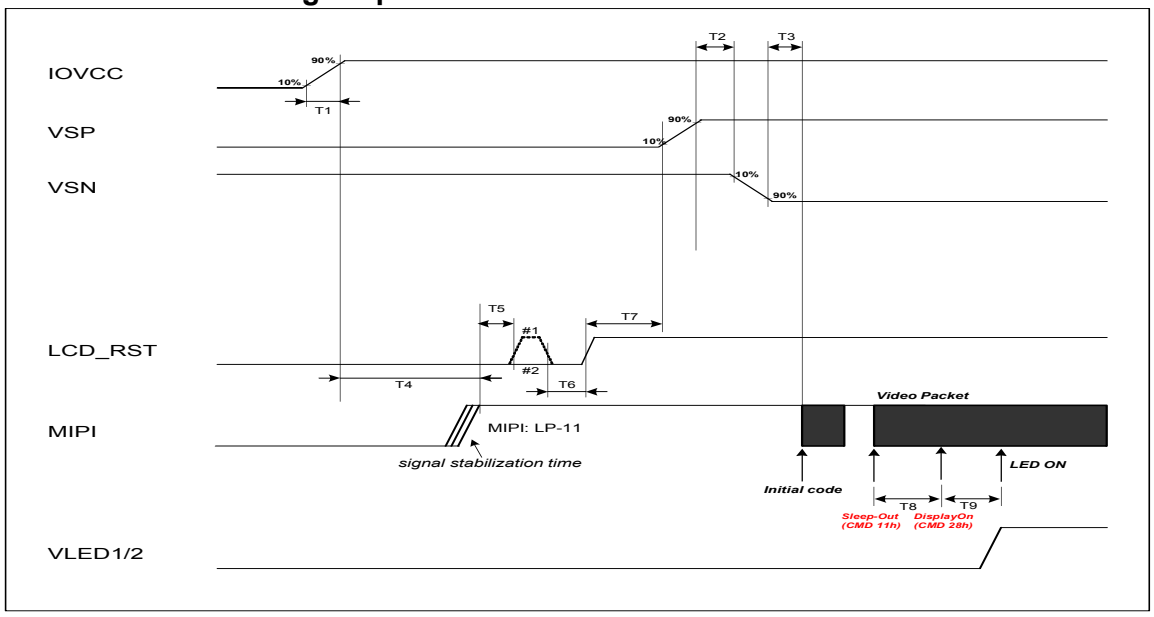
Signal	Item	Symbol	Min.	Typ.	Max.	Unit
	MIPI Data frequency	FDATA		943		MHz
DCLK	Frequency	1/Tc		158		MHz
DE	Vertical Total Time	TV	-	2608	-	TH
	Vertical Active Display Period	TVD	-	2560	-	TH
	Vertical Front Porch Period	TVFP	Note2	16	Note2	TH
	Vsync pulse width	TVPW	Note2	8	Note2	TH
	Vertical Back Porch Period	TVBP	note2	24	Note2	TH
	Horizontal Total Time	TH	-	1008		Tc
	Horizontal Active Display Period	THD	-	800	-	Tc
	Horizontal Front Porch Period	THFP	Note3	120		Tc
	Horizontal pulse width	THPW	-	8	-	Tc
	Horizontal Back Porch Period	THBP	Note3	80		Tc

Note1: Frame rate=60Hz
Note2: Vertical Period are dependent on GOA timing, and don't modify. TVFP+TVPW+TVBP>16
Note3: tHFP = 0.65us (min), tHBP= 0.64us (min)
Note4: Horizontal Period is set by per port
Note5: DCLK=Frame rate*TV*TH.
TV=TVD+TVFP+TVPW+TVBP
TH=THD+THFP+THPW+THBP

6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

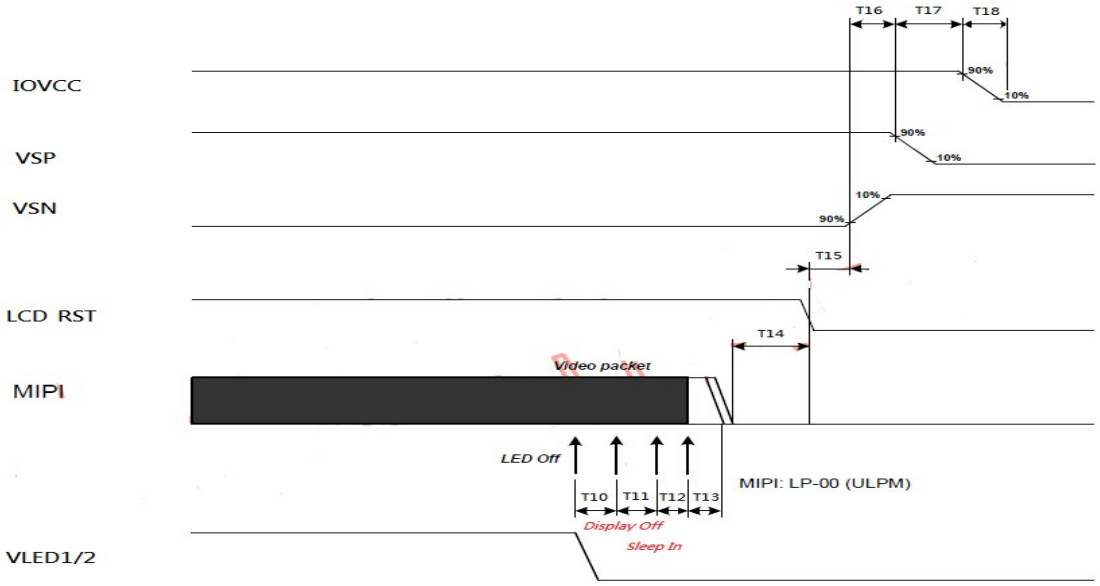
6.4.1 Power on Timing Sequence: IOVCC=1.7 to 1.9V



Note1: LCD_RST signal H to L to H (#1) is better than only L to H(#2)

Power Sequence Timing			
Parameter	Value		Unite
	Min.	Max.	
T1	0.5	2	ms
T2	10	-	ms
T3	0	-	ms
T4	15	-	ms
T5	1	-	ms
T6	10	-	us
T7	20	-	ms
T8	6	-	frame
T9	3	-	frame

6.4.2 Power off Timing Sequence: IOVCC=1.7 to 1.9V

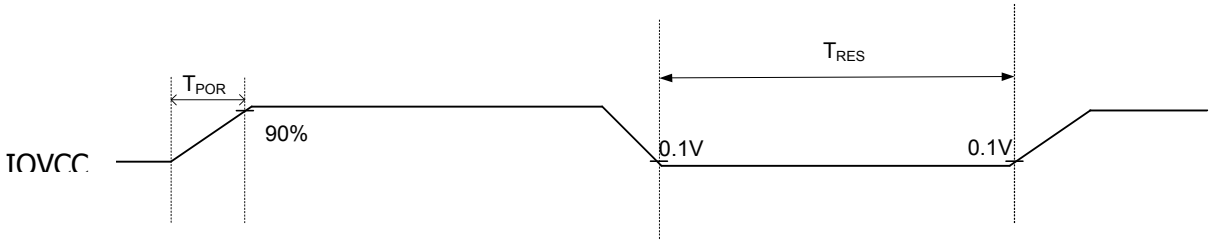


Power Sequence Timing			
Parameter	Value		Unite
	Min.	Max.	
T10	50	-	ms
T11	80	-	ms
T12	100	-	ms
T13	0	-	ms
T14	10	-	ms
T15	1	-	ms
T16	10	-	ms
T17	0	-	ms
T18	-	10	ms

a. IOVCC AC characteristic:

IOVCC= 1.8V, GND=AGND= 0V, TA= -20 to +85˚C)

6.4.3 Power reset Timing Sequence: IOVCC=1.7 to 1.9V



Parameter Symbol	Symbol	Min.	Typ.	Max.	Unit	Conditions
IOVCC power source slew time	TPOR	0.5		2	ms	From 0V to 90% IOVCC
IOVCC resettle time	TRES			500	ms	

6.5 Power ON/OFF MIPI comment

6.5.1 Power On Set Table

Step	Register Setting		Operation
	Register	Data	
1	Reset = LOW		
2	Power (IOVCC) ON		
3	15ms or more		
4	MIPI LP-11 status ON		
5	1ms or more		
6	Reset = HIGH		
7	20ms or more		
8	Power (VSP, VSN,) ON VSP ON◊ 10ms or more ◊ON VSN ON		

6.5.2 Power Off Set Table

Step	Register Setting		Operation
	Register	Data	
1	MIPI Video Pixel Stream OFF		
2	MIPI LP-11 Status OFF(LP-00)		
3	10ms or more		
4	Reset = LOW		
5	1ms or more		
6	Power (VSN, VSP, IOVCC) Off VSN ◊ 10ms or more ◊ VSP Off → IOVCC Off		

6.5.3 Display On & Sleep Out Set Table

Step	Data Type	Register Setting		Operation
		Register	Data	
1	39h	F0h	55h,AAh,52h,08h,00h	Switch page0
2	15h	C0h	0Dh	ESD detect signal
3	15h	62h	01h	Set ESD protect command
4	05h	11	-	Sleep Out
5	05h	29	-	Display On
6	MIPI Video Pixel Stream ON			
7	120ms or more			

6.5.4 Display Off & Sleep In Set Table

Step	Data Type	Register Setting		Operation
		Register	Data	
1	0x05	28	-	Display Off
2		20ms or more		
3	0x05	10	-	Sleep In
4		100ms or more		
5		MIPI Video Pixel Stream OFF		

7. Reliability Test Criteria

Items	Required Condition	Note
Temperature Humidity Bias	40 °C, 90%RH, 240 hours	
High Temperature Operation	50 °C, 240 hours	
Low Temperature Operation	0 °C, 240 hours	
Hot Storage	60 °C, 240 hours	
Cold Storage	-20 °C, 240 hours	
Thermal Shock Test	-20℃(30mins) / 60℃(30mins), 27cycle	
ESD	Contact : ±8KV Air : ±15KV	Note 1

Note1: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost

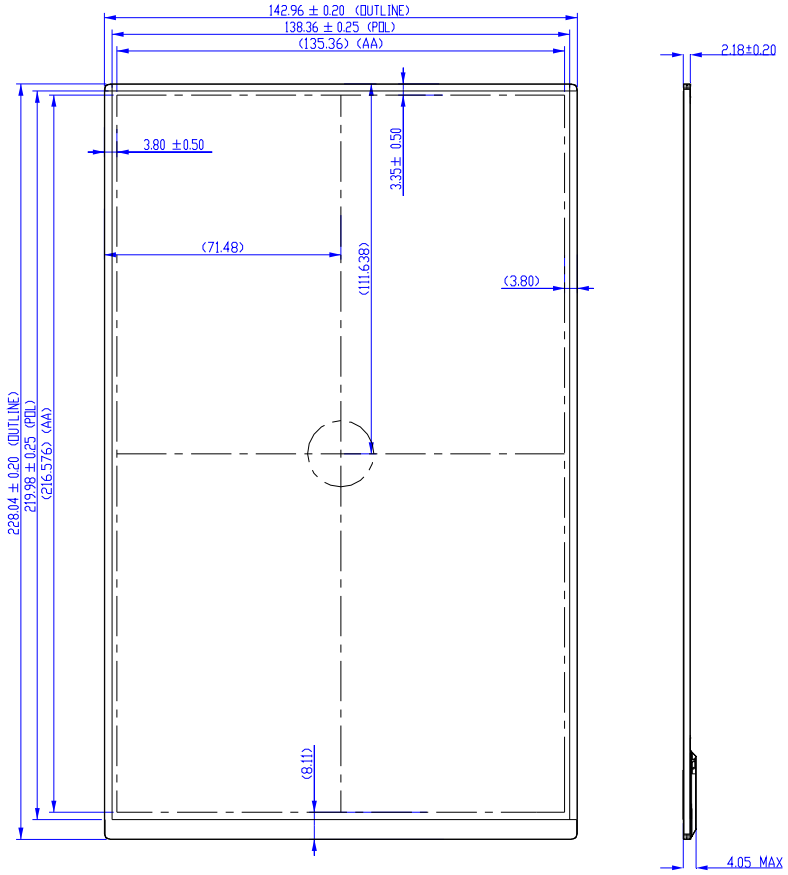
. Self-recoverable. No hardware failures.

Note2:

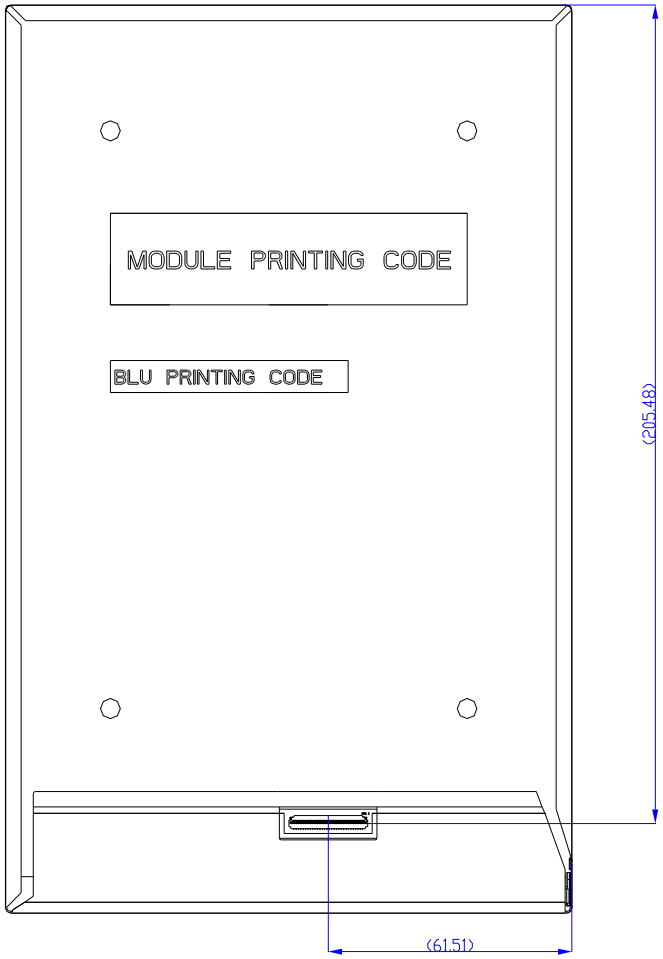
- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.

8. Mechanical Characteristics

8.1 LCM Outline Dimension (Front View)



8.2 LCM Outline Dimension (Rear View)



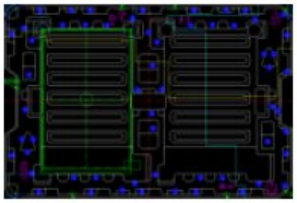
9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)

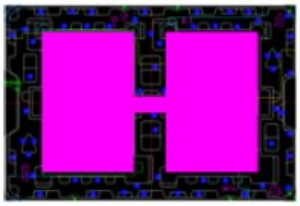
Label Size: 90mm x 23mm

9.2 Carton/Pallet Package

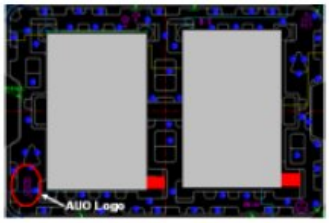
1、取出 PP 瓦楞



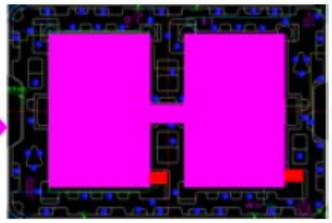
2、Tray 放置在 PP 瓦楞板上



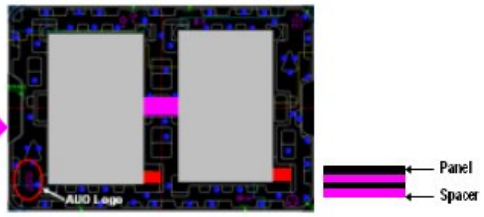
3、將第一層 EPE Spacer 放置在 Tray 上



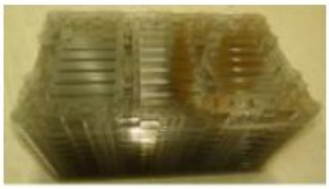
4、將 Panel 如圖示放置（P 板與 Tray 上的 AUO Logo 在同一側）



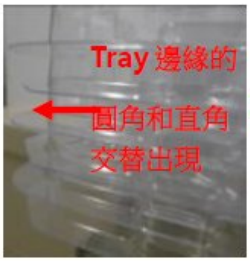
5、放置第二層 EPE Spacer



6、再於 Panel 上放置第二層 Panel，即 1PCS Tray 共裝載 4PCS Panel 和 2PCS Spacer



7、將 21PCS Tray 旋轉堆疊起來，最上層 1PCS Tray 為空，不放 Panel，即每摞 Tray 放置 80PCS panel 和 40PCS Spacer



8、將整摞 Tray 放入靜電袋中

9、將包裝完畢的整摞包材放入紙箱內，靜電袋折邊

10、將上層 EPE 放入紙箱中

11、使用 H 型膠帶封箱

10 Safety

10.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

10.2 Materials

10.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

10.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V0 in the module will complete the flammability rating exception approval process.

The printed circuit board will be made from material rated 94-V0 or better. The actual UL flammability rating will be printed on the printed circuit board.

10.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

10.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

UL 60950-1 second edition	U.S.A. Information Technology Equipment