(v) Preliminary Specifications
( ) Final Specifications

Module	**11.6”(11.58 ”) 16:9 Color TFT-LCD with LED Backlight design**
Model Name	**G116HAN01.0**
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
		Grace Hung	2018/08/06
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Fu Chuan Tsai	2018/08/06
Note: This Specification is subject to change without notice.		General Display Business Unit / AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.0 2018/08/06	All	First edition		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

G116HAN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 , 1920(H) x1080(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

G116HAN01.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	294.09 (11.58W")			
Active Area	[mm]	256.32(H) x 144.18(V)			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.1335 X 0.1335			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
White Luminance (I_{LED}=19mA) **(Note: I_{LED} is LED current)**	[cd/m^2]	350 typ. 300 min. (5 points average)			
Luminance Uniformity		70% min. (13 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.2 W max. (Including BL Power & Logic Power)			
Weight	[Grams]	200 max			
Physical Size **(Panel only) without bracket**	[mm]		Min.	Typ.	Max.
		Length	267.5	268.0	268.5
		Width	157.5 168.0	158.0 168.5	158.5 (w/o PCBA) 169.0 (w/ PCBA)
		Thickness	---	---	3.0
Electrical Interface		eDP 1.2 (2 lane)			
Glass Thickness	[mm]	0.4			
Surface Treatment		HC, Hardness 3H			

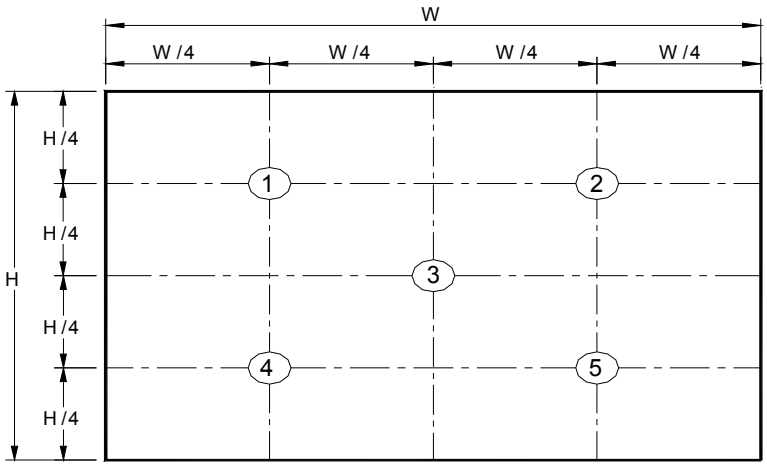
Support Color		16.7M colors (RGB 8-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

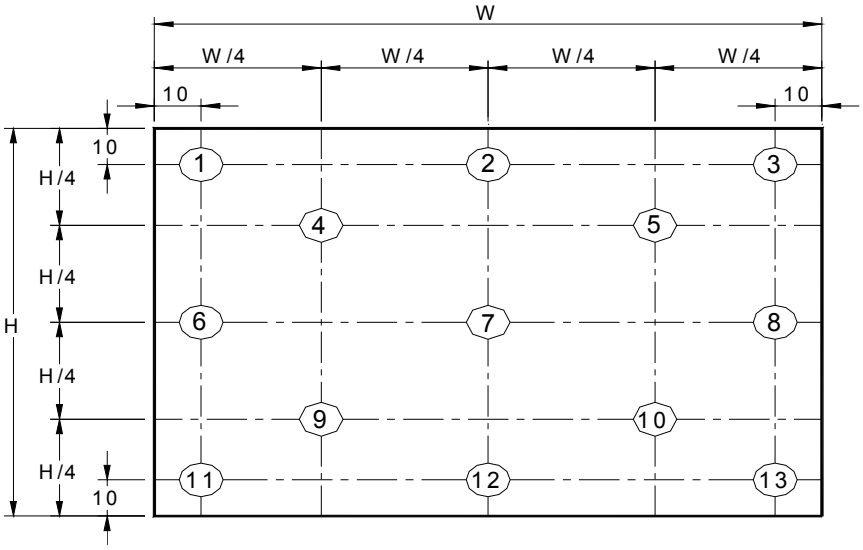
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=19mA			5 points average	300	350	---	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	85 85	89 89	--- ---	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	85 85	89 89	--- ---		
Luminance Uniformity		δ_{5P}	5 Points	---	80	---		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	70	---	---		2, 3, 4
Contrast Ratio		CR			800	-		4, 6
Cross talk		%		---	---	4		4, 7
Response Time		T_{RT}	Rising + Falling	---	25	35	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	TBD	TBD	TBD		4
		Ry		TBD	TBD	TBD		
	Green	Gx		TBD	TBD	TBD		
		Gy		TBD	TBD	TBD		
	Blue	Bx		TBD	TBD	TBD		
		By		TBD	TBD	TBD		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	52	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



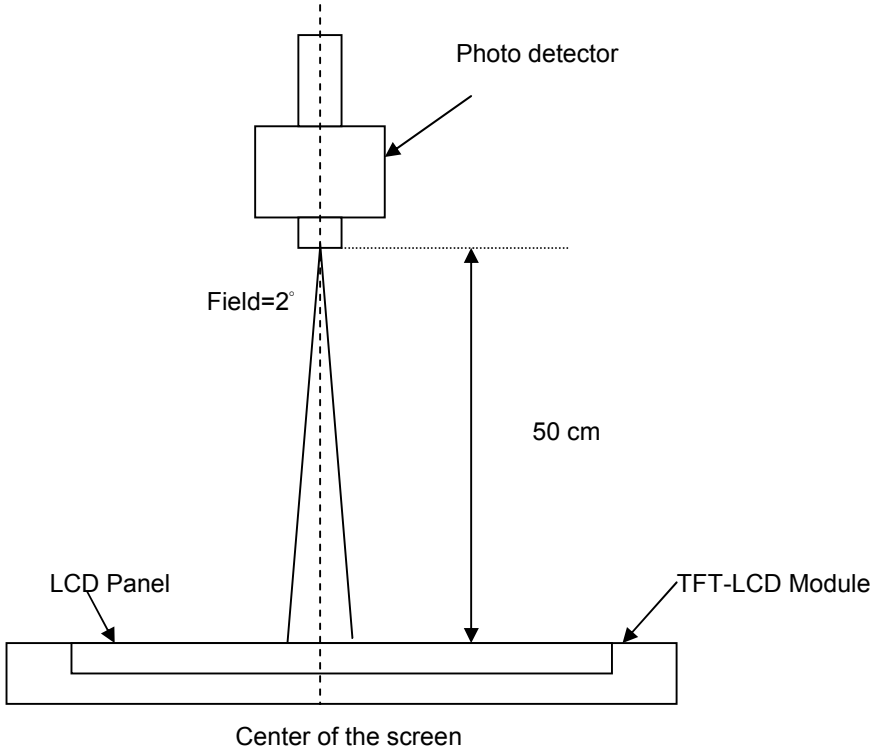
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Minimum Brightness of thirteen points}}{\text{Maximum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

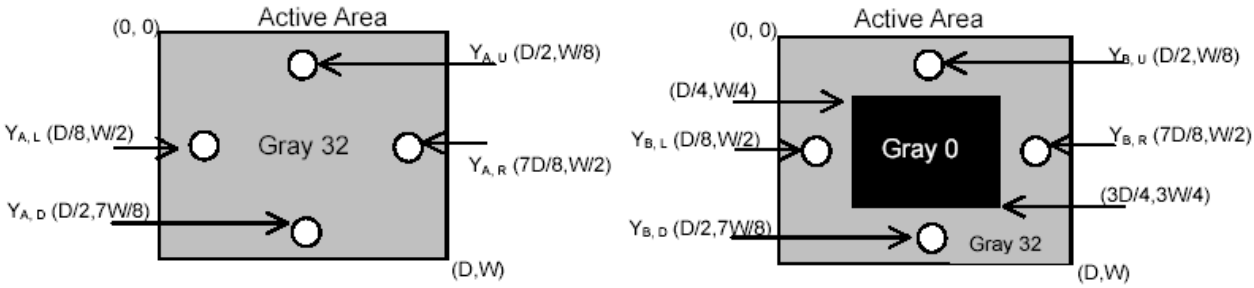
Note 7 : Definition of Cross Talk (CT)

CT = | YB – YA | / YA × 100 (%)

Where

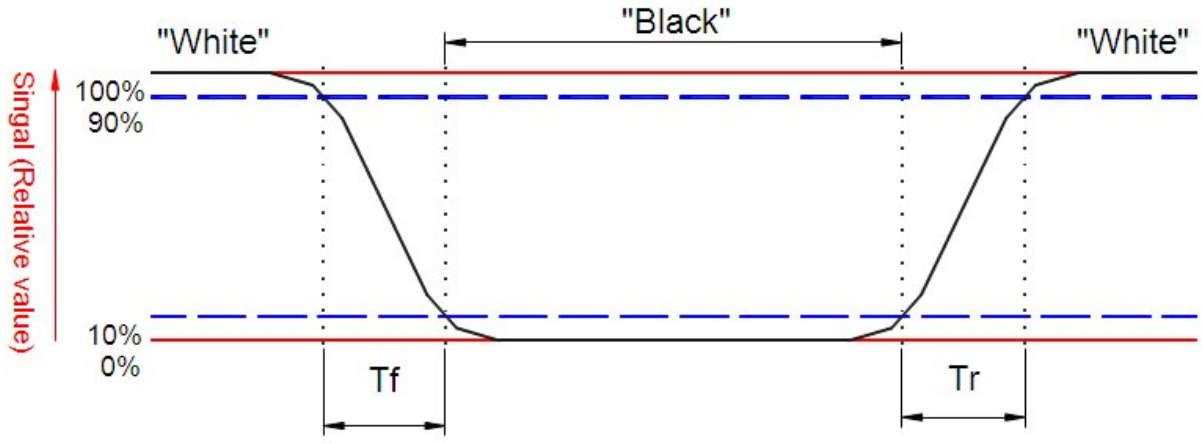
YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)



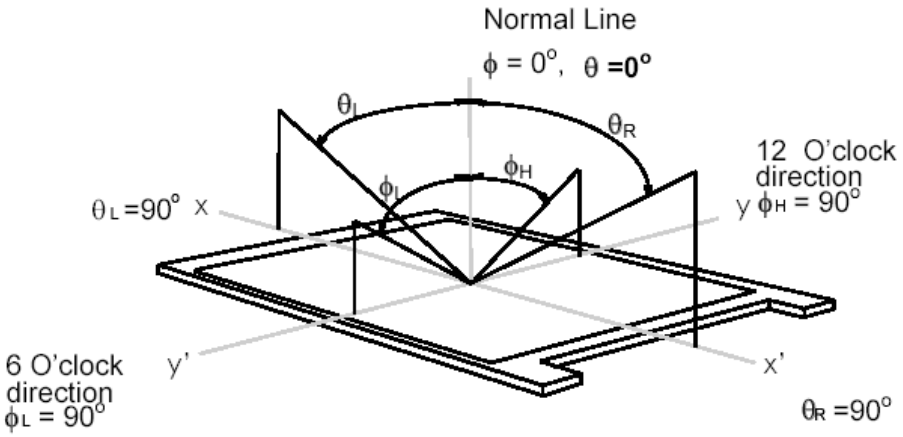
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (rising time) and from “White” to “Black” (falling time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



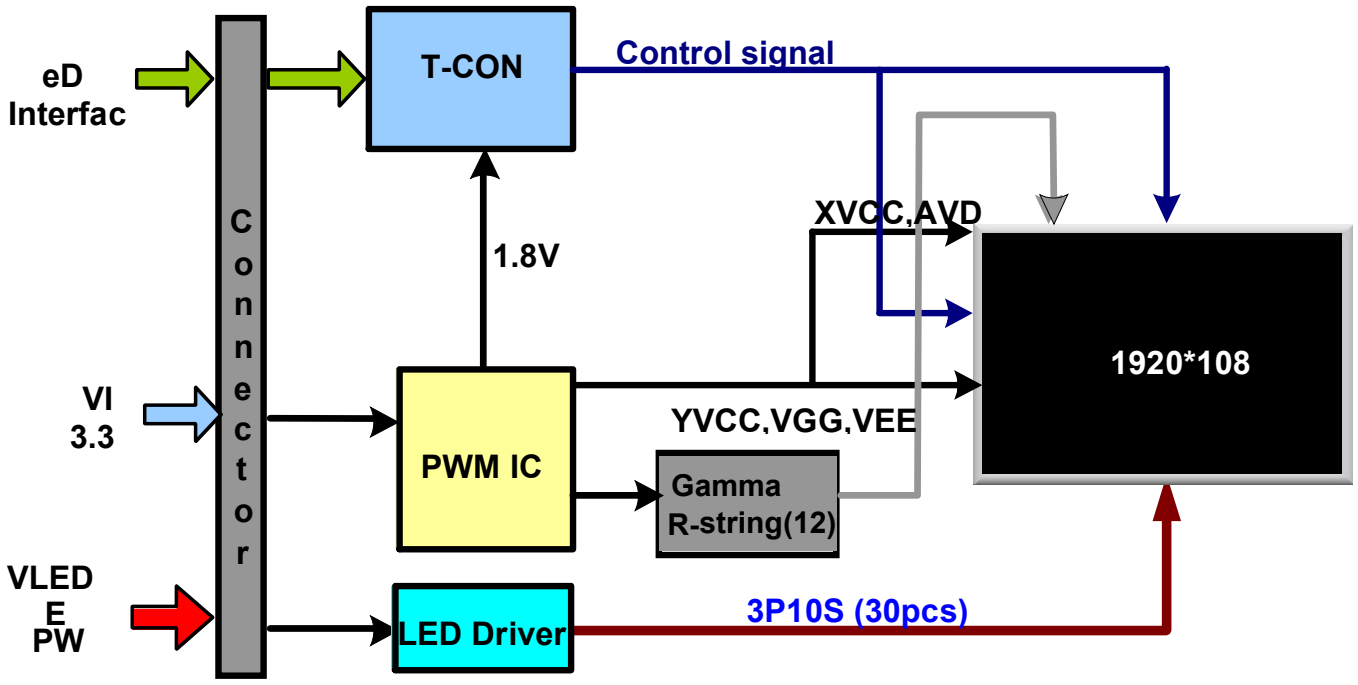
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

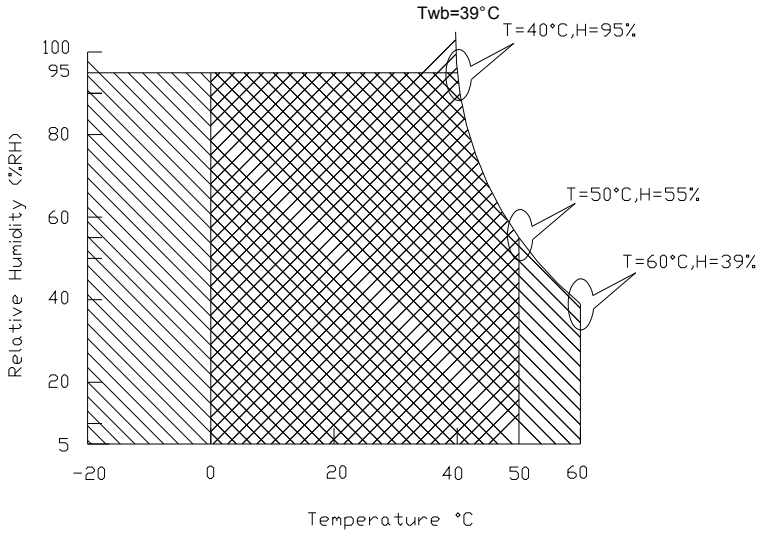
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

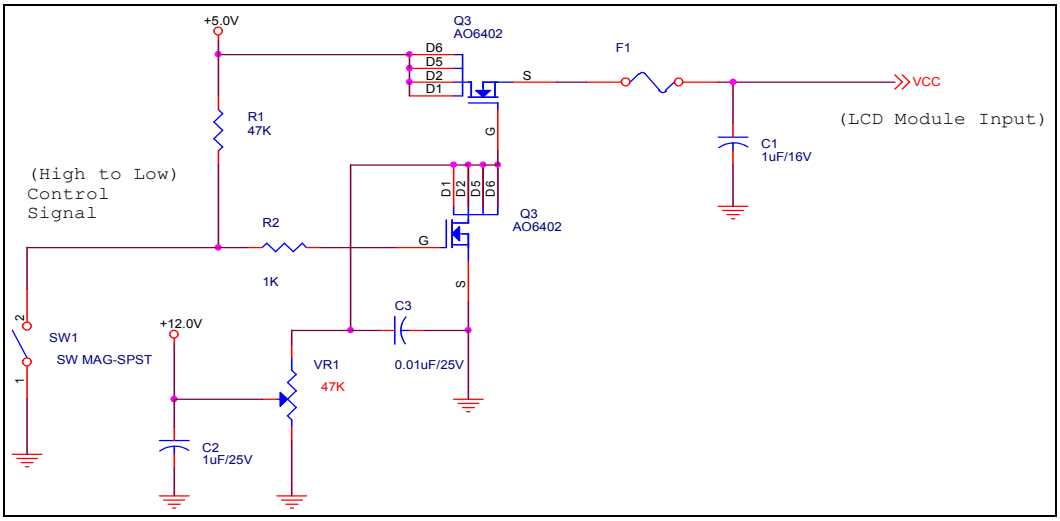
The power specification are measured under 25℃ and frame frenquency under 60Hz

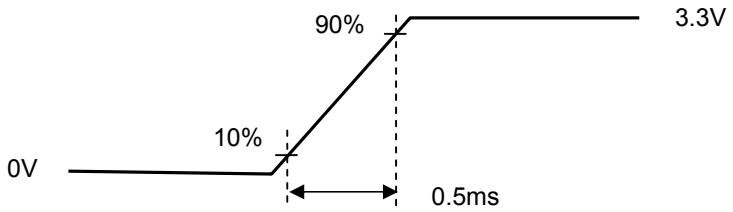
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	_	-	1000	[mW]	Note 1
IDD	IDD Current	_	_	303	[mA]	Note 1
IRush	Inrush Current	_	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Typical Measurement Condition: Mosaic Pattern

Note 2 : Measure Condition





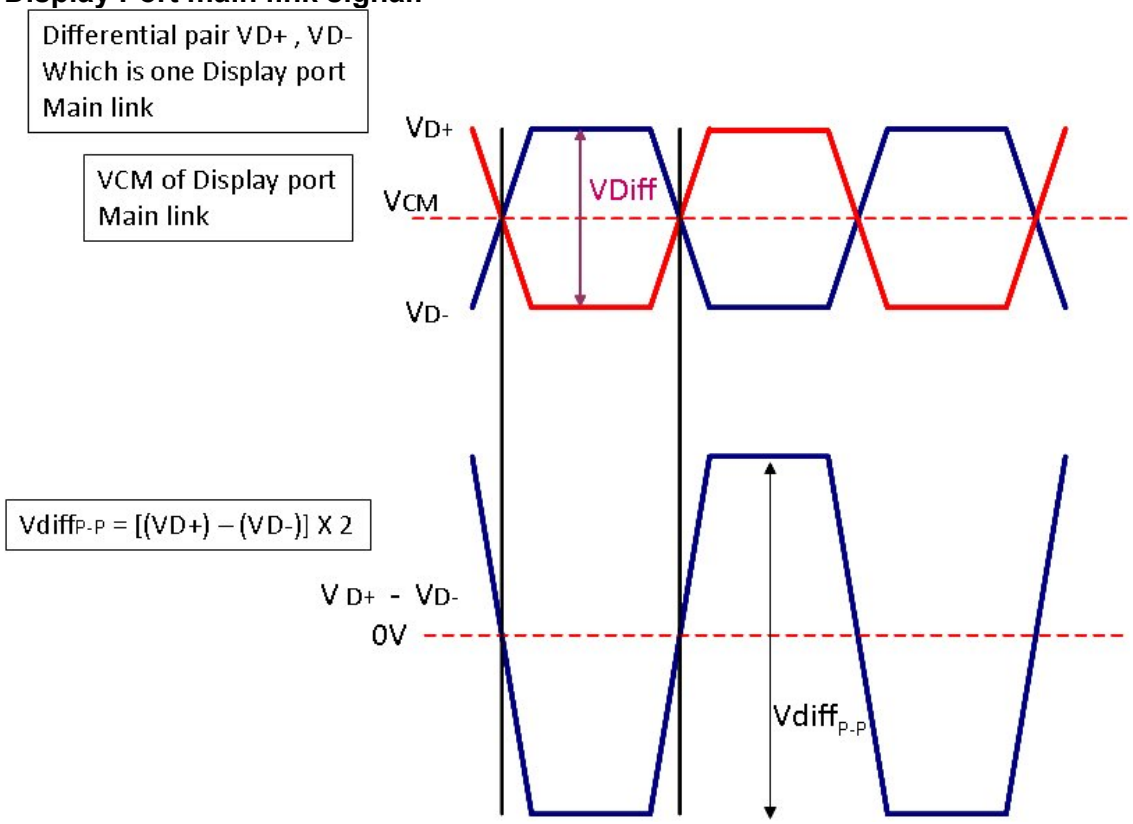
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

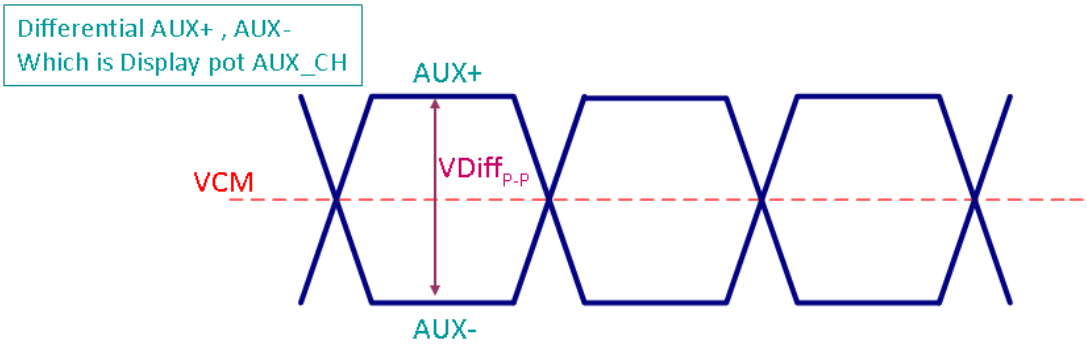
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.2	[Watt]	(Ta=25℃), Note 1
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=19mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0 (*Note 2)	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.2	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.2	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency *1	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1 (*Note 3)	--	100	%	

Note1: Recommend system pull up/down resistor no bigger than 10Kohm

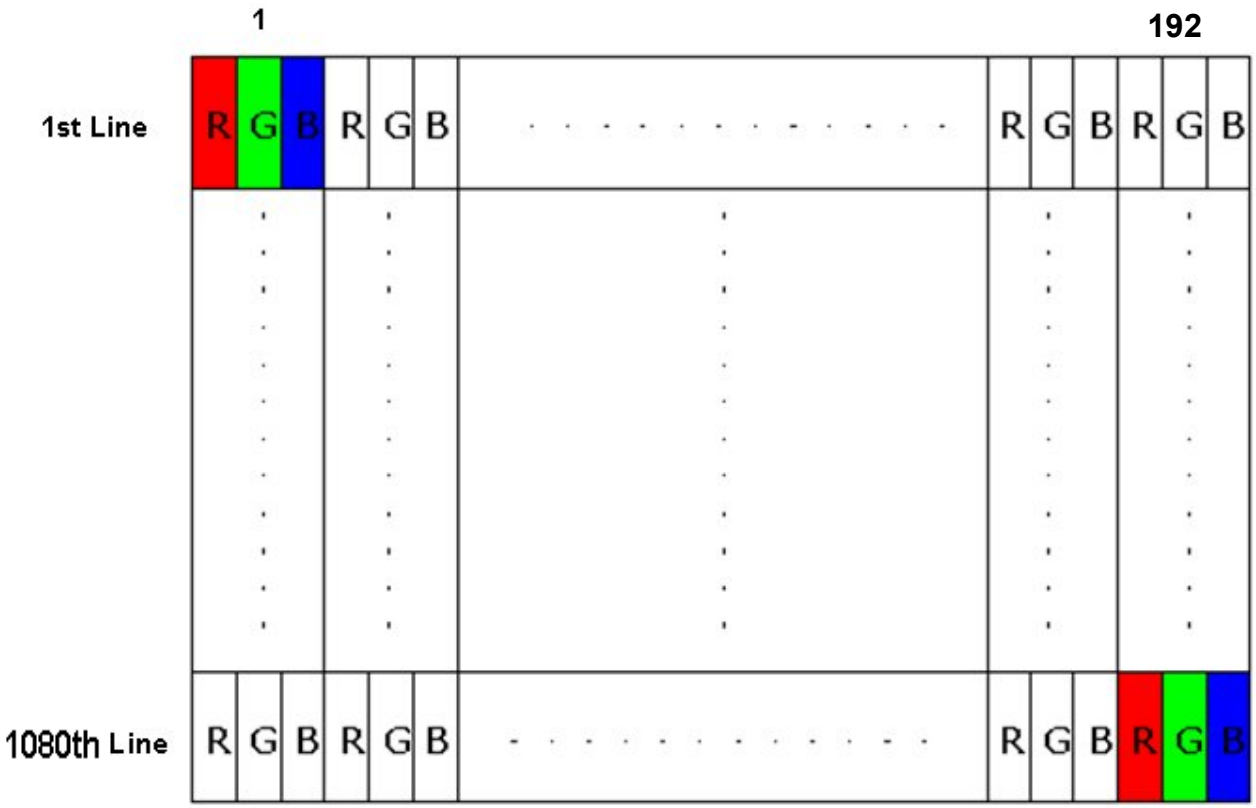
Note 2: Measured in panel VIN

Note 3: If the PWM duty ratio(min) is set between 5% to 1%, the PWM input frequency should be set below 1KHz. The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

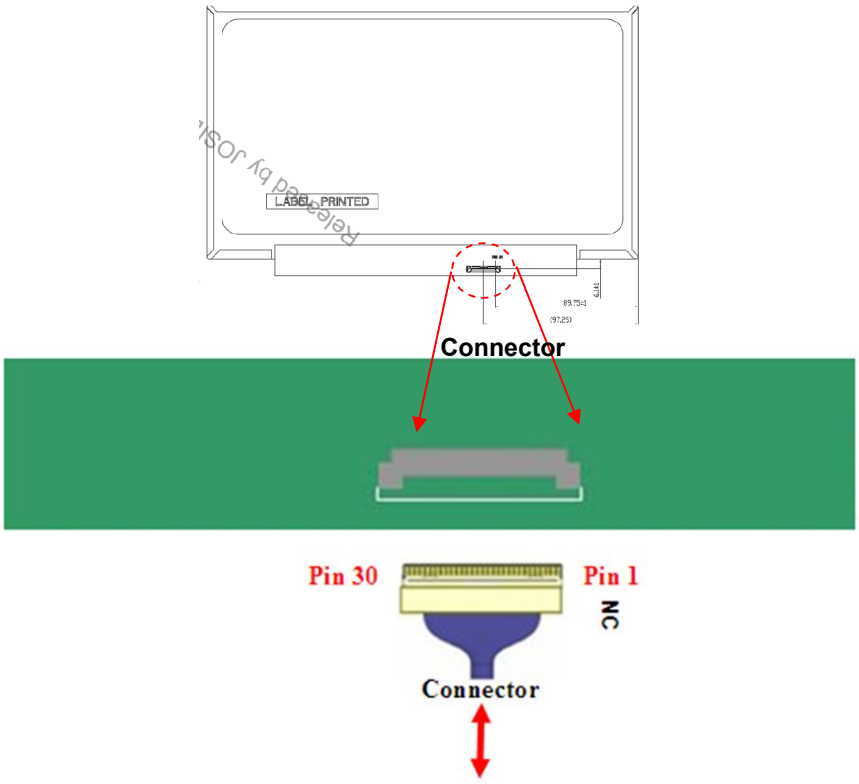
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or Compatible
Type / Part Number	STM MSAK24025P30M or Compatible
Mating Housing/Part Number	I-PEX 20453-030T-11 or Compatible

6.2.2 Pin Assignment

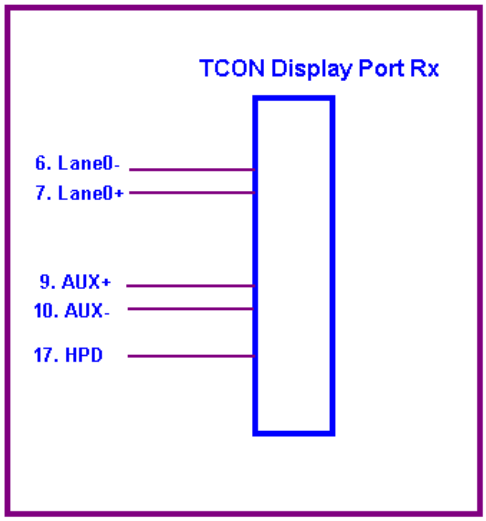
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal Name	Description
1	NC	NC
2	GND	Ground
3	Lane1_N	Signal Link Lane 1_N
4	Lane1_P	Signal Link Lane 1_P
5	GND	Ground
6	Lane0_N	Signal Link Lane 0_N
7	Lane0_P	Signal Link Lane 0_P
8	GND	Ground
9	AUX _P	Signal Auxiliary Channel_P
10	AUX _N	Signal Auxiliary Channel_N
11	GND	Ground
12	VDD	LCD logic and driver power
13	VDD	LCD logic and driver power
14	AGING	LCD Panel Self Test
15	GND	Ground
16	GND	Ground
17	HPD	HPD signal pin
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	LED_EN	Backlight On/Off
23	LED_PWM	System PWM signal input for dimming
24	NC-Reserved	Reserved for LCD manufacture's use(EDID_CLK)
25	NC-Reserved	Reserved for LCD manufacture's use(EDID_DATA)
26	V_LED	Backlight power
27	V_LED	Backlight power
28	V_LED	Backlight power
29	V_LED	Backlight power
30	NC	NC



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

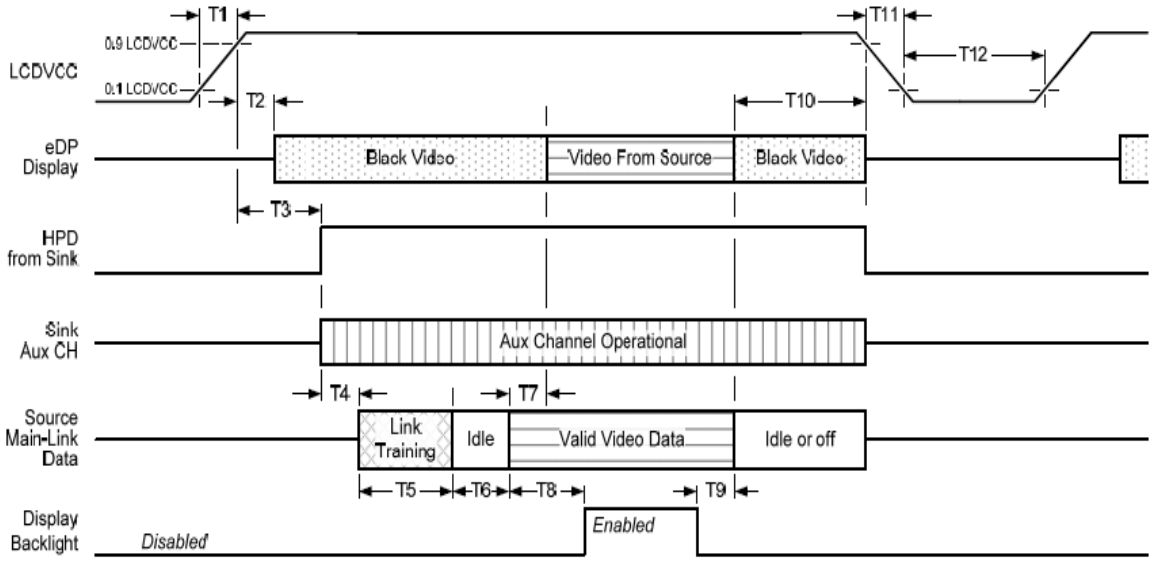
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}		138.5		MHz
Vertical Section	Period	T_V	1084	1111	1080+A	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	4	30	A	
Horizontal Section	Period	T_H	2050	2080	1920+B	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	130	160	B	

Note 1: DE mode olny

Note 2: The maximum clock frequency = (1920+B)*(1080+A)*60 < 149.1 MHz

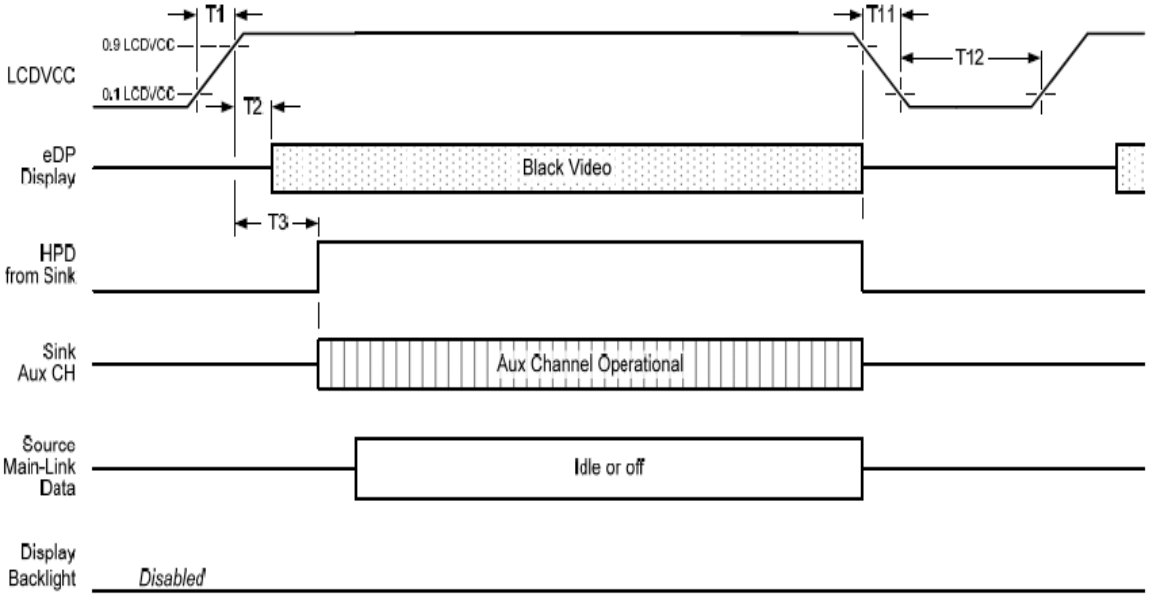
6.4 Power ON / OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

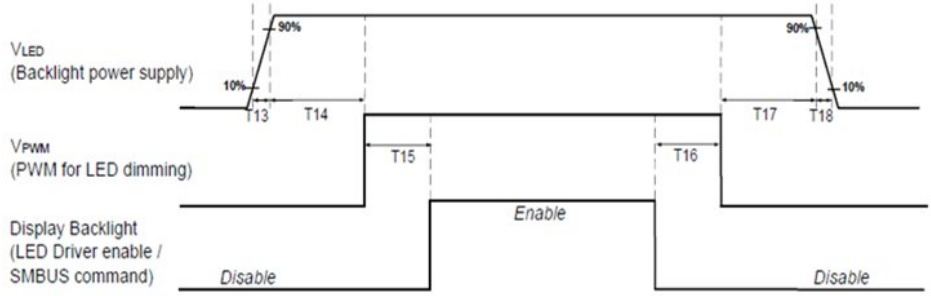
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

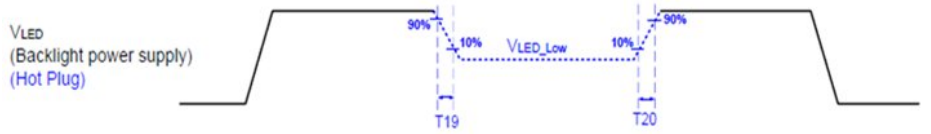


	Min (ms)	Max (ms)
T13	0.2	10
T14	0	-
T15	0	-
T16	0	-
T17	0	-
T18	0.2	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Note 1: If T14, T15, T16, T17 <10ms, the display garbage may occur. We suggest T14, T15, T16, T17 >10ms to avoid the display garbage.

Note 2: If T13 or T18 <0.5ms, the inrush current may cause the damage of fuse. If T13 or T18 <0.5ms, the inrush current I^2t is under typical melt of fuse Spec., there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	**Ta= 40℃, 90%RH, 300h**	
High Temperature Operation	**Ta= 50℃, Dry, 300h**	
Low Temperature Operation	**Ta= 0℃, 300h**	
High Temperature Storage	**Ta= 60℃, 300h**	
Low Temperature Storage	**Ta= -20℃, 300h**	
Thermal Shock Test	**Ta=-20℃(30min) ~ 60℃(30min), 100 cycles condition**	
ESD	**Contact : ±8 KV** **Air : ±15 KV**	Note 1

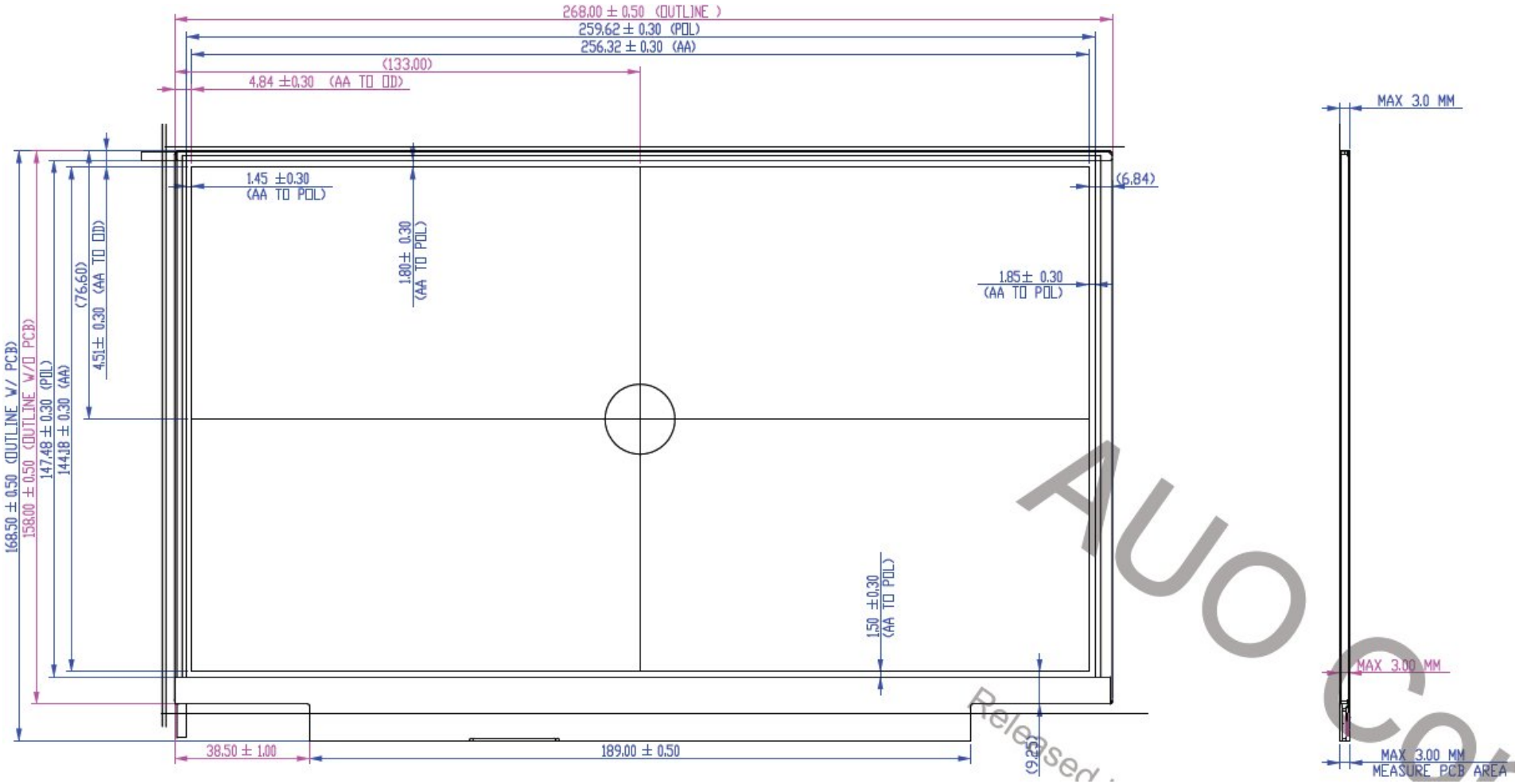
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

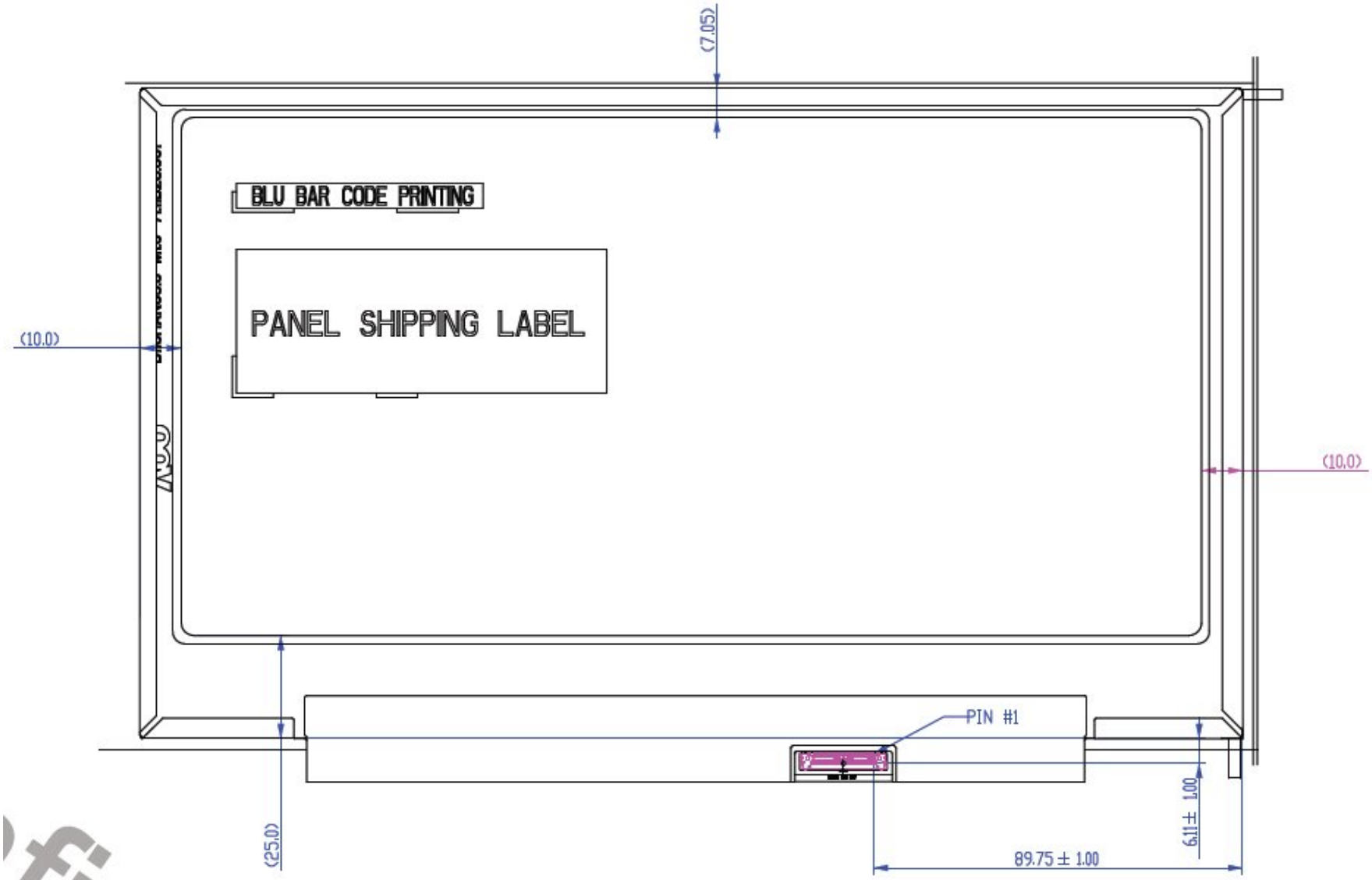
8. Mechanical Characteristics

8.1 LCM Outline Dimension

8.1.1 Standard Front View



8.1.2 Standard Rear View



9. Shipping and Package

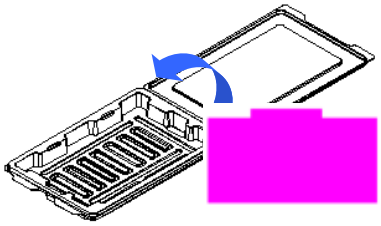
9.1 Shipping Label Format

9.2 Carton Label Format

9.3 Carton Package

不撕膜-撕膜把手貼在 P 板側的左上角.

Not tear film model. Please stick pull tape at top left corner of P board side.

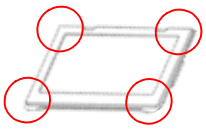


面板朝上.先放入 1PCS Spacer 再放入 1PCS Panel，共放入 4PCS PANEL ＋5PCS SPACER.

The module must be face up. First put in a piece of spacer then a piece of panel. Total 4 pieces of panel and 5 pieces of spacer in one tray box.

將 TRAY BOX 上蓋蓋上.

Cover the trav box.

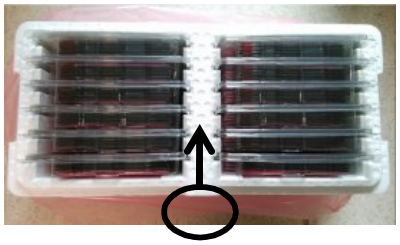


Check TRAY BOX 四周是否確實緊密配合.

Check whether all round of the tray box is closely match up.

➢將 EPS box 放入靜電袋中.

Put EPS box into anti-static bag.

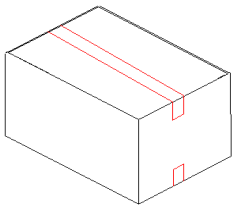


➢Tray Box 左右放置於 EPS 內，正面朝向 EPS box 箭頭所指方向，一邊放六盒共 12 盒。

Place tray boxes at left and right side of EPS box, attention the cover of tray box must toward the direction of arrow on the EPS box. Shown in the above

➢蓋上 EPS box 的蓋子，並用透明膠帶密封靜電袋，將靜電袋放入紙箱中。

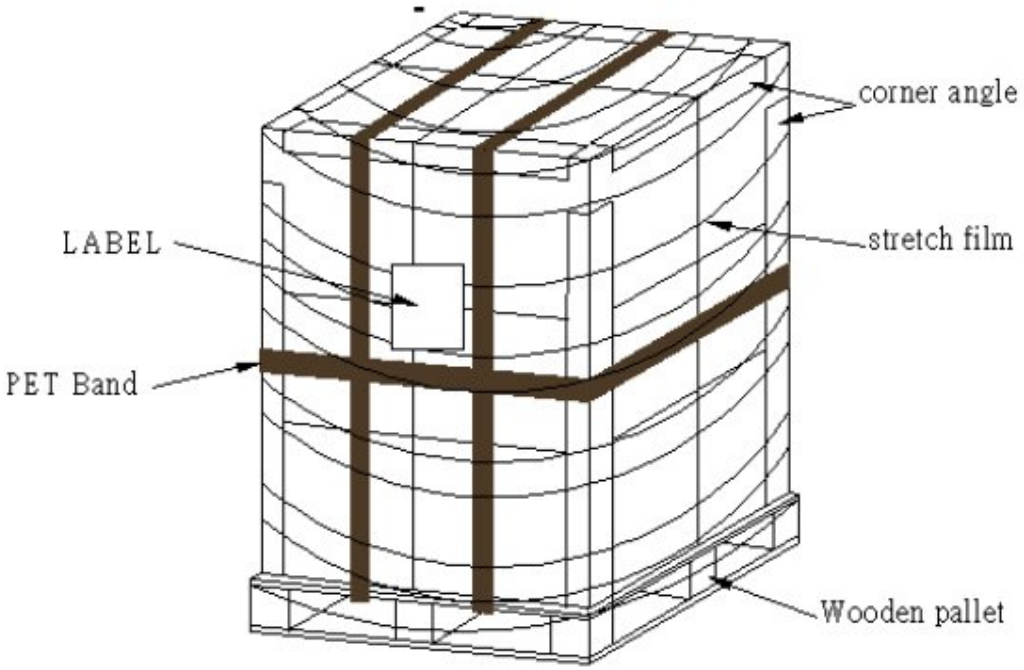
Cover the lid of EPS box, and seal anti-static bag with transparent tape, then put anti-static bag into carton.



➢合上紙箱的蓋子，並用透明膠帶密封。

Cover the lid of carton, and seal it with transparent tape.

9.4 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	5D	01011101	93	
0B	hex, LSB first	50	01010000	80	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	1A	00011010	26	
11	Year of manufacture	18	00011000	24	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A5	10100101	165	
15	**Max H image size** *(rounded to cm)*	1A	00011010	26	
16	**Max V image size** *(rounded to cm)*	0E	00001110	14	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	0A	00001010	10	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	A4	10100100	164	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	15	00010101	21	
1B	Red x **(Upper 8 bits)**	9E	10011110	158	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	4E	01001110	78	
1E	Green y	9B	10011011	155	
1F	Blue x	26	00100110	38	
20	Blue y	0F	00001111	15	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	

24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	3D	00111101	61	
37	Pixel Clock/10000 USB	37	00110111	55	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	BC	10111100	188	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	38	00111000	56	
3C	Vertical Blanking **Lower 8bits**	26	00100110	38	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	3A	00111010	58	
3F	HorzSync.Width	2A	00101010	42	
40	VertSync.Offset : VertSync.Width	8E	10001110	142	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	00	00000000	0	
43	Vertical Image Size **Lower 8bits**	90	10010000	144	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	

4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	31	00110001	49	1
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N

78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	35	00110101	53	5
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	61	01100001	97	