( ) Preliminary Specifications
(✓) Final Specifications

Module	15.6"FHD Color TFT-LCD
Model Name	G156HAN03.0
Note	LED backlight with driving circuit design

Customer	Date	Approved by	Date
			01/02/2019
Checked & Approved by	Date	Prepared by	Date
			01/02/2019
Customer's sign back page		General Display Business Division / AU Optronics corporation	

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1. Handling Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any direction.
9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
15) The data on this specification sheet is applicable when LCD module is placed in landscape position.
16) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.

2. General Description

G156HAN03.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.2M colors (RGB 6-bits+2FRC data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

G156HAN03.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	15.6"			
Active Area	[mm]	344.16 x 193.59			
Resolution		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.17925 x 0.17925			
Pixel Arrangement		R.G.B. Vertical Stripe			
Display Mode		AHVA, Normally Black			
Nominal Input Voltage VDD	[Volt]	+3.3 (Typ.)			
LCD Power Consumption	[Watt]	0.8W (Max.)			
LED Power Consumption	[Watt]	4.0W (Max.)			
Weight	[Grams]	370 (Max)			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length	350.36	350.66	350.96
		Width	215.65	216.15	216.65
		Thickness			3.2
Electrical Interface		2 Lane eDP1.2			
Surface Treatment		Anti-glare, 3H			
Support Color		16.2M colors			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -0 to +50 -20 to +60			
RoHS Compliance		Yes, RoHS Compliance			

2.2 Optical Characteristics

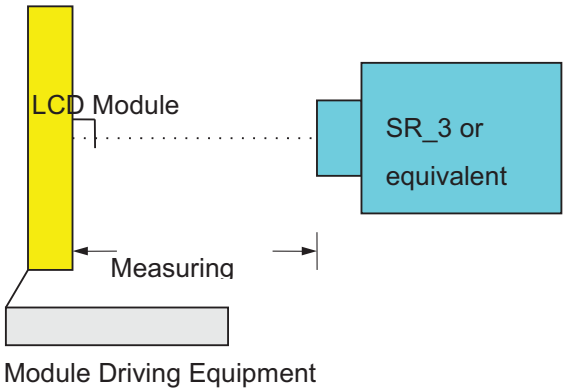
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance		cd/m^2	I_{LED}=50mA Center average	255	300	-	1, 2
Luminance Uniformity		%	9 Points	75	80		1, 2 , 3
Contrast Ratio		--		700	1000	-	1, 4
Response Time		msec	Rising + Falling	-	25	35	1, 5
Viewing Angle		degree	Horizontal (Right) CR = 10 (Left)	80 80	89 89	- -	1, 6
			Vertical (Upper) CR = 10 (Lower)	80 80	89 89	- -	
Color / Chromaticity Coodinates (CIE 1931)	Red	Rx	CIE 1931	0.534	0.584	0.634	4
		Ry		0.291	0.341	0.391	
	Green	Gx		0.29	0.34	0.39	
		Gy		0.526	0.576	0.626	
	Blue	Bx		0.108	0.158	0.208	
		By		0.080	0.130	0.18	
	White	Wx		0.263	0.313	0.363	
		Wy		0.279	0.329	0.379	
Color Gamut		%		-	45	-	

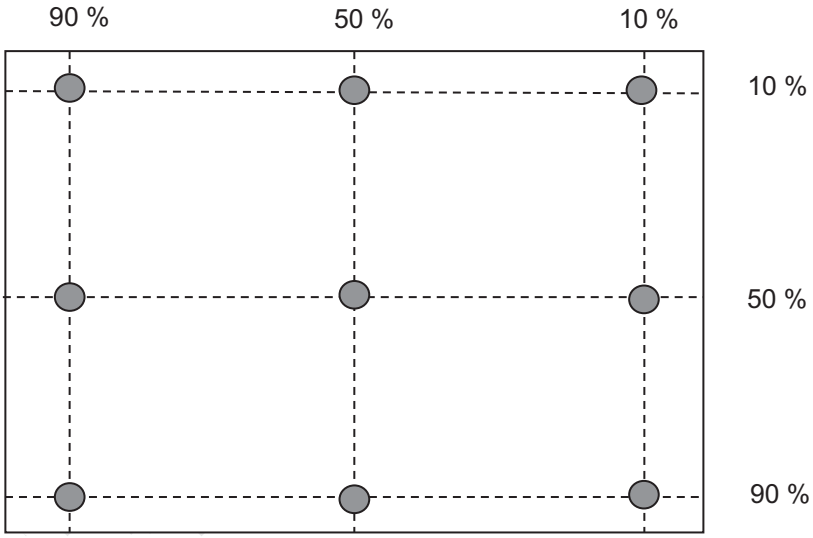
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

Aperture 1◦ with 50cm viewing distance
Test Point Center
Environment < 1 lux



Note 2: 9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance. And measured by TOPCON SR-3

$$\delta_{W9} = \frac{\text{Minimum Luminance of 9 points}}{\text{Maximum Luminance of 9 points}}$$

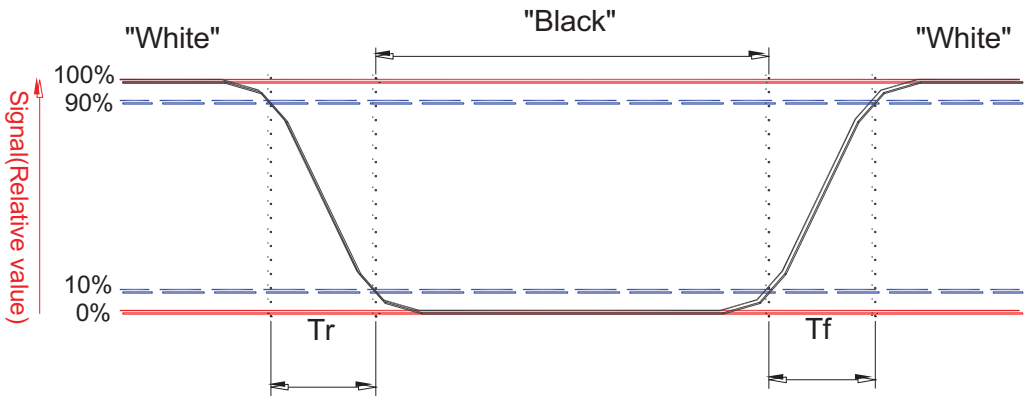
Note 4 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

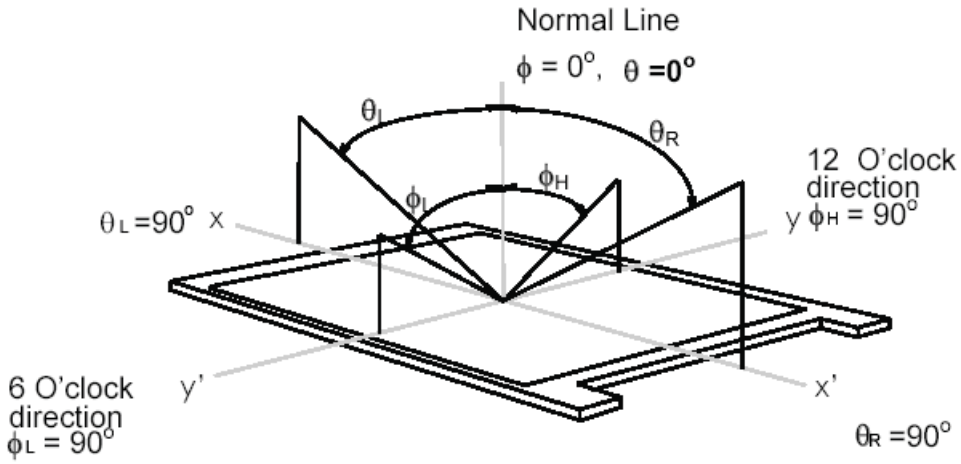
Note 5: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



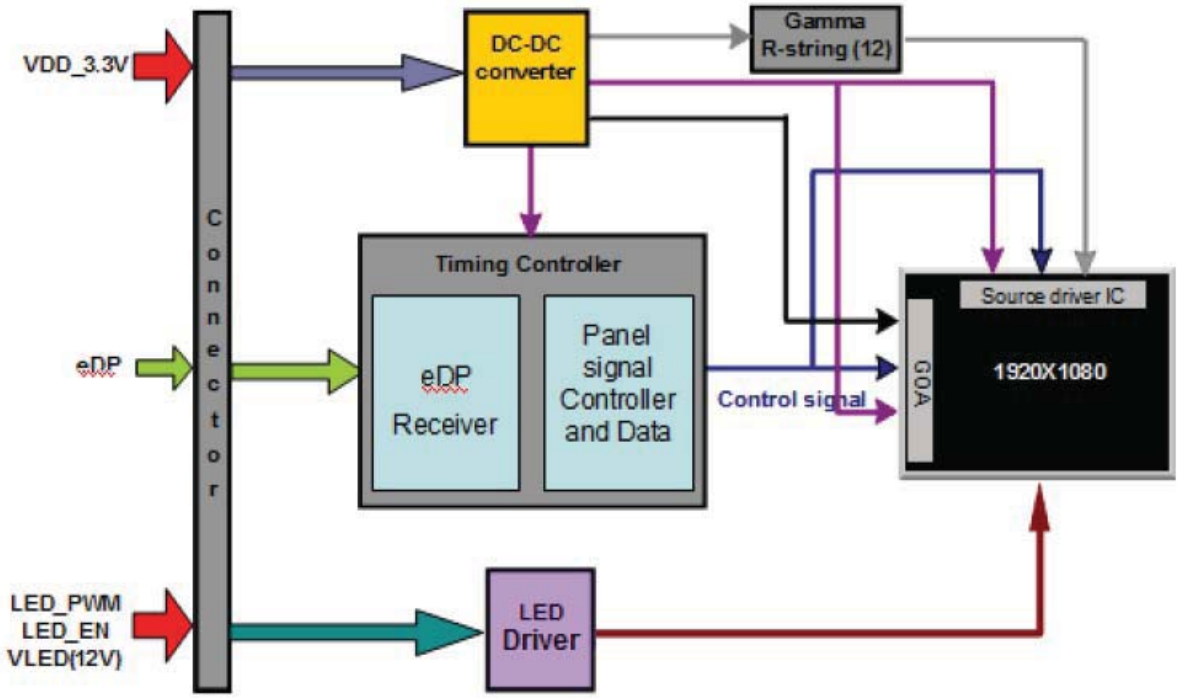
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD module.



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

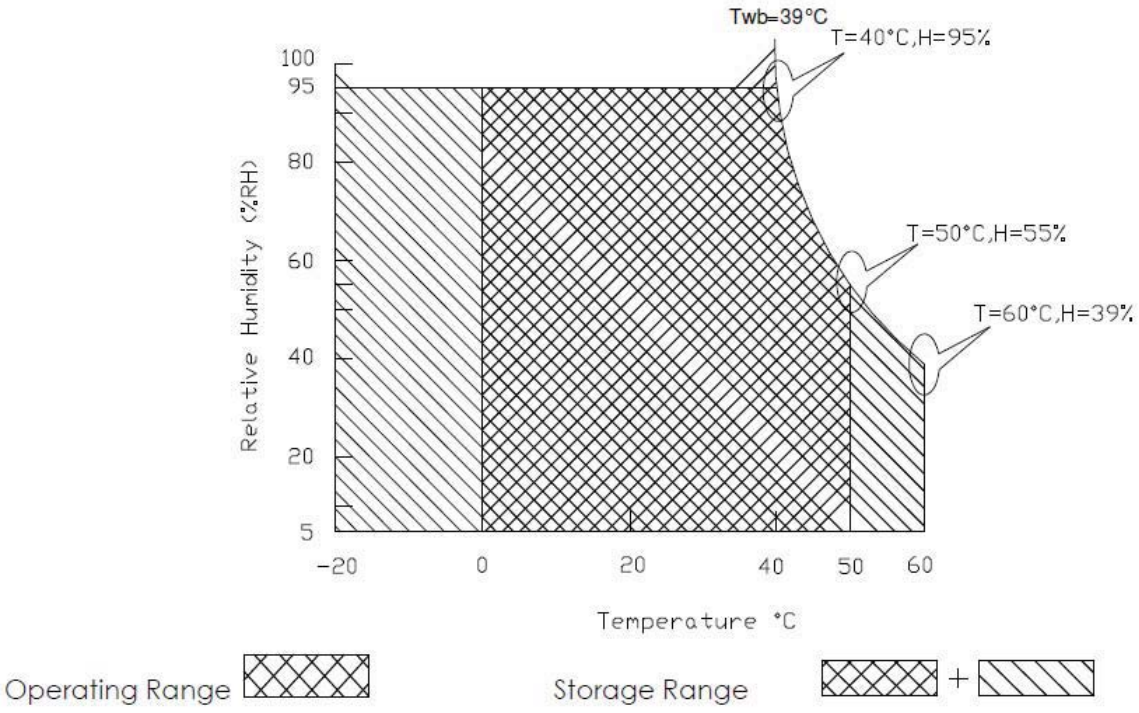
4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)
Note 2: Permanent damage to the device may occur if exceed maximum values
Note 3: LED specification refer to section 5.2
Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

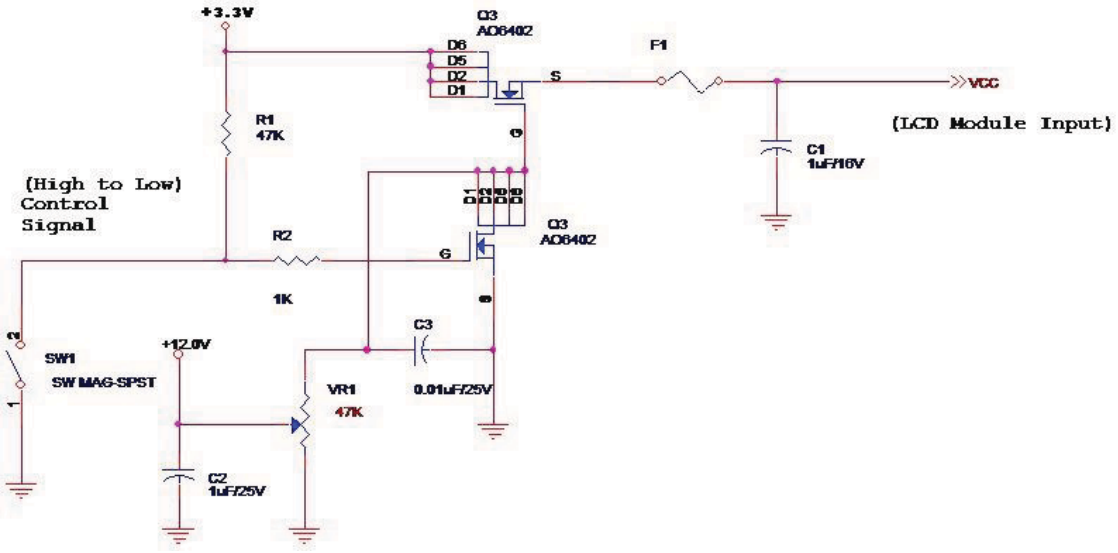
Input power specifications are as follows;

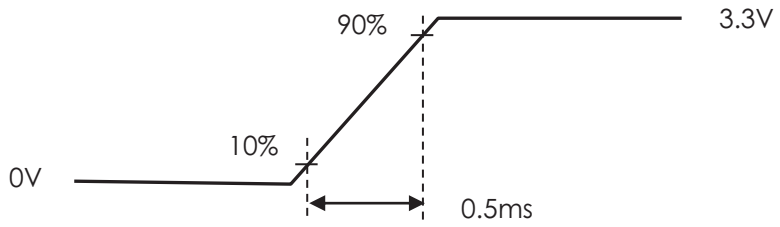
The power specification are measured under 25℃ and frame frenquency under 60Hz.

Symble	Parameter	Min	Typ	Max	Units	Remark
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	All Black Pattern (VDD=3.3V, at 60Hz)
IDD	IDD Current	-	-	0.22	[mA]	All Black Pattern (VDD=3.3V, at 60Hz)
IRush	Inrush Current	-	-	2000	[mA]	Note 1
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	All Black Pattern (VDD=3.3V, at 60Hz)

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. (Pmax=V3.3 x Iwhite)
Typical Measurement Condition: Mosaic Pattern

Note 2 : Measure Condition



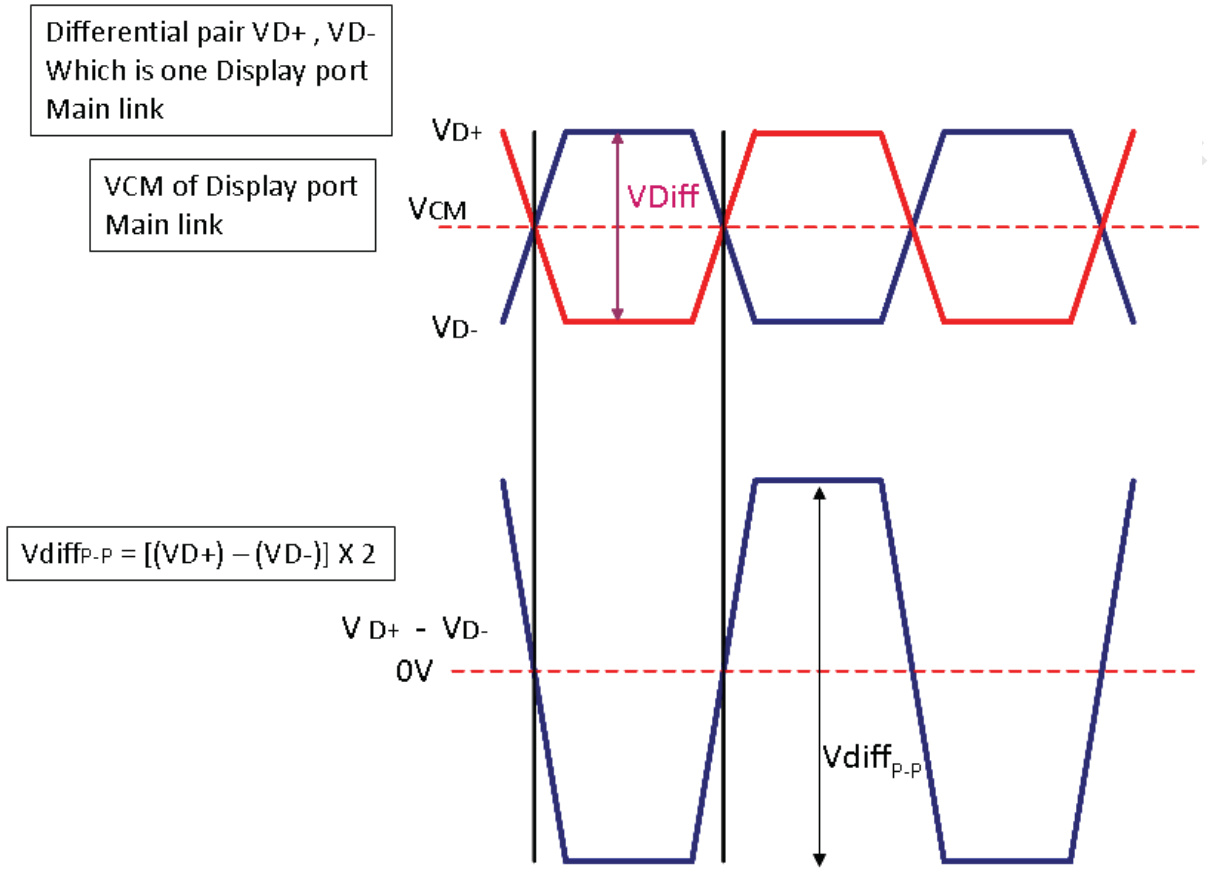


Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off. Signal electrical characteristics are as follows;

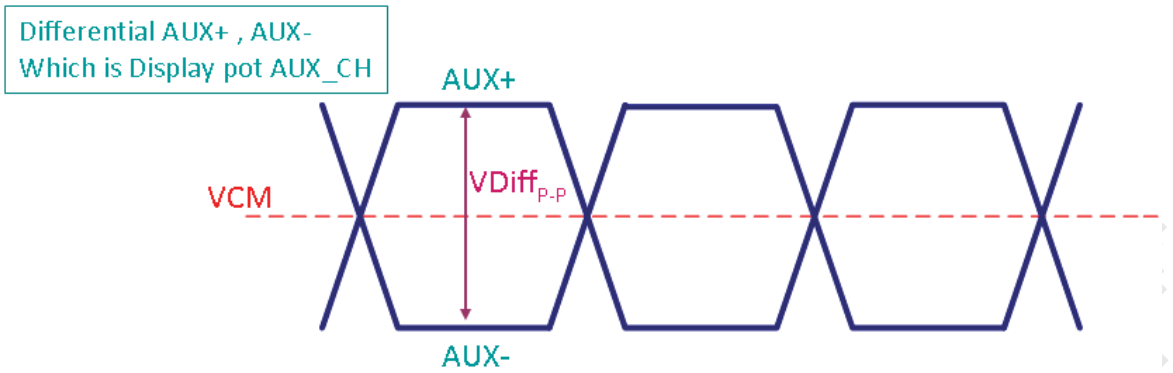
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff$_{P-P}$	Peak-to-peak Voltage at a receiving Device	150		1320	mV

Fallow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	3.6	4.0	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	30,000	-	-	Hour	(Ta=25℃), Note 2,3

Note 1: Ta means ambient temperature of TFT-LCD module. Calculator value for reference PLED = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: If G156HAN03.0 module is driven at high ambient temperature & humidity condition. The operating life will be reduced.

Note 3: Operating life means brightness goes down to 50% initial brightness. Min. operating life time is estimated data.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		0	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		0	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	-	100	%	

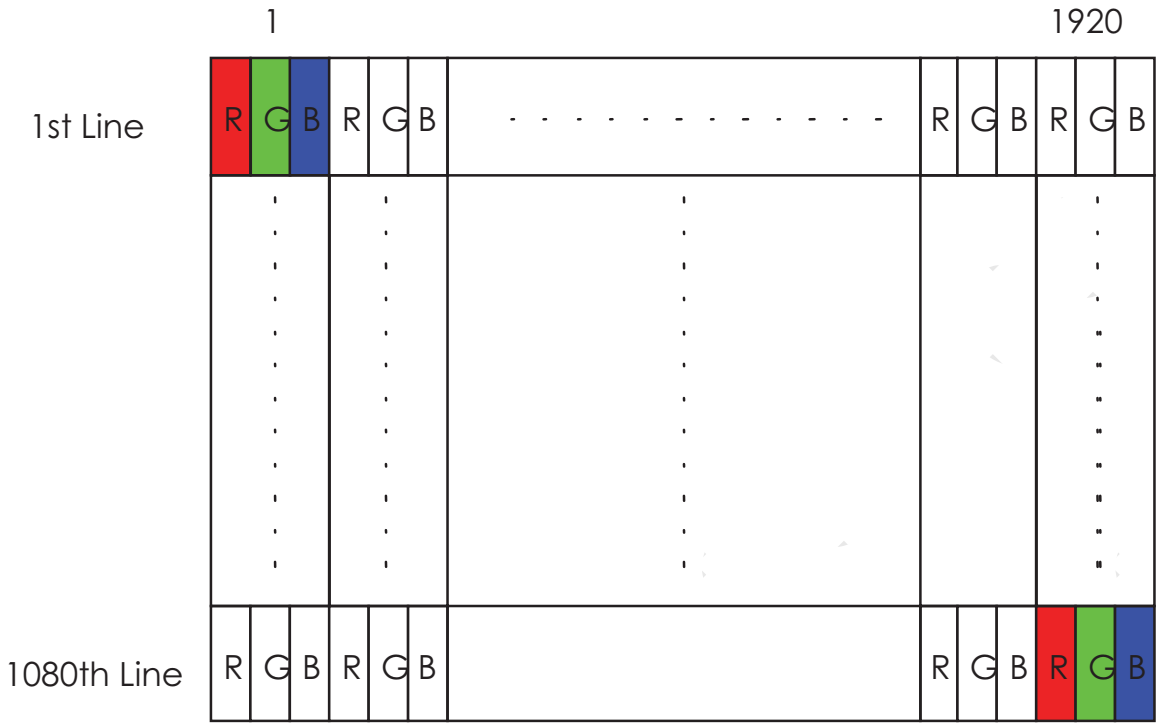
Note 1 : Recommanded system pull up/down resistor no bigger than 10kohm.

Note 2 : If the PWM duty ratio(min) is set between 5% to 1%，the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20765-030E-11A or compatible
Mating Housing/Part Number	IPEX 20453-030T-11 or compatible

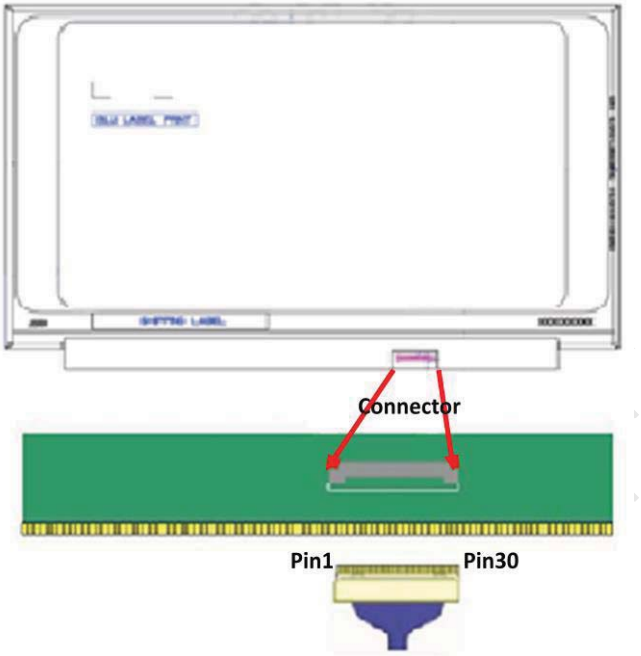
6.2.2 Pin Assignment (2 Lane)

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN No	Symbol	Function
1	NC	No Connect (Reserved for CM)
2	BL_PWR	Backlight power
3	BL_PWR	Backlight power
4	BL_PWR	Backlight power
5	BL_PWR	Backlight power
6	NC	No connect (Reverse for AUO TEST only)
7	NC	No connect (Reverse for AUO TEST only)
8	BL PWM DIM	System PWM signal Input
9	BL_Enable	Backlight On / Off
10	BL_GND	Backlight_ground
11	BL_GND	Backlight_ground
12	BL_GND	Backlight_ground
13	BL_GND	Backlight_ground
14	HPD	HPD signal pin
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	LCD_Self_Test	LCD Panel Self Test Enable
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	H_GND	High Speed Ground
21	AUX_CH_N	Comp Signal Auxiliary Ch.
22	AUX_CH_P	True Signal Auxiliary Ch.
23	H_GND	High Speed Ground
24	Lane0_P	True Signal Link Lane 0
25	Lane0_N	Comp Signal Link Lane 0
26	H_GND	High Speed Ground
27	Lane1_P	True Signal Link Lane 1
28	Lane1_N	Comp Signal Link Lane 1

29	H_GND	High Speed Ground
30	NC	No Connect

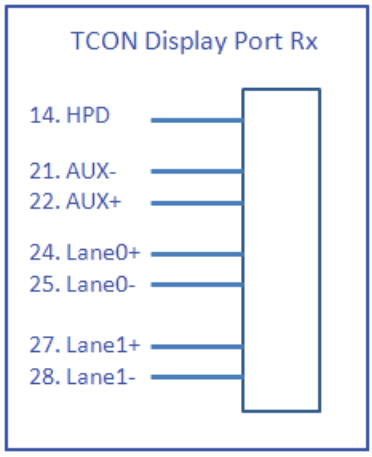
6.2.3 Connector Illustration



Note1：start from Left side refer to next page illustration.

Note2：Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of eDP inputs are as following.

Note3：Connector Illustration



6.3 Interface Timing

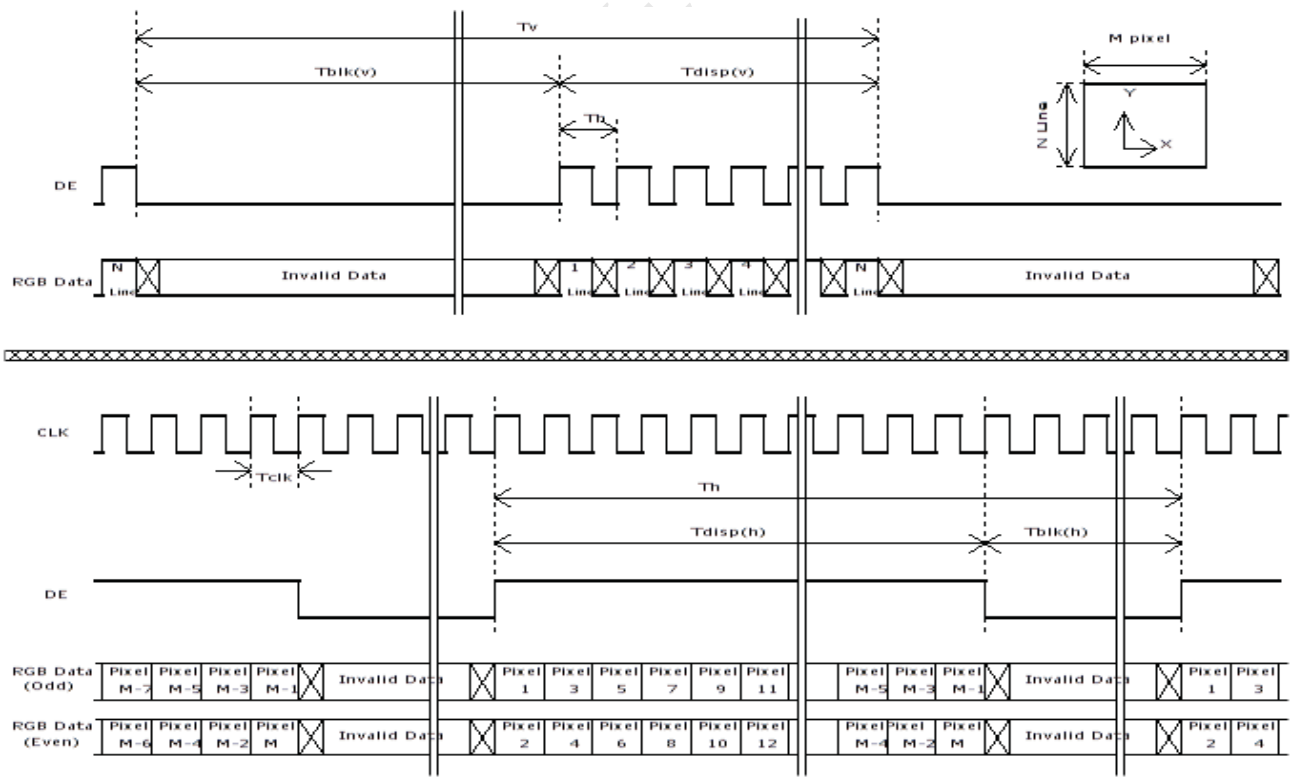
6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	-	141	-	MHz
Vertical Section	Period	T_V	1124	1128	1080+A	T_{Line}
	Active	T_{VD}	1080			
	Blanking	T_{VB}	44	48	A	
Horizontal Section	Period	T_H	2076	2082	1920+B	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	156	162	B	

Note 1 : DE mode only
Note 2 : The maximum clock frequency = (1920+B)*(1080+A)*60 < 150MHz
Note3 : Typical value refer to VESA STANDARD

6.3.2 Input Timing Diagram

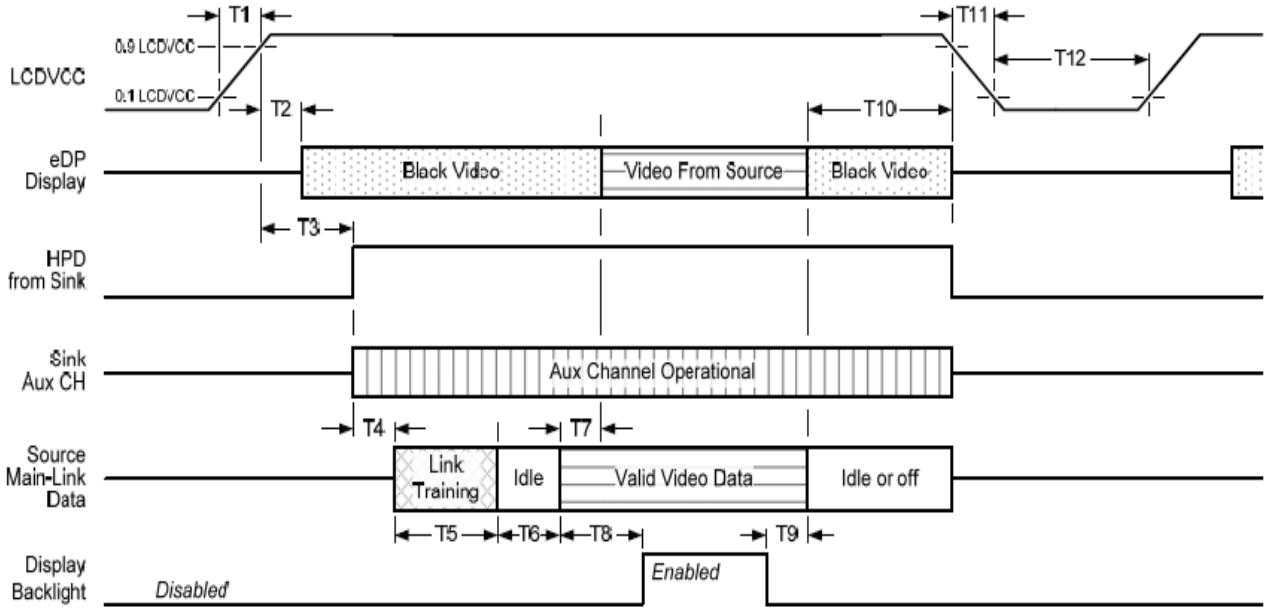


6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

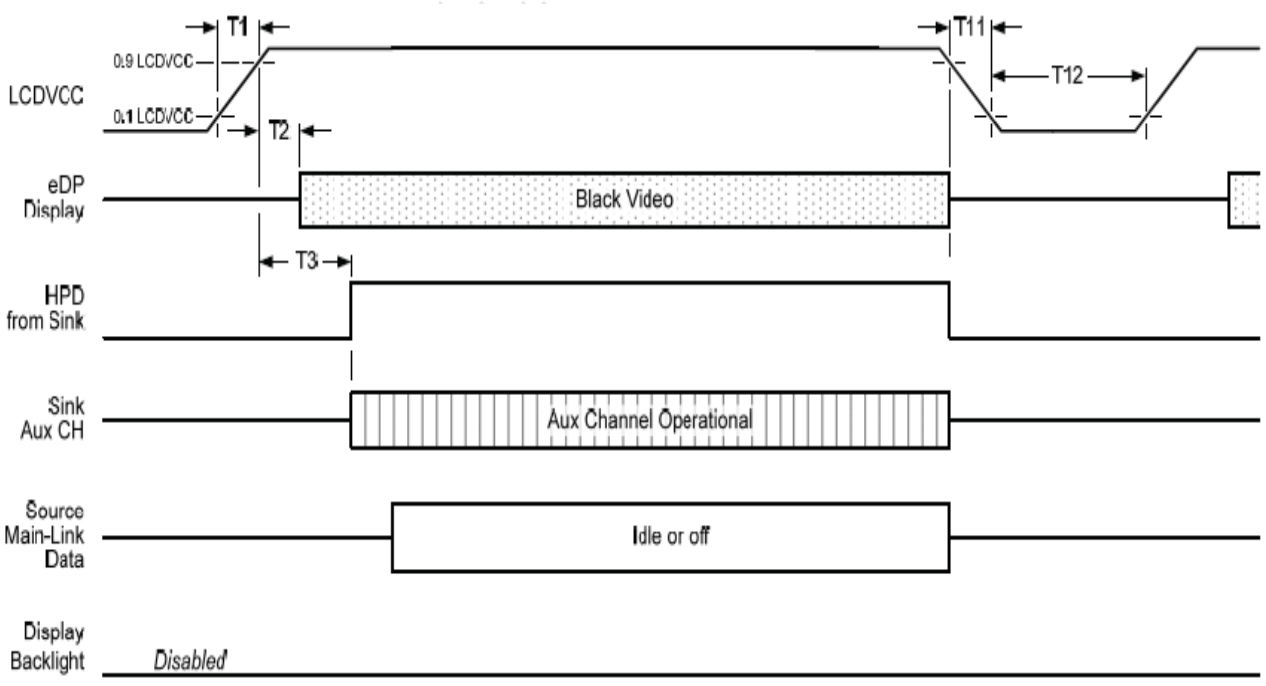
Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

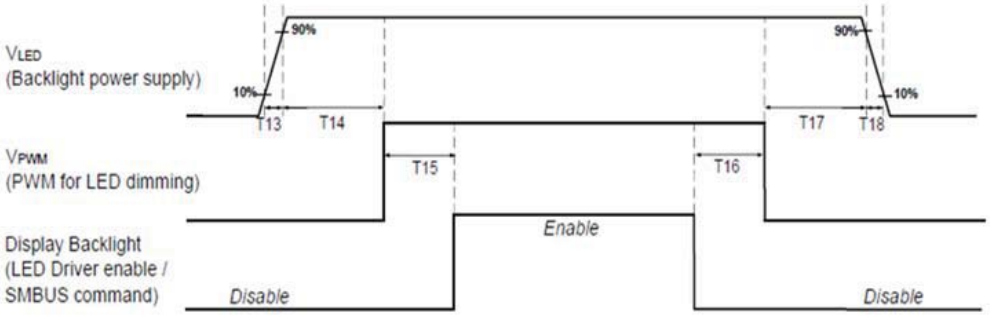
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCD VDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

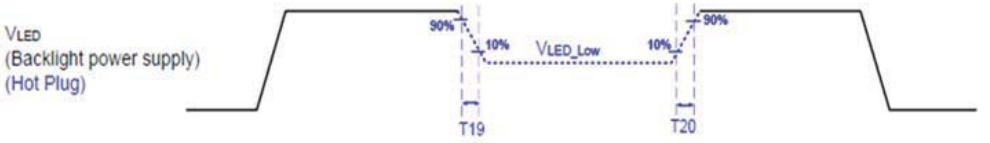


	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



7. Panel Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	Note 1,2
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH,300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 300h	
Thermal Shock Test	Ta= -20℃to 60℃, Duration at 30 min, 100 cycles	
Vibration	Test method: Non-Operation Acceleration: 1.5 G Frequency: 10 - 200 -10Hz Sweep: Sine wave vibration; 30 minutes each axis (X, Y, Z)	
Mechanical Shock	Test method: Non-Operation Acceleration: 220 G; Wave: Half-sine Active time: 2ms Direction: ±X,±Y,±Z (one time for each axis)	
ESD	Contact : ±8 KV / Operation, Class B Air : ±15 KV / Operation, Class B	Note 1

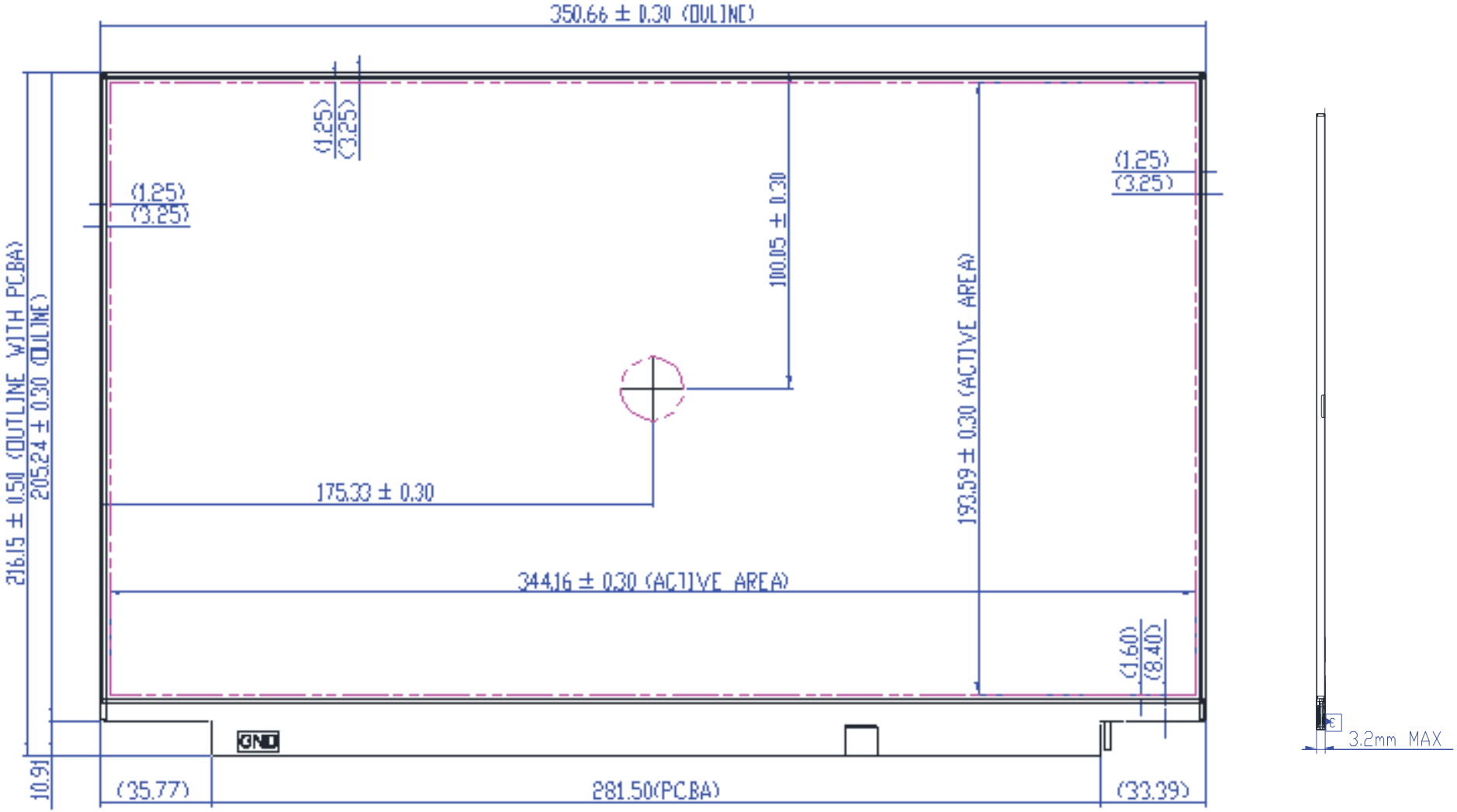
Note 1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures.

Note 2:

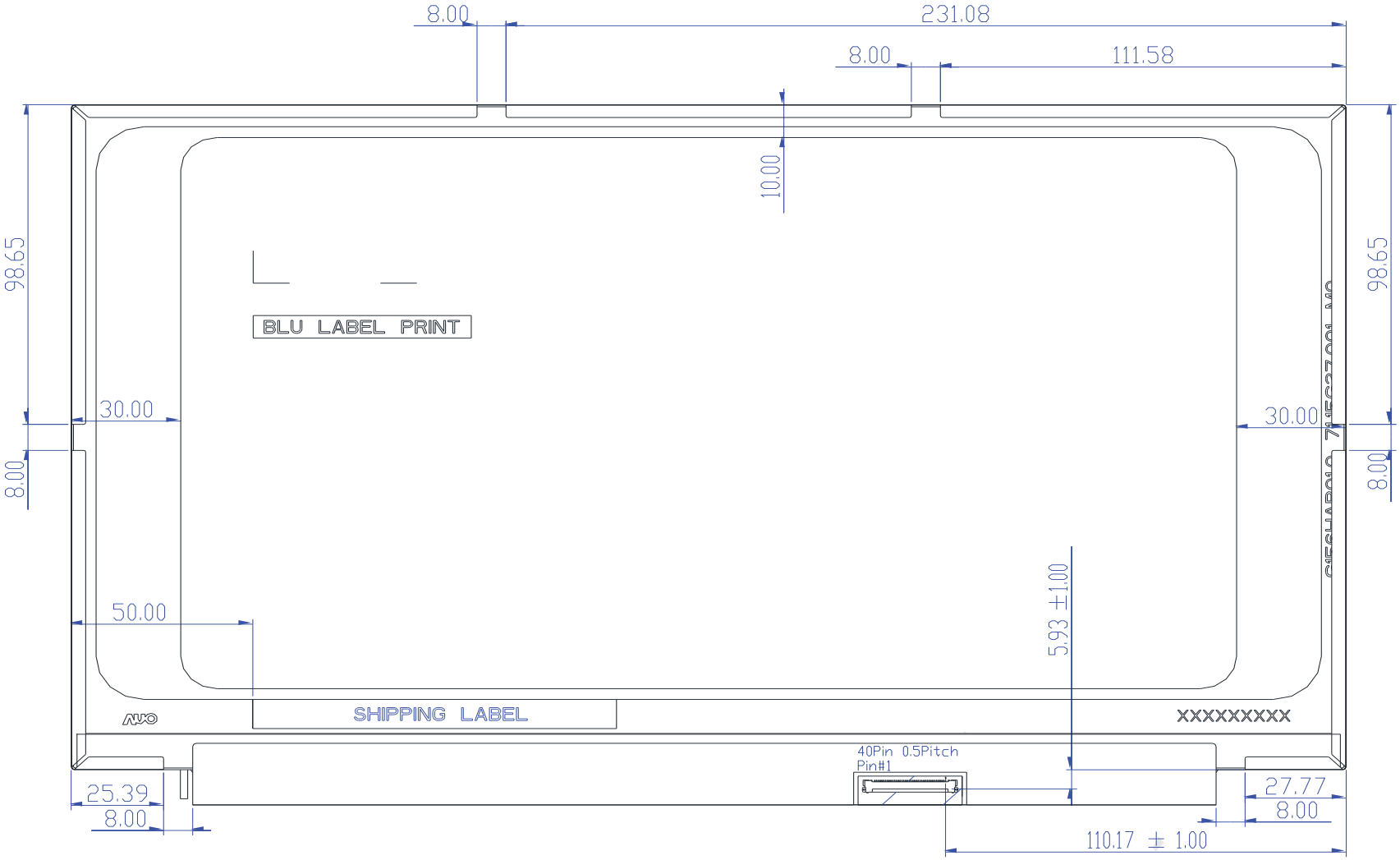
- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.
- No function failure occurs. Mura shall be ignored after high temperature reliability test

8. Mechanical Characteristics

8.1 LCM Outline Dimension (Front View)

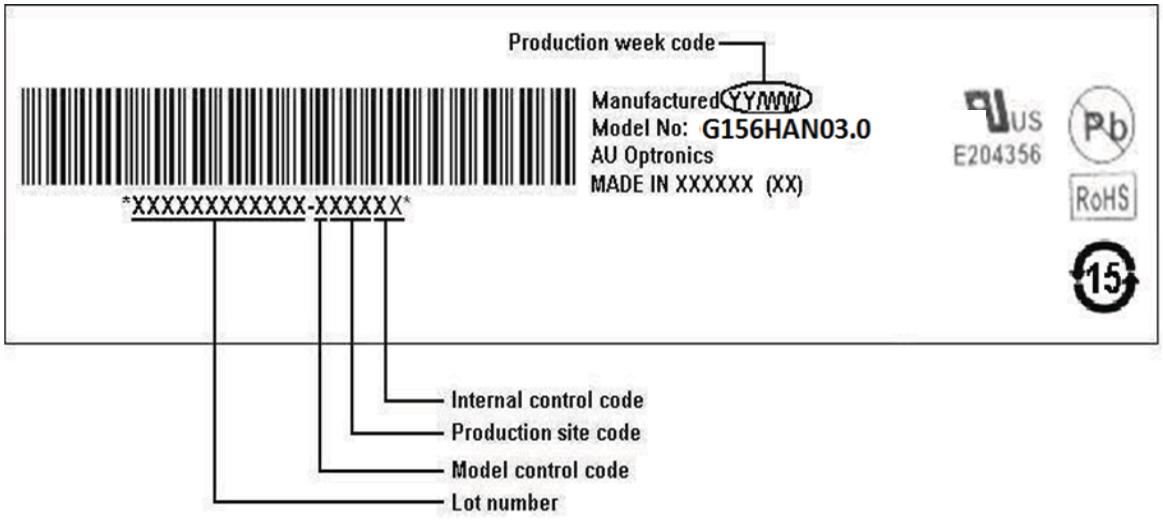


8.2 LCM Outline Dimension (Rear View)



9. Shipping and Package

9.1 Shipping Label (on the rear side of TFT-LCD display)



Note 1: For Pb Free products, AUO will add for identification.

Note 2: For RoHS compatible products, AUO will add for identification.

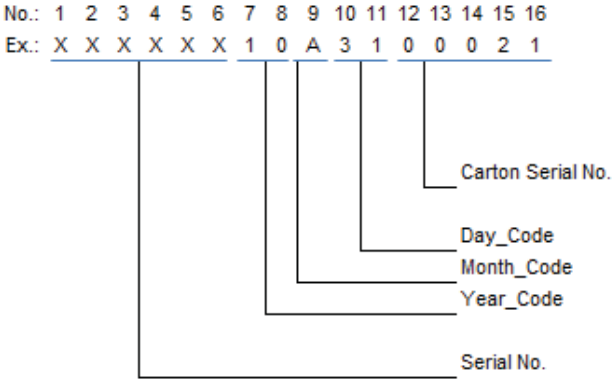
Note 3: For China RoHS compatible products, AUO will add for identification.

Note 4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

9.2 Carton Label and Package

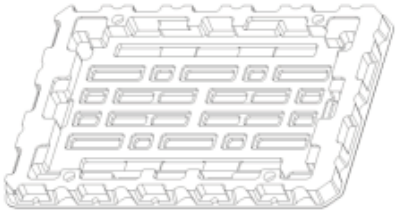
9.2.1 Carton Label Format

Carton number description:

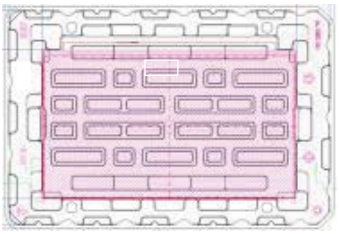


9.2.2 Carton Package

1、Put out PP Board

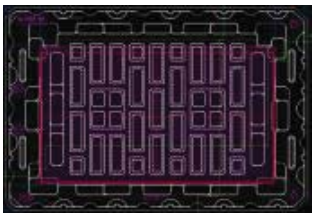


2、Tray placed on PP Board

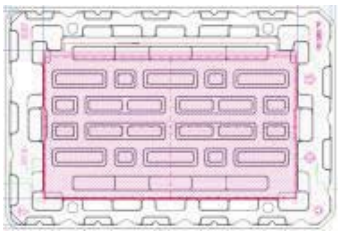


3、Put 1Pcs EPE Spacer into Tray

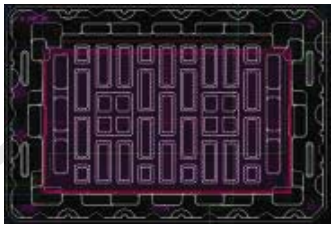
4、Put 1pcs panel on First Spacer , **CF upwards in Tray**



5、Put 1pcs Spacer on First Panel



6、Put 1pcs panel on Second Spacer **CF upwards in Tray**



7、Finally,
Put 1pcs Spacer on Second Panel，
1 Pcs Tray contained 2pcs Panel + 3pcs Spacer

8、Stack 14 layers PET tray as the method mention above (13tray+1dummy tray)

9、Insert the package from the sideway of the Antistatic Bag. Pack the bag, and then tape with scotch tape.

10、Placing EPE into carton

10、Placing trays into carton

11、Cover with EPE cushion

12、Sealing the carton with packing tape

Max capacity：26 TFT-LCD module per carton

Max weight: 13 Kg per carton

Outside dimension of carton: 524mm(L)*376mm(W)*385mm(H)

Pallet size： 1150 mm * 1070 mm * 132mm

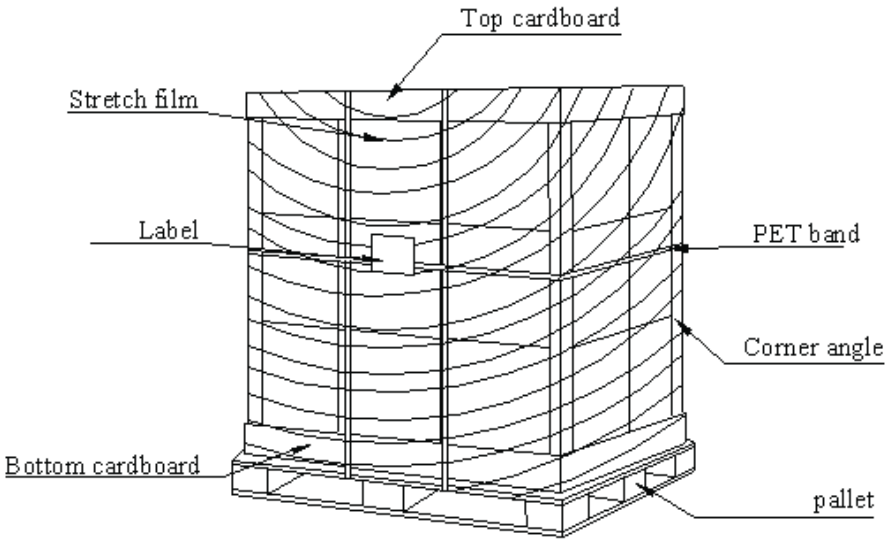
Box stacked

Module by air：(3*2) *3 layers，one pallet put 18 boxes，total 468 pcs module

Module by sea：(3*2) *3 layers + (3*2) *1 layers， two pallet put 24 boxes，total 624 pcs module

Module by sea_HQ：(3*2) *3 layers + (3*2) *2 layers， two pallet put 30 boxes，total 780 pcs module

9.3 Shipping Package of Palletizing Sequence



10. Handling guide

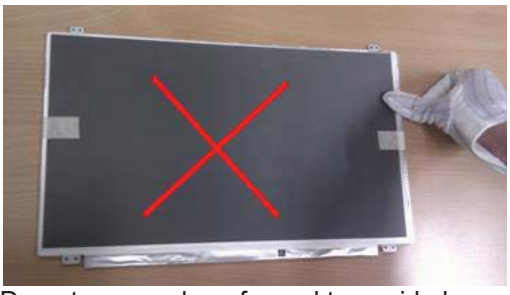
This is a thin and slime LCD model, and please be cautious when pulling it out of package or assembling it onto platform. Careless handlings, e.g. twist, bending, pressing, or collision, will result malfunction of LCD models.

(1) Handling method notice

Do not lift and hold the panel with single hand at right or left side from tray.

Lift and hold the panel up with both hands from tray.

(2) On the table notice



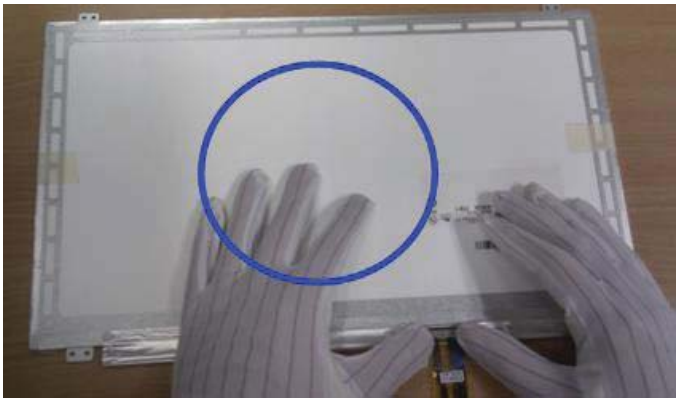
Do not press edge of panel to avoid glass broken.

Do not press the surface of the panel to avoid the glass broken or polarizer scratch.

Do not put anything or tool on the panel to avoid the glass broken or polarizer scratch.

(3) Cable assembly notice

Do not insert the connector with single hand and touching the PCBA.



Insert the connector by pushing right and left edge.

11. Appendix: EDID Description

G156HAN03 0 EDID Code					
Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	ED	11101101	237	
0B	hex, LSB first	30	00110000	48	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	1A	00011010	26	
11	Year of manufacture	1C	00011100	28	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A5	10100101	165	
15	**Max H image size** *(rounded to cm)*	22	00100010	34	
16	**Max V image size** *(rounded to cm)*	13	00010011	19	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	05	00000101	5	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	B5	10110101	181	
1B	Red x **(Upper 8 bits)**	94	10010100	148	
1C	Red y/ highER 8 bits	59	01011001	89	
1D	Green x	59	01011001	89	
1E	Green y	92	10010010	146	
1F	Blue x	28	00101000	40	
20	Blue y	1D	00011101	29	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	

34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	78	01111000	120	
37	Pixel Clock/10000 USB	37	00110111	55	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	B4	10110100	180	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	38	00111000	56	
3C	Vertical Blanking **Lower 8bits**	2E	00101110	46	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	6C	01101100	108	
3F	HorzSync.Width	30	00110000	48	
40	VertSync.Offset : VertSync.Width	AA	10101010	170	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	58	01011000	88	
43	Vertical Image Size **Lower 8bits**	C1	11000001	193	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	

6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	47	01000111	71	G
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	35	00110101	53	5
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	33	00110011	51	3
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	BB	10111011	187	
			SUM	6656	
			SUM to HEX	1A00	