CHIMEI INNOLUX DISPLAY CORPORATION

FOG

SPECIFICATION

Customer: _____

Model Name: HE080IA-01E

Date: 2012/12/28

Version: 01

☐ Preliminary Specification

■ Final Specification

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by
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Record of Revision

Version	Revise Date	Page	Content
Final-Spec.01	2012/12/28	All	Initial Release.

CHIMEI INNOLUX

Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	8 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	1024 × 3(RGB) × 768	
4	Display mode	Normally Black	
5	Dot pitch	0.05275(W) × 0.15825(H) mm	
6	Active area	162.05(W) × 121.54(H) mm	
7	Panel size	171.12 (W) ×132.62 (H) × 1.07(D) mm	Note 1
8	Surface treatment	HC	
9	Color arrangement	RGB-stripe	
10	Interface	4 Lane MIPI Video Mode	
11	Panel power consumption	0.415W(Typ)	
12	Weight	53g	

Note 1: Refer to Mechanical Drawing.

2. Pin Assignment

2.1. TFT LCD Panel Driving Section

Pin No.	Symbol	I/O	Function	Remark
1	NC	---	No connection	
2	VDD	P	Power Voltage for digital circuit	
3	VDD	P	Power Voltage for digital circuit	
4	GND	P	Ground	
5	Reset	I	Global reset pin	Note1
6	STBYB	I	Standby mode, Normally pulled high STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z	Note1
7	GND	P	Ground	
8	RXIN0-	I	- MIPI differential data input	
9	RXIN0+	I	+ MIPI differential data input	
10	GND	P	Ground	
11	RXIN1-	I	- MIPI differential data input	
12	RXIN1+	I	+ MIPI differential data input	
13	GND	P	Ground	
14	RXCLKIN-	I	- MIPI differential clock input	
15	RXCLKIN+	I	+ MIPI differential clock input	
16	GND	P	Ground	
17	RXIN2-	I	- MIPI differential data input	
18	RXIN2+	I	+ MIPI differential data input	
19	GND	P	Ground	
20	RXIN3-	I	- MIPI differential data input	
21	RXIN3+	I	+ MIPI differential data input	
22	GND	P	Ground	
23	NC	---	No connection	
24	NC	---	No connection	

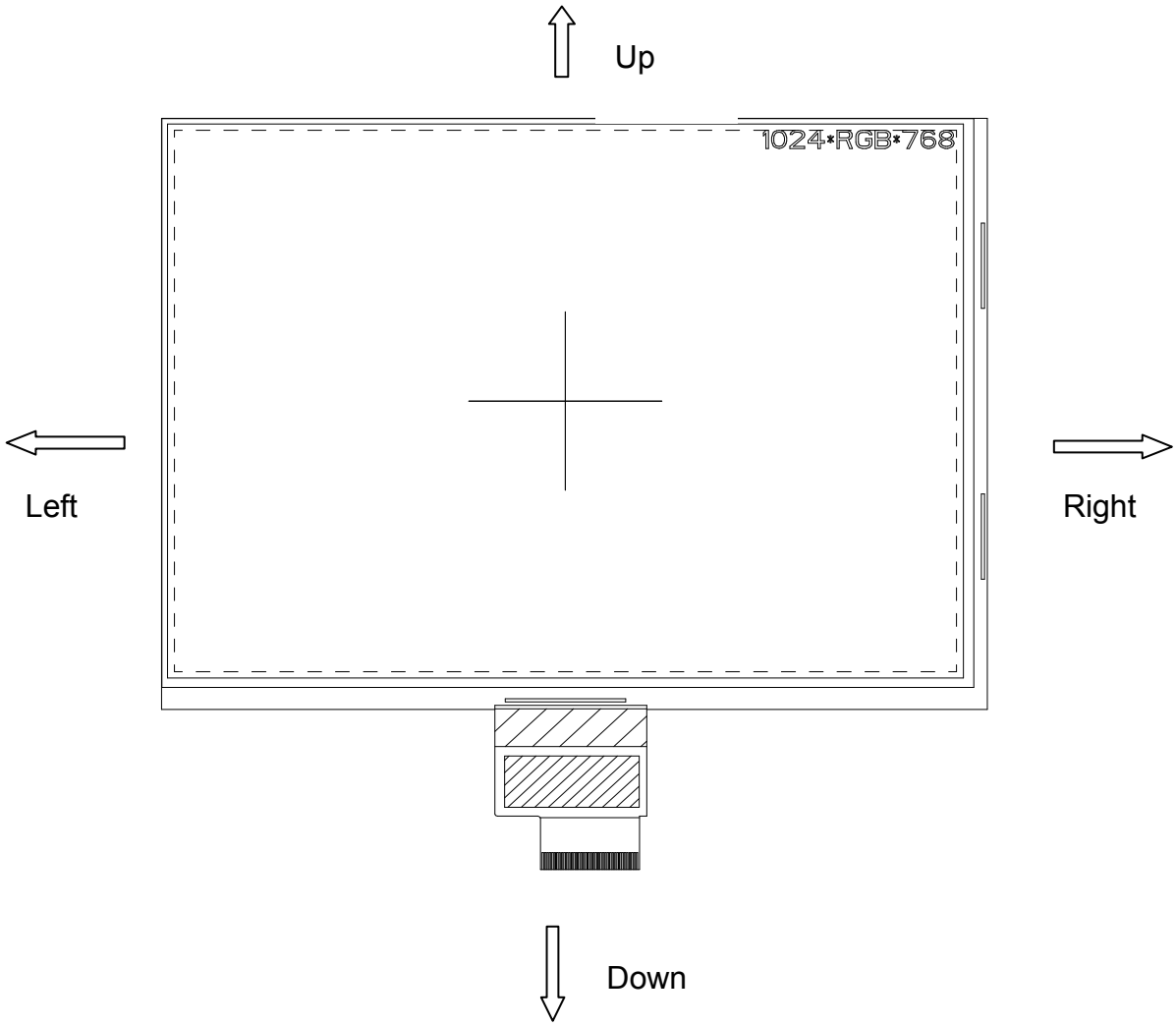
25	GND	P	Ground	
26	NC	---	No connection	
27	PINCTL	I	Enable pin control function. PINCTL = “L”, Disable pin control function. PINCTL = “H”, Enable pin control function.	
28	NC	---	No connection	
29	AVDD	P	Power for Analog Circuit	
30	GND	P	Ground	
31	LED-	P	LED Cathode	
32	LED-	P	LED Cathode	
33	NC	---	No connection	
34	NC	---	No connection	
35	VGL	P	Gate OFF Voltage	
36	NC	---	No connection	
37	NC	---	No connection	
38	VGH	P	Gate ON Voltage	
39	LED+	P	LED Anode	
40	LED+	P	LED Anode	

I: input, O: output, P: Power

Note1:

It’s recommended that control these two pins with GPIOs to follow our Power sequence for stable

Note: Definition of scanning direction.
Refer to the figure as below:



3. Operation Specifications

3.1. Absolute Maximum Rating (Note1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	V_{DD}	-0.3	2.0	V	
	AV_{DD}	8	13.5	V	
	V_{GH}	-0.3	40	V	
	V_{GL}	-20	0.3	V	
	V_{GH}-V_{GL}	-0.3	40	V	
Operation Temperature	T_{OP}	-10	60	℃	
Storage Temperature	T_{ST}	-20	70	℃	

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.1.1. Typical Operation Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	V_{DD}	1.8	1.85	1.95	V	Note 1
	AV_{DD}	9.8	10	10.2	V	
	V_{GH}	18.6	18.9	19.2	V	
	V_{GL}	-8.1	-7.8	-7.5	V	
Input logic high voltage	V_{IH}	$0.7V_{DD}$	-	V_{DD}	V	Note 2
Input logic low voltage	V_{IL}	0	-	$0.3V_{DD}$	V	

Note 1: V_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board .
Note 2: RESET,STBYB,PINCTL.

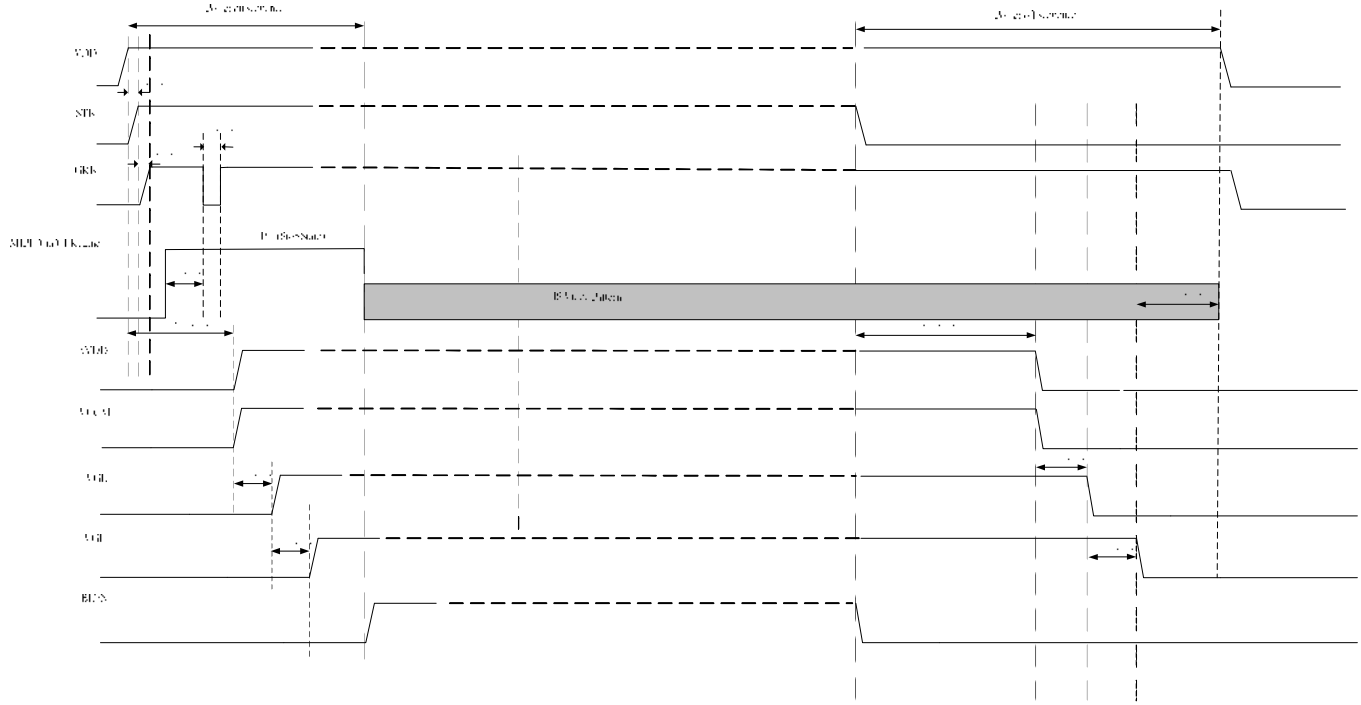
3.1.2. Current Consumption Note1

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{GH}	-	0.63	1	mA	VGH=18.9V
	I_{GL}	-	0.63	1	mA	VGL=-7.8V
	I_{VDD}	-	30	45	mA	Vcc=1.8V
	IAV_{DD}	-	35	50	mA	AVDD=10.0V

Note1: Frame Rate = 60 Hz, 4 Lane MIPI Video Mode

3.2. Power Sequence

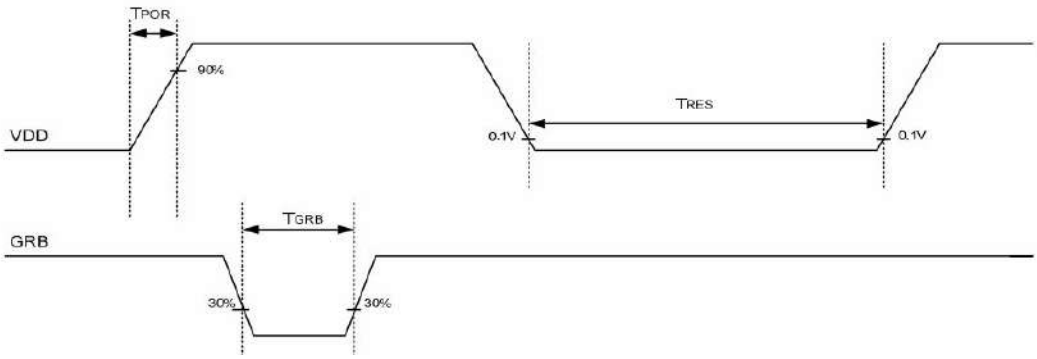
In order to prevent module from power on reset fail, the rising time of the digital power supply VDD should be less than 20 ms. It's strongly recommended that follow the Power Sequence to prevent display issue occur.



Basic AC Characteristic

VDD/GRB AC characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD power slew rate	T_{POR}	-	-	20	ms	From 0 to 90% VDD
GRB active pulse width	T_{GRB}	1	-	-	ms	VDD=VDD_IF= 1.85V
VDD resettle time	T_{RES}	1	-	-	s	

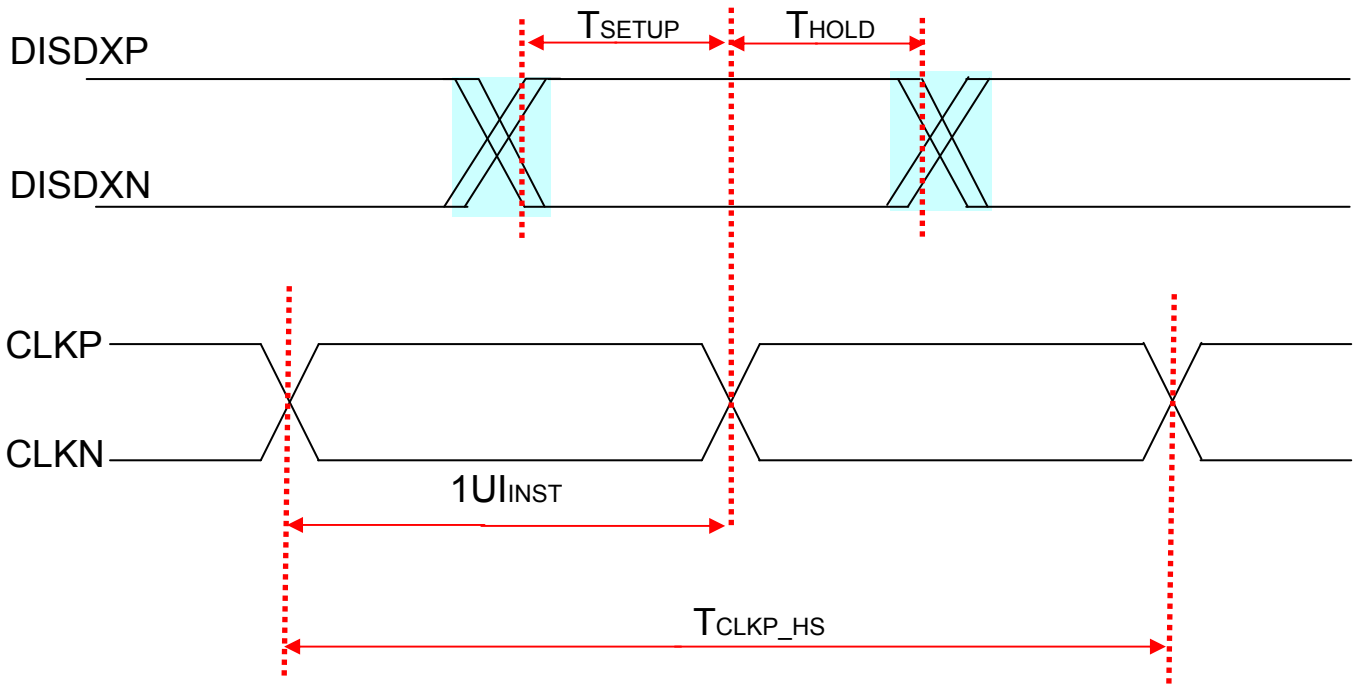


3.3. Timing Characteristics

3.3.1. AC Electrical Characteristics

3.3.1.1. HS Transmission

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
DSI Data Transfer Rate(HS)	T_{DSIR_HS}	80		500	Mbps
UI instantaneous	UI_{INST}	2	-	12.5	ns
Data to CLK Setup Time(measured at receiver)	$T_{SETUP(RX)}$	0.15	-	-	UI_{INST}
Data to CLK Hold Time(measured at receiver)	$T_{HOLD(RX)}$	0.15	-	-	UI_{INST}
20% - 80% rise time and fall time	T_R,T_F	150	-	-	ps

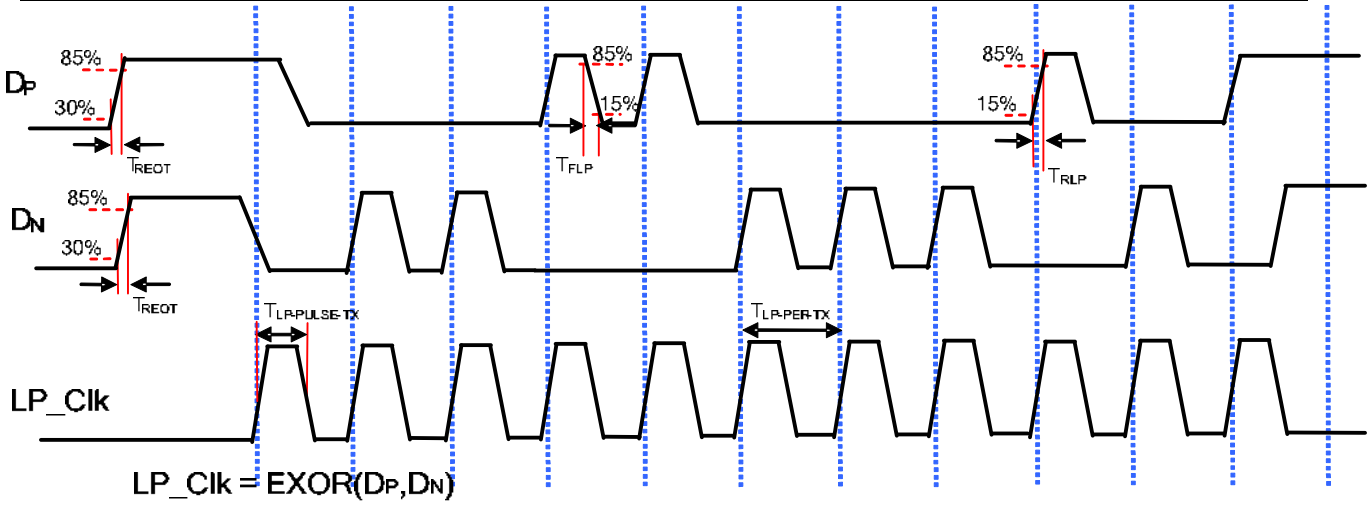


Data to Clock Timing Definitions

Note: X may be 0, 1, 2 or 3.

3.3.1.2. LP Transmission

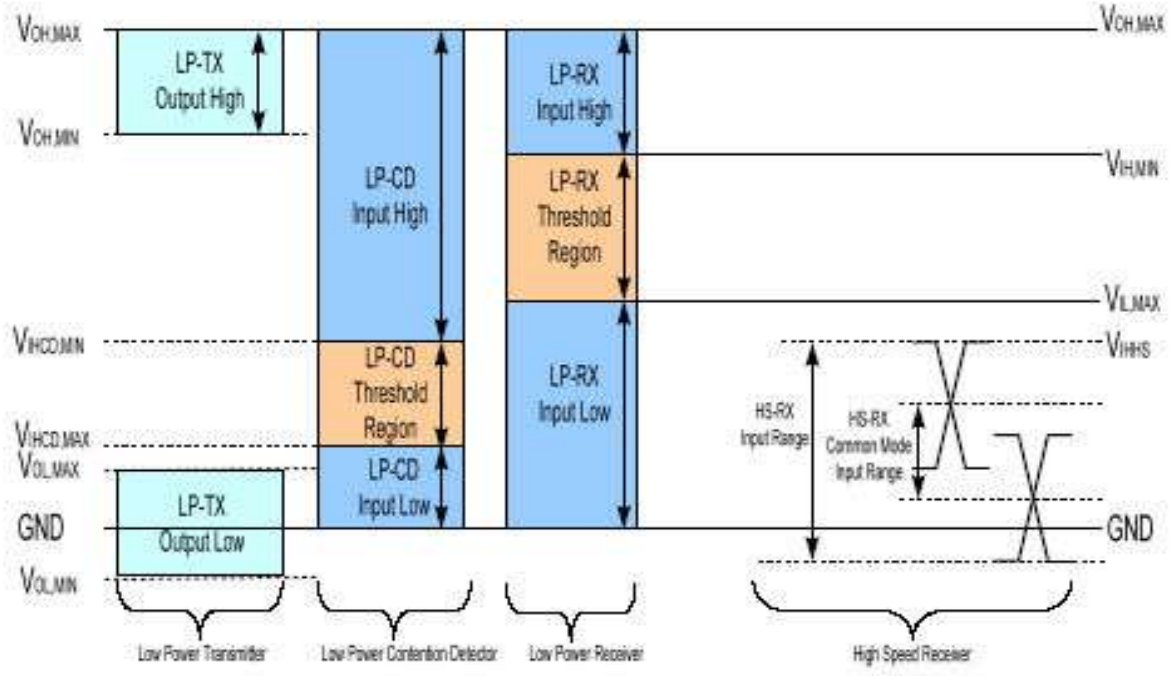
Parameter		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
15%-85% rising time and falling time		T_{RLP} / T_{FLP}	-	-	25	ns	
30%-85% rising time and falling time		T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$t_{LP-PULSE-TX}$	40	-	-	ns	
	All other pulses		20				
Period of the LP exclusive-OR clock		$t_{LP-PRE-TX}$	90	-	-	ns	



3.3.2. DC Electrical Characteristics

(VDD=1.8V, AVDD=10V, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	VILHS	-40	--	--	mV
Single-ended input high voltage	VIHHS	--	--	460	mV
Common-mode voltage	VCDRXDC	70	--	330	mV
Differential input impedance	ZID	--	TBD	--	ohm
HS transmit differential voltage(VOD=VDP-VDN)	|VOD|	--	TBD	--	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	--	1350	mV
Ground shift	VGNDSH	-50	--	50	mV
Logic 0 input threshold	VIL	0	--	550	mV
Logic 1 input threshold	VIH	880	--	1350	mV
Input hysteresis	VHYST	25	--	--	mV
Output low level	VOL	-50	--	50	mV
Output high level	VOH	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	--	TBD	--	ohm
Logic 0 contention threshold	VILCD,MAX	--	--	200	mV
Logic 0 contention threshold	VIHCD,MIN	450	--	--	mV



3.3.3. Timing

DE mode

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	fclk	52	65	71	MHz	Frame rate =60Hz
Horizontal display area	thd		1024		DCLK	
HS period time	th	1114	1344	1400	DCLK	
HS Blanking	thb+thfp	90	320	376	DCLK	
Vertical display area	tvd		768		H	
VS period time	tv	778	806	845	H	
VS Blanking	tvb+tvfp	10	38	77	H	

HV mode
Horizontal input timing

Item		Symbol	Values			Unit
			Min.	Typ.	Max.	
DCLK frequency@ Frame rate=60hz		fclk	52	65	71	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
Horizontal display area		thd		1024		
HSYNC pulse width	Min.	thpw		1		
	Typ.			--		
	Max.			140		
HSYNC back porch		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

HV mode
Vertical input timing

Item	Symbol	Values			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		768		H
VSYNC period time	tv	792	806	840	
VSYNC pulse width	tvpw	1	--	20	
VSYNC back porch	tvb	23	23	23	
VSYNC front porch	thfp	1	15	49	

3.4. Module Control Register

Following table list the MIPI control registers and bit name definition for HE080IA-01C.

Setting of all the MIPI registers will take effect at the coming valid Vsync signal except GRB bit.

All the MIPI control registers and bit name definition:

	Register address								MSB							LSB	default(hex)
No.	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	DI	D0	–
R01h	0	0	0	0	0	0	0	1	0	GRB								–
R10h	0	0	0	1	0	0	0	0	0	ENTER_SLEEP_MODE								–
R11h	0	0	0	1	0	0	0	1	0	EXIT_SLEEP_MODE								–
R36h	0	0	1	1	0	1	1	0	1/0	0	0	0	0	0	0	UPDN (0)	SHLR(1)	01
RB1h	1	0	1	1	0	0	0	1	1/0	0	0	HFRC(0)	DITHER (0)	0	RES[1:0](00)		–	00
RB2h	1	0	1	1	0	0	1	0	1/0	–	NBW (0)	–	2Lane_EN(0)	–	–	–	–	00
RB3h	1	0	1	1	0	0	1	1	1/0	–	–	–	–	–	FRAME (0)	–		00

R01h: GRB (Software Reset)

Address	01h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								N/A
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset register values and all source are set to GND (display off).								
Restriction	(1)It will be necessary to wait 20 msec before sending new command following software reset. (2)The display module loads all display supplier's factory default values to the registers during 5 msec.								

R10h: ENTER_SLEEP_MODE (Enter the Sleep-In Mode)

Address	10h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								Sleep In

Description	This command initiates the power-down sequence. The Sleep In profile will be executed when this command is received.
Restriction	This command has no effect when the display module is already in Sleep Mode.

R11h: EXIT_SLEEP_MODE (Exit the Sleep-In Mode)

Address	11h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								Sleep Out
Description	This command initiates the power-up sequence. The Sleep Out will load register value. It will be necessary to wait 5 msec before sending next command.								
Restriction	This command will not cause any visible effect on the display when the display is not in Sleep Mode								

R36h: SET_ADDRESS_MODE (Data Access Control)

Address	36h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	0	0	0	0	0	UPD	SHLR	01h
Description	UPDN: Gate up or down scan control. UPDN = “0”, set top to bottom scan direction. (default) UPDN = “1”, set bottom to top scan direction. SHLR: Source right or left sequence control. SHLR = “0”, set right to left scan direction. SHLR = “1”, set left to right scan direction. (default)								

RB1h: Panel Control Register

Address	B1h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	**0**	**HFRC (0)**	**DITHER (0)**	**0**	**RES[1:0] (00)**		–	00h

Description	HFRC: H-FRC selection. HFRC = “1” : H-FRC enable HFRC = “0” : H-FRC disable (Default) If DITHER=“0”,disable dithering function(H-FRC and FRC disable) DITHER: Dithering function enable control. DITHER = “1”, Enable internal dithering function DITHER = “0”, Disable internal dithering function (Default) RES[1:0]: =’’01’’ for 1024(RGB)*768 display resolution =’’00’’, for 1024(RGB)*600 display resolution (default)

RB2h: Panel Control Register

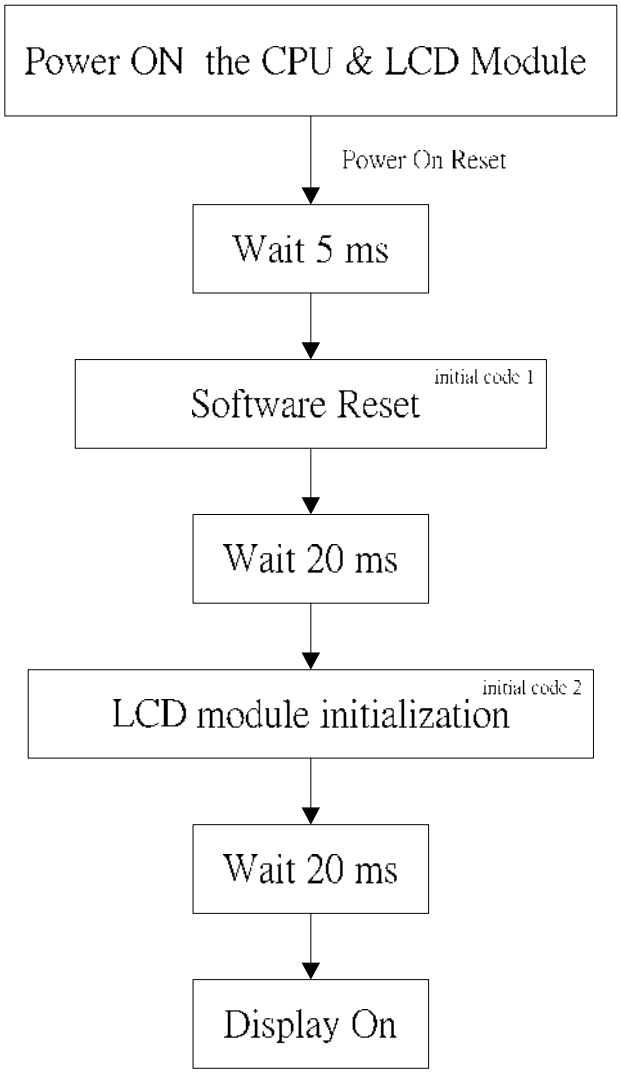
Address	B2h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	–	NBW(0)	–	2Lane_EN (0)	–	–	–	–	00h
Description	NBW: Normally black or normally white setting. NBW=’’1’’: Normally black. NBW=’’0’’: Normally white(default) 2Lane_EN:2 lane/4 lane setting 2Lane_EN=”1” : 2 lane 2Lane_EN=”0” : 4 lane(default)								

RB3h: Panel Control Register

Address	B3h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	–	–	–	–	–	FRAME (0)	–		00h
Description	FRAME: Frame inverse or not select. FRAME = ”1” , Uniform FRAME = ”0” , Frame inverse(Default)								

3.5. Software Configuration

If PINCTL set low , customer could set module control function(such as U/D、L/R control etc) by access panel register with DCS command. The module could accept either Generic packet or DCS packet in either Low-Power mode or High-Speed mode from MIPI master.
If input video data format is 24-bit RGB, 8-8-8 Format, the flow chart shows the step of software configuration.



Note: The figure above is just demonstrated the process of software reset. The power sequence should refer to Item 3.2 .

1. Initial code 1: Software Reset

The table below shows the related register and parameter

Register	Parameter	Description
0x01	00h	Module Software Reset

Here is an example of the packet format, the ECC is generated automatically.

Data ID	Data 0	Data 1	ECC
13h	01h	00h	~~

2. Initial code 2: LCD module initialization

Register	Parameter	Description
0xB1	30h	HFRC & Dithering Enable

Data ID	Data 0	Data 1	ECC
23h	B1h	30h	~~

When PINCTL pull Low the HFRC & Ditering HW Pin which were set on FPC will be disable. It would have required 'Initial code 2' to achieve display 24bit video data
If input video data format is 18bit or 16 bit, the initial code 2 is no need anymore.

As the Module is 4 Lane mode as default. If user want to use 2 lane mode, should send the command with **LP mode** as blew: (Note1)

Register	Parameter	Description
0xB2	10h	Set 2 Lane Mode

Data ID	Data 0	Data 1	ECC
23h	B2h	10h	~~

Note1: As the Max Speed of each lane is 500 Mbps. In two lane mode the LCM cann't achieve 60 frame per second refresh rate.

4. Optical Specifications

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180°(9 o'clock)	75	85	-	degree	Note 1
	θ_R	Φ=0°(3 o'clock)	75	85	-		
	θ_T	Φ=90°(12 o'clock)	75	85	-		
	θ_B	Φ=270°(6 o'clock)	75	85	-		
Response time	T_{ON+} T_{OFF}	Normal θ=Φ=0°		25	50	msec	Note 2 Note 3
Contrast ratio	CR		600	800	-	-	Note 4
Color chromaticity	W_X		0.238	0.288	0.338	-	Note 5
	W_Y		0.276	0.326	0.376	-	
Transmittance	Tr	-	3.8	4.3	-	%	

Test Conditions:

1. V_{CC}=1.8V, the ambient temperature is 25℃.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

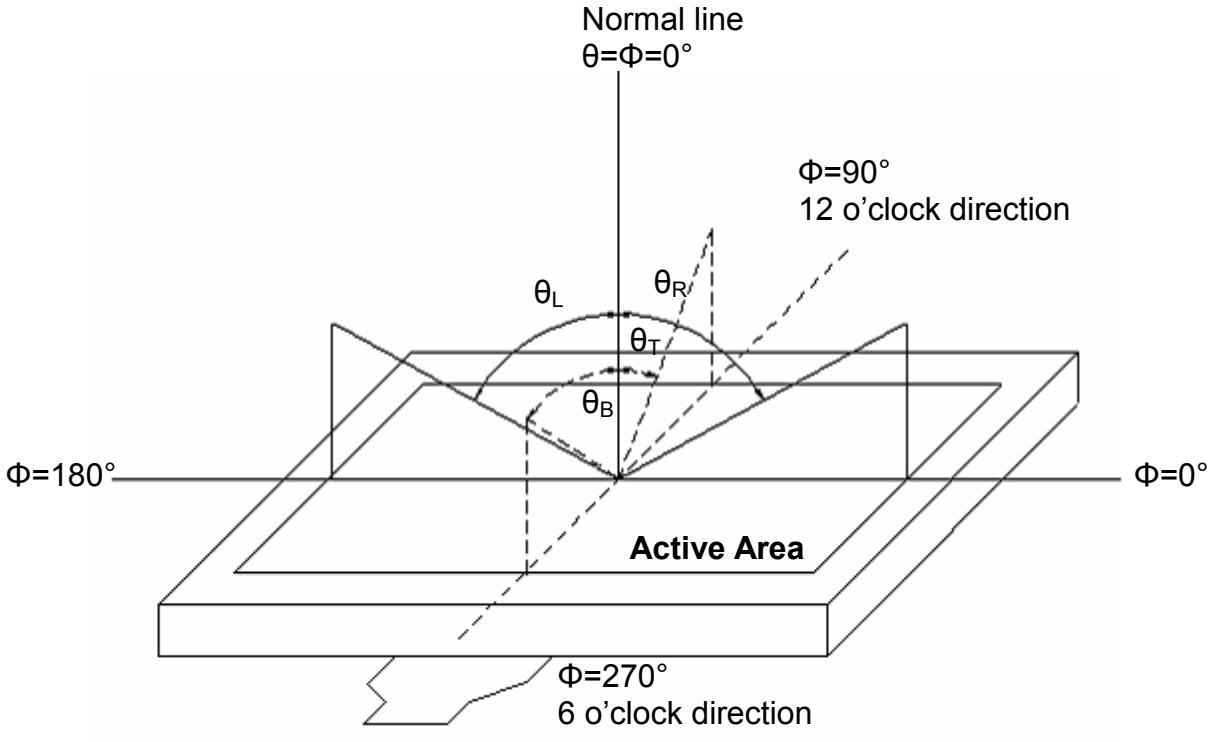


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm, Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/ Field of view: 1°/Height: 500mm.)

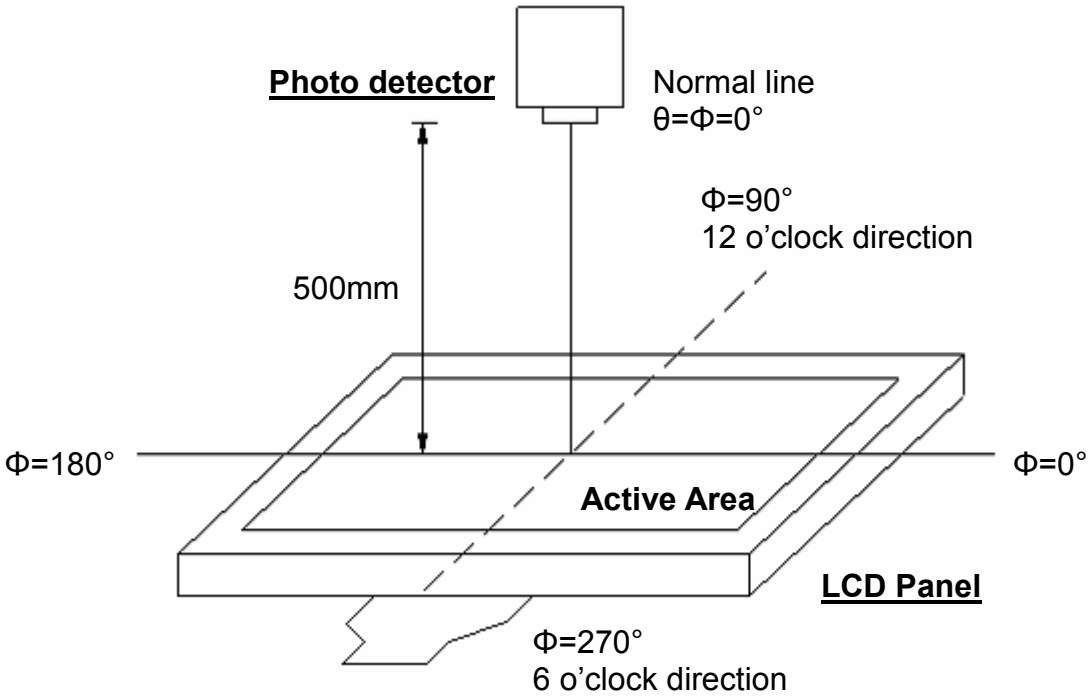


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

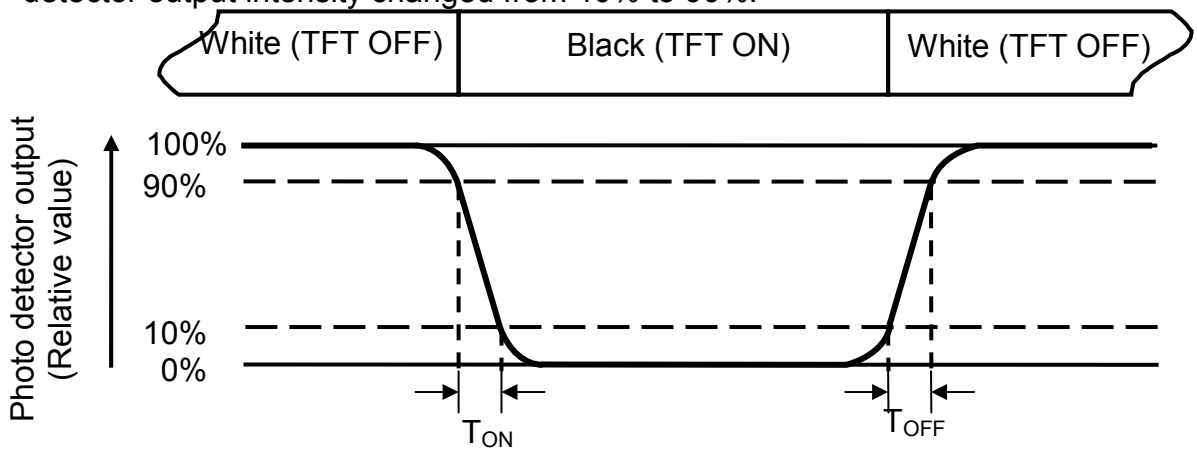


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of backlight

The backlight used C light.

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

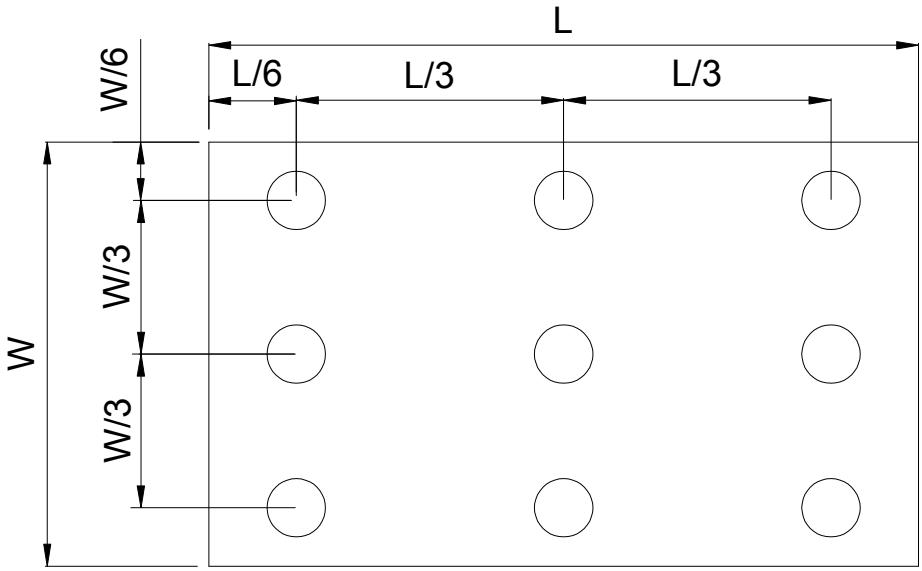


Fig. 4-4 Definition of measuring points

$\mathbf{B_{max}}$: The measured maximum luminance of all measurement position.
$\mathbf{B_{min}}$: The measured minimum luminance of all measurement position.

5. Reliability Test Items

(Note3)

Item	Test Conditions		Remark
High Temperature Storage	Ta = 70℃	240hrs	Note 1，Note 4
Low Temperature Storage	Ta = -20℃	240hrs	Note 1，Note 4
High Temperature Operation	Ts = 60℃	240hrs	Note 2，Note 4
Low Temperature Operation	Ta = -10℃	240hrs	Note 1，Note 4
Operate at High Temperature and Humidity	+60℃, 90%RH	240hrs	Note 4
Thermal Shock	-10℃/30 min ~ +60℃/30 min for a total 100 cycles, Start with cold temperature and end with high temperature.		Note 4
Package Vibration Test	Random Vibration : ISTA-3A 1Hz~200Hz,Grms=0.53 Half hours for direction of Z.		
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces		

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, after least 2 hours at room temperature.

6. General Precautions

6.1. Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

6.2. Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
2. The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
3. To avoid contamination on the display surface, do not touch the module surface with bare hands.
4. Keep a space so that the LCD panels do not touch other components.
5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

6.3. Static Electricity

1. Be sure to ground module before turning on power or operating module.
2. Do not apply voltage which exceeds the absolute maximum rating value.

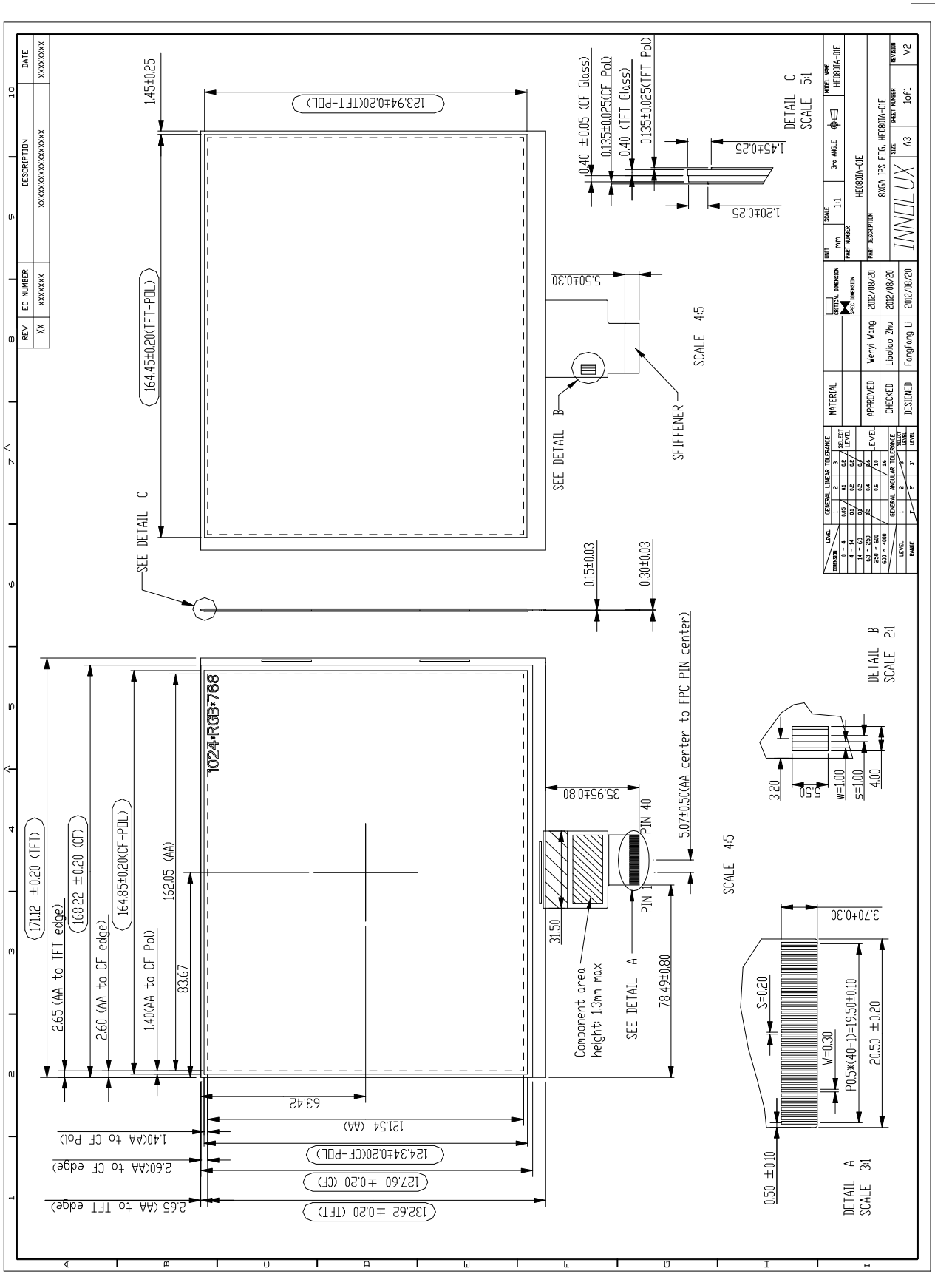
6.4. Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.
2. Do not store the module in surroundings containing organic solvent or corrosive gas.
3. Store the module in an anti-electrostatic container or bag.

6.5. Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.
2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

7. Mechanical Drawing



8. Package Drawing

8.1 Packaging Material Table

No	Item	Model (Material)	Dimensions(mm)	Unit Weight (Kg)	Quantity (pcs)	Remark
1	Panel size	HE080IA-01E	171.12×132.62×1.07	0.0525	60	
2	Partition	BC Corrugated Paper	512 × 350 × 225	0.290	1	
3	Dust-Proof Bag	PE	700 × 530	0.050	1	
4	PET-Tray	PE	505 ×338×16.5	0.24	21	
5	Carton	Corrugated Paper	530 × 355 × 255	0.810	1	
6	Total weight	9.43Kg±5%				

8.2 Packaging Quantity

(1) FOG quantity per PET-Tray:	3pcs
(2) Total FOG quantity in Carton:	20 layer x 3pcs/PET-Tray = 60pcs

8.3 Packaging Drawing