TITLE : HT12X21-220
Product Specification for Customer
Rev. C

BOE TFT-LCD SBU
BEIJING BOE OPTOELECTRONICS TECHNOLOGY
BOE HYDIS TECHNOLOGY

REVISION HISTORY

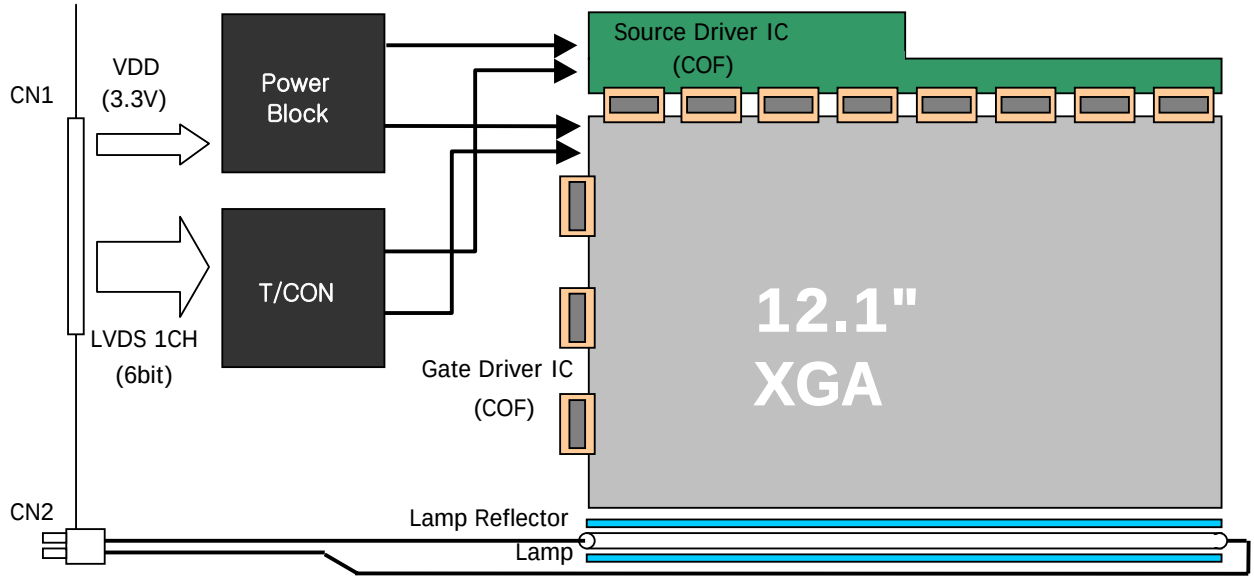
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
0		Initial Release	04.06.25	S.T.KO
A	E412-F018	Product label position changed from 14.8 to 4.0	04.12.31	E.S.PARK
B	E0507-F005	Interface connection - Add a EDID pin connection description	05.07.14	S.H.YUN
C	E0507-F021	EDID Data - Add a EDID data table - Add a EDID chip timing specification	05.08.04	S.H.YUN

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

12.1”XGA is a color active matrix TFT LCD module using AFFS (Advanced Fringe Field Switching: Wide viewing technology) mode and amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 12.1 inch diagonally measured active area with XGA resolutions (1024 horizontal by 768 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 262,144 colors. The TFT-LCD panel used for this module is a low reflection and higher color type.



1.2 Features

- LVDS Interface with 1pixel / clock
- 6-bit color depth, Display 262,144 colors
- Incorporated edge type back-light (1 lamp)
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) mode only
- EDID built on PCB
- RoHS

1.3 Applications

- Pen-type & Tablet PC

1.3 General Specification

The followings are general specifications at the model HT12X21-220

Parameter	Specification	Unit	Remarks
Active area	245.76 X 184.32	mm	
Number of pixels	1024(H) X 768(V)	pixels	
Pixel pitch	0.240(H) X 0.240(V)	mm	
Pixel arrangement	RGB Vertical stripe		
Display colors	262,144	colors	
Display mode	Normally Black		
Dimensional outline	270.0 (H) X 199.0(V) X 4.8 @ Lamp	mm	Note 2
Weight	305 typ.	g	
Back-light	Bottom edge side 1-CCFL type		Note 1
Surface treatment	Haze 25, Anti-glare & hard-coating (3H)		

Note 1. CCFL (Cold Cathode Fluorescent Lamp)
2. LCM Height 4.8 [mm] Typical (lamp), 6.7[mm] Typical (Pouch)

2.0 ABSOLUTE MAXIMUM RATINGS

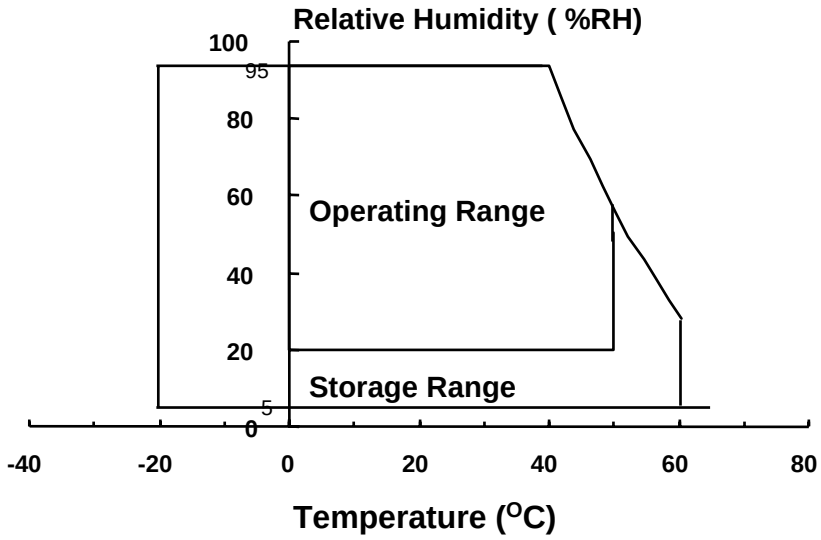
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed as below table

VSS = GND = 0V

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	
Logic Supply Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Lamp Current	I_{BL}	2.0	6.0	mArms	Note 1
Lamp frequency	F_L	30	80	kHz	Note 1
Operating Temperature (Humidity)	T_{OP} RH	0	+50 80	℃ %	Note 2
Storage Temperature (Humidity)	T_{SP} RH	-20	+60 90	℃ %	Note 2

Note 1. Permanent damage to the device may occur if maximum values are exceeded Functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 ^{O}C ≥ Ta)
Maximum wet - bulb temperature at 39 ^{O}C or less. (Ta > 40 ^{O}C) No condensation.



3.0 ELECTRICAL SPECIFICATIONS

[Ta = 25± 2℃]

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Permissible Input Ripple Voltage	V_{RF}	-	-	100	mV	AVV_{DD} = 3.3V
Power Supply Current	I_{DD}	-	240	-	mA	Note 1
High Level Differential Input Signal Voltage	V_{IH}	-	-	+ 100	mV	Vcm = 1.2 V Typ
Low Level Differential Input Signal Voltage	V_{IL}	- 100	-	-	mV	
Back-light Lamp Voltage	V_{BL}	-	600	-	V_{rms}	
Back-light Lamp Current	I_{BL}	2.0	5.0	6.0	mA	
Back-light Lamp operating Frequency	F_L	30	60	80	KHz	Note 2
Lamp Start Voltage		-	-	950	V_{rms}	25 ℃, Note 3
		-	-	1150	Vrms	0 ℃, Note 3
Lamp Life		10,000	-	-	Hrs	I_{BL} = 2.0~6.0 mA
Power Consumption	P_D	-	0.7	-	W	
	P_{BL}	-	3.0	-	W	I_{BL} = 5.0 mA Note 4
	P_{total}	-	3.7	-	W	

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for VDD = 3.3V, Frame rate = 60 Hz and Clock frequency = 65MHz.
   Test Pattern of power supply current
   a) Typ : Vertical color bar pattern
   b) Max : Gray 28 @ Vertical 2 Skip line pattern
2. The lamp frequency should be selected as different as possible from the horizontal synchronous frequency and its harmonics to avoid interference, which may cause line flow on the display
3. The voltage above this value should be applied to the lamps for more than 1 second to startup. Otherwise the lamps may not to be turned on.
4. Calculated value for reference ($V_{BL} \times I_{BL}$) excluding inverter loss.

4.0 OPTICAL SPECIFICATION

The measurement shall be executed after 30 minutes warm-up period.
Measuring equipment: TOPCON-BM5.

[VDD=3.3V, Frame rate=60Hz, Clock=65MHz, I_{BL} = 5.0mA, Ta = 25±2℃]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	80	-	Deg.	Note 1
		Θ_9		-	80	-	Deg.	
	Vertical	Θ_{12}		-	80	-	Deg.	
		Θ_6		-	80	-	Deg.	
Luminance Contrast ratio		CR		-	450	-		Note 2
Center Luminance of White		Y_w		150	180	-	cd/m^2	Note 3
White Luminance uniformity		Δ Y5		-	-	1.4		Note 4
White Chromaticity		x_w		0.275	0.305	0.335		Note 5
		y_w		0.300	0.330	0.360		
Reproduction of color	Red	x_R		0.543	0.573	0.603		
		y_R		0.303	0.333	0.363		
	Green	x_G		0.278	0.308	0.338		
		y_G		0.507	0.537	0.567		
	Blue	x_B		0.120	0.150	0.180		
		y_B		0.108	0.138	0.168		
Color reproduction				-	40	-	%	
Response Time		Total (Tr+Td)	Θ = 0°	-	40	-	ms	Note 6
Cross Talk		CT		-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface. (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Luminance of white is defined as a center point(#1) on LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Maximum Luminance of 5 points / Minimum Luminance of 5 points (see FIGURE 2)

5. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as FIGURE 3by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See FIGURE 4)

5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

The electronics interface connector is a model DF19L-20P-1H manufactured by Hirose or equivalent. The mating connector part number is DF19G-20S-1C manufactured by Hirose or equivalent. The connector interface pin assignments are listed in Table 5.

Terminal	Symbol	Functions	Remarks
1	VDD	Power supply +3.3 V	
2	VDD	Power supply +3.3 V	
3	VSS	Ground	
4	VSS	Ground	
5	RIN0 -	LVDS Negative data signal (-)	Tx pin #48
6	RIN0 +	LVDS Positive data signal (+)	Tx pin #47
7	VSS	Ground	
8	RIN1 -	LVDS Negative data signal (-)	Tx pin #46
9	RIN1 +	LVDS Positive data signal (+)	Tx pin #45
10	VSS	Ground	
11	RIN2 -	LVDS Negative data signal (-)	Tx pin #42
12	RIN2 +	LVDS Positive data signal (+)	Tx pin #41
13	VSS	Ground	
14	RCLKIN -	LVDS Negative clock signal (-)	Tx pin #40
15	RCLKIN +	LVDS Positive clock signal (+)	Tx pin #39
16	VSS	Ground	
17	VDD-EDID	EDID power supply (+3.3V)	
18	NC	No connection	
19	Clk-EDID	EDID Clock signal	
20	Data-EDID	EDID Data signal	

5.2. Back-light Interface

The Back-light interface connector is a model BHSR-02VS-1 manufactured by JST or equivalent.

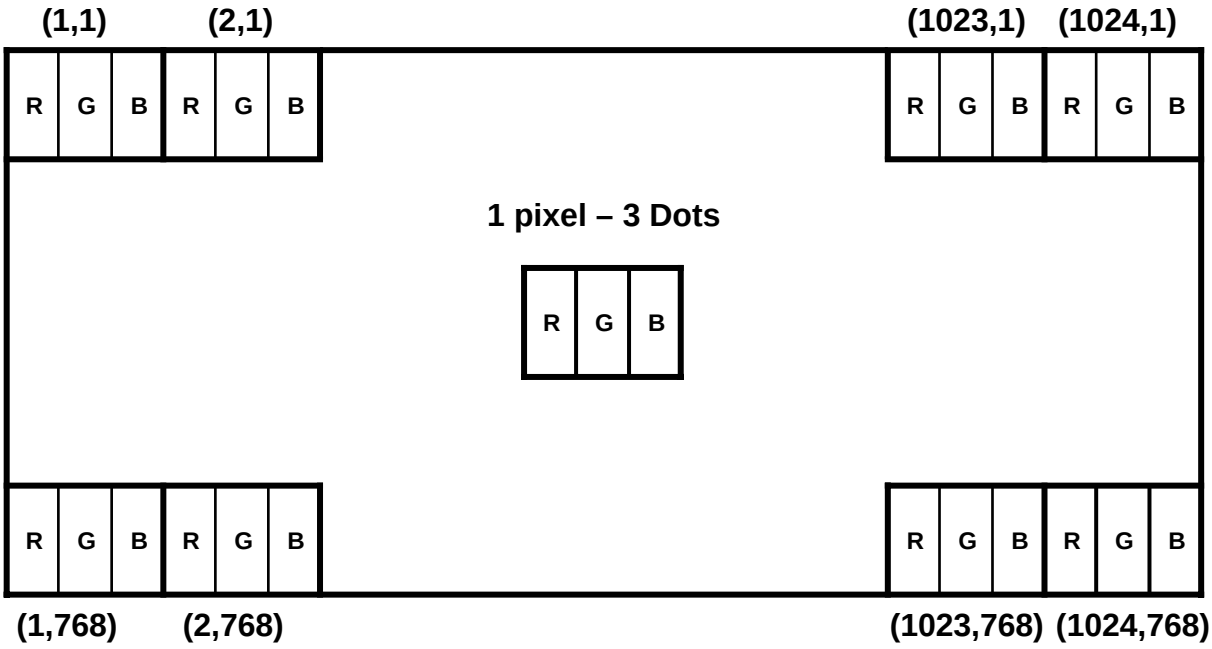
Pin No.	Symbol	Function	Color
1	HOT	High voltage	Pink
2	COLD	Ground	White

5.3. LVDS Interface

LVDS Transmitter THC63LVDM83A or equivalent.

Input Signal	Transmitter		Interface		DF19L-14P-1H	Remarks
	Pin No.	Pin No.	System (Tx)	TFT-LCD (Rx)	Pin No.	
R0	51	48 47	OUT0 – OUT0 +	IN0 – IN0 +	5 6	
R1	52					
R2	54					
R3	55					
R4	56					
R5	3					
G0	4					
G1	6	46 45	OUT1 – OUT1 +	IN1 – IN1 +	7 8	
G2	7					
G3	11					
G4	12					
G5	14					
B0	15					
B1	19					
B2	20	42 41	OUT2 – OUT2 _+	IN2 – IN2 +	9 10	
B3	22					
B4	23					
B5	24					
HSYNC	27					
VSYNC	28					
DE	30					
MCLK	31	40	CLKOUT -	CLKIN -	11	
		39	CLKOUT +	CLKIN +	12	

5.4. Data input Format



Display position of input data

6.0. SIGNAL TIMING SPECIFICATION

6.1 The 12.1" XGA LCM is operated by the only DE (Data enable) mode (LVDS Transmitter Input)

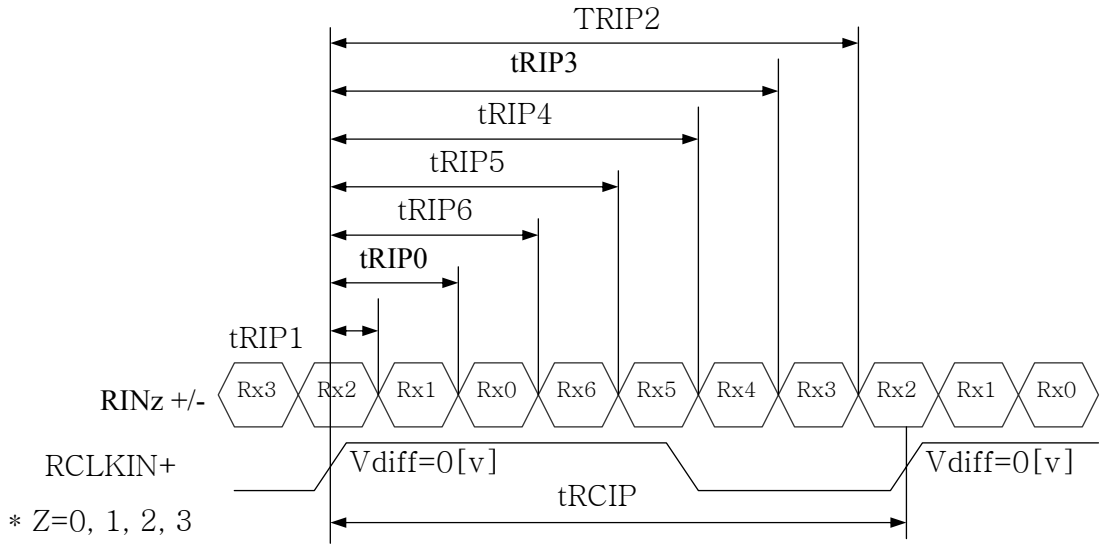
Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	-	65	80	MHz
	High Time	Tch	4.5	-	-	ns
	Low Time	Tcl	4.5	-	-	ns
Data	Setup Time	Tds	2.7	-	-	ns
	Hold Time	Tdh	0	-	-	ns
Data Enable Setup Time		Tes	2.7	-	-	ns
Frame Period		Tv	772	806	1022	lines
Vertical Display Period		Tvd	768	768	768	lines
One Line Scanning Period		Th	1100	1344	2046	clocks
Horizontal Display Period		Thd	1024	1024	1024	clocks

6.2 LVDS Rx Interface timing parameter

The specification of the LVDS Rx interface timing parameter

<LVDS Rx Interface Timing Specification>

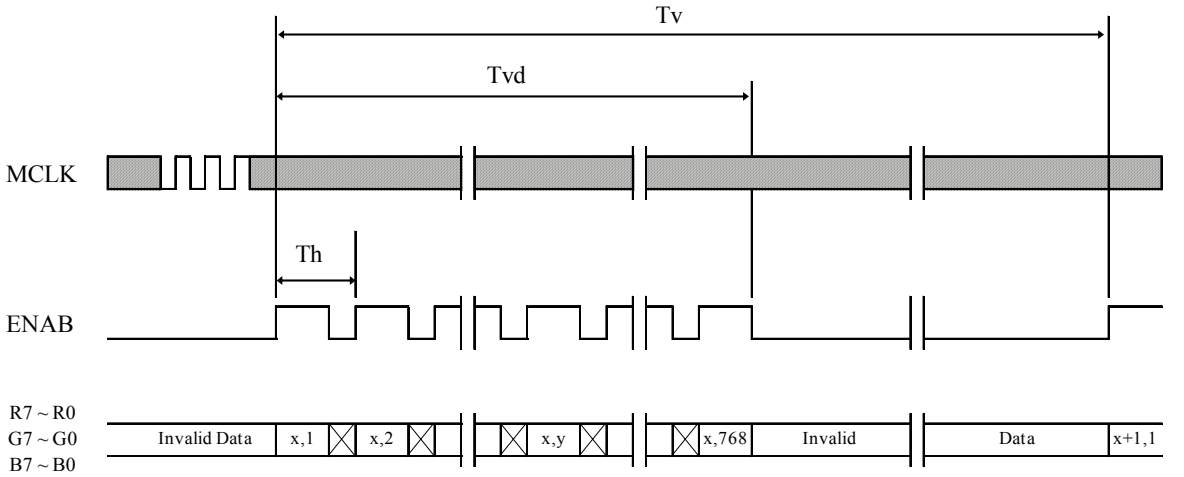
Item	Symbol	Min	Typ	Max	Unit	Remarks
CLKIN Period	tRCIP	12.50	15.38	-	ns	
Input Data 0	tRIP0	-0.4	0.0	+0.4	ns	
Input Data 1	tRIP1	tRICP/7-0.4	tRICP/7	tRICP/7+0.4	ns	
Input Data 2	tRIP2	2xtRICP/7-0.4	2xtRICP/7	2xtRICP/7+0.4	ns	
Input Data 3	tRIP3	3xtRICP/7-0.4	3xtRICP/7	3xtRICP/7+0.4	ns	
Input Data 4	tRIP4	4xtRICP/7-0.4	4xtRICP/7	4xtRICP/7+0.4	ns	
Input Data 5	tRIP5	5xtRICP/7-0.4	5ztRICP/7	5xtRICP/7+0.4	ns	
Input Data 6	tRIP6	6xtRICP/7-0.4	6xtRICP/7	6xtRICP/7+0.4	ns	

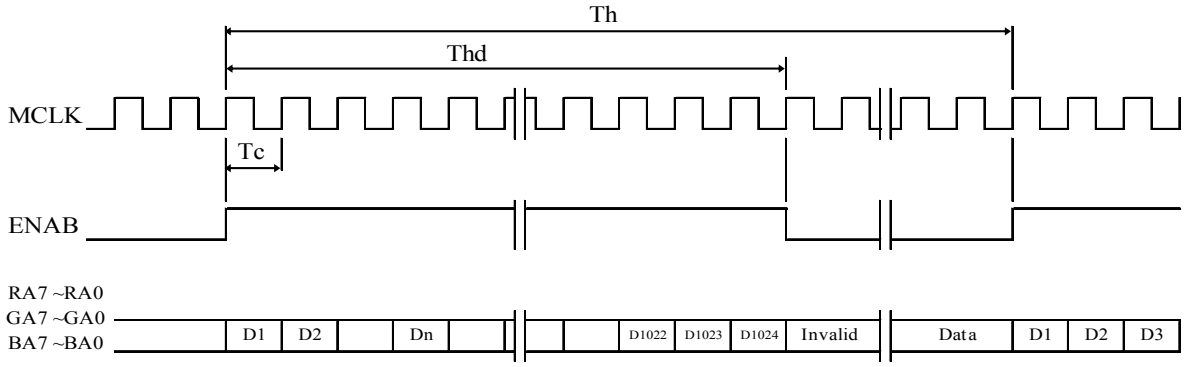


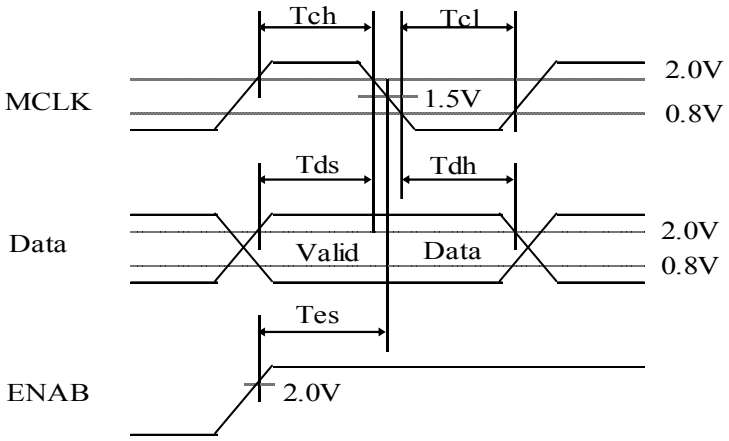
* Vdiff = (RINz+)-(RINz-), (RCLKIN+)-(RCLKIN-)

7.0 SIGNAL TIMING WAVEFORMS

Timing wave forms of interface signal





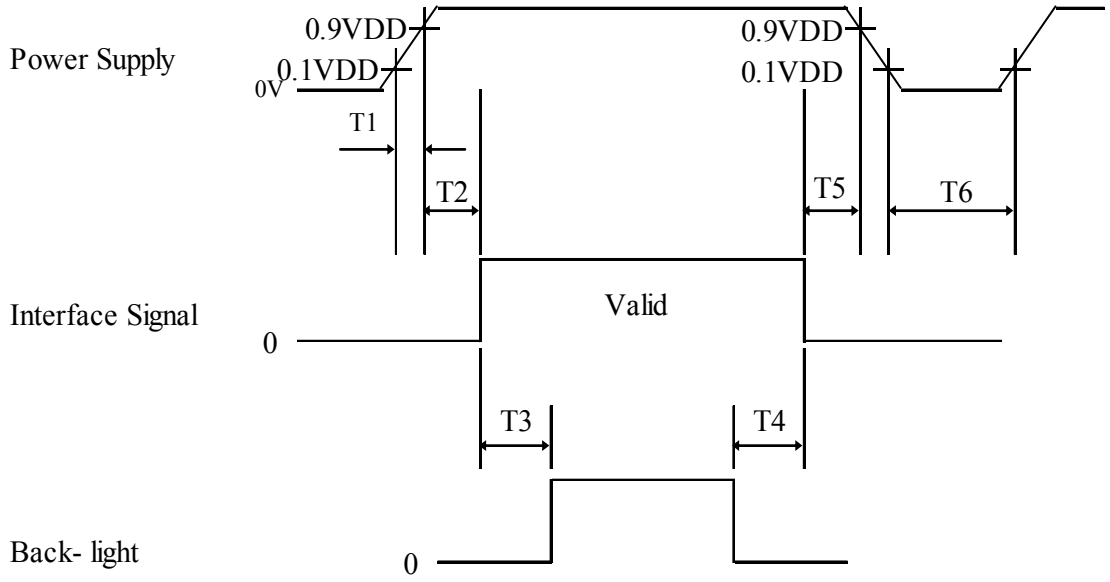


8.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

	Colors & Gray scale	Data signal																	
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△				↓						↓						↓		
	▽				↓						↓						↓		
	Brighter	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	△				↓						↓						↓		
	▽				↓						↓						↓		
	Brighter	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	△				↓						↓						↓		
	▽				↓						↓						↓		
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	△				↓						↓						↓		
	▽				↓						↓						↓		
	Brighter	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
	▽	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



- 0 < T1 ≤ 10 ms
- 0 < T2 ≤ 50 ms
- 100 ms ≤ T3, T4
- 0 < T5 ≤ 50 ms
- 1 sec < T6

Notes : 1. When the power supply VDD is 0V, Keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

FIGURE 5, 6 shown in appendix shows mechanical outlines for the model.

Parameter	Specification	Unit
Dimensional outline Horizontal Vertical Thickness	 277.0 ± 0.5 199.0 ± 0.5 4.8 Typ @ Lamp, 6.7 Typ @ Pouch	mm
Weight	305 Typ	gram
Active Area	246.76 (H) X 184.32 (V)	mm
Pixel Pitch	0.240 (H) X 0.240 (V)	mm
Number of Pixels	1024 (H) X 768 (V)	pixels

10.2 Mounting

See FIGURE 5. (shown in Appendix)

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an anti-glare coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABLITY TEST

The Reliability test items and its conditions are shown in below.

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240 hrs
4	High temperature operation test	Ta = 50 ℃, 240 hrs
5	Low temperature operation test	Ta = 0 ℃, 240 hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle
7	Vibration test (non-operating)	1.5G,10~500Hz for X,Y,Z axis 30 minutes for each axis
8	Shock test (non-operating)	150G,6msec,half sine (6 times)
9	Electro-static discharge test (non-operating)	Air : 150 pF, 330Ω, 15 KV Contact : 150 pF, 330Ω, 8 KV

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 EDID data table & timing specification of EDID Chip

13.1 EDID Data table

EDID chip is 24LC024 (Microchip) or equivalent .

Add (Hex)	Field name & comments	Data	Add (Hex)	Field name & Comments	Data
00	Header	00	1B	Red X : 0.573	92
01	Header	FF	1C	Red Y : 0.333	55
02	Header	FF	1D	Green X : 0.308	4E
03	Header	FF	1E	Green Y : 0.537	89
04	Header	FF	1F	Blue X : 0.150	26
05	Header	FF	20	Blue Y : 0.158	28
06	Header	FF	21	White X : 0.305	4E
07	Header	00	22	White Y : 0.330	54
08	ID System Manufacturer Name : BOE	09	23	Established timing I	00
09		E5	24	Established Timing II : XGA @ 60 Hz	08
0A	ID Product Code : 2200	98	25	Manufacturer's timings	00
0B		08	26	Standard timing ID1 (01h if not used)	01
0C	ID Serial number	00	27	Standard timing ID1 (01h if not used)	01
0D		00	28	Standard timing ID2 (01h if not used)	01
0E		00	29	Standard timing ID2 (01h if not used)	01
0F		00	2A	Standard timing ID3 (01h if not used)	01
10	Week of manufacture	00	2B	Standard timing ID3 (01h if not used)	01
11	Year of Manufacturer : 2004	0E	2C	Standard timing ID4 (01h if not used)	01
12	EDID Structure version : Ver 1.0	01	2D	Standard timing ID4 (01h if not used)	01
13	EDID Revision Number : Rev 0.3	03	2E	Standard timing ID5 (01h if not used)	01
14	Video input definition	80	2F	Standard timing ID5 (01h if not used)	01
15	Max H image size (cm) : 24 cm	18	30	Standard timing ID6 (01h if not used)	01
16	Max V image size (cm) : 18 cm	12	31	Standard timing ID6 (01h if not used)	01
17	Display Gamma : 2.2	78	32	Standard timing ID7 (01h if not used)	01
18	Feature : RGB Preferred timing	0A	33	Standard timing ID7 (01h if not used)	01
19	Red/Green low bits	8D	34	Standard timing ID8 (01h if not used)	01
1A	Blue/White low bits	51	35	Standard timing ID8 (01h if not used)	01

Add (Hex)	Field name & comments	Data	Add (Hex)	Field name & Comments	Data
36	Detailed timing descriptor #1	64	53	Tvbp min (line pulses)	20
37	Pixel clock (MHz) / 1000 : 65 MHz	19	54	Tvbp max (line pulses)	20
38	Horizontal active : 1024	00	55	Thp min (pixel clks)	20
39	Horizontal blanking : 320	40	56	Thp max (pixel clks)	20
3A	Horizontal active : blanking	41	57	Tvp min (line pulses)	20
3B	Vertical active : 768	00	58	Tvp max (line pulses)	20
3C	Vertical blanking : 38	26	59	Module revision	20
3D	Vertical active : blanking	30	5A	Monitor Descriptor #3	00
3E	Horizontal Sync offset : 24	18	5B	Flags	00
3F	Horizontal Sync pulse width : 136	88	5C	Flags	00
40	Ver sync offset : pulse width = 3 : 6	36	5D	Data type tag (binary coded)	FE
41	Hor Sync offset, PW : pulse width	00	5E	Flags	00
42	Horizontal image size (mm) : 245 mm	F5	5F	1st character : B	42
43	Vertical image size (mm) : 184 mm	B8	60	2nd character : O	4F
44	Horizontal & Vertical image size : 0	00	61	3rd character : E	45
45	Horizontal border : 0	00	62	4th character : Blank	20
46	Vertical border : 0	00	63	5th character : H	48
47	Flags : 0	18	64	6th character : Y	59
48	Monitor Descriptor #2	00	65	7th character : D	44
49	Flags	00	66	8th character : I	49
4A	Flags	00	67	9th character : S	53
4B	Data type Tag (Binary coded)	FE	68	10th character	0A
4C	Flags	00	69	11th character	20
4D	HSPW min (pixel clks)	20	6A	12th character	20
4E	HSPW max (pixel clks)	0A	6B	13th character	20
4F	Thbp min (pixel clks)	20	6C	Monitor Descriptor #4	00
50	Thbp max (pixel clks)	20	6D	Flags	00
51	VSPW min (line pulses)	20	6E	Flags	00
52	VSPW max (line pulses)	20	6F	Data type tag (binary coded)	FE

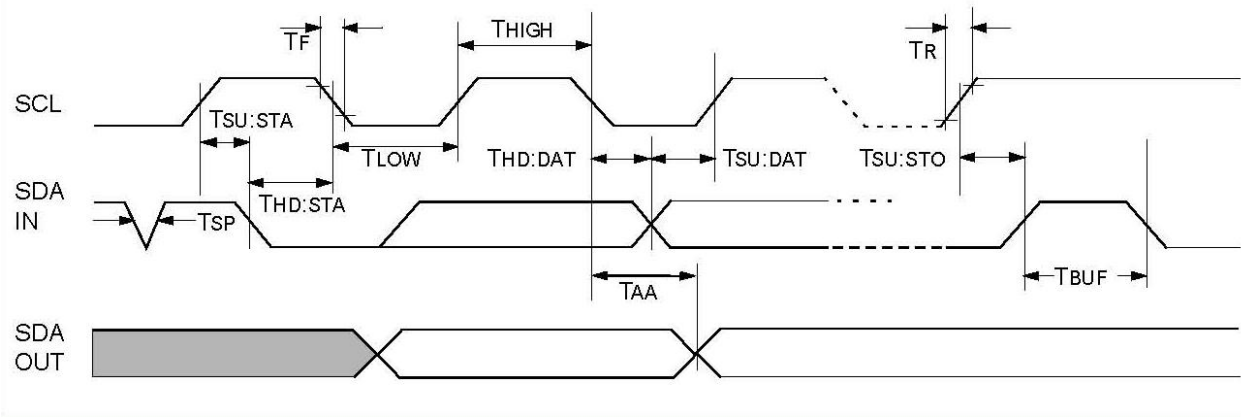
Add (Hex)	Field name & comments	Data	Add (Hex)	Field name & Comments	Data
70	Flags	00	78	8th character : -	2D
71	1st character : H	48	79	9th character : 2	32
72	2nd character : T	54	7A	10th character : 2	32
73	3rd character : 1	31	7B	11th character : 0	30
74	4th character : 2	32	7C	12th character	0A
75	5th character : X	58	7D	13th character	20
76	6th character : 2	32	7E	Extension Flag	00
77	7th character : 1	31	7F	Checksum	9D

13.2 EDID chip Timing specification

Parameter	Symbol	STD MODE		Vcc=2.5~5.5V Fast mode		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock Frequency	FCLK	-	100	-	400	KHz	
Clock high time	THIGH	4000	-	600	-	ns	
Clock low time	TLOW	4700	-	1300	-	ns	
SDA and SCL rise time	TR	-	1000	-	300	ns	Note 1
SDA and SCL fall time	TF	-	300	-	300	ns	Note 1
Start condition hold time	THD:STA	4000	-	600	-	ns	
Start condition setup time	TSU:STA	4700	-	600	-	ns	
Data input hold time	THD:DAT	0	-	0	-	ns	Note 2
Data input setup time	TSU:DAT	250	-	100	-	ns	
Stop condition setup time	TSU:STO	4000	-	600	-	ns	
Output valid from clock	TAA	-	3500	-	900	ns	Note 3
Bus free time	TBUF	4700	-	1300	-	ns	
Output fall time from VIH minimum to VIL maximum	TOF	-	250	20 + 0.1Ca	250	ns	Note 1
Input filter spike suppression (SDA and SCL pins)	TSP	-	50	-	50	ns	Note 3
Write-cycle time	TWC	-	10	-	10	ms	
Endurance		1M	-	1M	-		

Notes :

1. Not 100 % tested. C_B = Total capacitance of one bus line in pF
2. As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
3. The combined T_{SP} and V_{HYS} specifications are due to Schmitt Trigger inputs which provide improved noise spike suppression. This eliminated the need for a TI specification standard operation.
4. All parameters apply across the specified operation ranged unless otherwise noted (Vcc = 1.8V to 5.5 V, Temp = -40 ℃ to 85 ℃)



14.0 Appendix

Figure 1. Measurement Set up

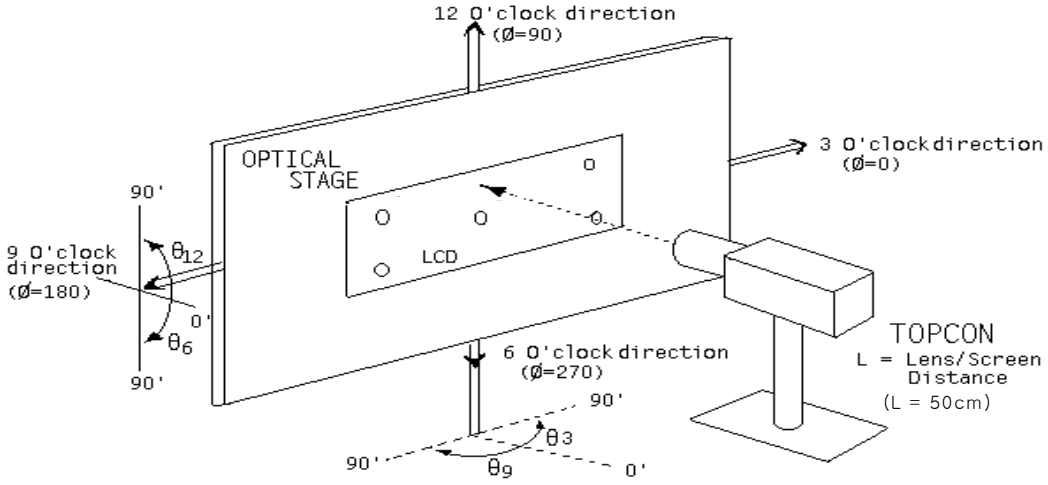


Figure 2. Average Luminance Measurement Locations & Uniformity Measurement Locations

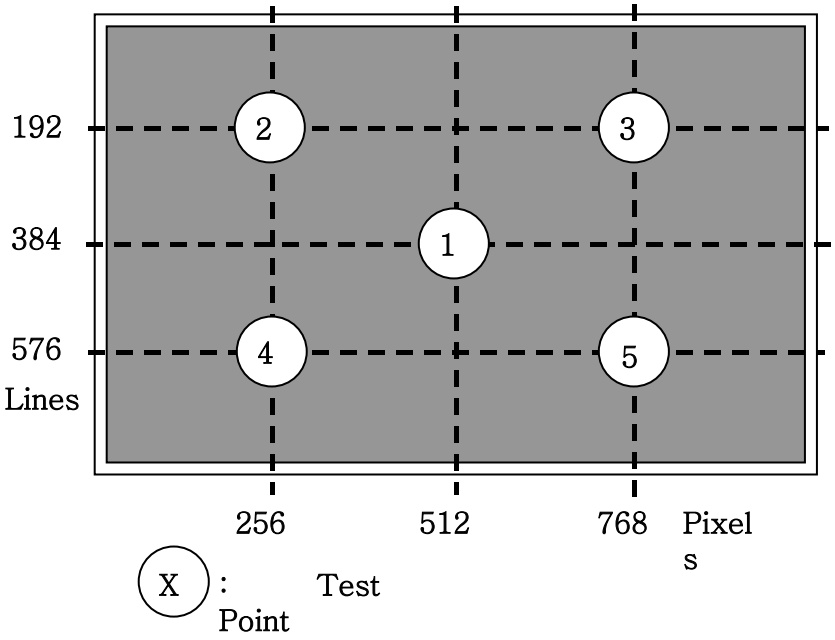


Figure 3. Response Time Testing

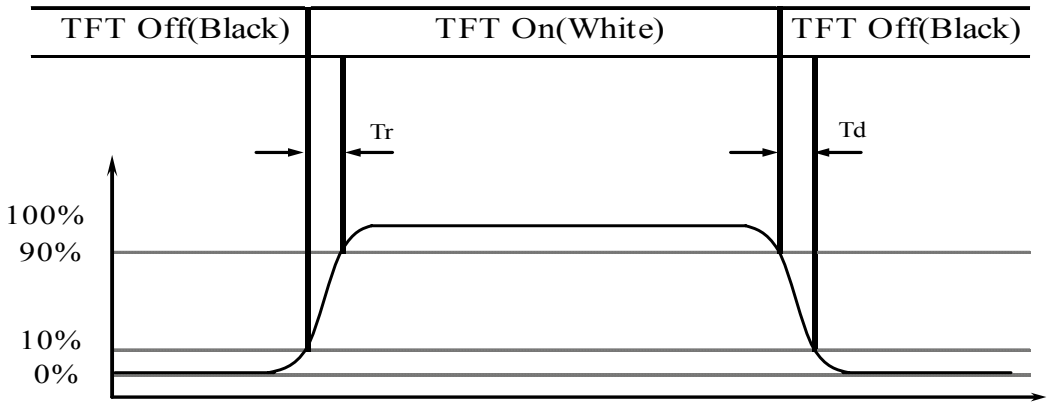
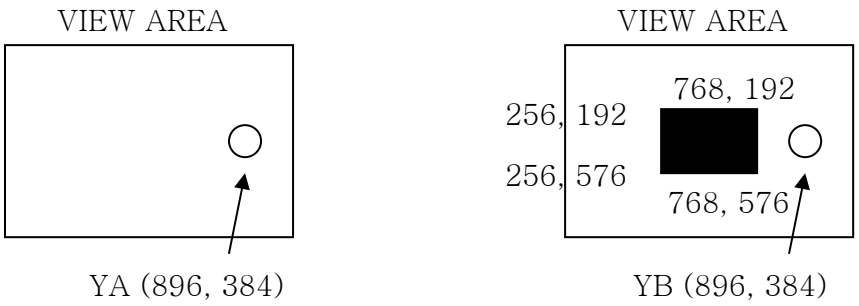


Figure 4. Cross Modulation Test Description



$$\text{Cross Talk} = \frac{YB - YA}{YA} \times 100$$

Where:
YA = Initial luminance of measured area (cd/m2)
YB = Subsequent luminance of measured area (cd/m2)
The location measured will be exactly the same in both patterns.

Figure 5. TFT-LCD Module Outline Dimension (Front View)

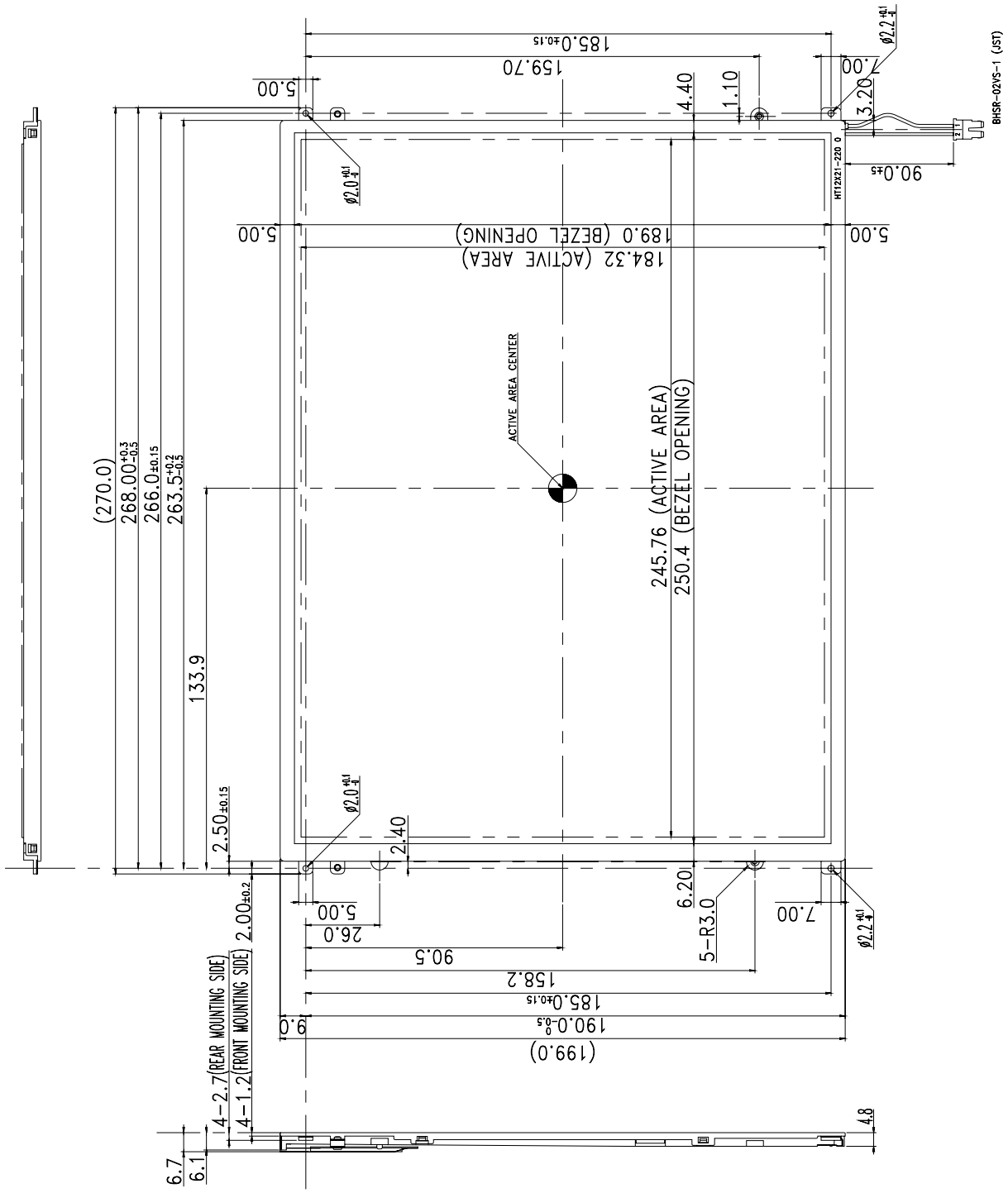


Figure 6. TFT-LCD Module Outline Dimensions (Rear view)