TITLE : HV101WU1-1E6

Product Specification

HYDIS Technologies

A4(210 X 297)

REVISION HISTORY

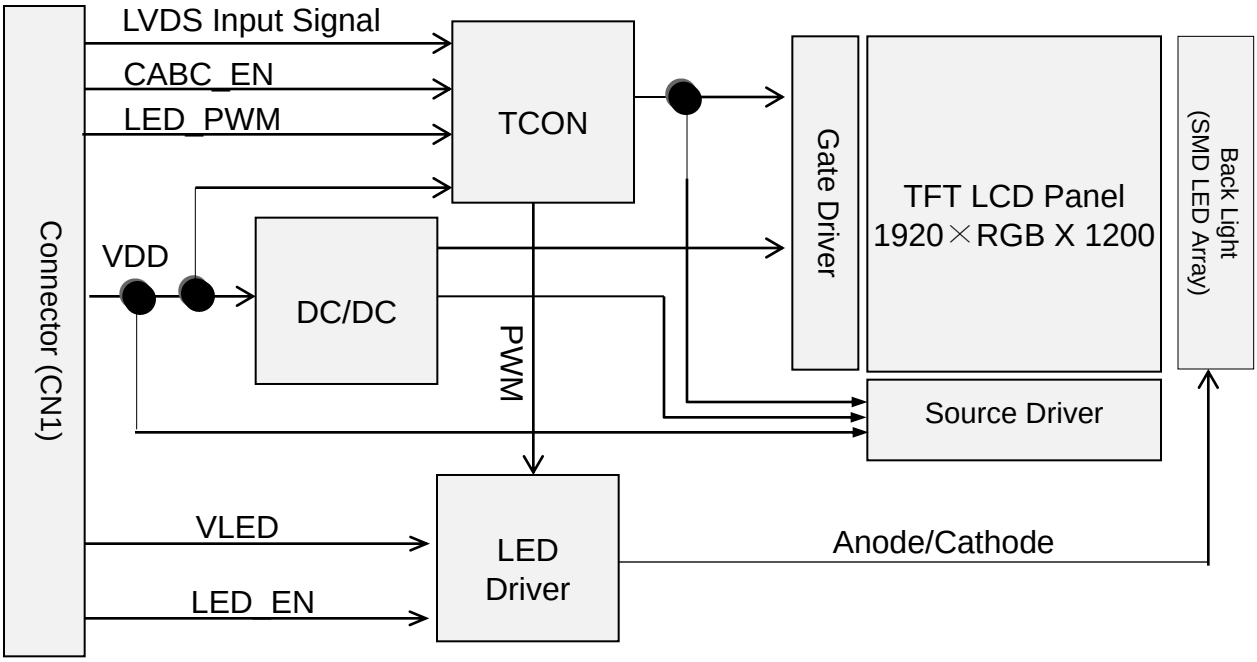
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
0		* Initial Release	2014.01.14	A.Y.SEO
A	E1401-F004	- Revise Product & Box label marking - Add inner box packing label	2014.02.03	A.Y.SEO
B	E1405-F002	- Revise Reliability Test Condition	2014.06.09	A.Y.SEO

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

HV101WU1-1E6 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 10.1 inch diagonally measured active area with WUXGA resolutions (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is a low reflection and higher color type.



1.2 Features

- 3.3 V Logic Power
- LVDS (2ch) Interface for 1920RGB x 1200 resolution. (Max 120MHz / Ch)
- 16.7M Colors (6bit + HFRC)
- Data Enable Signal Mode
- SMD LED (84EA) Top & Bottom alignment
- Green Product (RoHS) & Halogen free

1.3 Application

- Slate/Tablet

1.4 General Specifications

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	216.576(H) ×135.36(V)	mm	
Number of pixels	1920(H) ×RGB X 1200(V)	pixels	
Pixel pitch	0.1128 × 0.1128	mm	
Pixel arrangement	RGB Vertical Stripe		
Display colors	16.7M (6bit + HFRC)	colors	
Display mode	Normally Black		
Outline dimension	229±0.3(H)×153±0.3(V)×2.5±0.2(D)	mm	
Weight	144 ±5	g	
Back-light	Top & Bottom alignment, 84-LEDs type		

2.0 ABSOLUTE MAXIMUM RATINGS

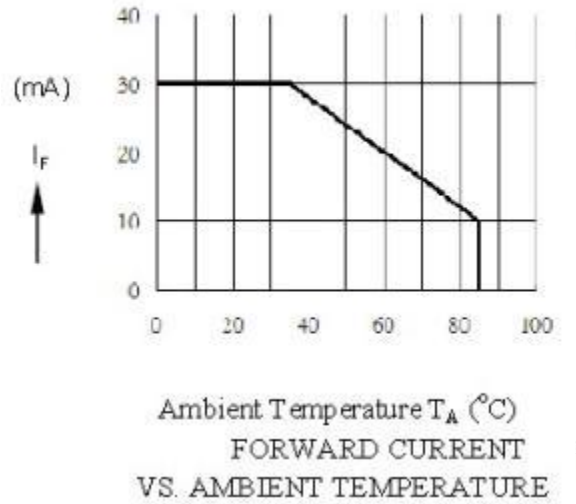
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.

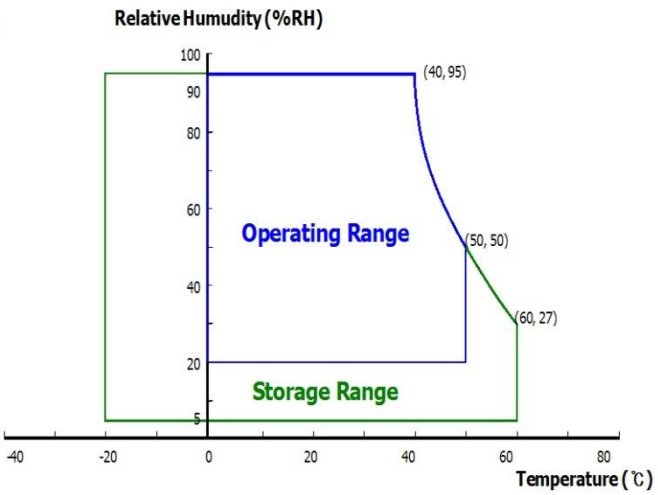
< Table 2. Absolute Maximum Ratings > Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Logic Power Supply Voltage	V_{DD}	-0.3	4.0	V	
Logic Power Supply Voltage	V_{CC}	-0.3	2.0	V	
Back-light Power Supply Voltage	HV_{DD}	-0.3	40	V	
Back-light LED Current	I_{LED}	-	30	mA	Note 1
Back-light LED Reverse Voltage	V_R	-	5	V	
Operating Temperature	T_{OP}	-0	+50	℃	Note 1, Note 2
Storage Temperature	T_{SP}	-20	+60	℃	

Note 1. Ambient temperature vs allowable forward current are shown in the figure below.

Note 2. Temperature and relative humidity range are shown in the figure below.
90% RH Max. (40℃ ≥ Ta)
Maximum wet - bulb temperature at 39℃ or less. (> 40℃) No condensation.





3.0 ELECTRICAL SPECIFICATIONS

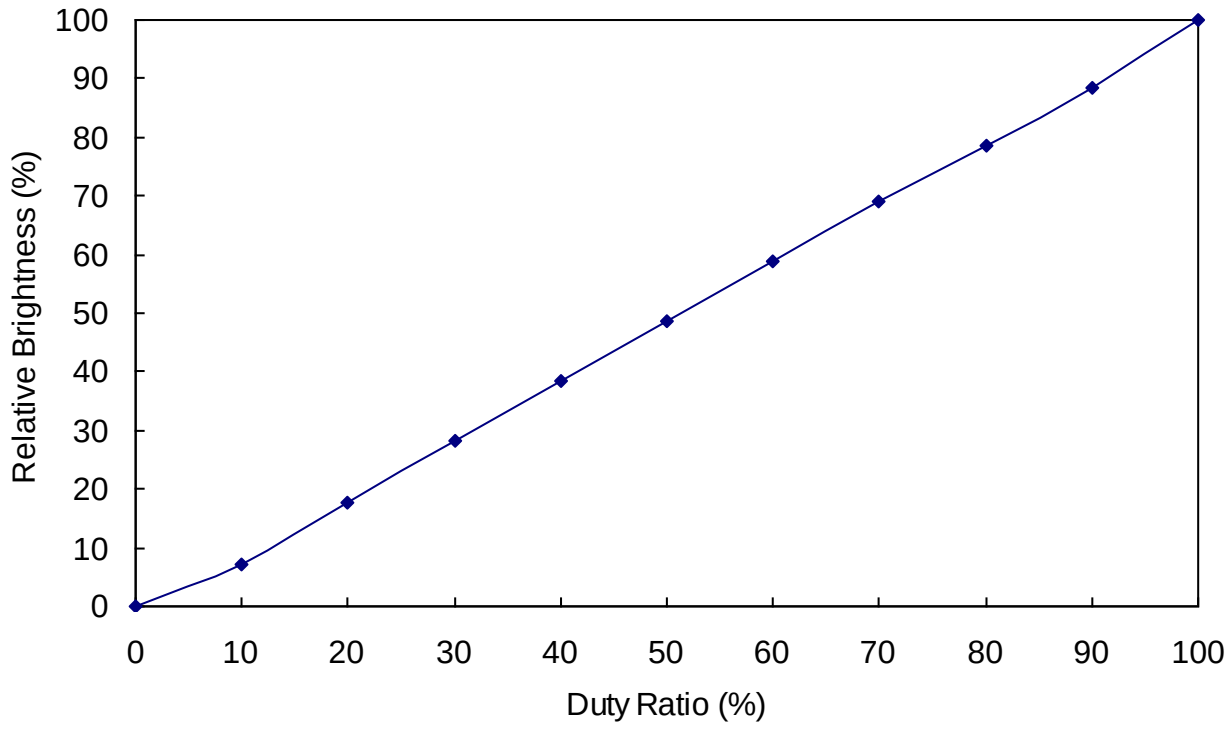
3.1 Electrical Specifications

< Table 3. Electrical Specifications >

Parameter		Min.	Typ.	Max.	Unit	Remarks
Logic Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Logic Power Supply Current	I_{DD}	-	280	-	mA	Vdd=3.3V, 25℃ Note 1
Back-light LED Voltage / Back-light LED Total Voltage	V_{LED} /V_{BL}	-	3.0/42.0	-	V	
Back-light LED Current / Back-light LED Total Current	I_{LED} /I_{BL}	-	20/120	-	mA	
VLED for LED Driver	VLED	6.5	12	25	V	For LED Driver
PWM Frequency for LED Driver	LED_PWM	0.1		20	KHz	
Logic voltage Range (EN, PWM)		0.0	3.3	5.5	V	
Power Consumption	P_{DD}	-	0.924	1.3	W	Note 2 Vdd=3.3V, 25℃
	PBL	-	5.04	5.20	W	
	Ptotal	-	5.928	6.5	W	

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.
(Test Pattern : White)
2. P_{BL} is calculated value for reference (VLED × ILED × # of LEDs (84EA)).
This value is without LED driver efficiency .

3.2 PWM Duty Ratio vs Brightness



Notes :

In case of duty ratio 0%, LED can't illuminate itself so this state is LED off.

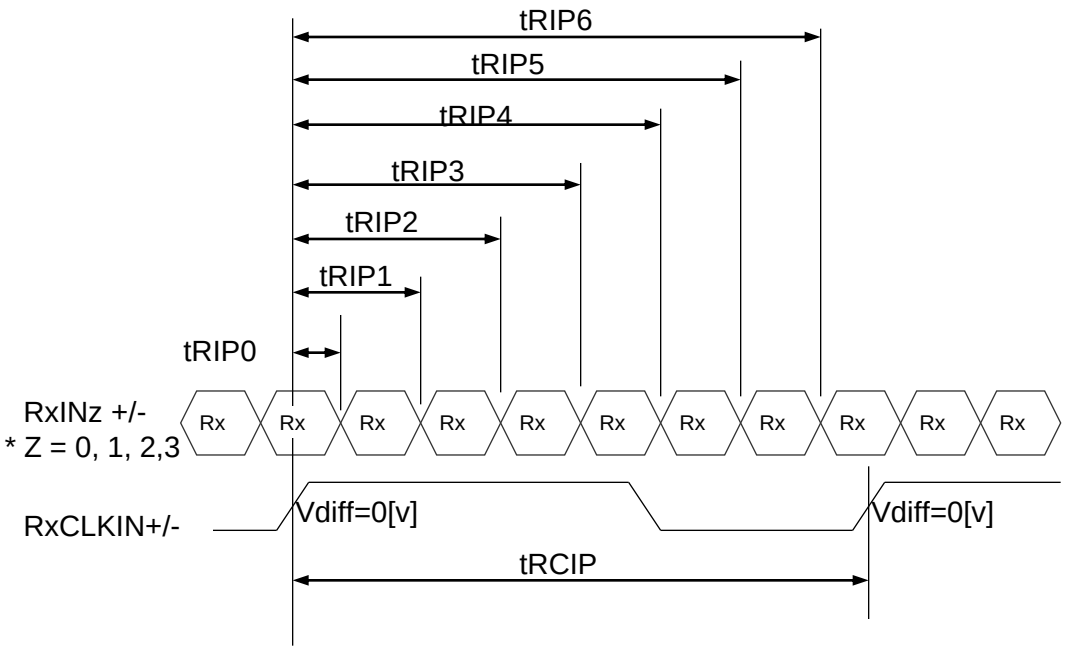
In case of duty ratio 100%, the brightness of LED is maximum and the state is LED on.

3.2 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter

< Table 4, LVDS Rx Interface Timing Specification>

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLKIN Period	tRCIP	-	13.23	-	nsec	
Input Data 0	tRIP0	-0.4	0.0	+0.4	nsec	
Input Data 1	tRIP1	tRICP/7-0.4	tRICP/7	tRICP/7+0.4	nsec	
Input Data 2	tRIP2	2 ×tRICP/7-0.4	2 ×tRICP/7	2 ×tRICP/7+0.4	nsec	
Input Data 3	tRIP3	3 ×tRICP/7-0.4	3 ×tRICP/7	3 ×tRICP/7+0.4	nsec	
Input Data 4	tRIP4	4 ×tRICP/7-0.4	4 ×tRICP/7	4 ×tRICP/7+0.4	nsec	
Input Data 5	tRIP5	5 ×tRICP/7-0.4	5 ×tRICP/7	5 ×tRICP/7+0.4	nsec	
Input Data 6	tRIP6	6 ×tRICP/7-0.4	6 ×tRICP/7	6 ×tRICP/7+0.4	nsec	

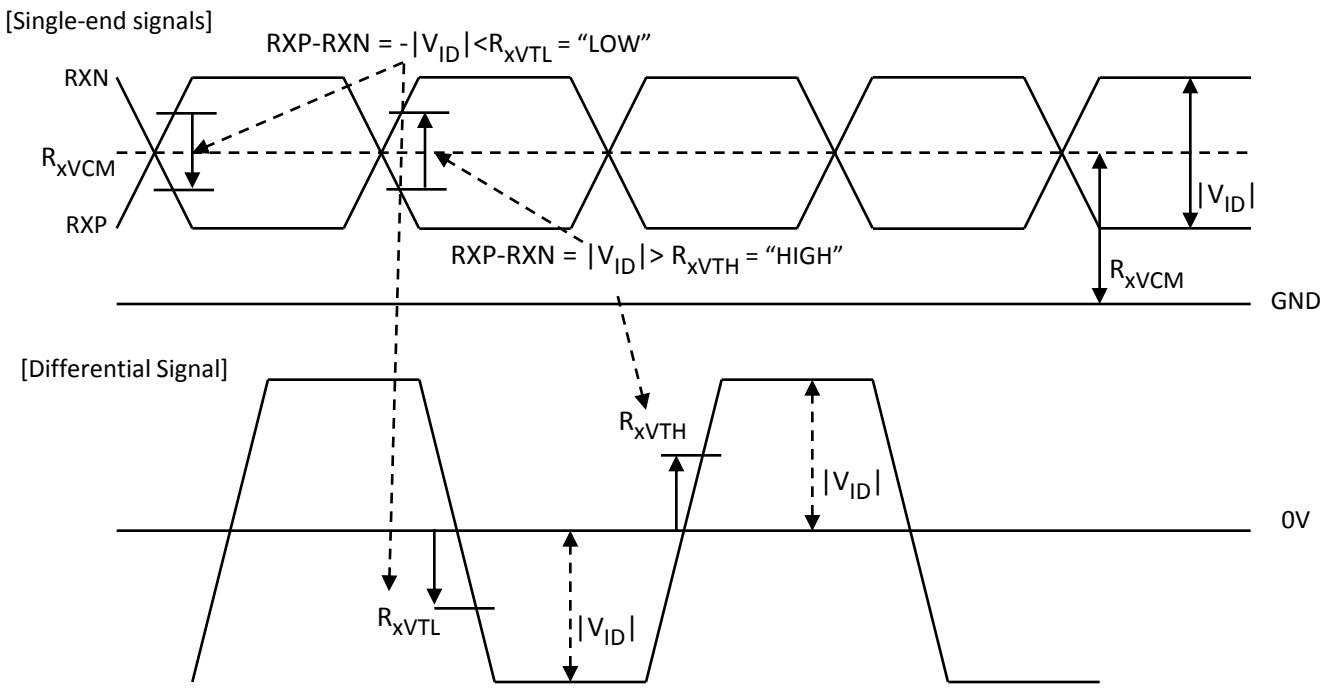


3.3 LVDS Interface DC Characteristic

< Table 5. LVDS Receiver DC Characteristics>

Parameter		Min.	Typ.	Max.	Unit	Remarks
Differential Input High Threshold voltage	R_{xVTH}	-	-	+100	mV	
Differential Input Low Threshold voltage	R_{xVTL}	-100			mV	
Input Voltage Range (Singled-end)	R_{xVIN}	0		2.4	V	VDDT : 3.3[V]
		0		VDD-0.4		VDDT : 2.5[V]
Input Common mode voltage	R_{xVCM}	$\|V_{ID}\|/2$		2.4- $\|V_{ID}\|/2$	V	VDDT : 3.3[V]
		$\|V_{ID}\|/2$		VDD-0.4- $\|V_{ID}\|/2$		VDDT : 2.5[V]
Differential input voltage	$\|V_{ID}\|$	100		600	mV	
Differential input leakage current	RV_{xLIK}	-10		+10	uA	
Clock Frequency	R_{xFCLK}	25		120	MHz	

*.VDDT : LVDS Receiver logic power input voltage



4.0 OPTICAL SPECIFICATIONS

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ12) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. V_{DD} shall be 3.3+/- 0.3V at 25°C.

4.2 Optical Specifications

<Table 6. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	89	-	Deg.	Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	600	750	-		Note 2
Luminance of White	1 Points	Y_w	Θ = 0°	650	700	-	cd/m^2	Note 4
White Luminance uniformity	9 Points	ΔY9		75	-	-	%	
White Chromaticity		W_x	Θ = 0°	0.281	0.311	0.341	-	Note 3
		W_y		0.327	0.357	0.387	-	
Reproduction of color	Red	R_x	Θ = 0°	0.576	0.606	0.636	-	
		R_y		0.320	0.350	0.380	-	
	Green	G_x		0.281	0.311	0.341	-	
		G_y		0.533	0.563	0.593	-	
	Blue	B_x		0.115	0.145	0.175	-	
		B_y		0.094	0.124	0.154	-	
Response Time		Total ($T_r + T_d$)	Ta= 25° C Θ = 0°	-	30	40	ms	Note 5
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 6

Notes :

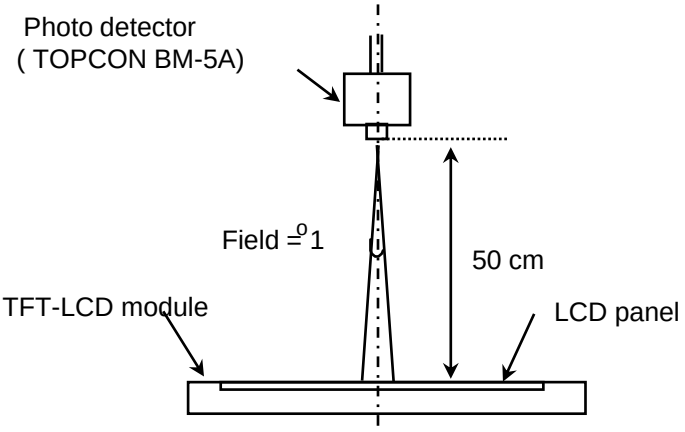
1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state (see Figure1). Luminance Contrast Ratio (CR) is defined mathematically as CR = Luminance when displaying a white raster / Luminance when displaying a black raster.

3. Reference only / Standard Front Surface Treatment Measured with green cover glass. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

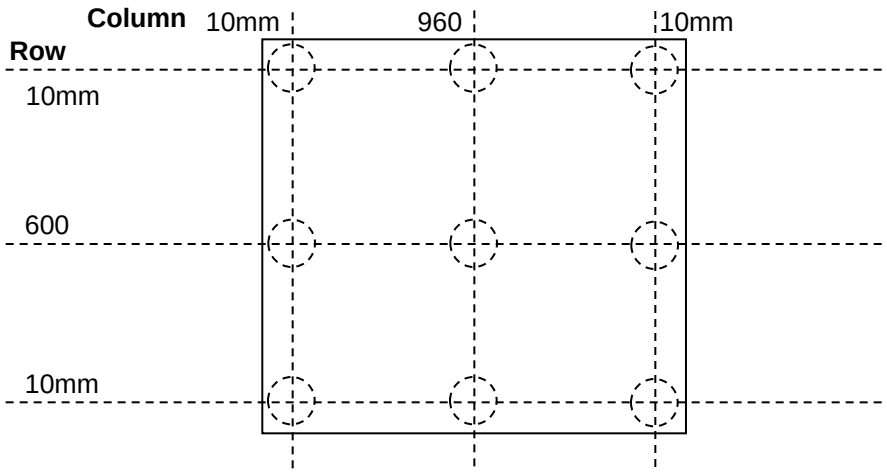
4.3 Optical Measurements

Figure 1. Measurement Set Up



Optical characteristics measurement setup

Figure 2. White Luminance and Uniformity Measurement Locations (9 points)



Note 4.
Luminance of white is defined as luminance values of 9 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 2 for a total of the measurements per display.

•Yw = (Sum of 9 Points Luminance / 9)
•ΔY9 = (Min Luminance of 9points /Max luminance of 9 point) * 100%
* LED Condition = (Duty Ratio 100%, LED current 20.0mA)

Figure 3. Response Time Testing

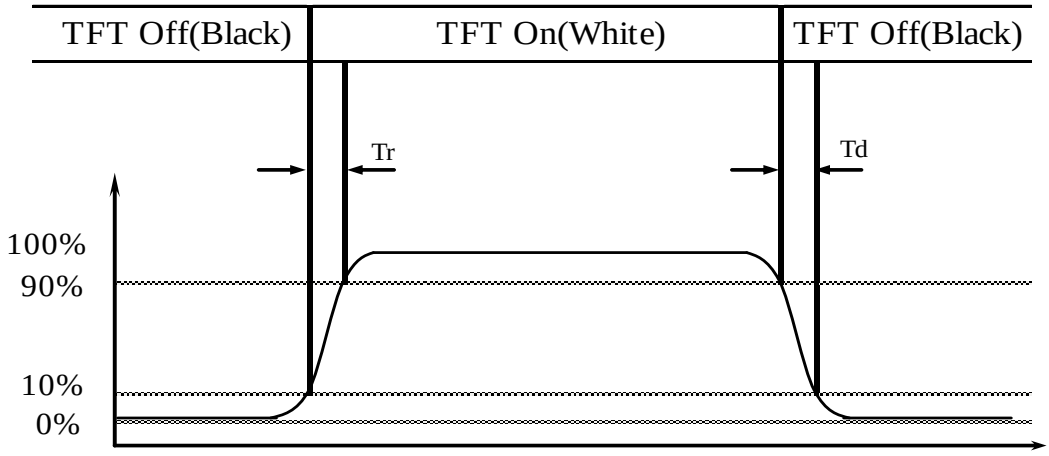
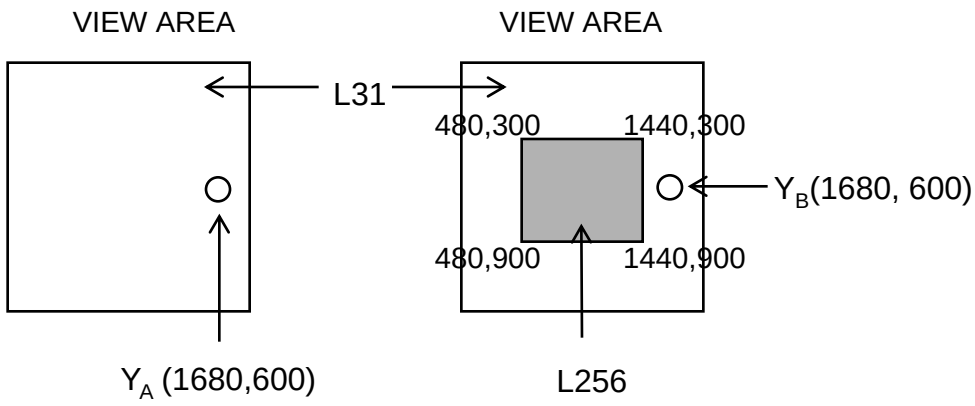


Figure 4. Cross Modulation Test Description



$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns

Note 5.

The electro-optical response time measurements shall be made as Figure 4 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Note 6.

Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark (Refer to Figure 4).

5.0 INTERFACE CONNECTIONS

5.1 Electrical Interface Connection

CN1	HYDIS side connector	AYF334535 (Panasonic)

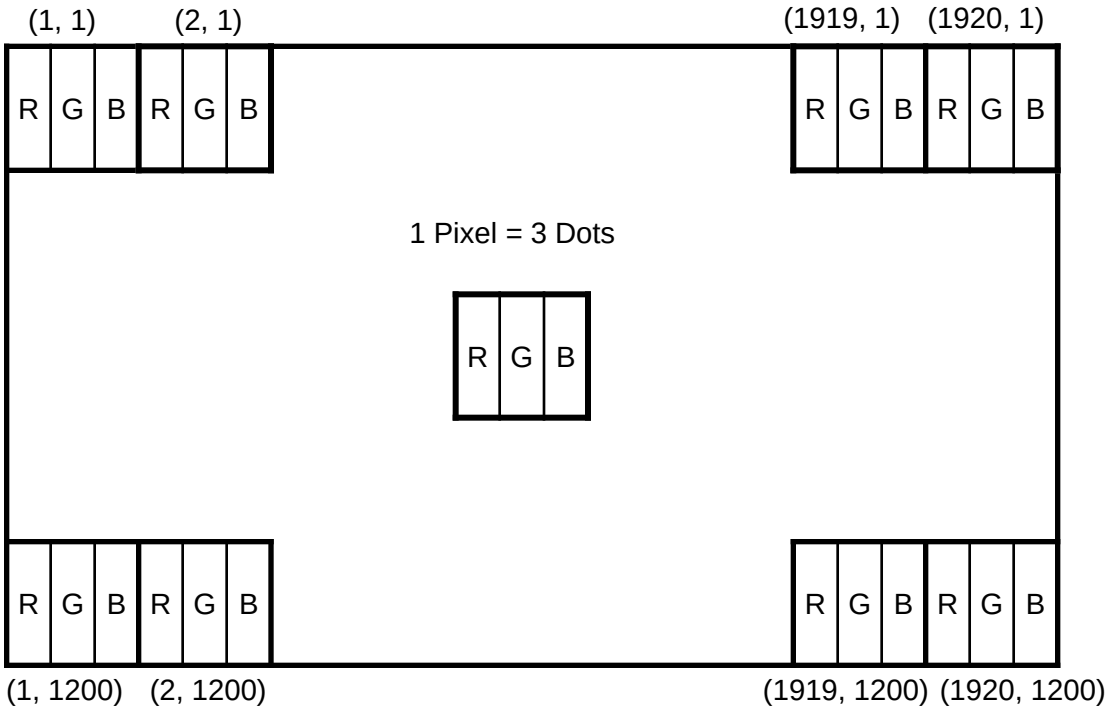
< Table 7, Electrical Interface Connection >

Pin No.	SYMBOL	FUNCTION
1	VDD	Power Supply, 3.3V(Typical)
2	VDD	Power Supply, 3.3V(Typical)
3	VDD	Power Supply, 3.3V(Typical)
4	VDD	Power Supply, 3.3V(Typical)
5	NC(BIST)	BIST testing (Only for Hydis)
6	ALVDS_3P	A LVDS Input Data Pair
7	GND	Ground
8	ALVDS_3N	A LVDS Input Data Pair
9	GND	Ground
10	GND	Ground
11	BLVDS_3P	B LVDS Input Data Pair
12	ALVDS_CLKP	A LVDS Input Data Pair
13	BLVDS_3N	B LVDS Input Data Pair
14	ALVDS_CLKN	A LVDS Input Data Pair
15	GND	Ground
16	GND	Ground
17	BLVDS_CLKP	B LVDS Input Data Pair
18	ALVDS_2P	A LVDS Input Data Pair
19	BLVDS_CLKN	B LVDS Input Data Pair
20	ALVDS_2N	A LVDS Input Data Pair
21	GND	Ground
22	GND	Ground
23	BLVDS_2P	B LVDS Input Data Pair
24	ALVDS_1P	A LVDS Input Data Pair

● **ALVDS : Channel A , BLVDS : Channel B**

Pin No.	SYMBOL	FUNCTION
25	BLVDS_2N	B LVDS Input Data Pair
26	ALVDS_1N	A LVDS Input Data Pair
27	GND	Ground
28	GND	Ground
29	BLVDS_1	B LVDS Input Data Pair
30	ALVDS_0P	A LVDS Input Data Pair
31	BLVDS_1N	B LVDS Input Data Pair
32	ALVDS_0N	A LVDS Input Data Pair
33	GND	Ground
34	GND	Ground
35	BLVDS_0P	B LVDS Input Data Pair
36	NC	NC
37	BLVDS_0N	B LVDS Input Data Pair
38	LED_EN	LED Enable Pin : High → Enable (Typ : 3.3V)
39	NC	NC
40	CABC_EN	CABC Function Enable Pin : High → Enable (Typ : 3.3V) Low or floating, When dose not use CABC Function
41	LED_PWM	PWM Signal for LED Dimming Control
42	VLED	LED Power Supply (12V)
43	VLED	LED Power Supply (12V)
44	VLED	LED Power Supply (12V)
45	VLED	LED Power Supply (12V)

5.2 Data Input Format



6.0. SIGNAL TIMING SPECIFICATIONS

6.1 The LCM is operated by the only DE (Data enable) mode

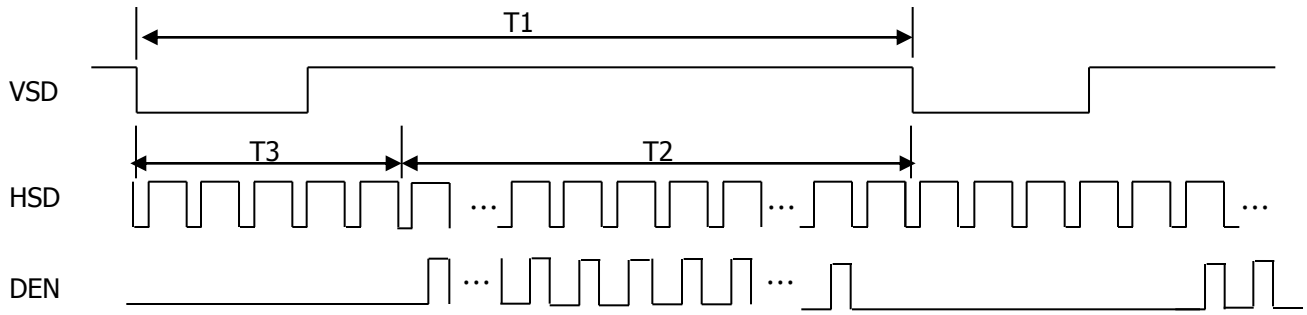
< Table 8, Signal Timing >

Item	Symbol	Min.	Typ.	Max.	Unit
Frame Rate	-	50	60	65	Hz
Frame Period	T1	1205	1235	1386	Lines
Vertical Display Time	T2		1200		Lines
Vertical Blanking Time	T3	5	35	186	Lines
1 Line Scanning Time	T4	1925	2080	2216	Clocks
Horizontal Display Time	T5		1920		Clocks
Horizontal Blanking Time	T6	5	160	296	Clocks
Clock Rate	1/T7	125.97	154	173.5	MHz

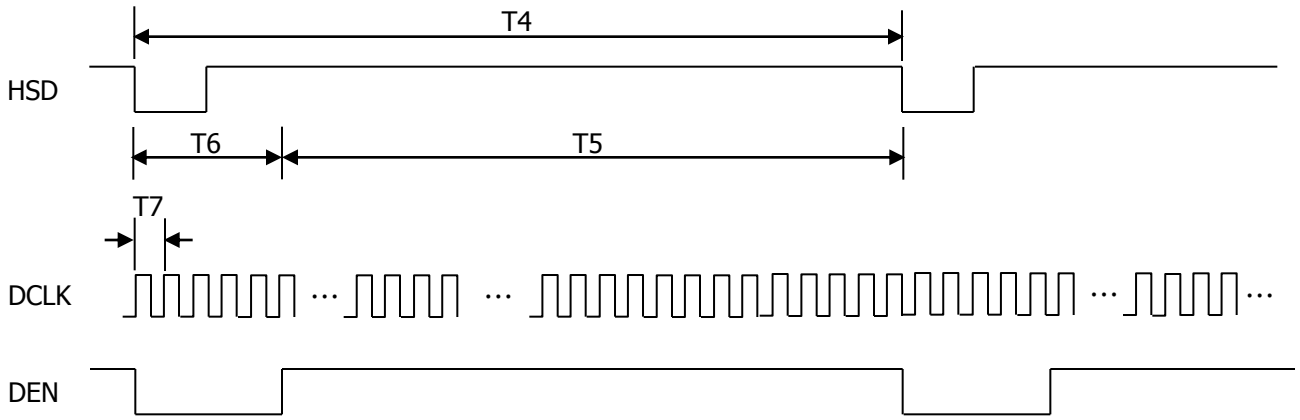
Note 1. This value only guarantee for the circuit-operation

7.0 SIGNAL TIMING WAVEFORMS

7.1 Vertical Input Timing Waveforms of Interface Signal



7.2 Horizontal Input Timing Waveforms of Interface Signal



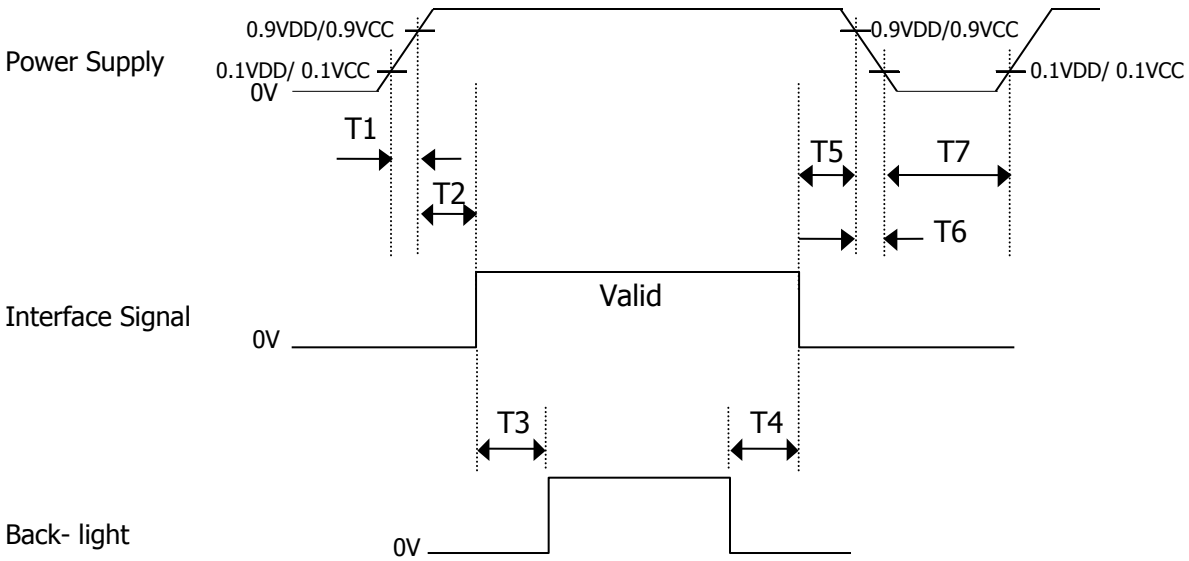
8.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

A total of 16.7M colors are displayed with dither & HFRC using 64 gray from 8bit input.

Colors & Gray Scale		Red data								Green data								Blue data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale Of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



- T1 ≤ 50 ms
- 100 ≤ T2 ≤ 150 ms
- 70ms ≤ T3
- 200 ms ≤ T4
- 0 ≤ T5 ≤ 50 ms
- 0 ≤ T6 ≤ 10ms
- 150ms ≤ T7

Notes : 1. When the power supply VDD/ VCC is 0V, Keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 5 & 6 shows mechanical outlines for the model

< Table 9, Mechanical Characters >

Parameter	Specification	Unit
Active Area	216.576(H) ×135.36(V)	mm
Number of pixels	1920(H) X 1200(V) (1 pixel = R + G + B dots)	
Pixel pitch	0.1128(H) X 0.1128(V)	mm
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M (6bit + HFRC)	
Display mode	Normally Black	
Outline dimension	229(H)×153(V)×2.5 (D) (Typ.)	mm
Weight	144 ±5	g
Back-light	Top & Bottom alignment 84-LEDs type (2 X 42 Array)	

10.2 Polarizer Hardness.

The surface of the LCD has a coating to reduce scratching.

10.3 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 150lux. The manufacture shall furnish limit samples of the panel showing the light leakage acceptable.

11.0 Mechanical Drawing

Figure 5. TFT-LCD Module Outline Dimension (Front View)

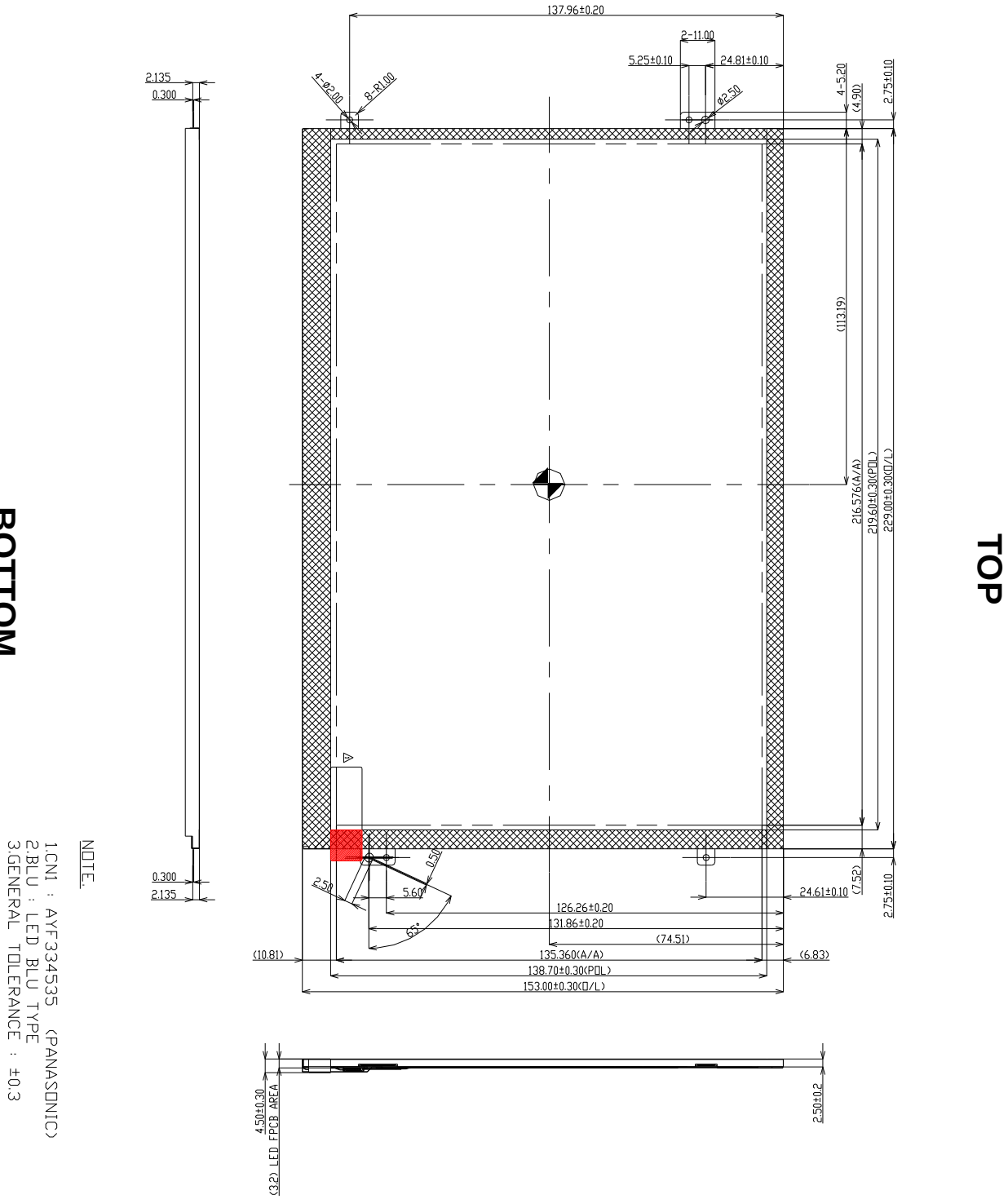
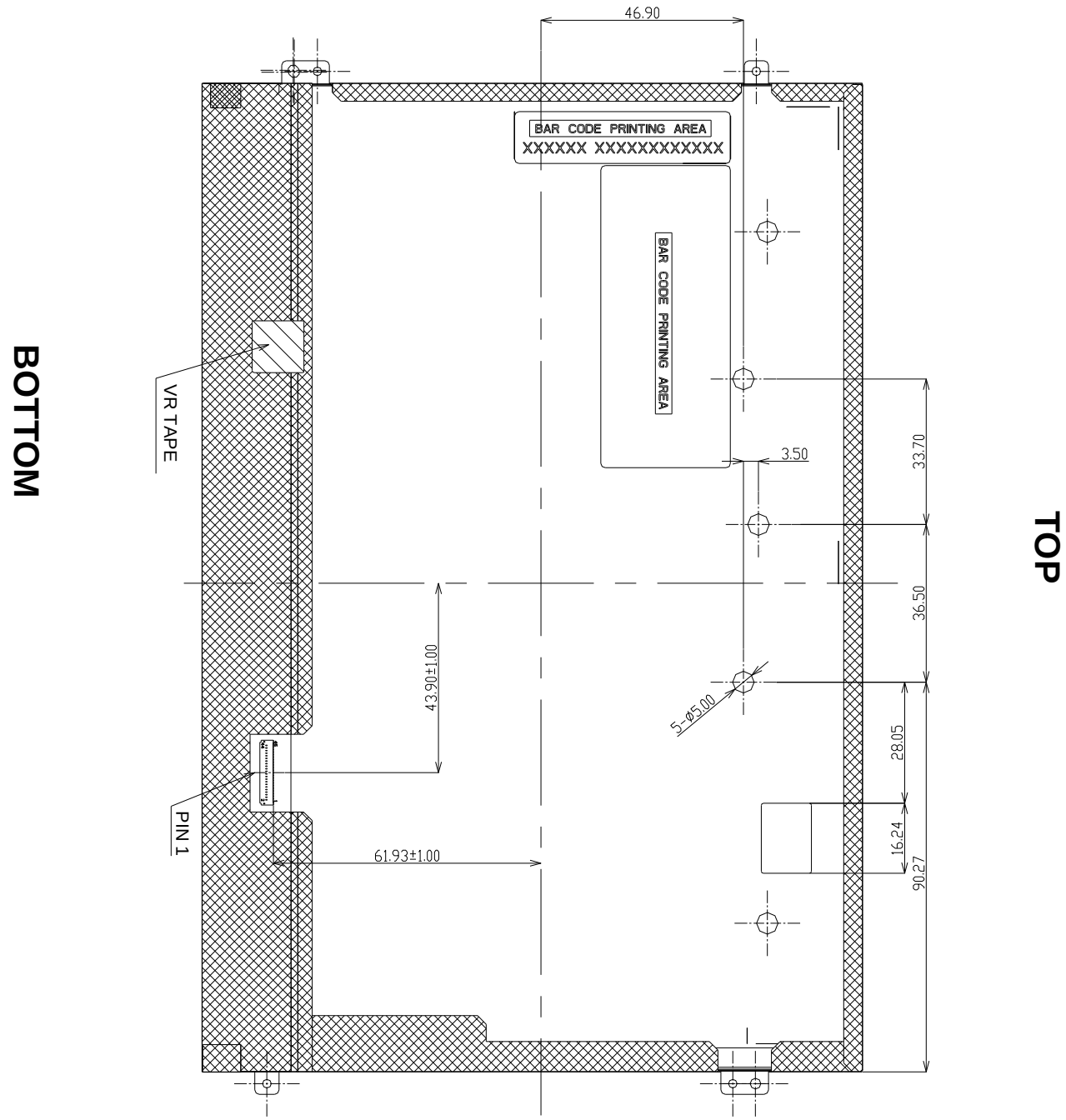


Figure 6. TFT-LCD Module Outline Dimensions (Rear view)



12.0 RELIABLITY TEST

The Reliability test items and its conditions are shown in below.

< Table10. Reliability Test >

No	Test Item	Conditions	Remark
1	High temperature storage	70 ℃ /240h	
2	Low temperature storage	-30 ℃ /240h	
3	High temperature /High humidity Storage	60℃/90%RH/240h	
4	High temperature operating	60 ℃ /240H	
5	Low temperature operating	-20 ℃ /240h	
6	High temperature /High humidity operating	50 ℃ /90%RH/240h	
7	Thermal Shock Storage	-30℃(30min) ~ +60℃(30min), 27cycles	
8	Shock test	980m/s^2,Action time: 6ms, Time:3times for each direction, Direction:+/-X, +/-Y, +/-Z	
9	Package Vibration test	Sine: 1.0G 10~50Hz, sweep 15min, 30min/axis. XYZ Random : 1.04Grms 2~200Hz, 30min/Z, 15min/X,Y PSD 2Hz 0.001g^2/Hz, 4~8Hz 0.03g^2/Hz 40Hz 0.003g^2/Hz, 55~70Hz 0.01g^2/Hz 200Hz 0.001g^2/Hz	
10	Package Drop test	1Angle, 3Edge, 6Face, ASTM D 4169 Assurance Level I	
11	ESD test	Air +/-10KV ,contact +/-6KV ,5times/9points/Active Area.	Note 1

Note 1 : ESD testing in assemble state. Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

13.0 HANDLING & CAUTIONS

13.1 Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

13.2 Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass (epoxy) material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

13.3 Cautions for the operation

- When the module is operating, do not lose MCLK, DE signals. If any one of these signals were lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

13.4 Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

13.5 Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

13.6 Cautions for the digitizer assembly

- When assembling FPC connector, do not flip connector past 90° due to possible damage to connector.
- When positioning digitizer underneath driver IC, do not lift driver IC past 90° due to possible damage to drive IC pattern.
- Please be warned that during assembly of digitizer, the opening or closing of FPC will result in possible electrostatic discharge damage to the LED

13.7 Other cautions

- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

14.0 LABELS

14.1 Product Label

HYDIS Barcode

1	2	3	4	5	6	7
X X	X	X	X X	X	X X X X	X X X X X X

No 1. Type

No 2. Rank / Grade

No 3. Line Classification (TOC : T)

No 4. Year (12 : 2012, 13 : 2013 …)

No 5. Month (1, 2, 3,…, 9, X, Y, Z)

No 6. FG Code

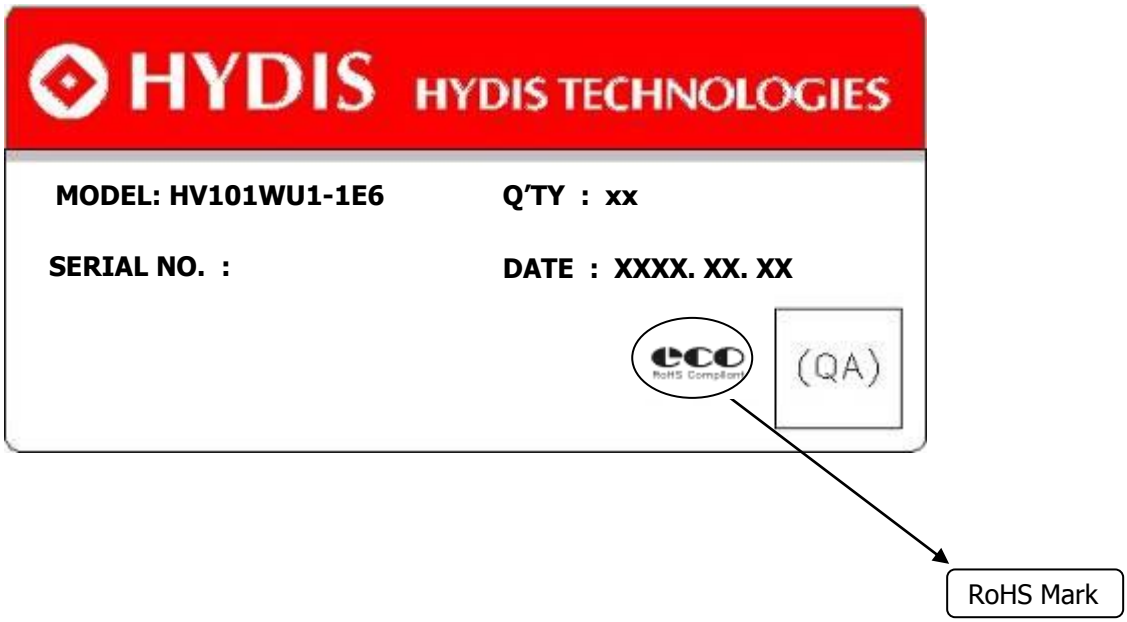
No 7. Serial Number

14.2 Inner Box Packing Label

14.2.1 Label Size : 110 mm (L) × 56 mm (W)

14.2.2 Contents

- Model : HV101WU1-1E6
- Q`TY : Module quantity in a box
- Serial No. : N/A
- Date : Packing Date

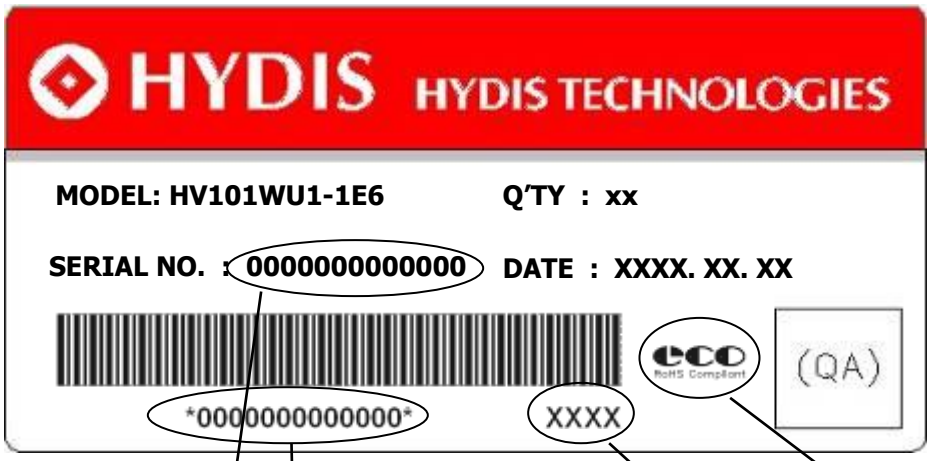


14.3 Outer Box Packing Label

14.3.1 Label Size : 110 mm (L) × 56 mm (W)

14.3.2 Contents

- Model : HV101WU1-1E6
- Q`TY : Module quantity in a box
- Serial No. : Box serial number. See the below figure for detail description.
- Date : Packing Date
- FG Code : FG Code of Product



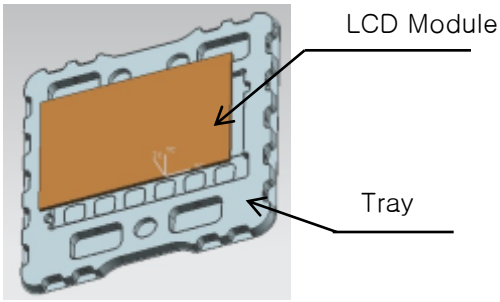
- 01~02 : Type
- 03 : Grade
- 04 : Line Classification → ex: H (HYDIS), T (TOC)
- 05~06 : Year
- 07 : Month
- 08 : ITEM-CODE → 0,A,B… …
- 09~13 : Serial No

FG CODE

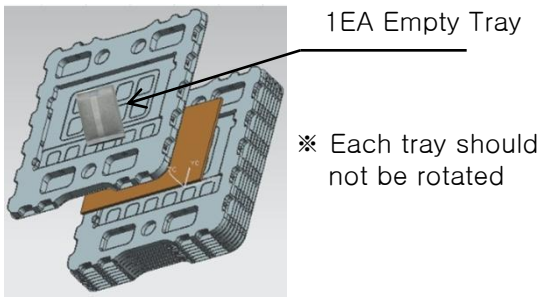
RoHS Mark

15.0 PACKING INFORMATION

15.1 Box Packing

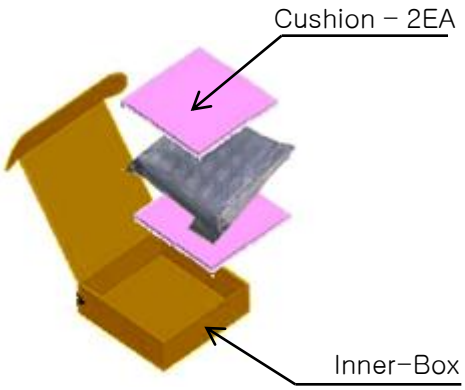


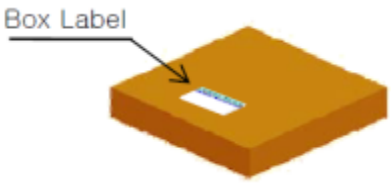
1EA Module per Tray



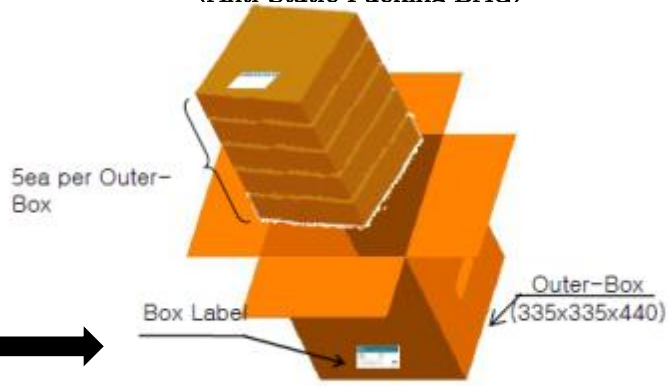
8EA Tray (7 + 1Cover-Tray)

Shielding Packing
(Anti Static Packing BAG)





7EA Module per Inner-Box



35EA LCD Modules Per Outer-Box

15.2 Pallet Packing

15.2.1 PALLET specification

(1) 18 box (max.) / 1 pallet

(2) Pallet : 1100(L) x 1100(W) x 120(H) mm

(3) Pallet stack :1005(L) x 1005(W) x 880(H)mm