TITLE : HV150UX1-102
Product Specification

Rev. 0

BOE HYDIS TECHNOLOGY

REVISION HISTORY

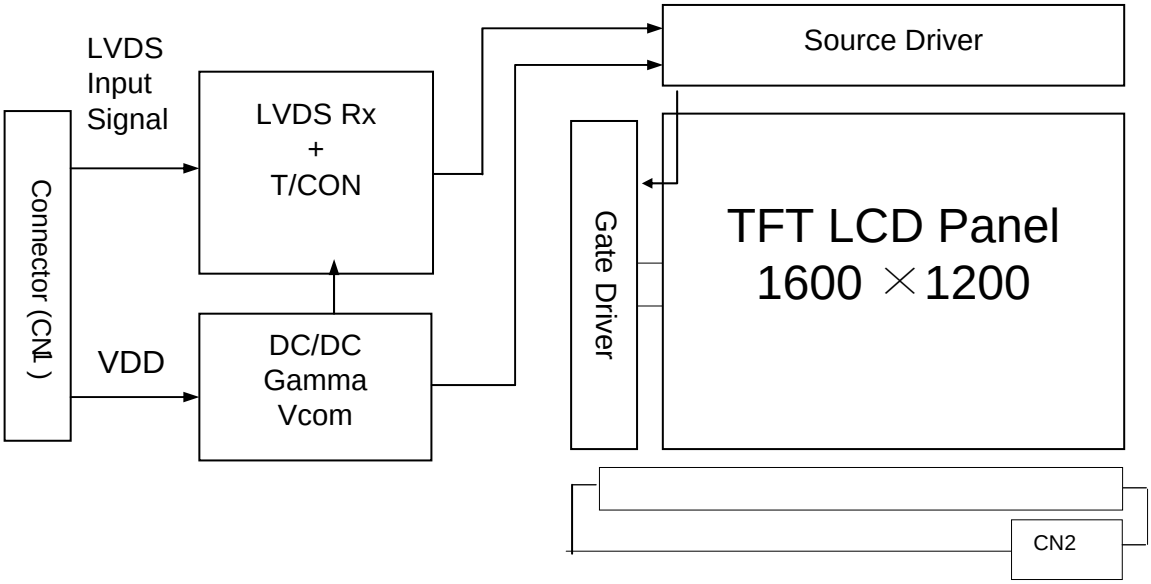
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
O		Initial release	2006.6.16	JY. JEONG

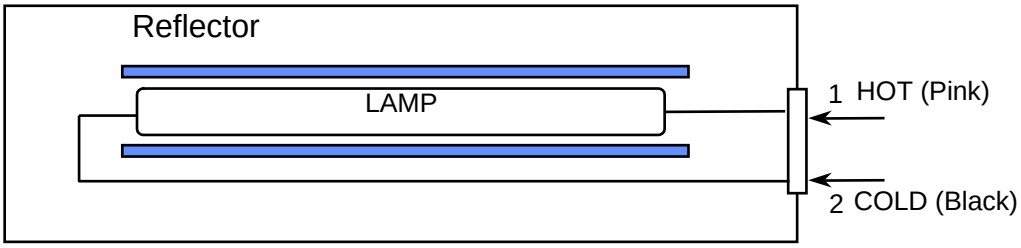
Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

HV150UX1-102 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.0 inch diagonally measured active area with UXGA resolutions (1600 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 262,144 colors. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The DC/AC inverter for back-light driving is not built in this model.





Note) The output of the inverter may change according to the material of the reflector.

1.2 Features

- 15.0 UXGA FFS
- Thin and light weight
- 3.3 V power supply
- 2 Channel LVDS Interface
- sRGB Mode support
- Single CCFL (Bottom side/Horizontal Direction)
- 262,144 colors
- Data enable signal mode
- Side Mounting Frame
- Green Product (RoHS)
- On Board EDID chip
- High contrast ratio

1.3 General Specification

The followings are general specifications at the model HV150UX1-102. (listed in Table 1.)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	304.8 (H) ×228.6 (V) (15.0” diagonal)	mm	
Number of pixels	1600(H) ×1200(V)	pixels	
Pixel pitch	0.1905(H) ×0.1905(V)	mm	
Pixel arrangement	RGB Vertical stripe		
Display colors	262,144	colors	
Display mode	Normally Black		
Dimensional outline	317.3±0.5(H) ×242.0±0.5(V) ×6.5(D:max)	mm	
Weight	540 (typ.)	g	
Surface treatment	AG(H45%)/AR/2H		
Back-light	Bottom edge side, 1-CCFL type		Note 1
Power consumption	P_D : 2.0 (2.2 @ sRGB Mode)	W	
	P_{BL} : 4.1	W	IL=6.5mA
	P_{total} : 6.2 (6.3 @ sRGB Mode)	W	

Note 1: CCFL (Cold Cathode Fluorescent Lamp)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

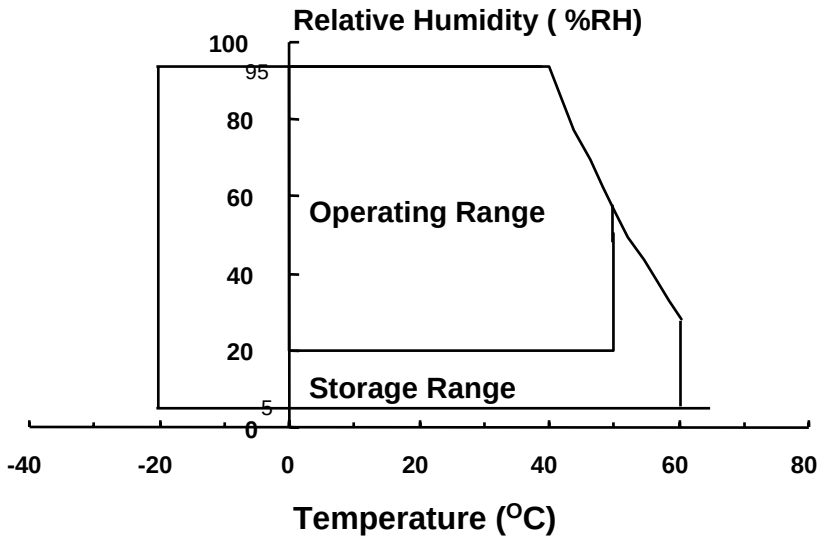
< Table 2. Absolute Maximum Ratings>

Ta=25+/−2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	
Logic Supply Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Lamp Current	I_L	3.0	7.0	mArms	(1)
Lamp frequency	F_L	45	80	kHz	
Operating Temperature	T_{OP}	0	+50	℃	(2)
Operating Humidity	RH_{OP}	-	80	%	
Storage Temperature	T_{SP}	-20	+60	℃	
Storage Humidity	RH_{ST}	-	90	%	

Note (1) Permanent damage to the device may occur if maximum values are exceeded Functional operation should be restricted to the condition described under normal operating conditions.

Note (2) Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 ^{O}C ≥ Ta)
Maximum wet - bulb temperature at 39 ^{O}C or less. (Ta > 40 ^{O}C) No condensation.



3.0 ELECTRICAL SPECIFICATIONS

3.1Electrical Specifications

< Table 3. Electrical specifications >

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Note1
Permissible Input Ripple Voltage	V_{RF}	-	-	100	mV	At V_{DD} = 3.3V
Power Supply Current	I_{DD}	-	610 (670)	850 (910)	mA	Note1 (sRGB mode)
High Level Differential Input Signal Voltage	V_{IH}	-	-	+ 100	mV	Vcm = 1.2 V typ
Low Level Differential Input Signal Voltage	V_{IL}	- 100	-	-		
Back-light Lamp Voltage	V_{BL}	600	630	770	V_{rms}	Note2
Back-light Lamp Current	I_{BL}	3.0	6.5	7.0	mA	
Back-light Lamp operating Frequency	F_L	45	60	80	KHz	One Lamp , Note3
Lamp Start Voltage		1,180	940	-	V_{rms}	At Ta = 25℃ Note 4
		1,420	1,180	-	Vrms	At Ta = 0℃ Note 4
Lamp Life		12,000	15,000	-	Hrs	At I_{BL}= 6.5 mA, Max. Note5
Power Consumption	P_D	-	2.0 (2.2)	-	W	Note1
	P_{BL}	-	4.1	-	W	Note6, I_{BL}=6.5mA
	P_{total}	-	6.2 (6.3)	-	W	Note1

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for 3.3V at 25℃.
Logic current or power in () is the value in case of sRGB
a) Typ : Window XP pattern
b) Max : Vertical sub line pattern (L255)

2. Reference value, which is measured with Samsung Electric SIC-180 Inverter.
(V_{BL} Min is value at I_{BL} Min and V_{BL} Max is value at I_{BL} Max)
3. The lamp frequency should be selected as different as possible from the horizontal synchronous frequency and its harmonics to avoid interference which may cause line flow on the display.
4. For starting the backlight unit, the output voltage of DC/AC's transformer should be larger than the minimum lamp starting voltage.
(1,180 Vrms at 25 ℃ & 1,420 Vrms at 0 ℃)
If an inverter has shutdown function it should keep its output for more than 1 second even if the lamp connector open. Otherwise the lamps may not to be turned on.
5. End of Life shall be determined by the time when any of the following is satisfied under continuous lighting at 25℃ and I_{BL} = 6.5[mA] Max Only.
• Intensity drops to 50% of the Initial Value.
6. Calculated value for reference ($V_{BL} \times I_{BL}$)

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCONE BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of Θ and Φ equal to 0°. We refer to ΘØ=0 (=Θ3) as the 3 o'clock direction (the "right"), ΘØ=90 (= Θ12) as the 12 o'clock direction ("upward"), ΘØ=180 (= Θ9) as the 9 o'clock direction ("left") and ΘØ=270(= Θ6) as the 6 o'clock direction ("bottom"). While scanning Θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement... VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2.1 Optical Specifications

<Table 4. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	85	89	-	Deg.	
		Θ_9		85	89	-	Deg.	Note 1
	Vertical	Θ_{12}		85	89	-	Deg.	
		Θ_6		85	89	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	350	500	-		Note 2
Center Luminance of White	1 Point	Y_w	Θ = 0° IBL = 6.5mA	170	200	-	cd/m^2	
White Luminance uniformity	5 Points	ΔY5		80	85	-	%	
	13 Points	ΔY13		50	60	-	%	
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343		Note 3
		W_y		0. 299	0.329	0.359		
Reproduction of Color	Red	R_x		0.545	0.575	0.605		
		R_y		0.304	0.334	0.364		
	Green	G_x		0.274	0.304	0.334		
		G_y		0.516	0.546	0.576		
	Blue	B_x		0.118	0.148	0.178		
		B_y		0.105	0.135	0.165		
Color Reproduction				-	45	-	%	
Response Time	Rise	T_r	Ta= 25° C Θ = 0°	-	20	30	ms	
	Decay	T_d		-	20	30		
Cross Talk		CT	Θ = 0°	-	-	2.0	%	

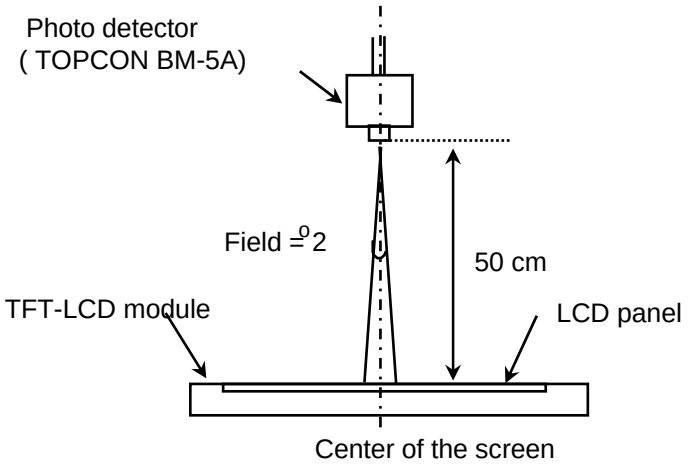
Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE1 shown in Appendix).

2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state .
(see FIGURE1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically as CR = Luminance when displaying a white raster / Luminance when displaying a black raster.

3. The color chromaticity coordinates specified in Table 4. shall be calculated from the spectral data measured with all pixels first in red, green, blue, and white. Measurements shall be made at the center of the panel.

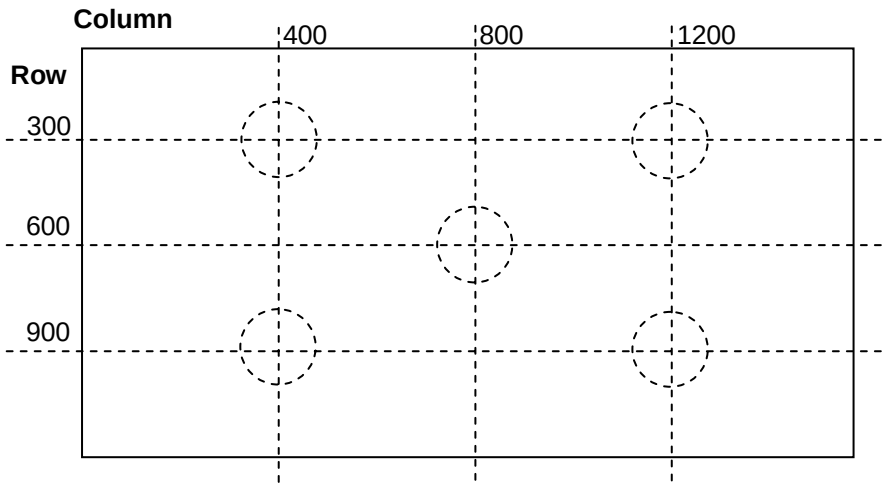
4.3 Optical measurements

Figure 1. Measurement Set Up



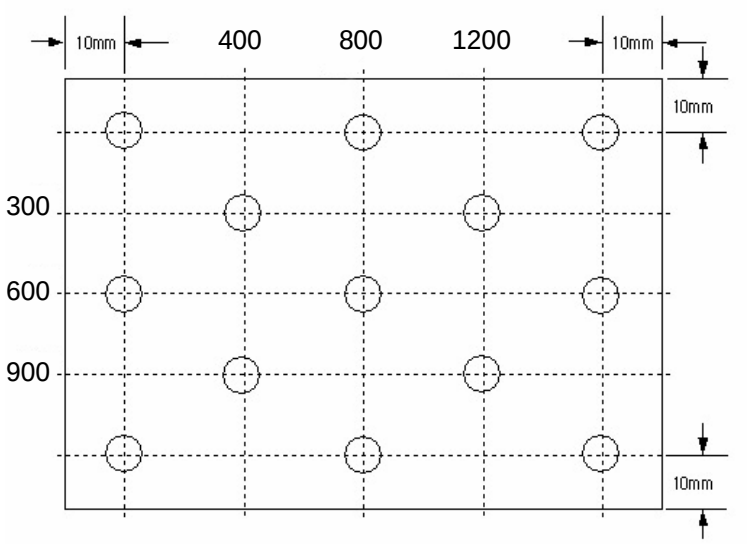
Optical characteristics measurement setup

Figure 2. White Luminance and Uniformity Measurement Locations



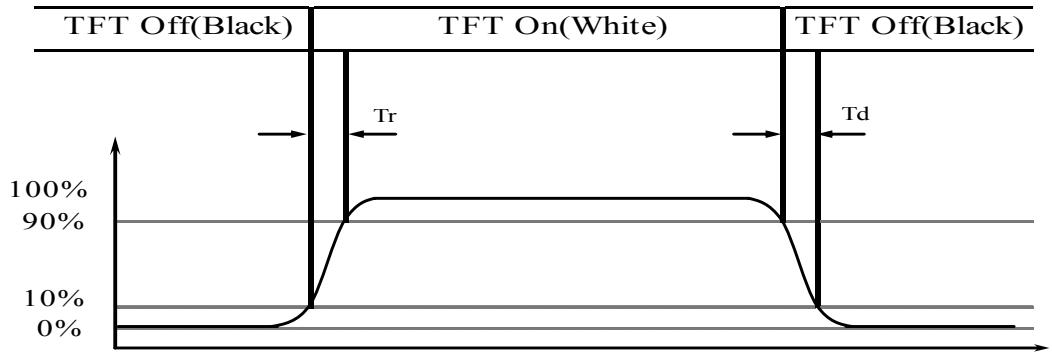
Center Luminance of white is defined as luminance values of center 1 point. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

Figure 3. Uniformity Measurement Locations (13 points)



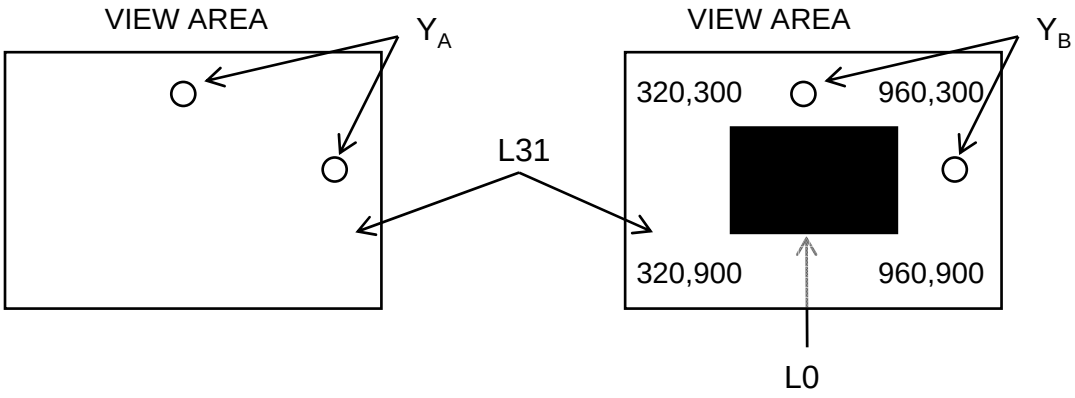
The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see FIGURE 2) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see FIGURE 3).

Figure 4. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 4 (shown in Appendix) by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr and 90% to 10% is Td.

Figure 5. Cross Modulation Test Description



Test point of Y_A , Y_B : Horizontal - 1400, 600
Vertical - 800, 150

$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)
Y_B = Subsequent luminance of measured area (cd/m^2)
The location measured will be exactly the same in both patterns

Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark (Refer to FIGURE 5).

5.0 INTERFACE CONNECTION.

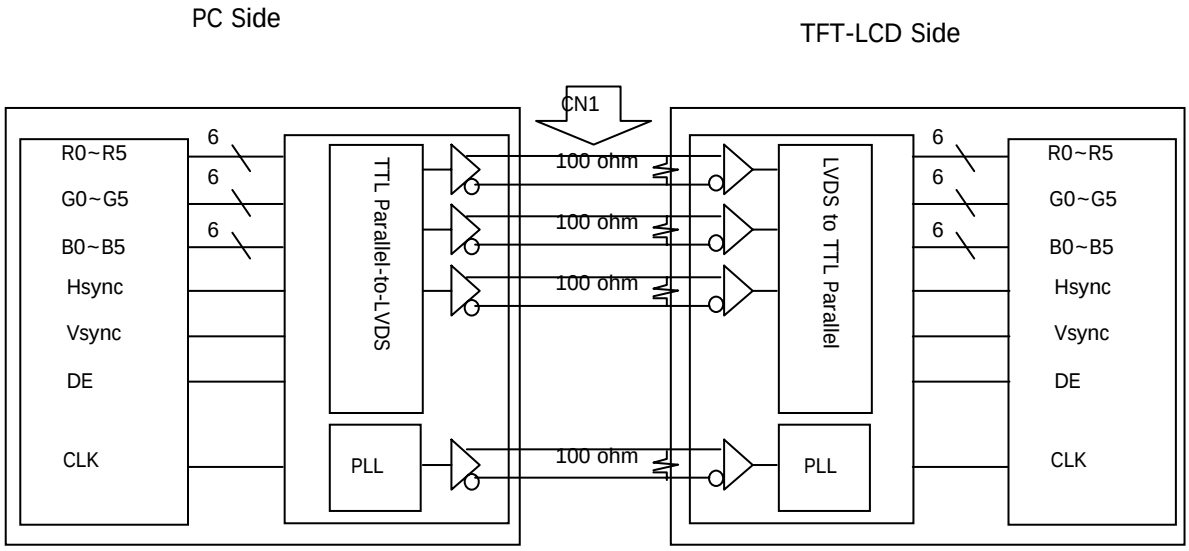
5.1 Electrical Interface Connection

The electronics interface connector is a model FI-XB30S-HFxx manufactured by JAE or equivalent. The mating connector part number is FI-X30H or FI-X30M equivalent. The connector interface pin assignments are listed in Table 5.

<Table 5. Pin Assignments for the Interface Connector>

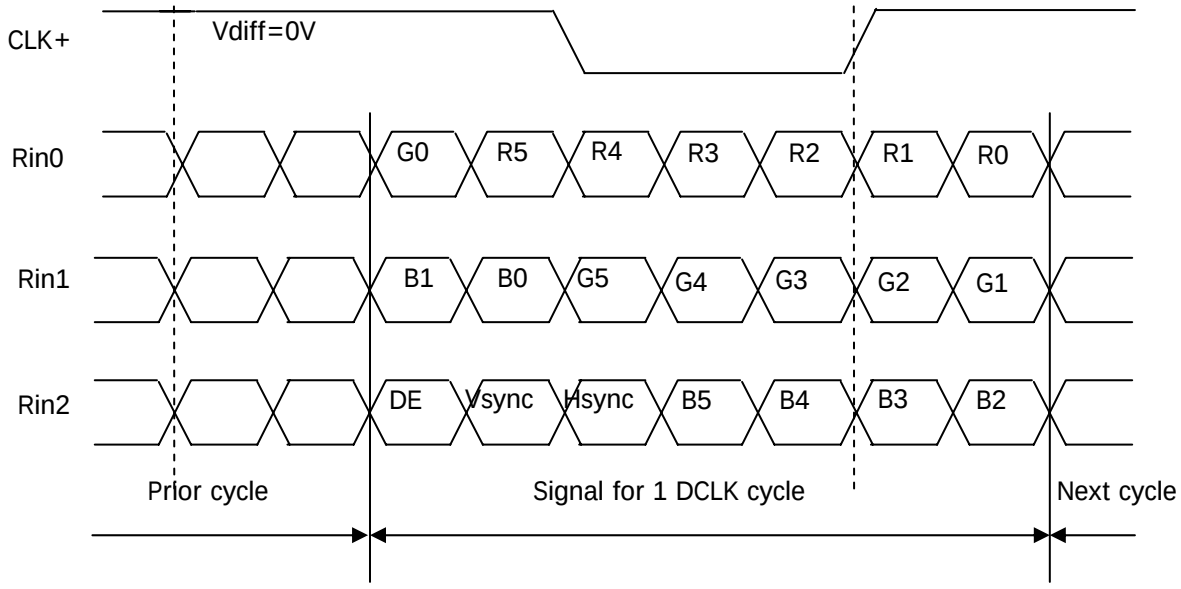
Terminal	Symbol	Functions
1	GND	GND
2	VDD	Power Supply : +3.3V (typical)
3	VDD	Power Supply : +3.3V (typical)
4	V_{EDID}	Reserved (for V_{EDID})
5	NC	Reserved (for Supplier test point)
6	CLK_{EDID}	Reserved (for Ckl_{EDID})
7	$DATA_{EDID}$-	Reserved (for $DATA_{EDID}$)
8	O_RIN0-	-LVDS differential data input (R0~R5,G0) (Odd pixel)
9	O_RIN0+	+LVDS differential data input (R0~R5,G0) (Odd pixel)
10	VSS	GND
11	O_RIN1-	-LVDS differential data input (G1~G5,B0,B1) (Odd pixel)
12	O_RIN1+	+LVDS differential data input (G1~G5,B0,B1) (Odd pixel)
13	VSS	GND
14	O_RIN2-	-LVDS differential data input (B2~B5,HS,VS,DE) (Odd pixel)
15	O_RIN2+	+LVDS differential data input (B2~B5,HS,VS,DE) (Odd pixel)
16	VSS	GND
17	O_CLKIN-	-LVDS differential Clock input (Odd pixel)
18	O_CLKIN+	+LVDS differential Clock input (Odd pixel)
19	VSS	GND
20	E_RIN0-	-LVDS differential data input (R0~R5,G0) (Even pixel)
21	E_RIN0+	+LVDS differential data input (R0~R5,G0) (Even pixel)
22	VSS	GND
23	E_RIN1-	-LVDS differential data input (G1~G5,B0,B1) (Even pixel)
24	E_RIN1+	+LVDS differential data input (G1~G5,B0,B1) (Even pixel)
25	VSS	GND
26	E_RIN2-	-LVDS differential data input (B2~B5,HS,VS,DE) (Even pixel)
27	E_RIN2+	+LVDS differential data input (B2~B5,HS,VS,DE) (Even pixel)
28	VSS	GND
29	E_CLKIN-	-LVDS differential Clock input (Even pixel)
30	E_CLKIN+	+LVDS differential Clock input (Even pixel)

5-2. LVDS Interface



Note. Transmitter : Thine THC63LVDM63A or equivalent. Transmitter is not contained in Module.

5.3.LVDS Input signal



Note. Pin connection in case of using Thine THC63LVDM63A

<Table 6. Pin connection in case of using Thine THC63LVDM63A>

Input signal	Transmitter	Input signal	Transmitter
DCLK	CLK IN(26)	G4	TB3(10)
R0	TA0(44)	G5	TB4(12)
R1	TA1(45)	B0	TB5(13)
R2	TA2(47)	B1	TB6(15)
R3	TA3(48)	B2	TC0(16)
R4	TA4(1)	B3	TC1(18)
R5	TA5(3)	B4	TC2(19)
G0	TA6(4)	B5	TC3(20)
G1	TB0(6)	Hsync	TC4(22)
G2	TB1(7)	Vsync	TC5(23)
G3	TB2(9)	DE	TC6(25)

5.4. I2C Interface for EDID & CMF

The I2C Interface is used for EDID function of SPWG and color management function.

<Table 7. EDID & CMF Electrical Interface>

Address No.	Symbol	Function	IC ref.
000	EDID	EEPROM IC of EDID for Panel Information	IC1
100	CMF	EEPROM IC of EDID for Color management	IC2

5.5. I2C Host Interface Command

The parameters of CMF can be changed through the I2C line.
The commands sets of the I2C control is shown in the following table.

<Table 8. The command sets of the I2C control>

Operation	Mode CMD [7:0]	Command
Write	0000 0010	Basic Resister Write
	0000 0110	All Resister Write
Save and Reboot	0000 1010	Resister Save
	0000 1100	All Data Save
	0000 1110	Reboot
Read	0000 0001	Status (MODE STS) Read
	0000 0011	Basic Resister Read
	0000 0111	All Resister Read
Reset	0000 1111	Software Reset
Reserved	Other Patterns	Reserved

The status of CMF is returned in STATUS stage. High 4 bits of MODE_STS express the status, and low 4 bits are uncertain value.

I) In DATA stage, serial data is sent and received according to the operation mode selected in MODE stage. The restart and forced termination in the middle of transmission are processed as an access error, and the error is notified by status bit.

Mode Sts [7:0]	Status
0000 xxxx	Normal Operation
0001 xxxx	Basic Resister Access Error
0010 xxxx	Reserved
0011 xxxx	Resister Access Error
0100 xxxx	Reserved
0101 xxxx	Saving data
0110 xxxx	Booting data
0111 xxxx	Check sum Error
1000 xxxx	EEPROM Access Error
Other Patterns	Reserved

5.6.Back-light Interface

The Back-light interface connector is a model BHSR-02VS-1 manufactured by JST or equivalent. And the mating connector part number is SM02B-BHSS-1-TB (JST) or equivalent. The connector interface pin assignments are listed in Table 8.

<Table 8. Back-light Electrical Interface>

Terminal No.	Symbol	Function	Color
1	VL	CCFL Power Supply (High Voltage)	Pink
2	GL	CCFL Power Supply (GND Side)	Black

6.0. SIGNAL TIMING SPECIFICATION

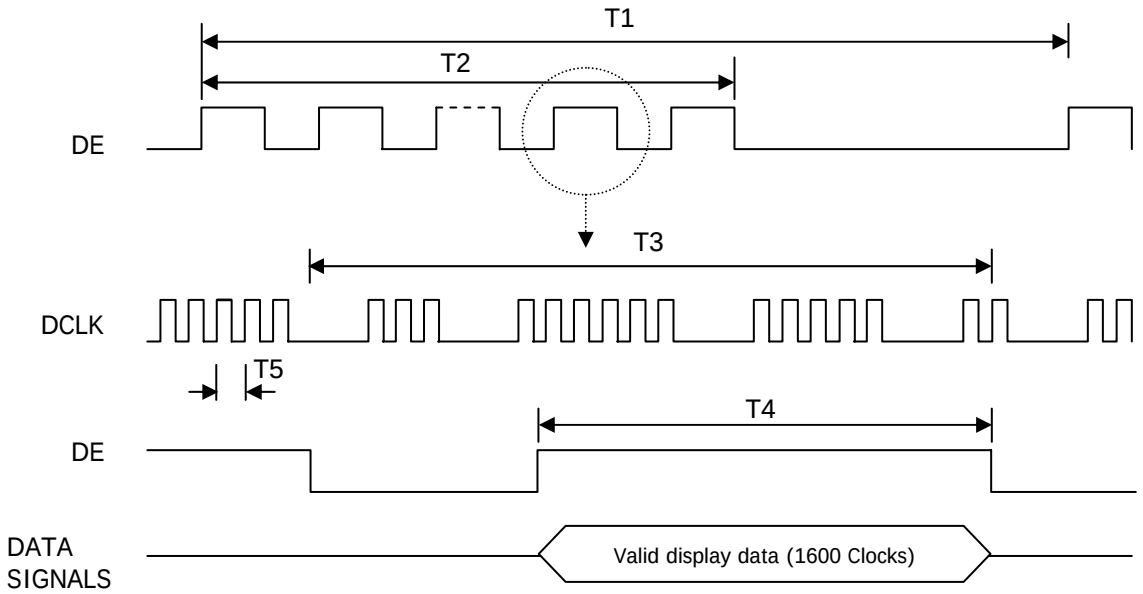
The specification of the signal timing parameters are listed in Table 9.

<Table 9. Signal Timing Specification.>

Item	Symbols	Min	Typ	Max	Unit
Frame Period	T1	28.57	16.67	15.87	ms
Vertical Display Period	T2	-	16	-	ms
One line Scanning Period	T3	-	13.3	-	us
Horizontal Display Period	T4	-	9.9	-	us
Clock Frequency	1/T5	47.25	81	85	MHz

7.0 SIGNAL TIMING WAVEFORMS

7.1 Timing wave forms of interface signal

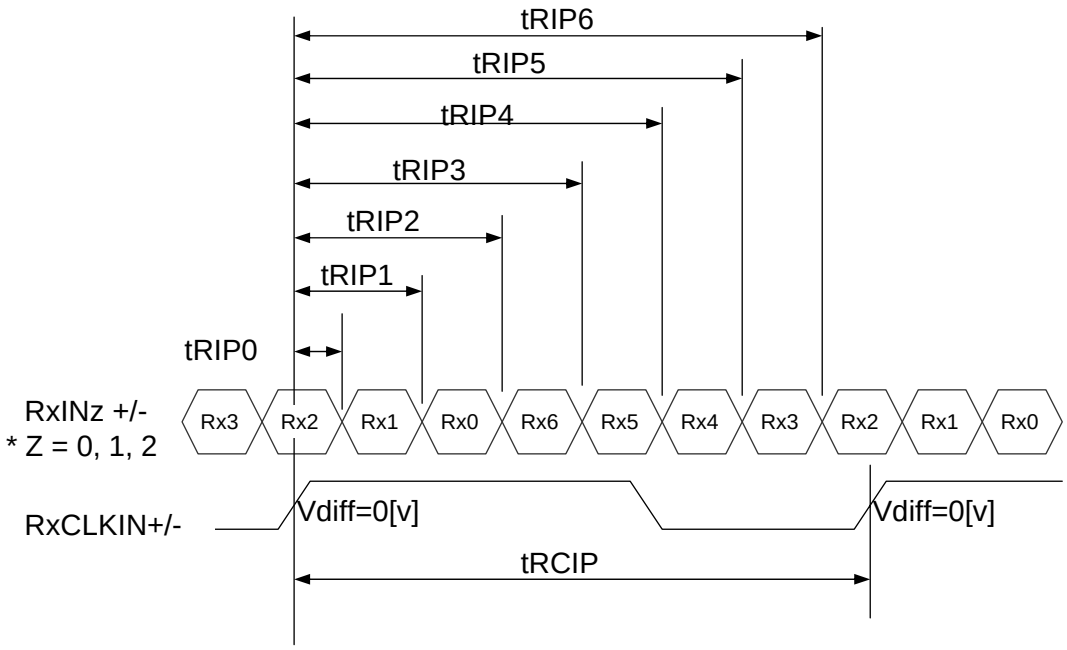


7.2 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is listed in Table 10.

<Table 10. LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
PLL Set	tRPLL	-	-	10.0	msec	
CLKIN Period	tRCIP	11.77	12.35	21.16	nsec	
Input Data 0	tRIP0	-0.4	0.0	+0.4	nsec	
Input Data 1	tRIP1	tRICP/7-0.4	tRICP/7	tRICP/7+0.4	nsec	
Input Data 2	tRIP2	2 ×tRICP/7-0.4	2 ×tRICP/7	2 ×tRICP/7+0.4	nsec	
Input Data 3	tRIP3	3 ×tRICP/7-0.4	3 ×tRICP/7	3 ×tRICP/7+0.4	nsec	
Input Data 4	tRIP4	4 ×tRICP/7-0.4	4 ×tRICP/7	4 ×tRICP/7+0.4	nsec	
Input Data 5	tRIP5	5 ×tRICP/7-0.4	5 ×tRICP/7	5 ×tRICP/7+0.4	nsec	
Input Data 6	tRIP6	6 ×tRICP/7-0.4	6 ×tRICP/7	6 ×tRICP/7+0.4	nsec	



8.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

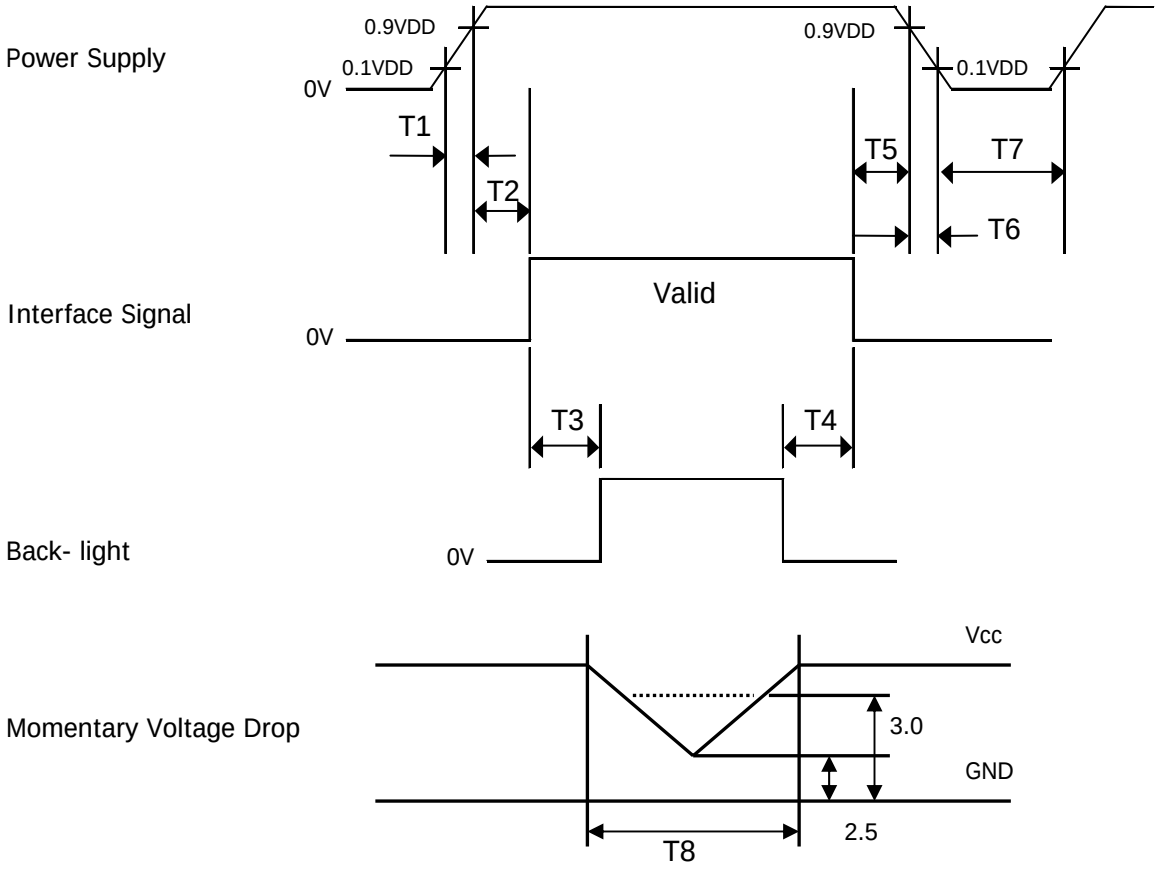
Each color is displayed in sixty-four gray scales from a 6 bit data signal input. A total of 262,144 colors are derived from the resultant 18 bit data. Table 11. shows the input signals, basic display colors and gray scale for each color.

<Table 11. Input signals, Basic display colors and Gray scale for each color.>

	Colors & Gray scale	Data signal																	
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
	▽	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



- T1 ≤ 10 ms
- 0 ≤ T2 ≤ 50 ms
- 200ms ≤ T3
- 0 ≤ T4
- 0 ≤ T5
- 0 ≤ T6 ≤ 10ms
- 150ms ≤ T7
- T8 ≤ 10 ms (When 2.5V ≤ Vcc < 3.0 V)

Notes : 1. When the power supply VDD is 0V, Keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
Back Light must be turn on after power for logic and interface signal are valid.
3. Display operated normally when the momentary voltage drop happened.

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

FIGURE 6 (located in Appendix) shows mechanical outlines for the model HV150UX1-101. Other parameters are shown in Table 12.

<Table 12. Dimensional Parameters>

Parameter	Specification	Unit
Dimensional outline	317.3±0.5 ×242.0±0.5×6.5 max	mm
Weight	540 (typ.)	gram
Back-light	Connector : BHSR-02VS-1	
	CCFL, Horizontal & Bottom side lamp type	
	Length : 40.0±5.0	mm

10.2 Mounting

See FIGURE 6 & 7. (shown in Appendix)

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an anti-glare coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABLITY TEST

The Reliability test items and its conditions are shown in below.

<Table 13. Reliability test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 1000hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = 0 ℃, 1000hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle
7	Vibration test (non-operating)	(1.5G),10~300Hz for X,Y,Z axis 30 minutes for each axis
8	Shock test (non-operating)	220G,2msec,half sine (6 times)
9	Electro-static discharge test (non-operating)	Air : 150 pF, 330Ω, 15 KV Contact : 150 pF, 330Ω, 8 KV

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product label

1	2	3	4	5	6				7					
X	X	X	X	X	X	X	X	-	X	X	X	X	X	X

Type designation

No 1. Control Number

No 2. Rank / Grade

No 3. Company (H:BOE HYDIS, O:BOE OT)

No 4. Year (5 : 2005, 6 : 2006, …)

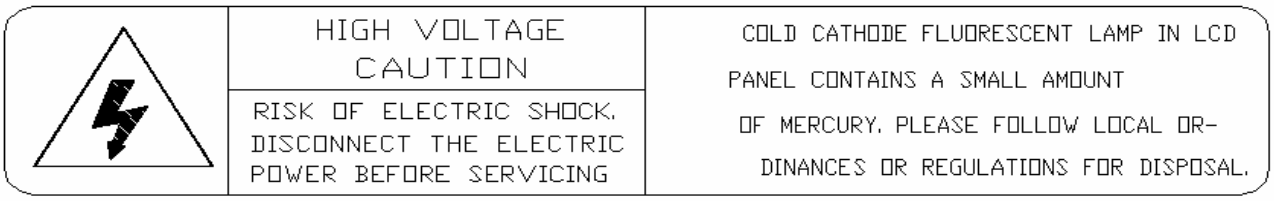
No 5. Month (1, 2, 3,…, 9, X, Y, Z)

No 6. Product Identification

No 7. Serial Number

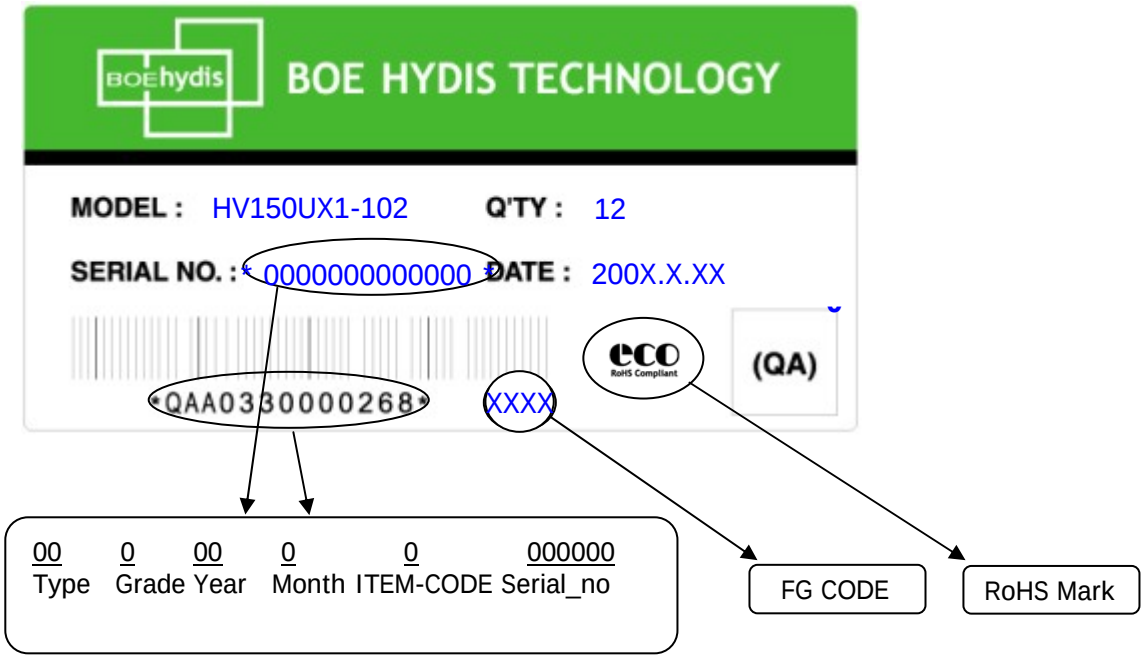
No 8. Fujitsu Label Code

(2) High voltage caution label



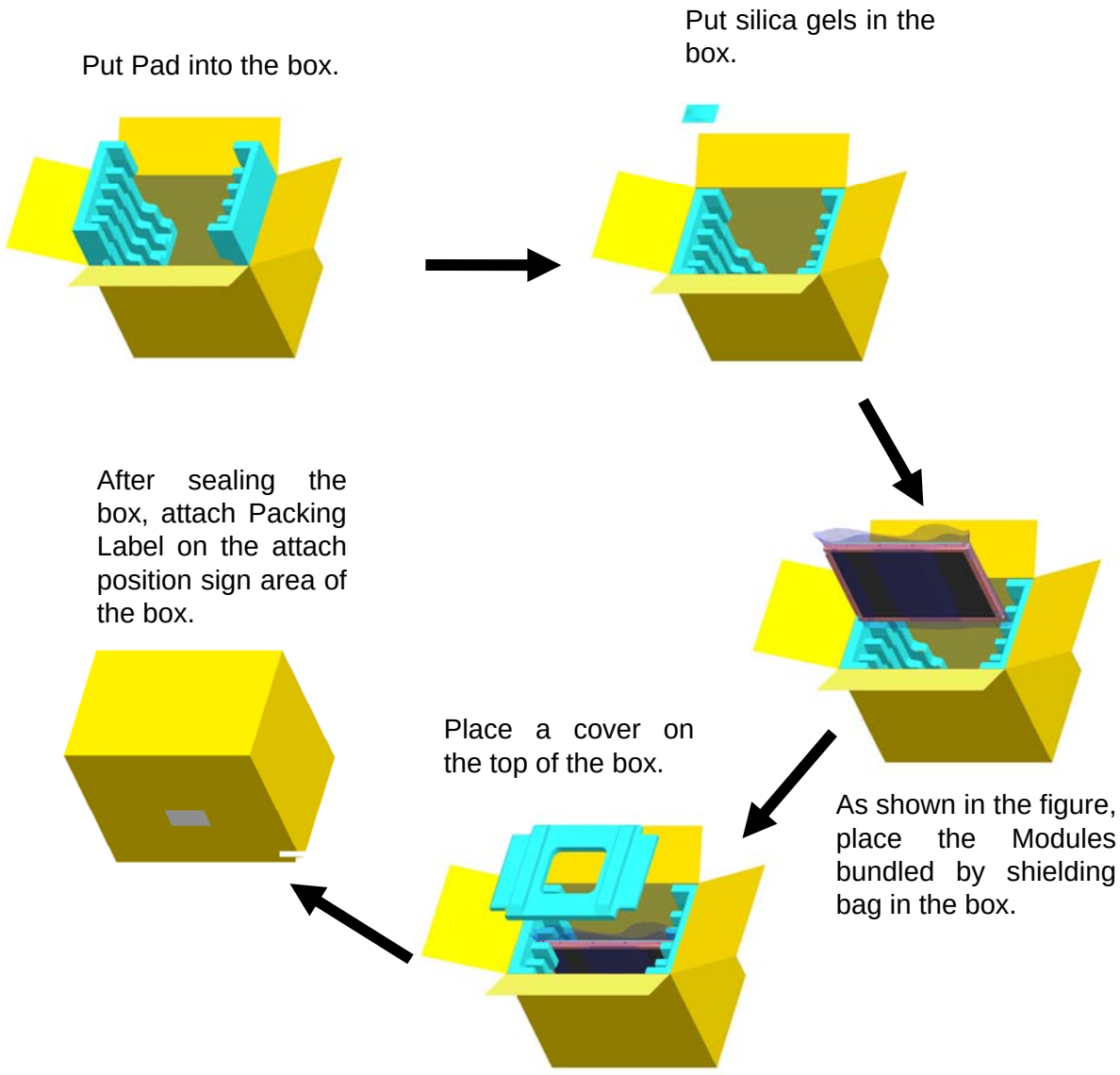
(3) Box label

Label Size: 108 mm (L) × 56 mm (W)
Contents
Model: HV150UX1-101
Q`ty: Module Q`ty in one box
Serial No.: Box Serial No. See next figure for detail description.
Date: Packing Date
FG Code: FG Code of Product



14.0 PACKING INFORMATION

14.1 Packing order



14.2 Notes

- Box Dimension: 333mm(W)X 333mm(D)X 435(H)
- Package Quantity in one Box: 10pcs

15.0 EDID data table

EDID chip is 24LC024 (Microchip) or equivalent .

Add (Hex)	Field name & comments	Data	Add (Hex)	Field name & Comments	Data
00	Header	00	1B	Red X : 0.569 (10010001)	91
01	Header	FF	1C	Red Y : 0.332 (01010100)	54
02	Header	FF	1D	Green X : 0.312 (01001111)	4F
03	Header	FF	1E	Green Y : 0.544 (100001011)	8B
04	Header	FF	1F	Blue X : 0.149 (00100110)	26
05	Header	FF	20	Blue Y : 0.132 (00100001)	21
06	Header	FF	21	White X : 0.313 (01010000)	50
07	Header	00	22	White Y : 0.329 (01010100)	54
08	ID System Manufacturer Name : LEN	30	23	Established timing I	21
09		AE	24	Established Timing II	08
0A	ID Product Code : UXGA FFS	46	25	Manufacturer's timings	00
0B		40	26	Standard timing ID1 (01h if not used)	81
0C	ID Serial number	00	27	Standard timing ID1 (01h if not used)	80
0D		00	28	Standard timing ID2 (01h if not used)	A9
0E		00	29	Standard timing ID2 (01h if not used)	40
0F		00	2A	Standard timing ID3 (01h if not used)	01
10	Week of manufacture	00	2B	Standard timing ID3 (01h if not used)	01
11	Year of Manufacturer : 2006	10	2C	Standard timing ID4 (01h if not used)	01
12	EDID Structure version : Ver 1.0	01	2D	Standard timing ID4 (01h if not used)	01
13	EDID Revision Number : Rev 3	03	2E	Standard timing ID5 (01h if not used)	01
14	Digital I/P, Non TMDS CRGB	80	2F	Standard timing ID5 (01h if not used)	01
15	Max H image size (cm) : 30.45 cm	1E	30	Standard timing ID6 (01h if not used)	01
16	Max V image size (cm) : 22.8375 cm	16	31	Standard timing ID6 (01h if not used)	01
17	Display Gamma : 2.2	78	32	Standard timing ID7 (01h if not used)	01
18	Active off, RGB color	EA	33	Standard timing ID7 (01h if not used)	01
19	Red/Green low bits = 10111101	BD	34	Standard timing ID8 (01h if not used)	01
1A	Blue/White low bits = 00110000	30	35	Standard timing ID8 (01h if not used)	01

Add (Hex)	Field name & comments	Data	Add (Hex)	Field name & Comments	Data
36	Detailed timing descriptor #1	48	53	Hor Sync offset, PW : pulse width	00
37	Pixel clock (MHz) / 1000 : 162 MHz	3F	54	Horizontal image size (mm):304.5 mm	30
38	Horizontal active : 1600	40	55	Vertical image size (mm):228.375 mm	E4
39	Horizontal blanking : 560	30	56	Horizontal & Vertical image size : 0	10
3A	Horizontal active : blanking	62	57	Horizontal border : 0	00
3B	Vertical active : 1200	B0	58	Vertical border : 0	00
3C	Vertical blanking : 50	32	59	Flags : 0	19
3D	Vertical active : blanking	40	5A	Detailed timing descriptor #3	00
3E	Horizontal Sync offset : 64	40	5B	ASCII data string Tag (Supplier Name)	00
3F	Horizontal Sync pulse width : 192	C0	5C		00
40	Ver sync offset : pulse width = 1 : 3	13	5D		0F
41	Hor Sync offset, PW : pulse width	00	5E		00
42	Horizontal image size (mm):304.5 mm	30	5F	Horizontal active pixel / 8 - 31	A9
43	Vertical image size (mm):228.375 mm	E4	60	Image Aspect Rate (4:3)	43
44	Horizontal & Vertical image size : 0	10	61	Low refresh rate #1 (50 Hz)	32
45	Horizontal border : 0	00	62	Horizontal active pixel / 8 – 31	A9
46	Vertical border : 0	00	63	Image aspect rate (4:3)	43
47	Flags : 0	19	64	Low refresh rate #2 (40 Hz)	28
48	Detailed timing descriptor #2	BC	65	Brightness (1/10 nit)	14
49	Pixel clock (MHz) / 1000 : 135 MHz	34	66	Feature flag (FFS mode)	06
4A	Horizontal active : 1600	40	67	Reserved 00H	00
4B	Horizontal blanking : 560	30	68	EISA manufacturer code (3CharacterID)	09
4C	Horizontal active : blanking	62	69	Compressed ASCII	E5
4D	Vertical active : 1200	B0	6A	Panel supplier reserved –product code	00
4E	Vertical blanking : 50	32	6B	(Hex, LSB first)	00
4F	Vertical active : blanking	40	6C	Detailed timing descriptor #4	00
50	Horizontal Sync offset : 64	40	6D	ASCII data string Tag (Supplier P/N)	00
51	Horizontal Sync pulse width : 192	C0	6E		00
52	Ver sync offset : pulse width = 1 : 3	13	6F		FE

Add (Hex)	Field name & comments	Data	Add (Hex)	Field name & Comments	Data
70	ASCII data string Tag (Supplier P/N)	00	78	1	31
71	H	48	79	-	2D
72	V	56	7A	1	31
73	1	31	7B	0	30
74	5	35	7C	2	32
75	0	30	7D	SP (space)	0A
76	U	55	7E	Extension Flag	00
77	X	58	7F	Checksum	A0

15.2 EDID chip Timing specification

Parameter	Symbol	STD MODE		High Speed Mode		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock Frequency	FCLK	-	100	-	400	KHz	-
Clock high time	THIGH	4000	-	600	-	ns	-
Clock low time	TLOW	4700	-	1300	-	ns	-
SDA and SCL rise time	TR	-	1000	-	300	ns	note 1
SDA and SCL fall time	TF	-	300	-	300	ns	note 1
Start condition hold time	THD:STA	4000	-	600	-	ns	
Start condition setup time	TSU:STA	4700	-	600	-	ns	
Data input hold time	THD:DAT	0	-	0	-	ns	note 2
Data input setup time	TSU:DAT	250	-	100	-	ns	
Stop condition setup time	TSU:STO	4000	-	600	-	ns	
Output valid from clock	TAA	-	3500	-	900	ns	note 3
Bus free time	TBUF	4700	-	1300	-	ns	
Output fall time from VIH minimum to VIL maximum	TOF	-	250	20 + 0.1Ca	250	ns	note 1
Input filter spike suppression (SDA and SCL pins)	TSP	-	50	-	50	ns	note 3
Write-cycle time	TWC	-	10	-	10	ms	
Endurance		1M	-	1M	-		

15.3 CMF chip Timing specification

Parameter	Symbol	STD MODE		High Speed Mode		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock Frequency	FCLK	-	100	-	400	KHz	-
Clock high time	THIGH	4000	-	600	-	ns	-
Clock low time	TLOW	4700	-	1300	-	ns	-
SDA and SCL rise time	TR	-	1000	-	300	ns	note 1
SDA and SCL fall time	TF	-	300	-	300	ns	note 1
Start condition hold time	THD:STA	4000	-	600	-	ns	
Start condition setup time	TSU:STA	4700	-	600	-	ns	
Data input hold time	THD:DAT	0	-	0	-	ns	note 2
Data input setup time	TSU:DAT	250	-	100	-	ns	
Stop condition setup time	TSU:STO	4000	-	600	-	ns	
Output valid from clock	TAA	-	3500	-	900	ns	note 3
Bus free time	TBUF	4700	-	1300	-	ns	
Output fall time from VIH minimum to VIL maximum	TOF	-	250	20 + 0.1Ca	250	ns	note 1
Input filter spike suppression (SDA and SCL pins)	TSP	-	50	-	50	ns	note 3
Write-cycle time	TWC	-	10	-	10	ms	
Endurance		1M	-	1M	-		

Figure 6. TFT-LCD Module Outline Dimension (Front View)

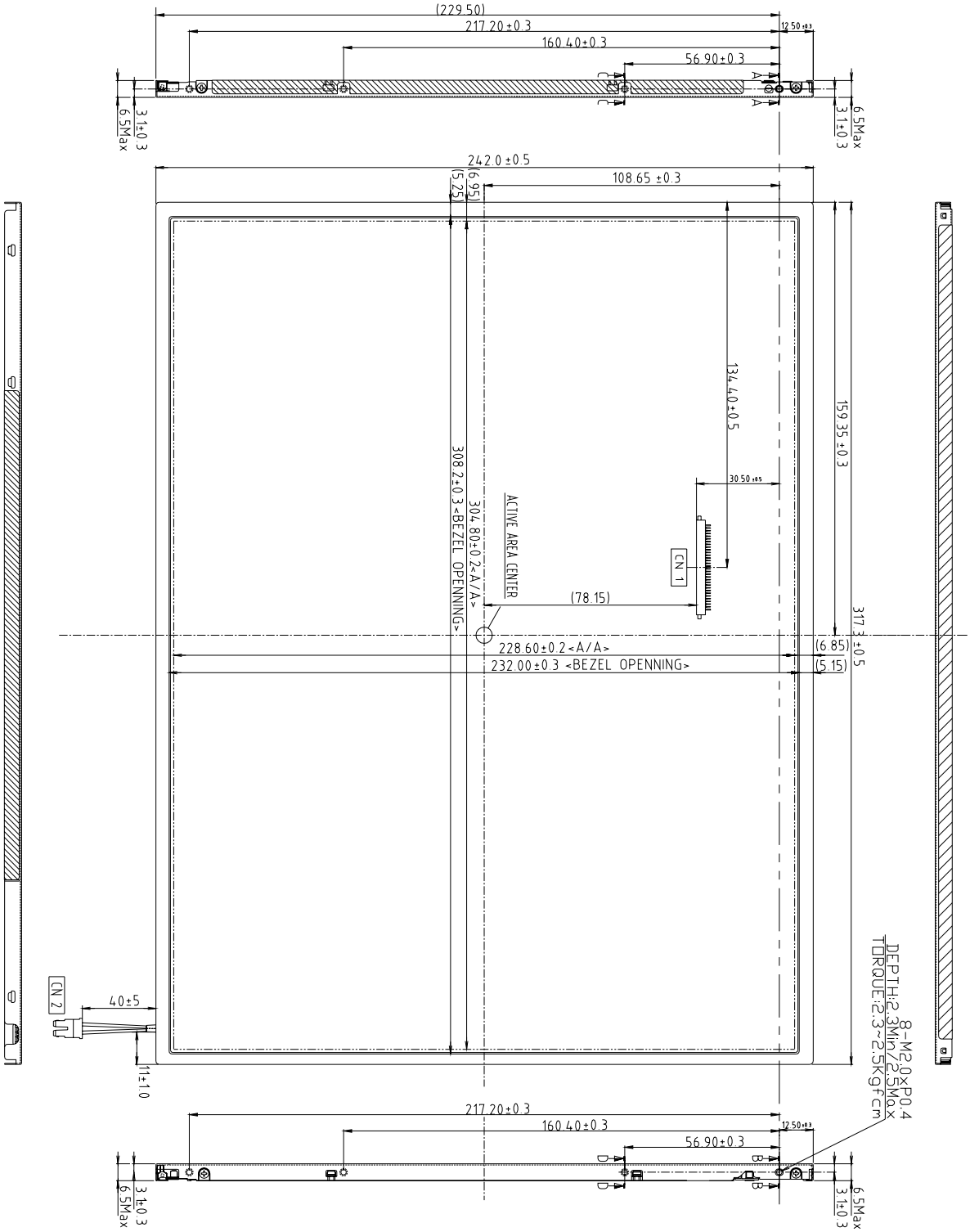


Figure 7. TFT-LCD Module Outline Dimensions (Rear view)