Engineering Specification

Type 21.3 QSXGA Monochrome TFT/LCD Module
Model Name:IAQS80F

Document Control Number : OEM I-980F-01

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Sales Support
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ii Record of Revision

Date	Document Revision	Page	Summary
October 8,2002	OEM I-980F-01	All	First Edition for customer. Based on Internal Spec. as of August 14,2002.

1.0 Handling Precautions

- If any signal or power line deviates from the power on/off sequence, it may cause shortening the life of the LCD module and/or damage the electrical components. Also, hot plug-in operation may cause the similar damages as above.
- The LCD panel and the CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may break or crack if dropped on a hard surface. Handling with care is necessary.
- The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be applied to exemption conditions of the flammability requirements (4.4.3.3, EN60950 or UL1950) in an end product.
- Please handle with care when mounted in the system cover. Mechanical damage for the lamp cable / lamp connector may cause safety problems.
- After installation of the TFT Module into an enclosure (Monitor frame, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/ twisting forces are applied to the TFT Module from out side. Otherwise the TFT Module may be damaged.
- Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- Also, when removing a protection sheet from the module surface, please take some actions against static electricity, like earth band, ionic shower, etc.
- Since front polarizer is easily damaged, pay attention not to scratch it.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- Do not open nor modify the Module Assembly.
- Prevent continuous 10 hours or over same pattern displaying, to avoid image sticking.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporationg this product.

2.0 General Description

This specification applies to the Type 21.3 Monochrome TFT/LCD Module 'IAQS80F'.
This module is designed for a module with neutral white (0.294, 0.309) and DICOM gamma curve.
The screen format and electrical interface are intended to support the QSXGA (2560(H) x 2048(V)) screen with sensor area (176(H) x 16(V)) at the top of the screen. Supported gray scales are native 8bit level (8-bit per Tri-subpixels data driver). All input signals are LVDS (Low Voltage Differential Signaling) interface compatible. This module contains an inverter card for backlight.

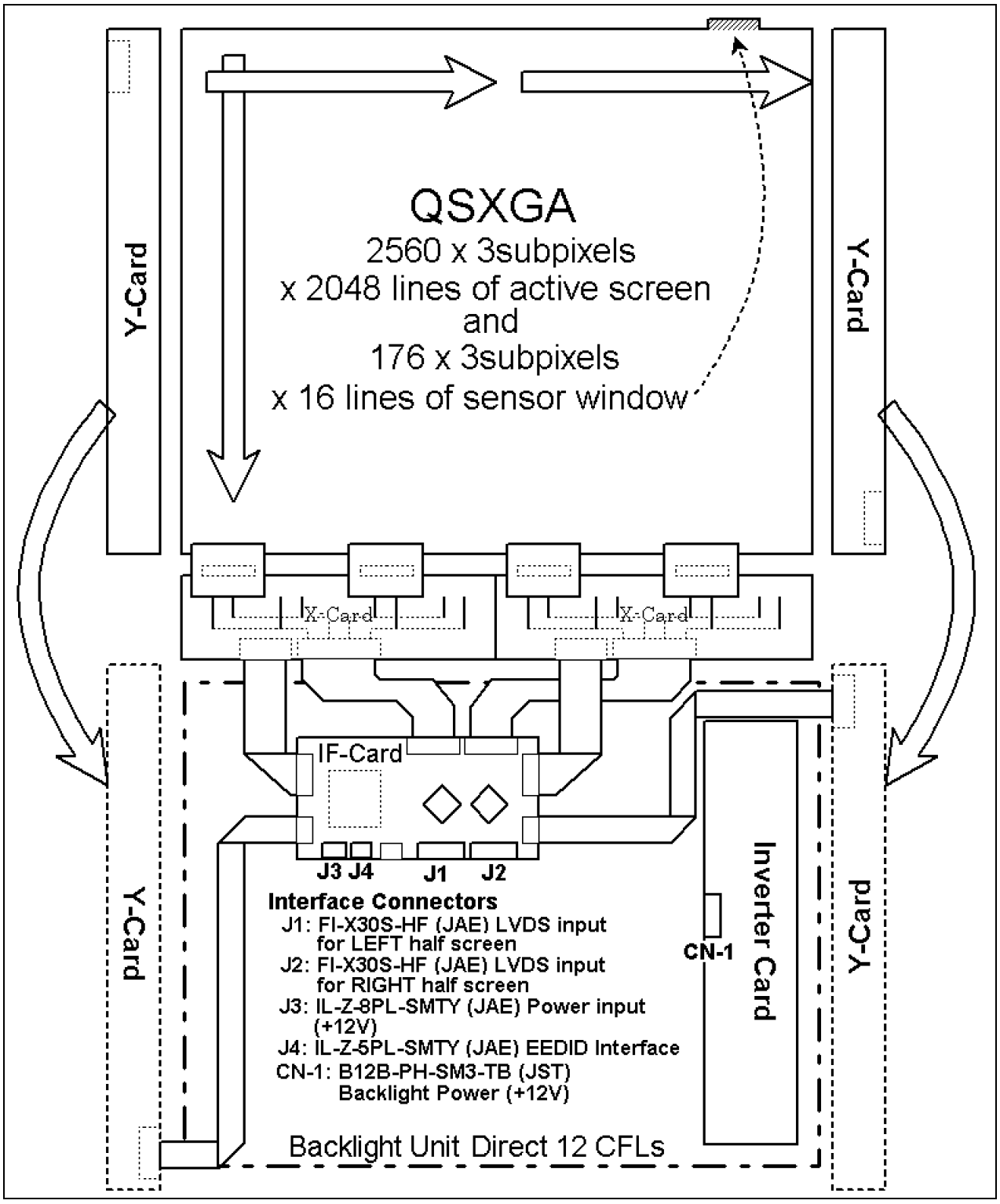
2.1 Characteristics

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [cm]	54.09
Pixels	2560(H) x 2048(V)
Sensor Window	176(H) x 16(V) Top/Right at landscape
Active Area [mm]	422.4(H) x 337.92(V)
Sensor Window [mm]	29.04(H) x 2.64(V)
Pixel Pitch [mm]	0.165 x 0.165
Pixel Arrangement	Tri-subpixels per one Pixel, Vertical Stripe
Weight [grams]	2,970 Typ.
Physical Size [mm]	459.8(W) x 375.3(H) x 48.5(D) Typ. (w/ inverter)
Display Mode	Dual Domain IPS, Normally Black
Supported Grayscale	8-bits per each subpixel
White Luminance [cd/m^2]	750 Typ., 600 Min.
Contrast Ratio	600:1 Typ. (In the Dark room)
Optical Rise Time/Fall Time [msec]	25 Typ. / 25 Typ.
Input Voltage [V]	+12 +5/-8% (Logic, Inverter)
Power Consumption [W]	Logic 8.1 Typ., Inverter 44 Typ.
Electrical Interface	LVDS (5pairs) x4 (Rightx2, Leftx2)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 **(Note)** -20 to +60

Note : Max. Operating Temperature 50 deg.C in the spec means the temperature measured at the point of the front surface of the LCD glass cell.

2.2 Functional Block Diagram

The following diagram shows the functional block diagram for the Type 21.3 Monochrome TFT/LCD Module.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows;

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VIN	-0.3	+17.6	V	
Backlight Voltage	VBL	-0.3	+17.6	V	
Brightness control	VDIM	-0.3	+5.3	V	
Backlight on signal	BLON	-1.0	+5.3	V	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Relative Humidity	HOP	8	80	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Relative Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	**(Note 2)**
Shock			50 11	G ms	Half sine wave **(Note 2)**

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.
Max. Operating Temperature 50 deg. C in the spec means the temperature measured for the point of the front surface of the LCD glass cell.

Note 2 : Vibration Specification
- Sine Vibration:10-200-10Hz, 1.5G, 30 min, X, Y, Z Axis, Each One Time.

Shock Specification
- Half sine wave:50G 11msec. -X+/-, -Y+/-, -Z+/- (Total 6 directions), Each one time Shock.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≧10 (Left) Vertical (Upper) K≧10 (Lower)	85 85 85 85	- - - -
Contrast ratio		600	400 Min.
Response Time	Rising	25	50 Max.
(ms)	Falling	25	50 Max.
White Balance	White x	0.294	±0.030
	White y	0.309	±0.030
White Luminance (cd/m^2)		750 Typ. (Center)	600 Min.

5.0 Physical Interface

Physical interface is described in accordance with the connectors on the LCD module.
These connectors are capable of accommodating the following signals and will be the following components or IDT approved types.

5.1 Signal Connectors

All video signals are provided through the LVDS cable from Monitor Card. These connectors are the input connector of video signals. The LVDS signals, which are provided from monitor card, are described on the following table.

Signal Connectors

Connector	Function	Type	Manufacturer	Mating Connector
J1	LVDS Input for Left Half Screen	FI-X30S-HF	JAE	FI-X30H (for Harness) FI-X30M (for FPC)
J2	LVDS Input for Right Half Screen	FI-X30S-HF	JAE	FI-X30H (for Harness) FI-X30M (for FPC)
J3	DC Input	IL-Z-8PL-SMTY	JAE	IL-Z-8S-S125C3
J4	EEDID Interface	IL-Z-5PL-SMTY	JAE	IL-Z-5S-S125C3

LVDS Signals Input Pin Assignment (J1 and J2)

Pin #	Signal Name	
	J1	J2
1	RAEIN0-	RBEIN0-
2	RAEIN0+	RBEIN0+
3	GND	GND
4	RAEIN1-	RBEIN1-
5	RAEIN1+	RBEIN1+
6	GND	GND
7	RAEIN2-	RBEIN2-
8	RAEIN2+	RBEIN2+
9	GND	GND
10	RAECLKIN-	RBECLKIN-
11	RAECLKIN+	RBECLKIN+
12	GND	GND
13	RAEIN3-	RBEIN3-
14	RAEIN3+	RBEIN3+
15	GND	GND

Pin #	Signal Name	
	J1	J2
16	GND	GND
17	RAOIN0-	RBOIN0-
18	RAOIN0+	RBOIN0+
19	GND	GND
20	RAOIN1-	RBOIN1-
21	RAOIN1+	RBOIN1+
22	GND	GND
23	RAOIN2-	RBOIN2-
24	RAOIN2+	RBOIN2+
25	GND	GND
26	RAOCLKIN-	RBOCLKIN-
27	RAOCLKIN+	RBOCLKIN+
28	GND	GND
29	RAOIN3-	RBOIN3-
30	RAOIN3+	RBOIN3+

Voltage levels of all input signals are LVDS compatible in those connectors, J1 and J2. Refer to "Signal Electrical Characteristics for LVDS".

Logic DC Input Pin Assignment (J3)

Pin #	Signal Name
1	Return
2	Return
3	Return
4	Return
5	Vin
6	Vin
7	Vin
8	Vin

EEDID Interface Pin Assignment (J4)

Pin #	Signal Name
1	EEDID Vcc
2	Reserved
3	SCL
4	SDA
5	GND

5.2 Back Light Connector

Backlight Connector on Inverter Card

Connector	Function	Connector Type	Manufacturer	Mating Connector
CN-1	Input for Backlight	B12B-PH-SM3-TB	JST	PHR-12

Inverter Input Connector (CN-1)

Pin #	Signal Name
1	VBL
2	VBL
3	VBL
4	VBL
5	VBL
6	GND
7	GND
8	GND
9	GND
10	GND
11	VDIM
12	BLON

5.3 Interface Signal Description

Signal Description for J1, J2

SIGNAL NAME		Description
J1	J2	
RAEIN0-	RBEIN0-	Negative LVDS differential data input (Even data, LVDS-RxE-0)
RAEIN0+	RBEIN0+	Positive LVDS differential data input (Even data, LVDS-RxE-0)
RAEIN1-	RBEIN1-	Negative LVDS differential data input (Even data, LVDS-RxE-1)
RAEIN1+	RBEIN1+	Positive LVDS differential data input (Even data, LVDS-RxE-1)
RAEIN2-	RBEIN2-	Negative LVDS differential data input (Even data, LVDS-RxE-2)
RAEIN2+	RBEIN2+	Positive LVDS differential data input (Even data, LVDS-RxE-2)
RAEIN3-	RBEIN3-	Negative LVDS differential data input (Even data, LVDS-RxE-3)
RAEIN3+	RBEIN3+	Positive LVDS differential data input (Even data, LVDS-RxE-3)
RAECLKIN-	RBECLKIN-	Negative LVDS differential clock input (Even clock, LVDS-RxE-CLK)
RAECLKIN+	RBECLKIN+	Positive LVDS differential clock input (Even clock, LVDS-RxE-CLK)
RAOIN0-	RBOIN0-	Negative LVDS differential data input (Odd data, LVDS-RxO-0)
RAOIN0+	RBOIN0+	Positive LVDS differential data input (Odd data, LVDS-RxO-0)
RAOIN1-	RBOIN1-	Negative LVDS differential data input (Odd data, LVDS-RxO-1)
RAOIN1+	RBOIN1+	Positive LVDS differential data input (Odd data, LVDS-RxO-1)
RAOIN2-	RBOIN2-	Negative LVDS differential data input (Odd data, LVDS-RxO-2)
RAOIN2+	RBOIN2+	Positive LVDS differential data input (Odd data, LVDS-RxO-2)
RAOIN3-	RBOIN3-	Negative LVDS differential data input (Odd data, LVDS-RxO-3)
RAOIN3+	RBOIN3+	Positive LVDS differential data input (Odd data, LVDS-RxO-3)
RAOCLKIN-	RBOCLKIN-	Negative LVDS differential clock input (Odd clock, LVDS-RxO-CLK)
RAOCLKIN+	RBOCLKIN+	Positive LVDS differential clock input (Odd clock, LVDS-RxO-CLK)
GND	GND	Ground

Note :

1. Input signals of odd and even clock shall be the same timing.
2. The module uses a 100-ohm resister between positive and negative data lines of each receiver input.
3. Even: First Pixel, Odd: Second Pixel
4. J1: Stripe A (Left Half), J2: Stripe B (Right Half)

Signal Description for J3

SIGNAL NAME	Description
Return	Return to Power Supply (Ground)
Vin	+12V Power Supply

Signal Description for J4

SIGNAL NAME	Description
EEDID Vcc	+3.3V Power Supply for EEDID Chip
SCL	EEDID Clock
SDA	EEDID Data
Reserved	Reserved

Backlight Power Connector Signal Description for CN-1 on Inverter Card

SIGNAL NAME	Description
VBL	Power source line. 11.0 - 12.6 V
GND	Ground line for VBL, BLON, VDIM. To connect screw hole pattern through 0 ohm resister
VDIM	Dimming control voltage input. (0 - 3V) 0V: Maximum brightness, 3V: Minimum brightness
BLON	Backlight on and off control signal. High (active): Backlight on, Low (inactive): Backlight off

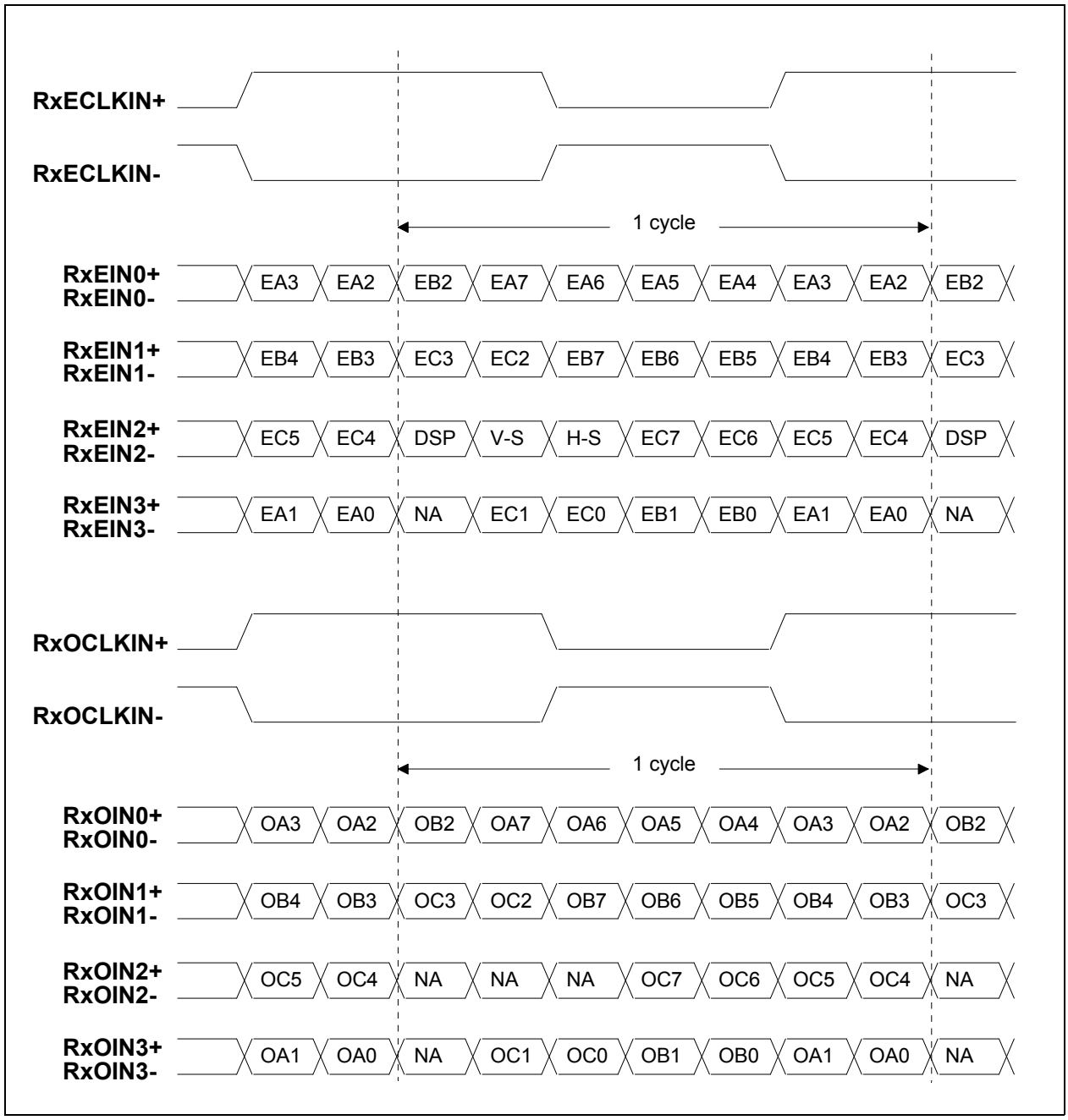
Note : Refer to the attached drawing for the connector position and pin No. 1 position.

Signal Description

SIGNAL NAME	Description
+A7 (EA7/OA7) +A6 (EA6/OA6) +A5 (EA5/OA5) +A4 (EA4/OA4) +A3 (EA3/OA3) +A2 (EA2/OA2) +A1 (EA1/OA1) +A0 (EA0/OA0) (EVEN/ODD)	A Sub Pixel Data 7 (MSB) A Sub Pixel Data 6 A Sub Pixel Data 5 A Sub Pixel Data 4 A Sub Pixel Data 3 A Sub Pixel Data 2 A Sub Pixel Data 1 A Sub Pixel Data 0 (LSB) A Sub Pixel Data: Each A Sub pixel's brightness data consists of these 8 bits pixel data.
+B7 (EB7/OB7) +B6 (EB6/OB6) +B5 (EB5/OB5) +B4 (EB4/OB4) +B3 (EB3/OB3) +B2 (EB2/OB2) +B1 (EB1/OB1) +B0 (EB0/OB0) (EVEN/ODD)	B Sub Pixel Data 7 (MSB) B Sub Pixel Data 6 B Sub Pixel Data 5 B Sub Pixel Data 4 B Sub Pixel Data 3 B Sub Pixel Data 2 B Sub Pixel Data 1 B Sub Pixel Data 0 (LSB) B Sub Pixel Data: Each B Sub pixel's brightness data consists of these 8 bits pixel data.
+C7 (EC7/OC7) +C6 (EC6/OC6) +C5 (EC5/OC5) +C4 (EC4/OC4) +C3 (EC3/OC3) +C2 (EC2/OC2) +C1 (EC1/OC1) +C0 (EC0/OC0) (EVEN/ODD)	C Sub Pixel Data 7 (MSB) C Sub Pixel Data 6 C Sub Pixel Data 5 C Sub Pixel Data 4 C Sub Pixel Data 3 C Sub Pixel Data 2 C Sub Pixel Data 1 C Sub Pixel Data 0 (LSB) C Sub Pixel Data: Each C Sub pixel's brightness data consists of these 8 bits pixel data.
DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 74.0MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.

Note : Output signals from any system shall be Hi-Z state when Vin is off.

LVDS per each channel becomes as below. Each channel has Hsync (H-S), Vsync (V-S) and DSPTMG (DSP).



Note : A/B/C data 7: MSB, A/B/C data 0: LSB, DSP = DSPTMG, V-S = Vsync, H-S = Hsync, x: A (Stripe A)or B(Stripe B)

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Each signal characteristics are as follows;

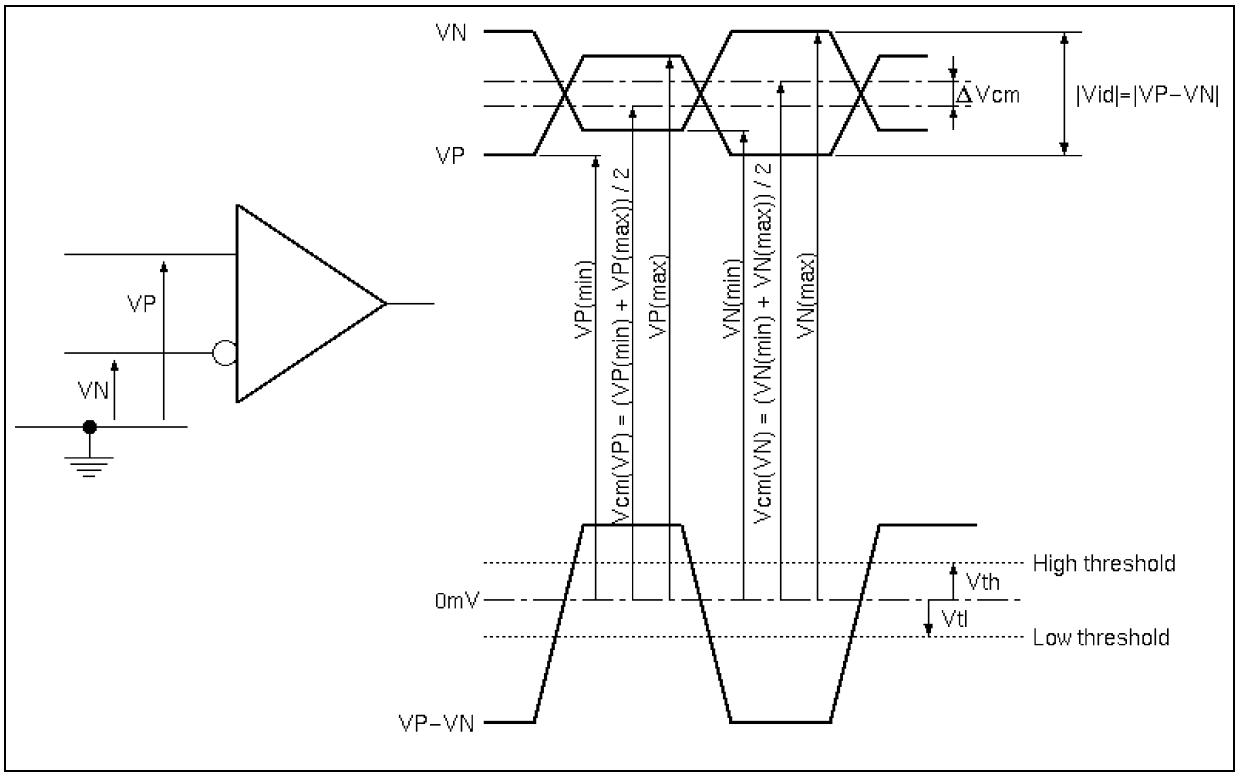
Electrical Characteristics

Parameter	Symbol	Min	Max	unit	Conditions
Differential Input High Threshold	Vth		+100	[mV]	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100		[mV]	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100	600	[mV]	
Common Mode Input Voltage	Vic	$0.825+\frac{\lvert Vid \rvert}{2}$	$2.0-\frac{\lvert Vid \rvert}{2}$	[V]	Vth-Vtl=200mV
Common Mode Voltage Offset	△Vcm	-50	+50	[mV]	Vth-Vtl=200mV

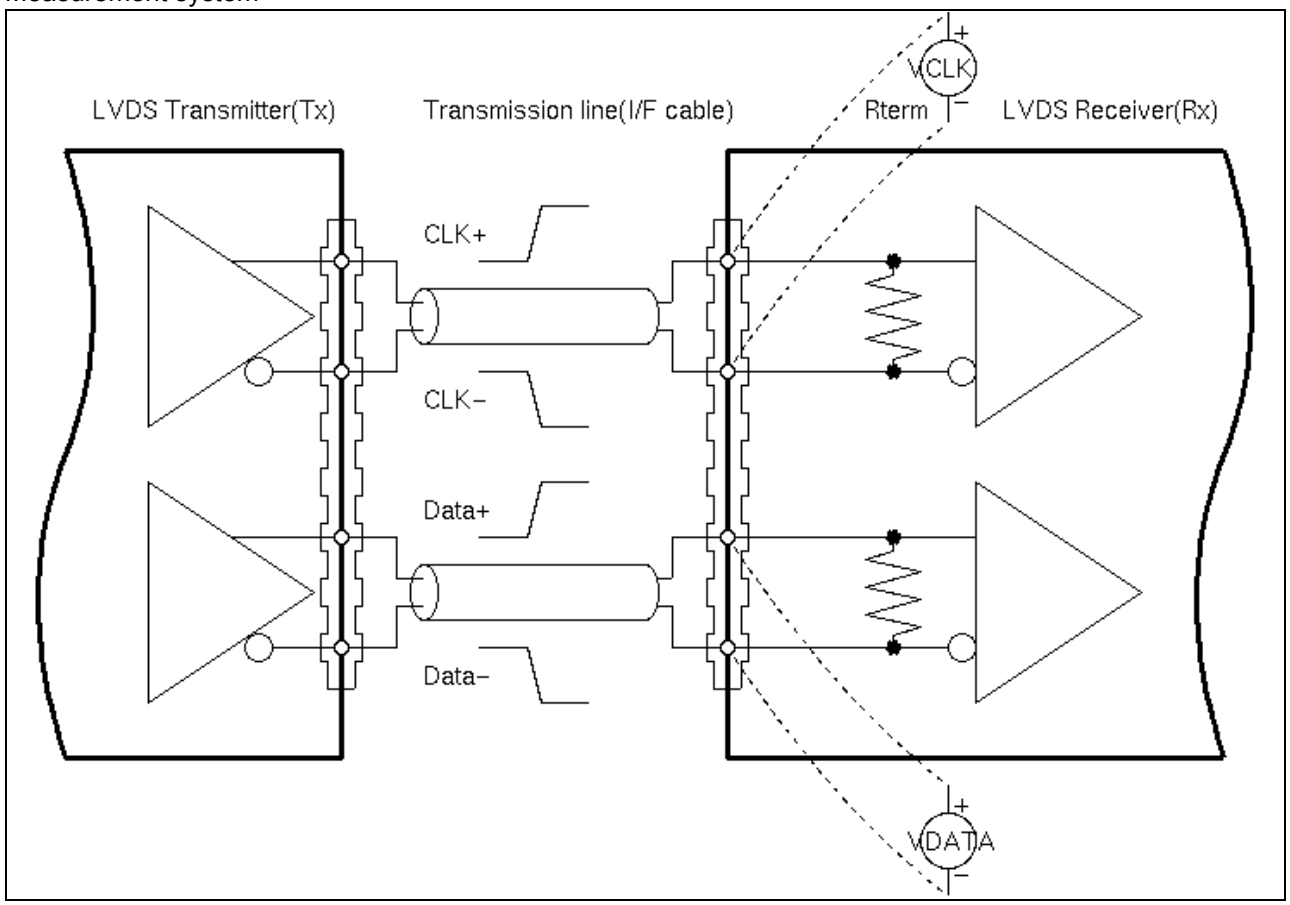
Note:

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see Figure Measurement system).
- IAQS80F has a 100-ohm resister between poritive and negative lines of each LVDS signal input.

Voltage Definitions



Measurement system



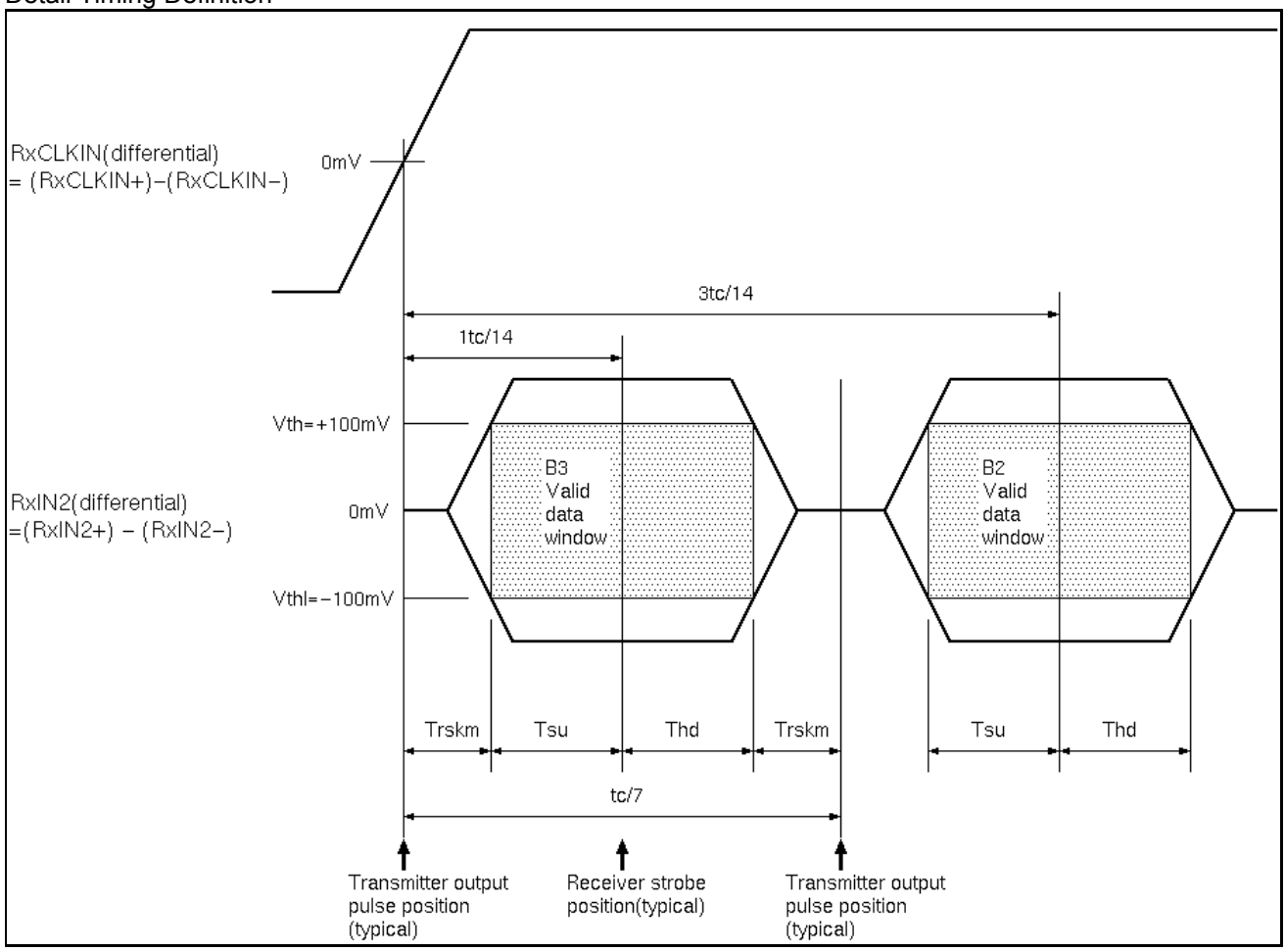
LVDS Receiver AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc		74.0		[MHz]	
Cycle Time	tc		13.5		[ns]	
Data Setup Time **(Note 2)**	Tsu	500			[ps]	fc = 74.0[MHz], tCCJ < 50[ps], Vth-Vtl=200[mV], Vcm=1.2[V], △Vcm=0[V]
Data Hold Time **(Note 2)**	Thd	500			[ps]	
Cycle-to-cycle jitter **(Note 3)**	TCCJ	-150		+150	[ps]	
Cycle Modulation Rate **(Note 4)**	tCJavg			20	[ps/clk]	

Note :

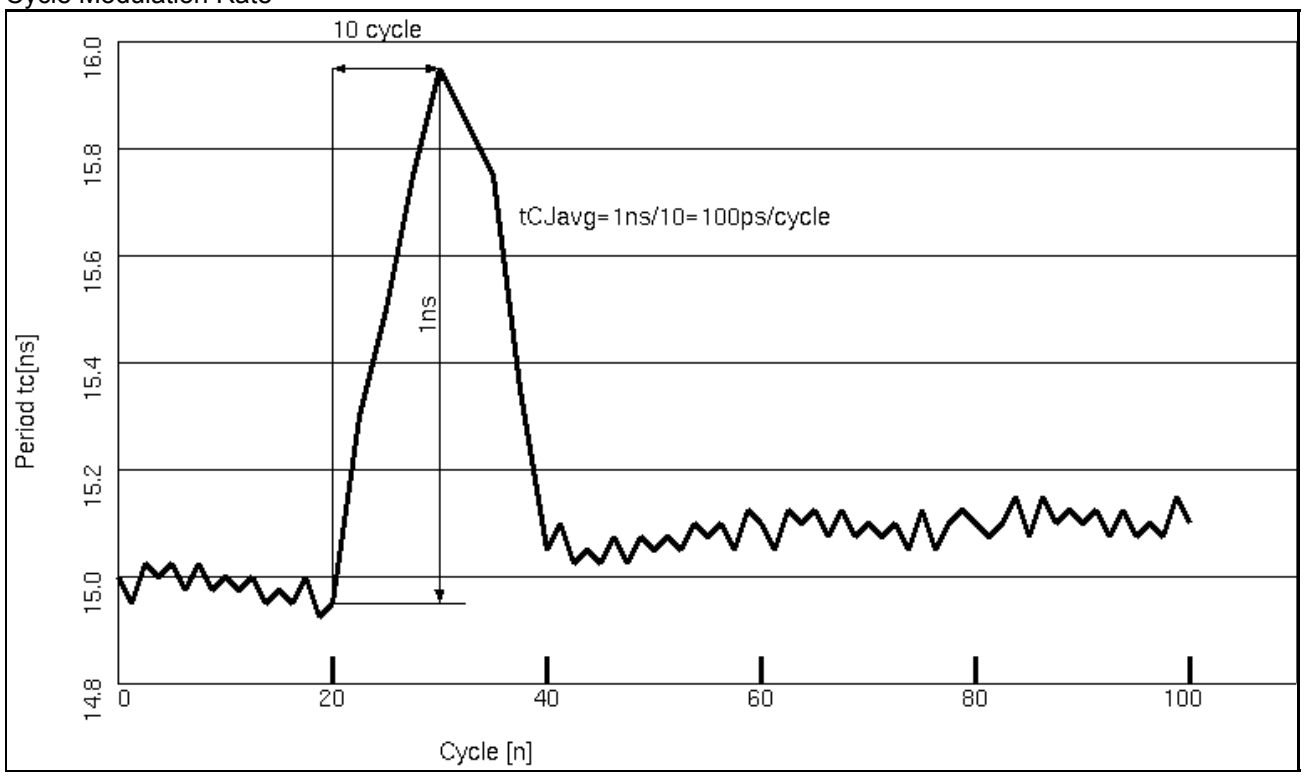
1. All values are at Vin=12.0[V], Ta=25[C deg.].
2. See figure "LVDS Format" and "Detail Timing Definition" for definition.
3. Jitter is the magnitude of the change in input clock period.
4. This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. Figure "Cycle Modulation Rate" illustrates a case against this requirement. This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Detail Timing Definition



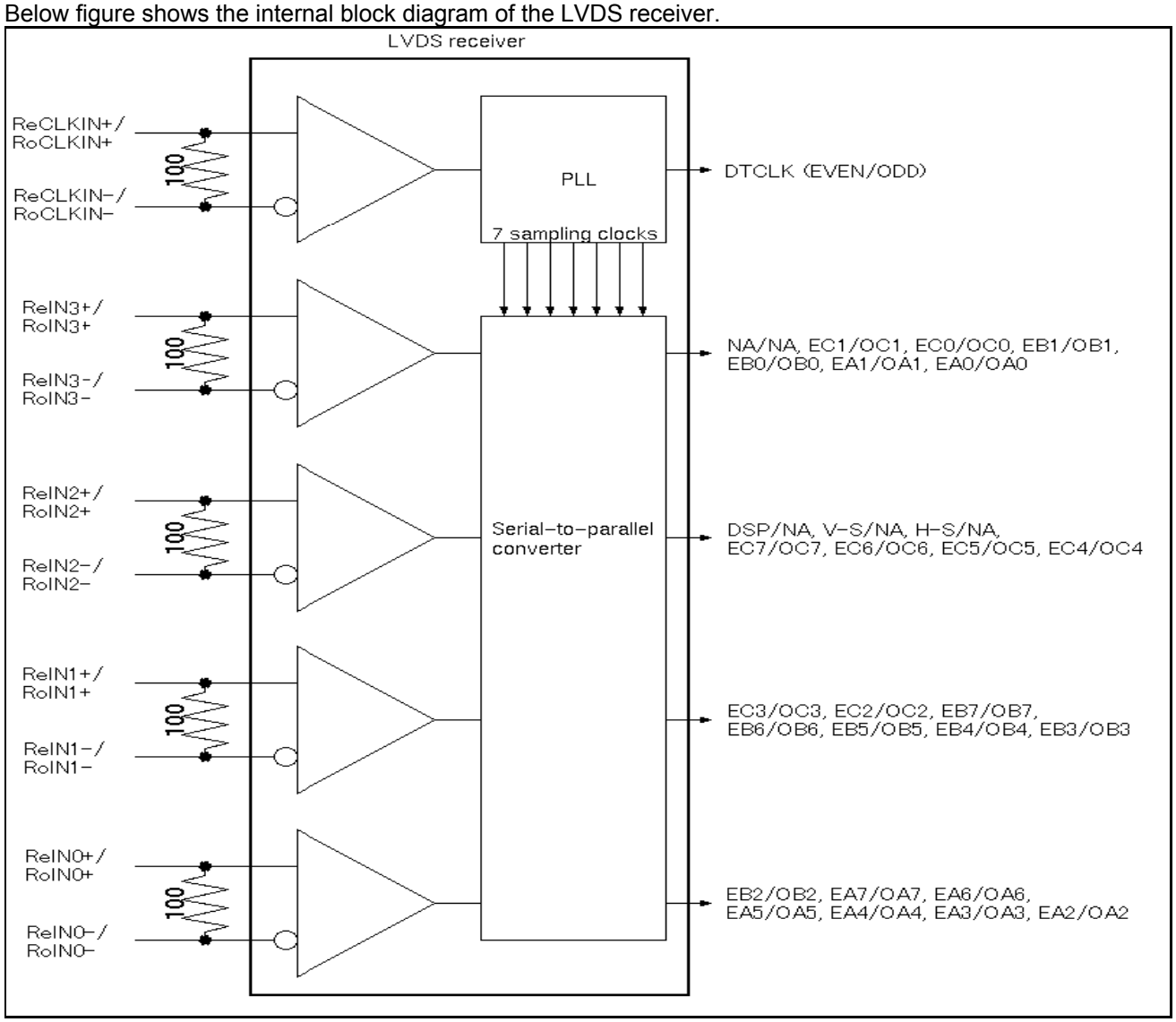
Note : Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

Cycle Modulation Rate



LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver.

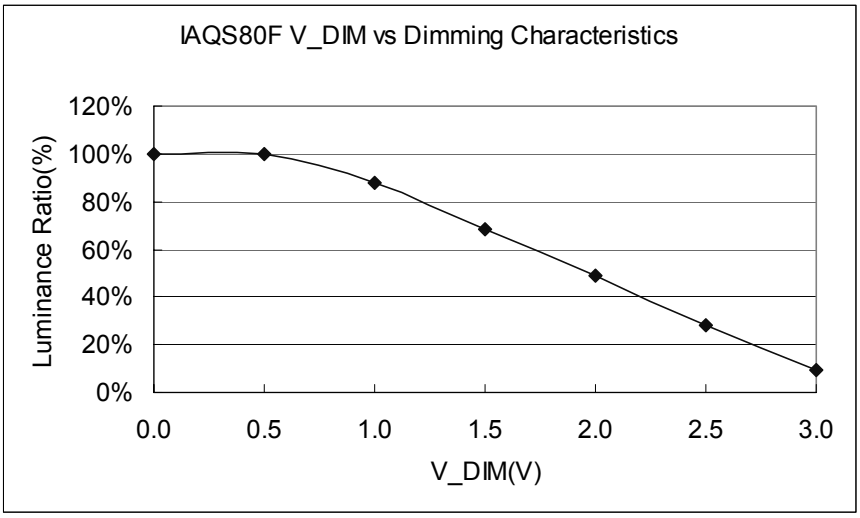


5.4.2 Back Light Control Signal Electrical Characteristics

Inverter Input Signal Electrical Characteristics

NAME	Description	Min	Typ	Max	Unit	Note
BLON	High level voltage	2.0	3.0	5.0	[V]	
	Low level voltage	-0.3	0.0	0.8	[V]	
	Current	-1.0	-	1.0	[mA]	
VDIM	Input Voltage range	0.0	-	3.0	[V]	0[V] : Brightness Max 3[V] : Brightness Min
	Current	-1.0	-	1.0	[mA]	

The following chart is the VDIM versus Dimming Range for your reference.



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

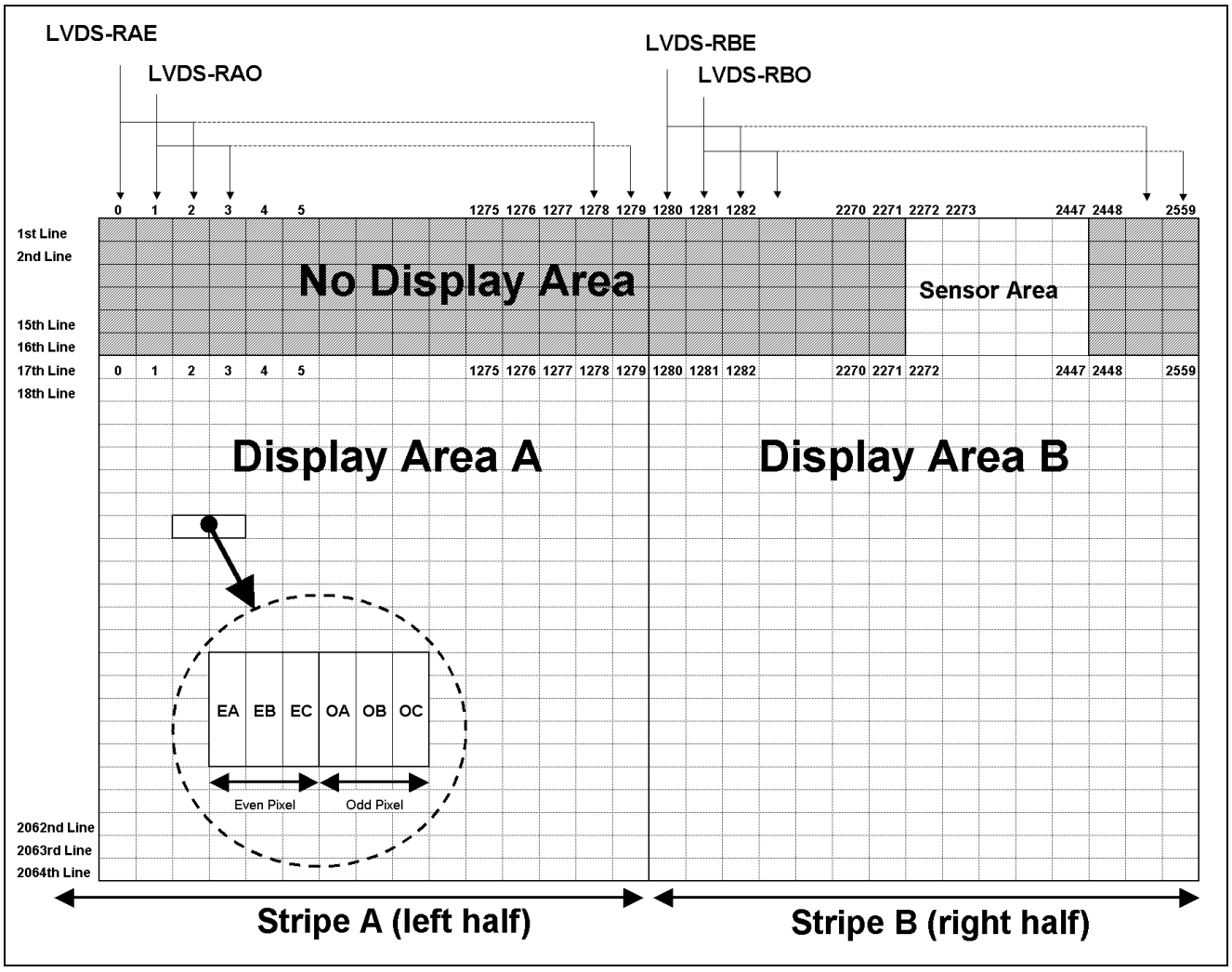
Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

6.0 Pixel format image

Following figure shows the relationship between the input signals and the LCD pixel format image.
IAQS80F has 4 sets of LVDS interface and they are bundled to two channels. The screen is divided into two vertical stripe screens (Stripe A and Stripe B) and each channel controls one of the half-size screens (1280 pixels x 2064 lines included sensor lines). Channel A and Channel B are corresponding to Stripe A and Stripe B individually.
Channel A includes 2 sets of LVDS (LVDS-A-E and LVDS-A-O) and the other channels are also the same manner.

Screen Format



7.0 Interface Timings

7.1 Timing Characteristics

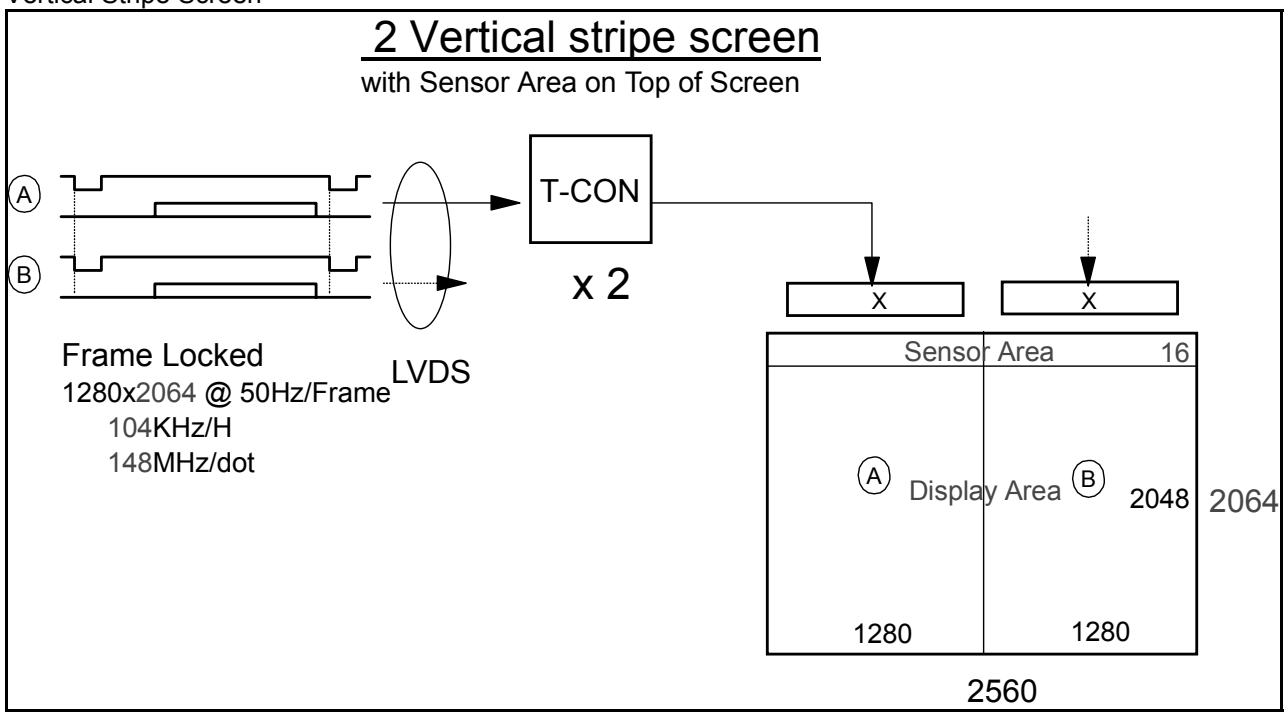
The TFT screen is divided to 2 vertically and each vertical stripe screen has the interface channel to be input video timing. So the number of channel is 2.

Timings among channels should be synchronized with each other (Frame Lock).
==> Same Clock source, Same V/H-Sync timing, Same Video timing

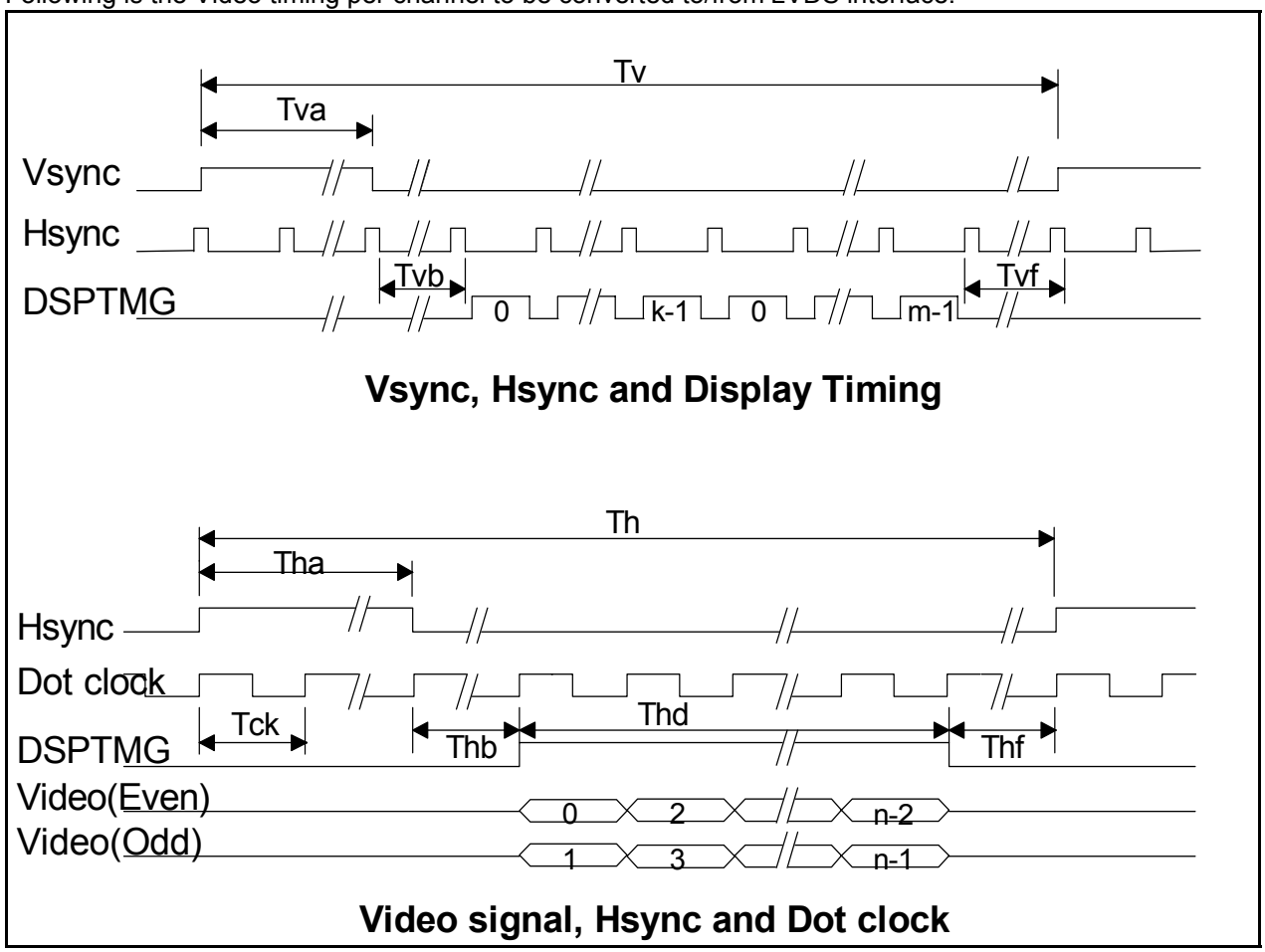
The interface of channel is LVDS (Dual pixel inputs).

The sensor area exists the top of screen. And it is recommended for these areas to be filled with the same image of 1st line of actual displayed image except for calibration time.

Vertical Stripe Screen



Following is the Video timing per channel to be converted to/from LVDS interface.



Vsync, Hsync and Display Timing

Video signal, Hsync and Dot clock

Note :

1. The sensor lines exist on top of screen, and it is recommended for this area to be filled with the same image of 1st line of actual displayed image except for calibration time. And also these lines need DSPTMG.
2. Even dot for 1st dot, Odd dot for 2nd dot.

Timing Characteristics

Signal	Item	Symbol	Min.	Typ.	Max.	Unit
DTCLK	Dot Clock Freq.	Fdck	71	74	76	[MHz]
DTCLK	Dot Clock period	Tck	13.16	13.51	14.08	[ns]
+V-Sync	Refresh Rate	1/Tv		50.06		[Hz]
+V-Sync	Frame period	Tv		20.00		[ms]
+V-Sync	Total line	Tv	2072	2076	2303	[lines]
+V-Sync	V-front porch	Tvf	1	3		[lines]
+V-Sync	V-active level	Tva	1	1		[lines]
+V-Sync	V-back porch	Tvb	6	8	127	[lines]
+V-Sync	V-Blank	Tvf+Tva+Tvb	8	12	255	[lines]
+DSPTMG	Display Lines / frame	k+m	-	2064	-	[lines]
+DSPTMG	Sensor Lines / frame	k	-	16	-	[lines]
+DSPTMG	Normal Lines / frame	m	-	2048	-	[lines]
+H-Sync	H-Scan Rate	1/Th		103.9		[kHz]
+H-Sync	H-Scan Rate	Th		9.62		[us]
+H-Sync	Cycle	Th	680	712	1023	[tck]
+H-Sync	H-front porch	Thf	32	56		[tck]
+H-Sync	H-active level	Tha	4	8		[tck]
+H-Sync	H-back porch	Thb	4	8		[tck]
+H-Sync	H-Blank	Thf+Tha+Thb	40	72	383	[tck]
+DSPTMG	Display clocks	Thd	-	640	-	[tck]
+DSPTMG	Display Pixels	n	-	1280	-	[pixels]

Note :

1. H/V sync Polarity will be acceptable both positive and negative. DSPTMG (Data Enable) should be Active High.
2. Vsync should not be changed at Hsync leading edge (+/- 6 [tck]).
3. Even Dot clock and Odd Dot clock in each channel should have completely the same clock source. The skew should be within +/- 1.5[ns].
4. All timing among channels should be synchronized (Vsync, Hsync, DSPTMG, Video and clocks) and the skew of Vsync etc. among channels should be within +/- 1 Tck.
5. All channels should be activated any time after Power On (because it does not have Auto Refresh protection).

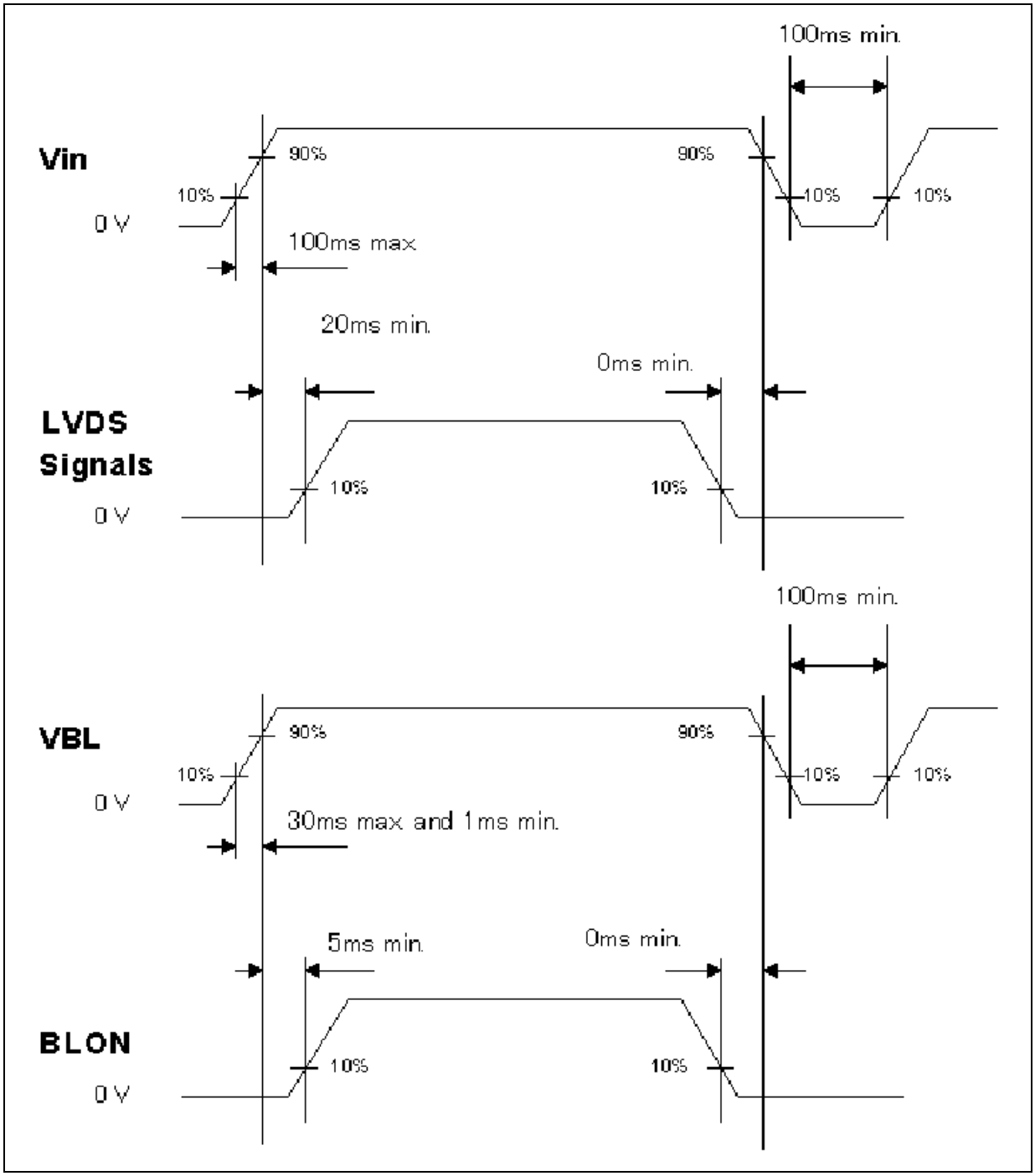
8.0 Power Consumption

SYMBOL	PARAMETER	Min.	Typ.	Max.	UNITS	CONDITION
Vin	Logic/LCD Drive Voltage	11.0	12.0	12.6	[V]	
Iin(1)	Vin Current (1)			1.7	[A]	Vin=11.0 to 12.6[V] **(Note 1)**
Iin(2)	Vin Current (2)	0.7		1.0	[A]	Vin=12.0[V] **(Note 2)**
Pin(1)	Vin Power (1)		8.1		[W]	Vin=12.0[V] **(Note 3)**
Pin(2)	Vin Power (2)			18.3	[W]	Vin=11.0 to 12.6[V] **(Note 2)**
Vin rp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	
Vin ns	Allowable Logic/LCD Drive Ripple Noise			100	[mVp-p]	
VBL	Backlight Power Voltage	11.0	12.0	12.6	[V]	
IBL	VBL Current	3.2	4.0	4.7	[A]	2 minutes after Power ON
		3.0	3.7	4.2	[A]	30 minutes after Power ON
PBL	Backlight Power Consumption **(Note 4)**		44.0	50.0	[W]	VBL=12.0[V] Max. brightness.
			8.0	10.0	[W]	VBL=12.0[V] Min. brightness.
				0.5	[W]	VBL=12.0[V] Stand-by
VBL rp	Allowable Backlight Drive Ripple Voltage			100	[mVp-p]	
VBL ns	Allowable Backlight Drive Ripple Noise			100	[mVp-p]	

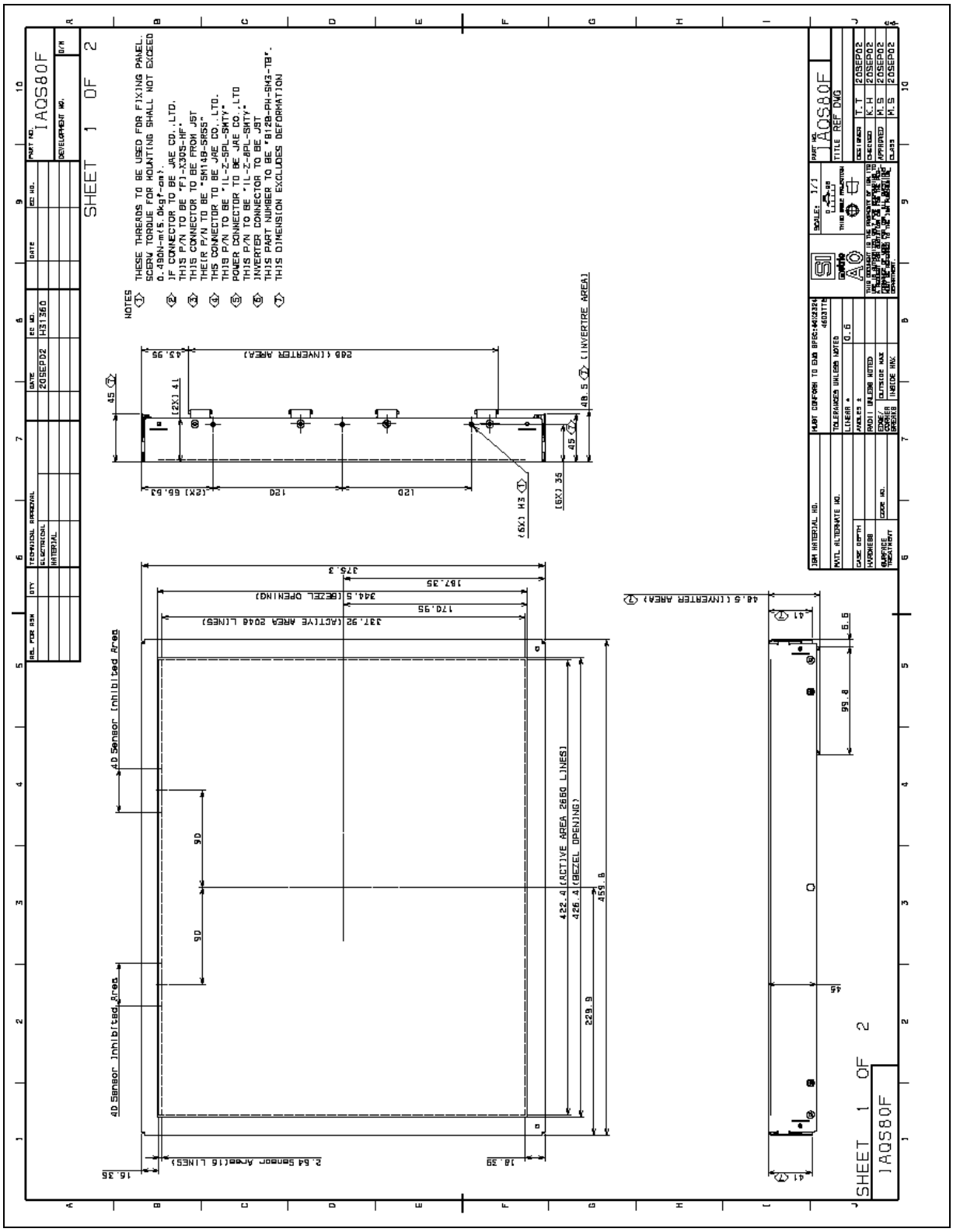
Note :
1. Horizontally-Sub-pixel/Vertically-Double-pixel Checker
2. All White (L255) Screen
3. Horizontal Gray Bar(Left=black, Right=White)
4. Measurement after CCFL luminance saturation. (minimum 60 minutes.)

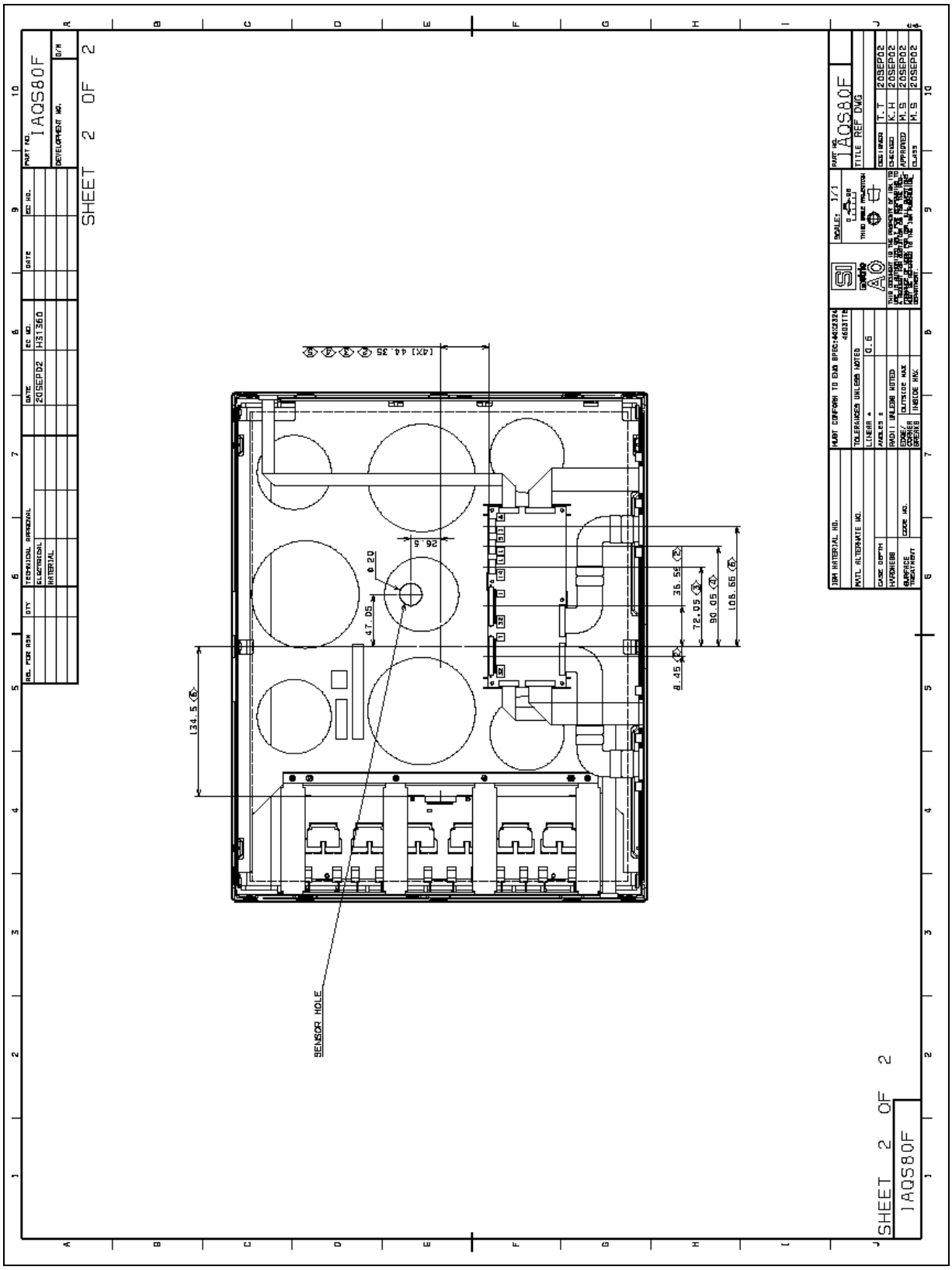
9.0 Power ON/OFF Sequence

Vin power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vin is off.

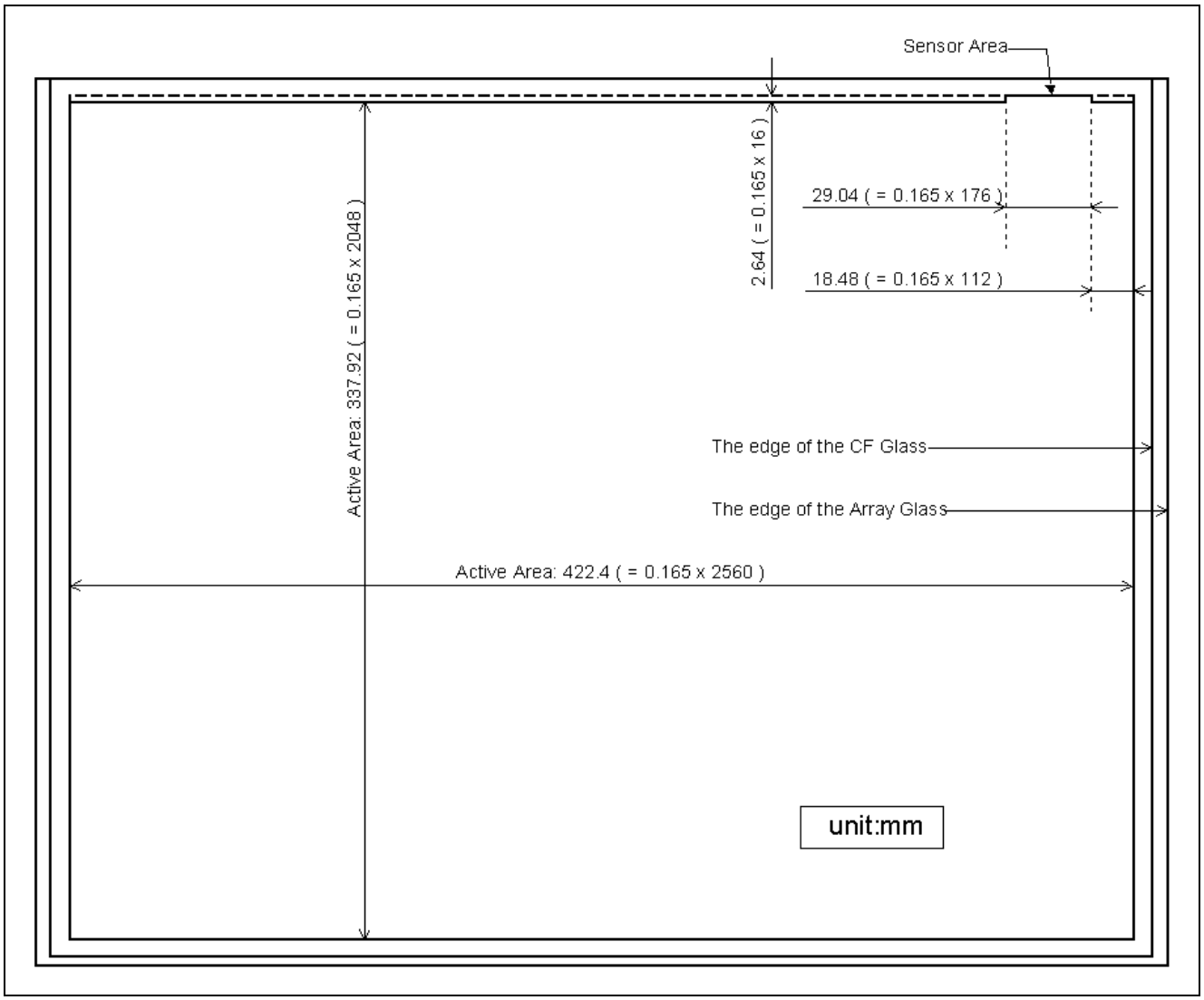


10.0 Mechanical Characteristics





Active Area / Sensor Area



11.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

Conditions of Acceptability - When installed in the end-product, consideration shall be given to the following;

1. This component has been judged on the basis of the required spacing in the Standard for Safety of Information Technology Equipment, CSA/UL 60950, Third Edition, dated December 1, 2000, Sub-clause 2.10, which would cover the component itself if submitted for Listing.
2. The inverter output circuit is Limited Current Circuits.
3. The unit is intended to be supplied by SELV and Limited Power Source. Also separated form electrical ports, which may produce high temperature that could cause ignition by as least 13mm of air or by a solid barrier of material of V-1 minimum.
4. The terminals and connectors are suitable for factory wiring only.
5. A suitable Fire/Electrical enclosure shall be considered at end-product evaluation.

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