Engineering Specification

Type 14.1 SXGA+ Color TFT/LCD Module
Model Name:IASX16C

Document Control Number : OEM I-916C-01

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Sales Support
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ii Record of Revision

Date	Document Revision	Page	Summary
November 11, 2002	OEM I-916C-01	All	First Edition for customer. Based on Internal Spec. as of April 11, 2002 and development team's information. (Lamp Cable Length : 90mm)

1.0 Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.
- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.
- CMOS ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.
- Do not press the reflector sheet at the LCD module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- Please handle with care when mount in the system cover. Mechanical damage for lamp cable/lamp connector may cause safety problems.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.5, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 or UL60950) in an end product.
- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL60950).
- The fluorescent lamp in the liquid crystal display(LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Never apply detergent or other liquid directly to the screen.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
- Do not touch the front screen surface in your system, even bezel.
- Gently wipe the covers and the screen with a soft cloth.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the Type 14.1 Color TFT/LCD Module 'IASX16C'.
This module is designed for a display unit of a notebook style personal computer.
The screen format and electrical interface are intended to support the SXGA+ (1400(H) x 1050(V)) screen.
Support color is native 262k colors (RGB 6-bit data driver).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

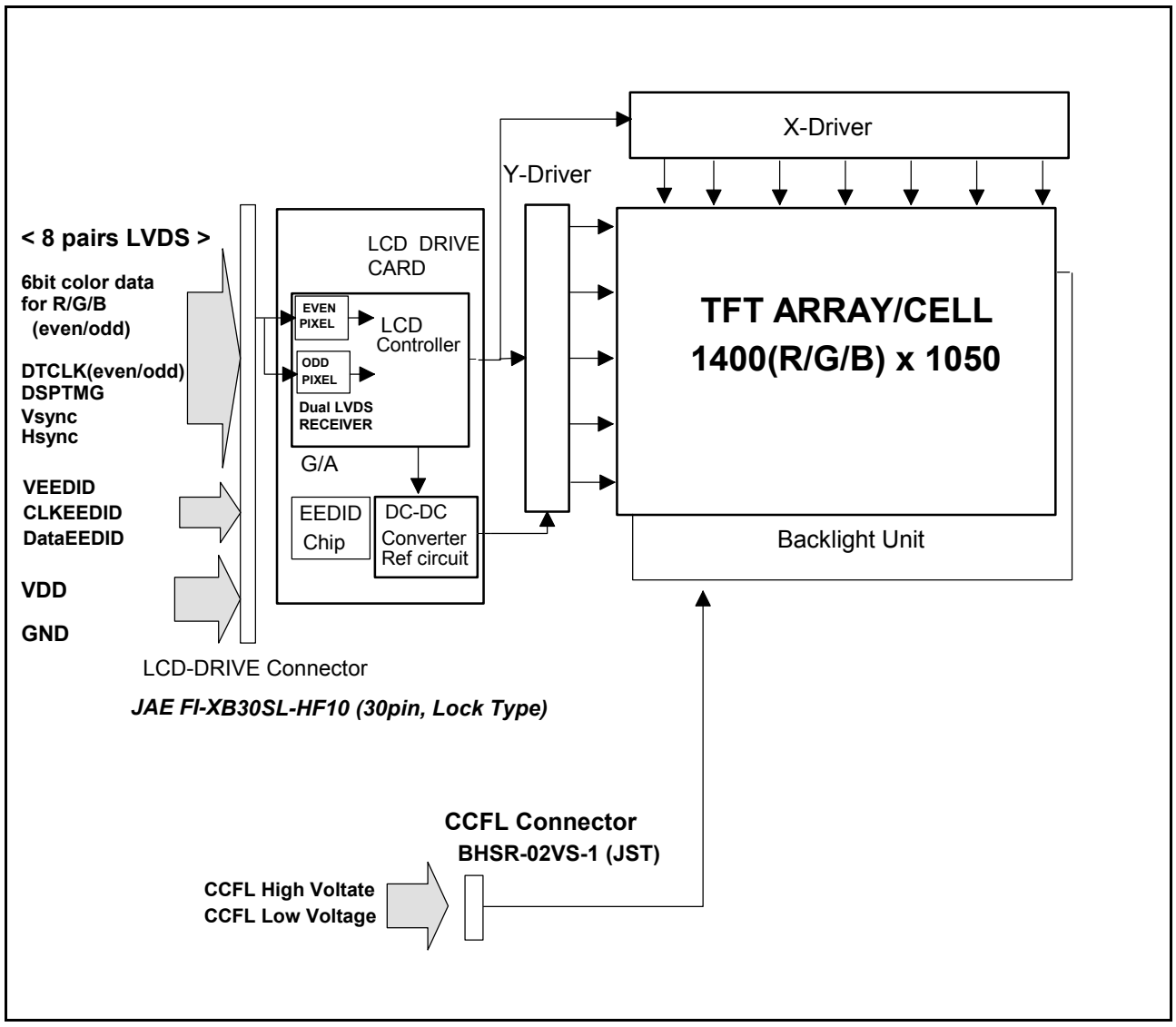
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [cm]	35.7
Active Area [mm]	285.6(H) x 214.2(V)
Pixels H x V [pixels]	1400(x3) x 1050
Pixel Pitch [mm]	0.204(per one triad) x 0.204
Pixel Arrangement	R.G.B. Vertical Stripe
Display Mode	Normally White
White Luminance [cd/m^2]	170 Typ. (5pts) @ CFL current =6.5mA
Contrast Ratio	250 : 1 Typ.
Optical Rise Time+Fall Time [msec]	45 Typ. , 50 Max.
Nominal Input Voltage [Volt]	+3.3 Typ. (+3.0 to +3.6:VDD)
Logic Power Consumption [watt]	1.8 Typ.
Backlight Power Consumption [watt]	4.0 Typ.(@CFL current 6.5mA without Inverter loss)
Weight [grams]	405 Typ.
Physical Size [mm]	299.0(W) x 226.5(H) x 5.2(D) Typ.
CCFL Cable Length [mm]	90 Typ.
Electrical Interface	8 pairs LVDS(R/G/B Data (6-bit), 3 sync signals, Clock), EEDID (clock, data)
Support Color	Native 262K colors (RGB 6-bit data driver)
Temperature Range [deg. C]	0 to +50 (Operating) -20 to +60 (Storage, Shipping)

2.2 Functional Block Diagram

The following diagram shows the functional block of the Type 14.1 Color TFT/LCD Module.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	+4.0	V	
Input Voltage of Signal	Other Inputs	-0.3	VDD+0.3	V	
Lamp Ignition Voltage	VCFL	-	+1,650	Vrms	Ta = 0 [deg.C]
CFL Current	ICFL	-	7	mArms	
CFL Peak Inrush Current	ICFLP	-	20	mArms	Ta = 25 [deg.C] **(Note 1)**
Operating Temperature	TOP	0	+50	deg.C	**(Note 2)**
Operating Relative Humidity	HOP	8	95	%RH	**(Note 2)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 2)**
Storage Relative Humidity	HST	5	95	%RH	**(Note 2)**
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note :

1. Duration : 50 [msec] Max.
2. Maximum Wet-Bulb should be 39 degree C and No condensation.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≥10 (Left) Vertical (Upper) K≥10 (Lower)	40 40 15 30	- - - -
Contrast ratio		250	-
Response Time (ms)	Rising + Falling	-	50 Max.
Color Chromaticity (CIE)	Red x	0.577	-
	Red y	0.338	-
	Green x	0.310	-
	Green y	0.544	-
	Blue x	0.158	-
	Blue y	0.124	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2) ICFL 6.5 mA		180 Typ. Center 170 Typ. 5 points average	-

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30SL-HF10
Mating Type / Part Number	FI-X30M, FI-X30C2L

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Signal Connector Pin Assignment

Pin #	Signal Name
1	FG (GND)
2	GND
3	VDD
4	VDD
5	V_{EEDID} **(Note 2,3)**
6	NC (Reserved, **Note 1**)
7	CLK_{EEDID} **(Note 2,4)**
8	$Data_{EEDID}$ **(Note 2,4)**
9	ReIN0- **(Note 5)**
10	ReIN0+**(Note 5)**
11	GND
12	ReIN1-**(Note 5)**
13	ReIN1+**(Note 5)**
14	GND
15	ReIN2-**(Note 5)**
16	ReIN2+**(Note 5)**

Pin #	Signal Name
17	GND
18	ReCLKIN-**(Note 5)**
19	ReCLKIN+**(Note 5)**
20	GND
21	RoIN0-**(Note 5)**
22	RoIN0+**(Note 5)**
23	GND
24	RoIN1-**(Note 5)**
25	RoIN1+**(Note 5)**
26	GND
27	RoIN2-**(Note 5)**
28	RoIN2+**(Note 5)**
29	GND
30	RoCLKIN-**(Note 5)**
31	RoCLKIN+**(Note 5)**
32	FG (GND)

Note:

1. 'Reserved' pins are not allowed to connect any other line.
2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3".
   This module uses Serial EEPROM BR24C02FV (ROHM) or compatible as a EEDID function.
3. V_{EEDID} power source shall be the current limited circuit which has not exceeding 1A. (Reference Document : "Enhanced Display Data Channel (E-DDC™) Proposed Standard", VESA)
4. Both CLK_{EEDID} line and $Data_{EEDID}$ line are pulled-up with 10K ohm resistor to V_{EEDID} power source line at LCD panel, respectively.
5. Voltage levels of all input signals are LVDS compatible. Refer to "Signal Electrical Characteristics for LVDS", for voltage levels of all input signals

5.3 Interface Signal Description

Signal Description

PIN #	SIGNAL NAME	Description
1	FG	Frame Ground
2	GND	Ground
3	VDD	+3.3V Power Supply
4	VDD	+3.3V Power Supply
5	Veedid	DDC 3.3V Power Supply
6	NC	Reserved
7	CLKeedid	DDC Clock
8	DATAeedid	DDC Data
9	ReIN0-	Negative LVDS differential data input (Even R0-R5, G0)
10	ReIN0+	Positive LVDS differential data input (Even R0-R5, G0)
11	GND	Ground
12	ReIN1-	Negative LVDS differential data input (Even G1-G5, B0-B1)
13	ReIN1+	Positive LVDS differential data input (Even G1-G5, B0-B1)
14	GND	Ground
15	ReIN2-	Negative LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
16	ReIN2+	Positive LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
17	GND	Ground
18	ReCLKIN-	Negative LVDS differential clock input (Even)
19	ReCLKIN+	Positive LVDS differential clock input (Even)
20	GND	Ground
21	RoIN0-	Negative LVDS differential data input (Odd R0-R5, G0)
22	RoIN0+	Positive LVDS differential data input (Odd R0-R5, G0)
23	GND	Ground
24	RoIN1-	Negative LVDS differential data input (Odd G1-G5, B0-B1)
25	RoIN1+	Positive LVDS differential data input (Odd G1-G5, B0-B1)
26	GND	Ground
27	RoIN2-	Negative LVDS differential data input (Odd B2-B5)
28	RoIN2+	Positive LVDS differential data input (Odd B2-B5)
29	GND	Ground
30	RoCLKIN-	Negative LVDS differential clock input (Odd)
31	RoCLKIN+	Positive LVDS differential clock input (Odd)
32	FG	Frame Ground

Note:

- Input signals of odd and even clock shall be the same timing.
- The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
- Even: First Pixel , Odd: Second Pixel

SIGNAL NAME	Description
+RED 5 (ER5/OR5) +RED 4 (ER4/OR4) +RED 3 (ER3/OR3) +RED 2 (ER2/OR2) +RED 1 (ER1/OR1) +RED 0 (ER0/OR0) (EVEN/ODD)	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 (EG5/OG5) +GREEN 4 (EG4/OG4) +GREEN 3 (EG3/OG3) +GREEN 2 (EG2/OG2) +GREEN 1 (EG1/OG1) +GREEN 0 (EG0/OG0) (EVEN/ODD)	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 (EB5/OB5) +BLUE 4 (EB4/OB4) +BLUE 3 (EB3/OB3) +BLUE 2 (EB2/OB2) +BLUE 1 (EB1/OB1) +BLUE 0 (EB0/OB0) (EVEN/ODD)	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 54MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Only active high signal is acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
VDD	Power Supply
GND	Ground
V_{EEDID}	EEDID Power Supply
CLK_{EDID}	EEDID Clock
$Data_{EEDID}$	EEDID data

Note: Output signals except V_{EEDID} ,CLK_{EEDID} and $Data_{EEDID}$ from any system shall be Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

The LVDS receiver equipped in this LCD module is compatible with ANSI/TIA/TIA-644 standard.

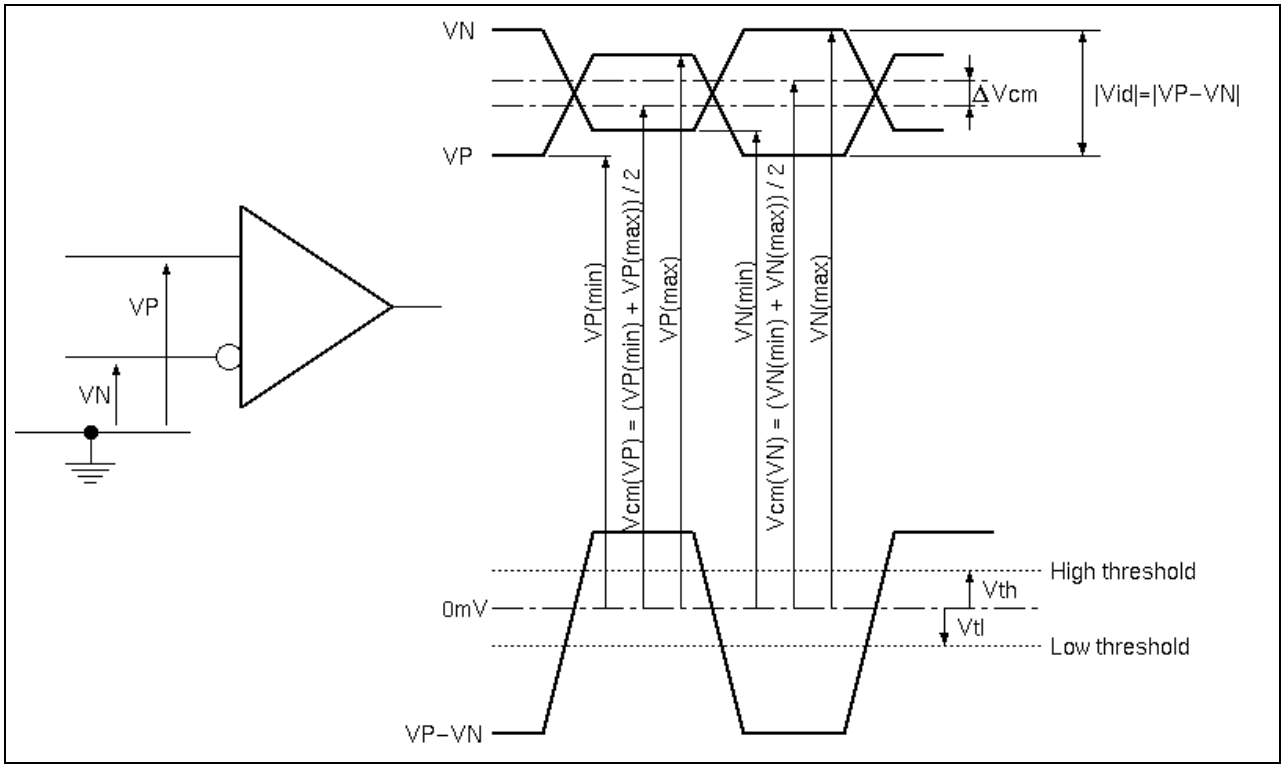
Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	
Differential Input Low Threshold	Vtl	-100			mV	
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	0.825 +|Vid|/2		2.4 -|Vid|/2	V	
Common Mode Voltage Offset	△Vcm	-50		+50	mV	

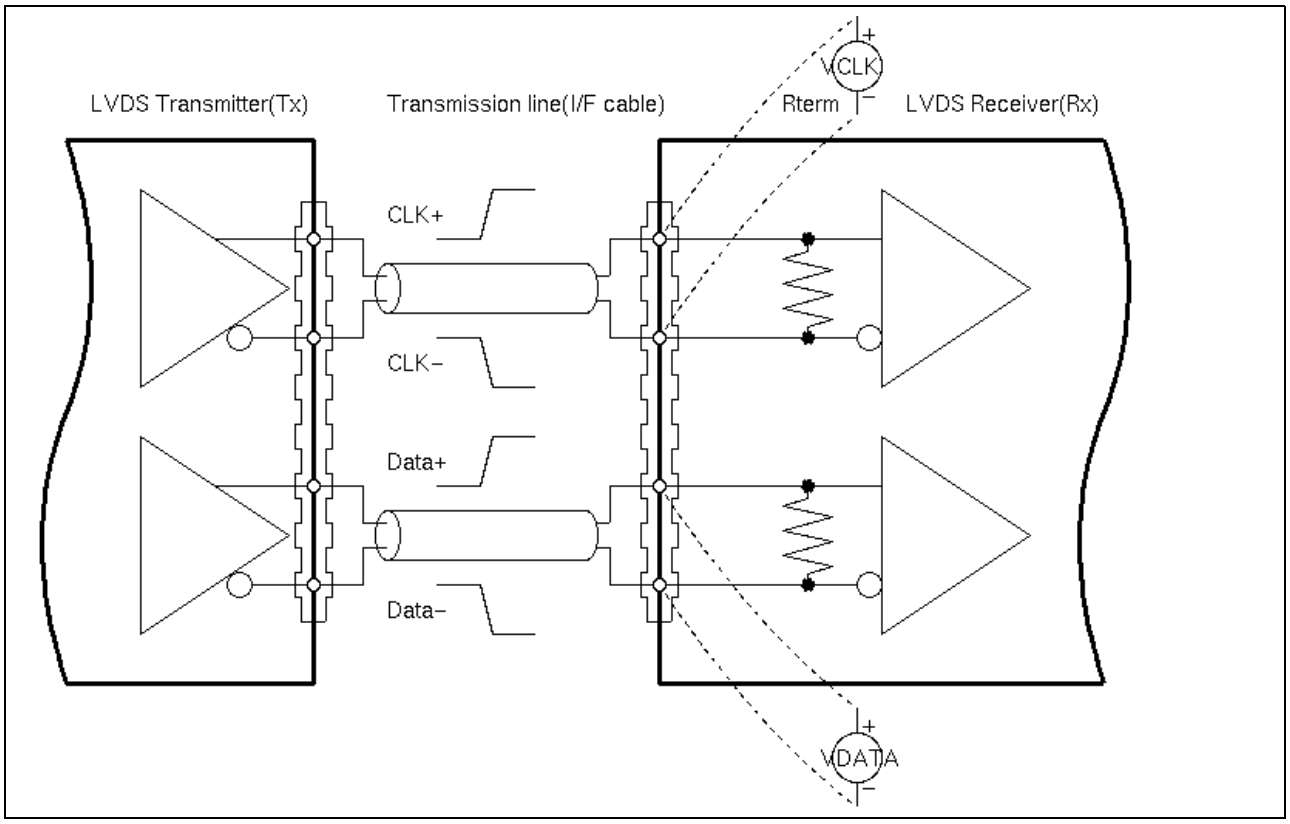
Note :

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD. (See Figure **"Measurement system"**).

Voltage Definitions



Measurement System



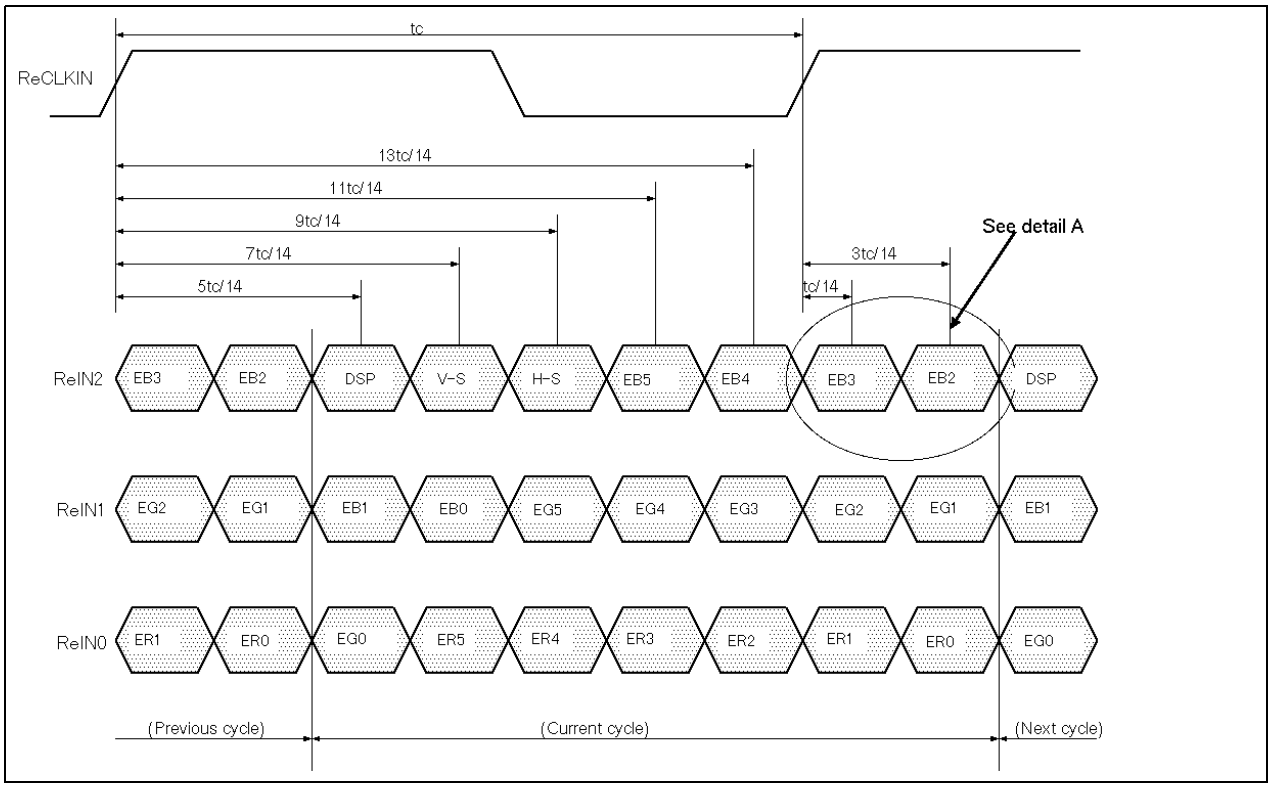
Timming Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	51	54	57	MHz	
Cycle Time	tc	17.5	18.5	19.6	ns	
Data Setup Time**(Note 1)**	Tsu	700			ps	fc = 54MHz, tCCJ < 50ps, Vth-Vtl = 200mV, Vcm = 1.2V, △Vcm = 0
Data Hold Time**(Note 2)**	Thd	700			ps	
Cycle-to-cycle jitter**(Note 3)**	tCCJ	-150		+150	ps	fc = 54MHz, Tsu=Thd=1080ps
Cycle Modulation Rate**(Note 4)**	tCJavg			20	ps/clk	fc = 54MHz, Tsu=Thd=1080ps

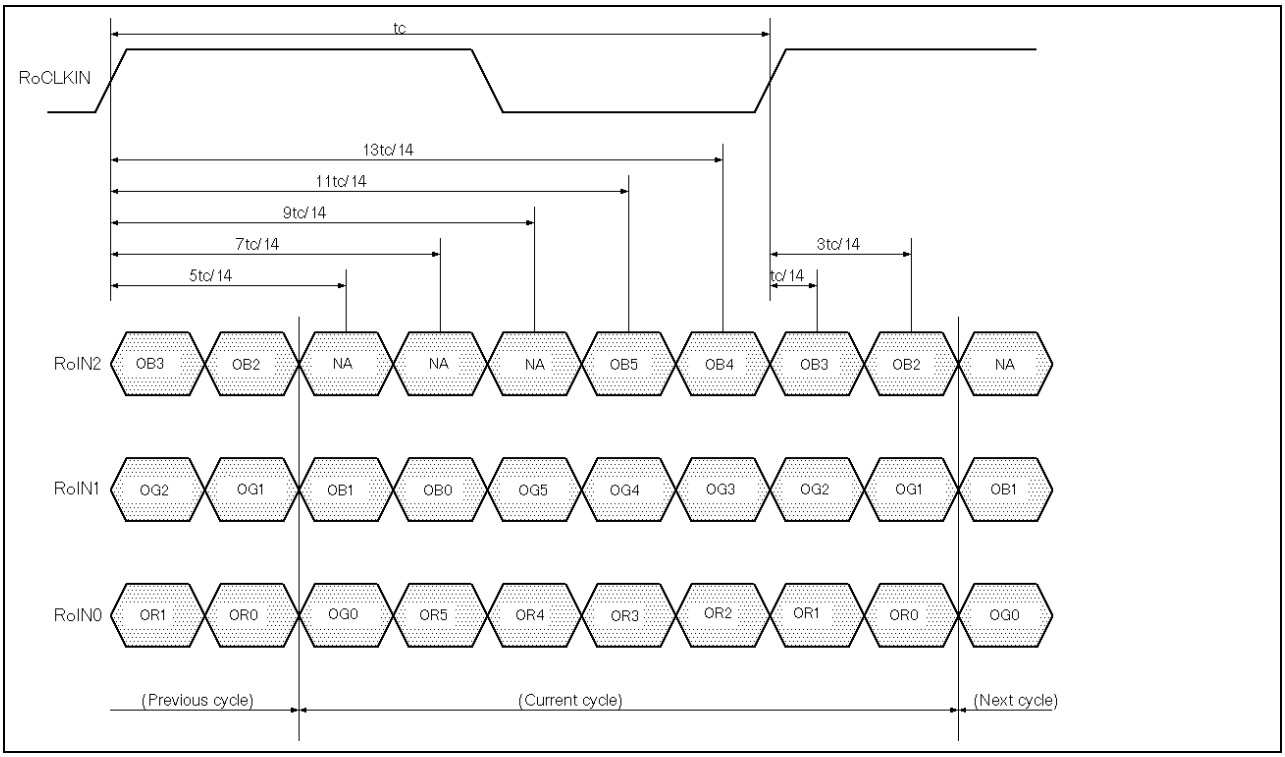
Note:

1. All values are at VDD=3.3V, Ta=25 degree C.
2. See "Timing Definition" and "Timing Definition(detail A)" for definition.
3. Jitter is the magnitude of the change in input clock period.
4. This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. Figure "Cycle Modulation Rate" illustrates a case against this requirement.
   This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

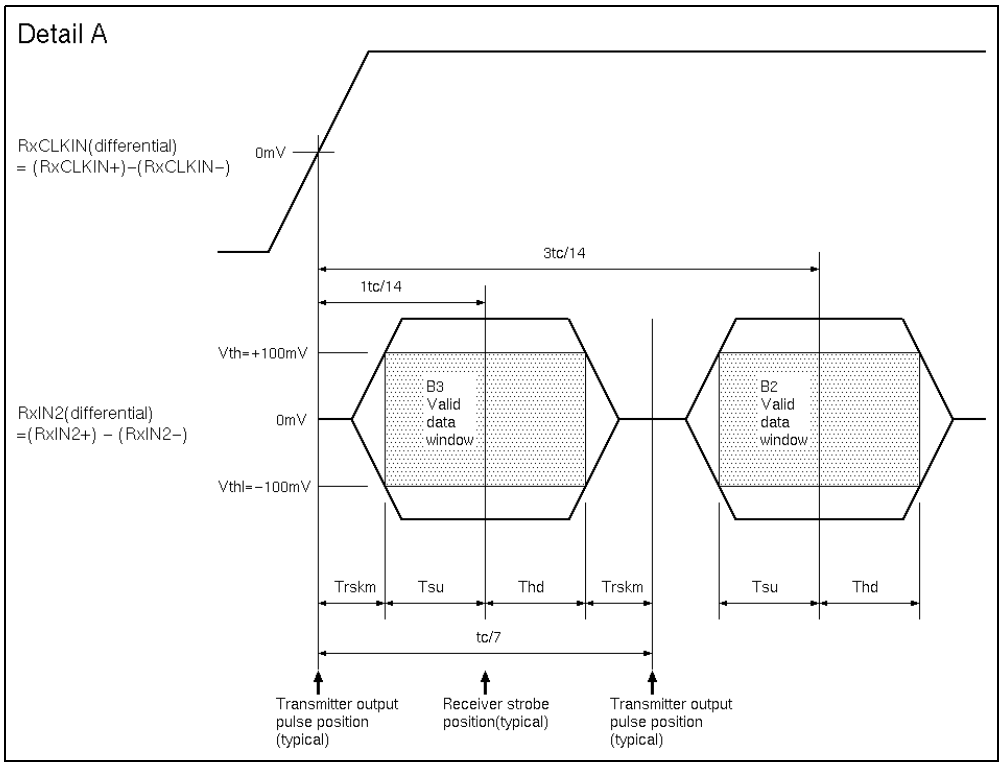
Timing Definition (Even)



Timing Definition (Odd)

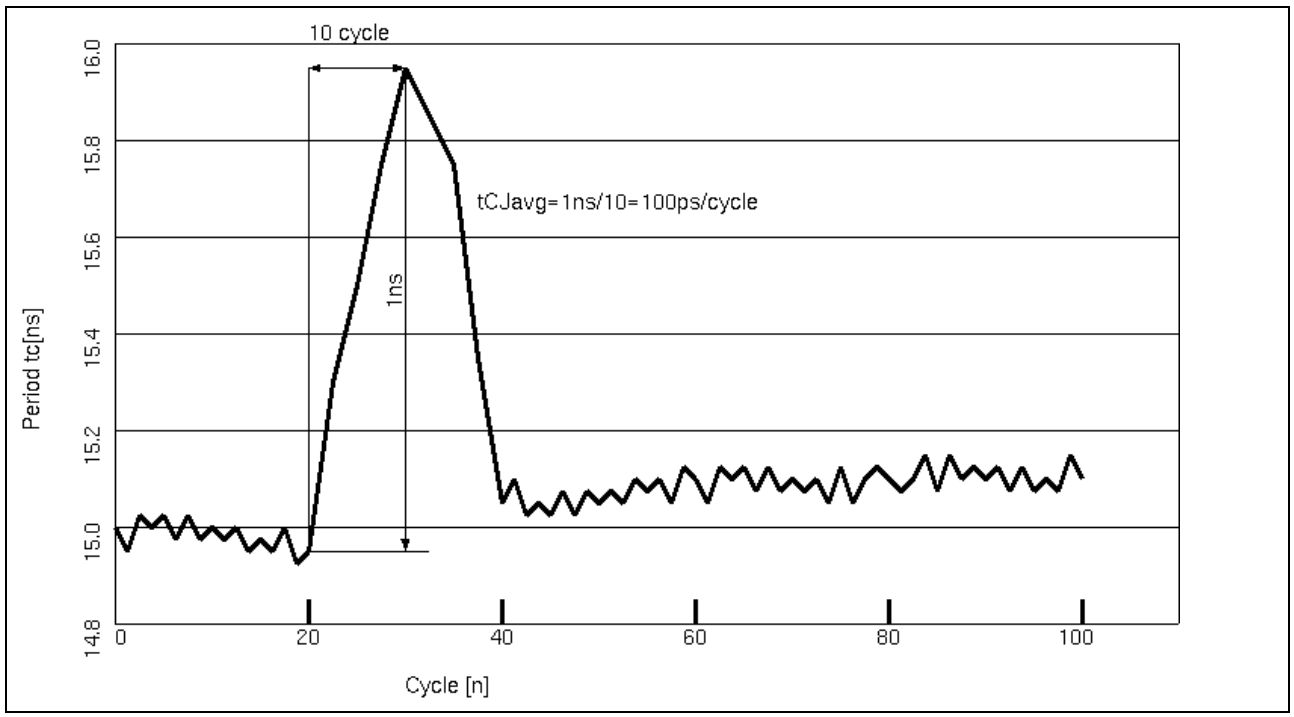


Timing Definition (detail A)



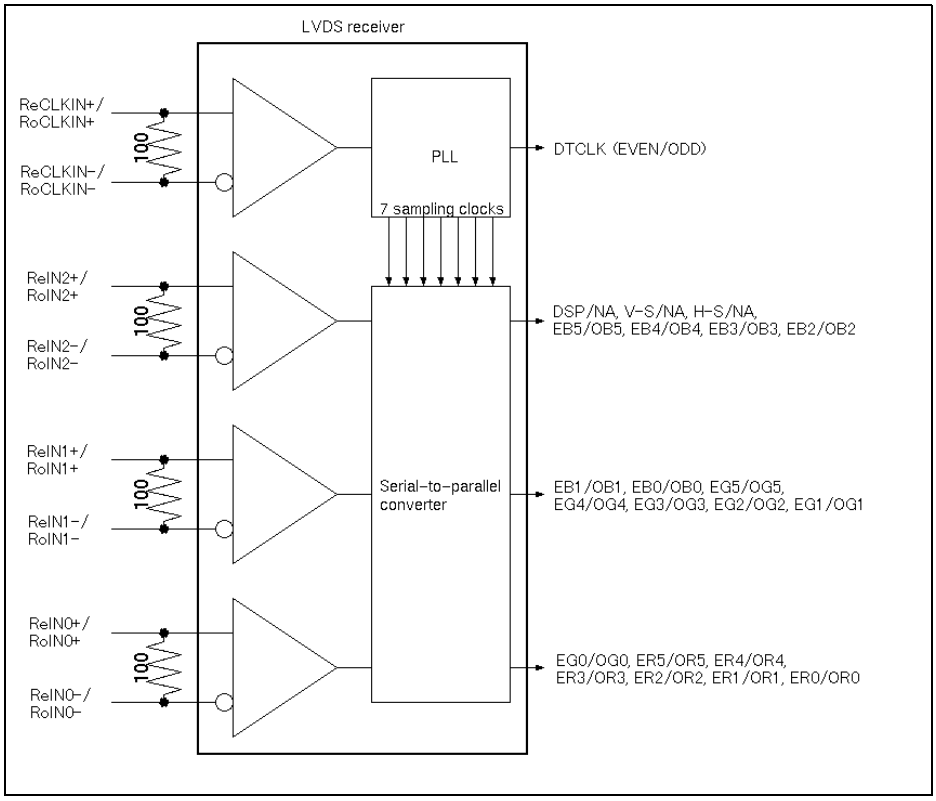
Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

Cycle Modulation Rate



5.4.2 LVDS Receiver Internal Circuit

The following figure shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

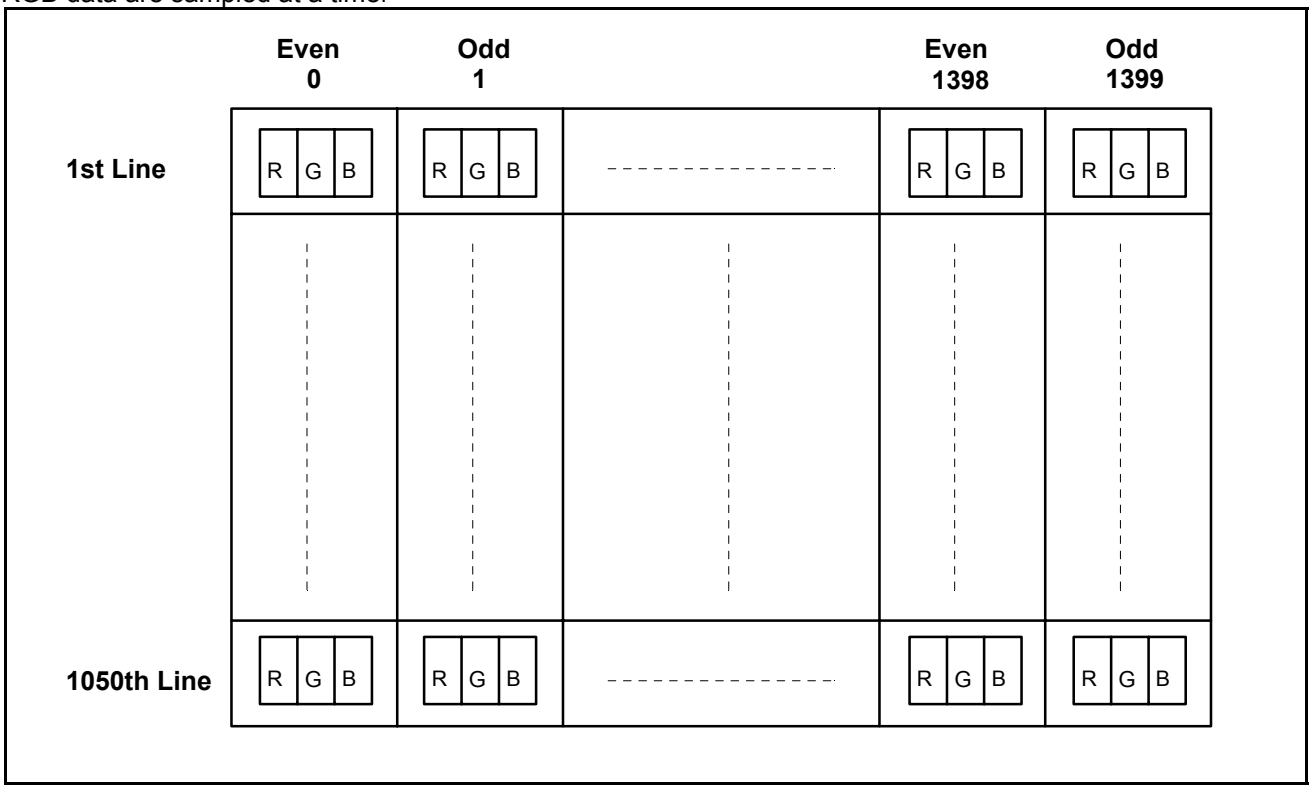
- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Even and odd pair of RGB data are sampled at a time.



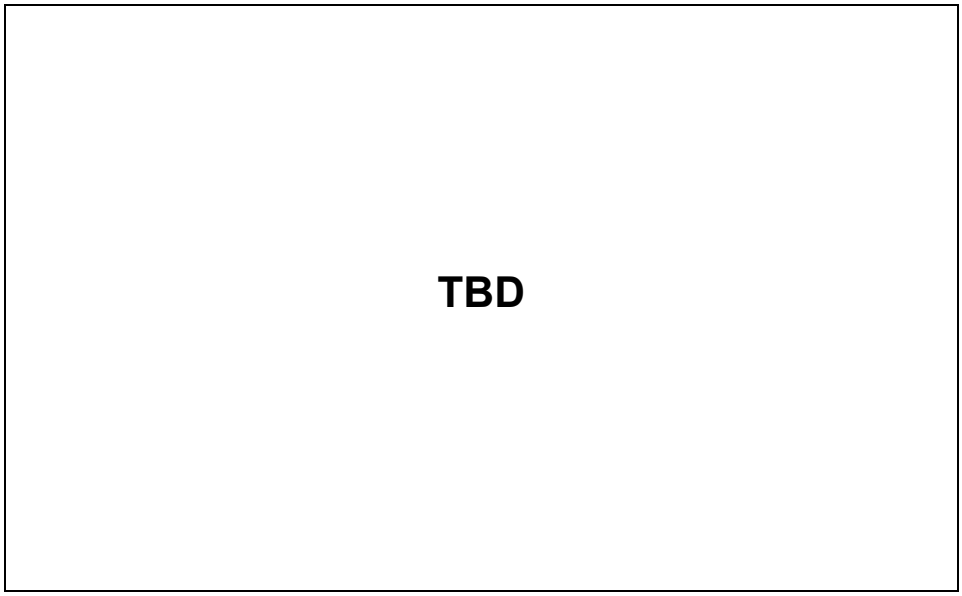
7.0 Parameter guide line for CFL Inverter

SYMBOL	PARAMETER	MIN	D.P-1 Note1	MAX	UNITS	CONDITION
(L63)	White Luminance (Center) (5 points average)	 - -	 180 170	 - -	 [cd/m^2] [cd/m^2]	Ta=25[deg. C]
ICFL	CFL current	3.0	6.5	7.0	[mArms]	Ta=25[deg. C] **(Note2,5)**
ICFLP	CFL Peak Inrush Current			20	[mA]	Ta=25[deg. C] **(Note2,6)**
FCFL	CFL Frequency	40		60	[kHz]	Ta=25[deg. C] **(Note 3)**
VCFLi	Inverter Ignition Voltage	1,600			[Vrms]	Ta=0[deg. C]
VCFL	CFL Voltage (Reference)		615		[Vrms]	Ta=25[deg. C]
PCFL	CFL Power consumption		4.0		[W]	Ta=25[deg. C] **(Note 4)**

Note :

1. Design Point-1
2. If it exceeds MIN/MAX values, then"CFL Life" , "ON/OFF Cycle", and "SAFETY" will not be guaranteed.
3. CFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD.
4. Calculated value for reference (ICFL x VCFL = PCFL).
5. It should be employed the inverter which has `Duty Dimming`, if ICFL is less than 4[mA].
6. Duration: 50msec MAX

The following chart is Luminance versus Lamp Current for your reference.



8.0 Interface Timings

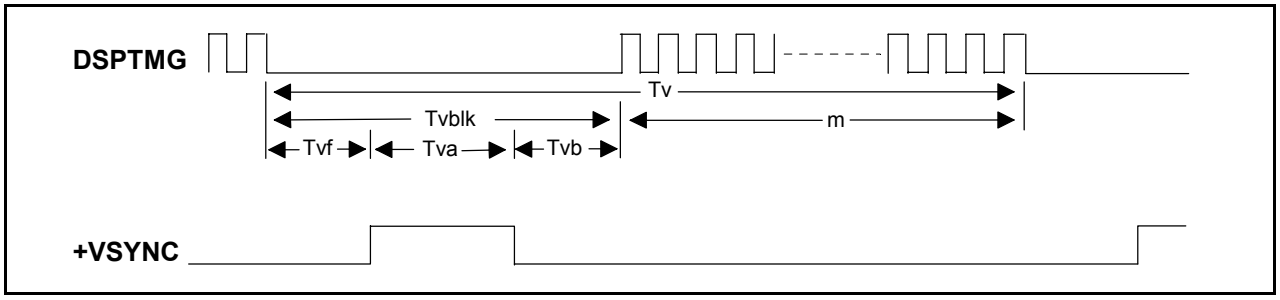
8.1 Timing Characteristics

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	51	54	57	[MHz]
		Tck	17.5	18.5	19.6	[nsec]
+V-Sync	Frame Rate	Fv		60		[Hz]
		Tv		16.67		[msec]
		Nv	1058	1066	2046	[lines]
	V-Sync Width	Tva	15.78	46.7		[usec]
		Nva	1	3	62	[lines]
	V-Back Porch(*1)	Nvb	6	12	125	[lines]
	V-Front Porch	Nvf	1	1		[lines]
+DSPTMG	V-Line	m	1050	1050	1050	[lines]
+H-Sync	Scan Rate	Fh		63.98		[KHz]
		Th		15.63		[usec]
		Nh	762	844	1023	[Tck]
	H-Sync Width	Tha		1.037		[usec]
		Tha	8	56	250	[Tck]
	H-Back Porch	Thb	26	64	300	[Tck]
	H-Front Porch	Thf	8	24		[Tck]
+DSPTMG	Display	Thd		12.96		[usec]
		Nhd	700	700	700	[Tck]
+DATA	Data Even/Odd	n	1400	1400	1400	[dots]

Note:
- Both positive H-Sync and positive V-Sync polarity is recommended.
- V-Sync should static with active high (positive pulse) signal from when VPD is supplied and its polarity should not be changed.
- V-back porch (Nvb) period should be fixed between each V-Frame.
- The timing interval between V-Sync falling edge and H-Sync falling edge should be fixed between each V-Frame. (V-Sync and H-Sync polarity are assumed to be positive in this case.)

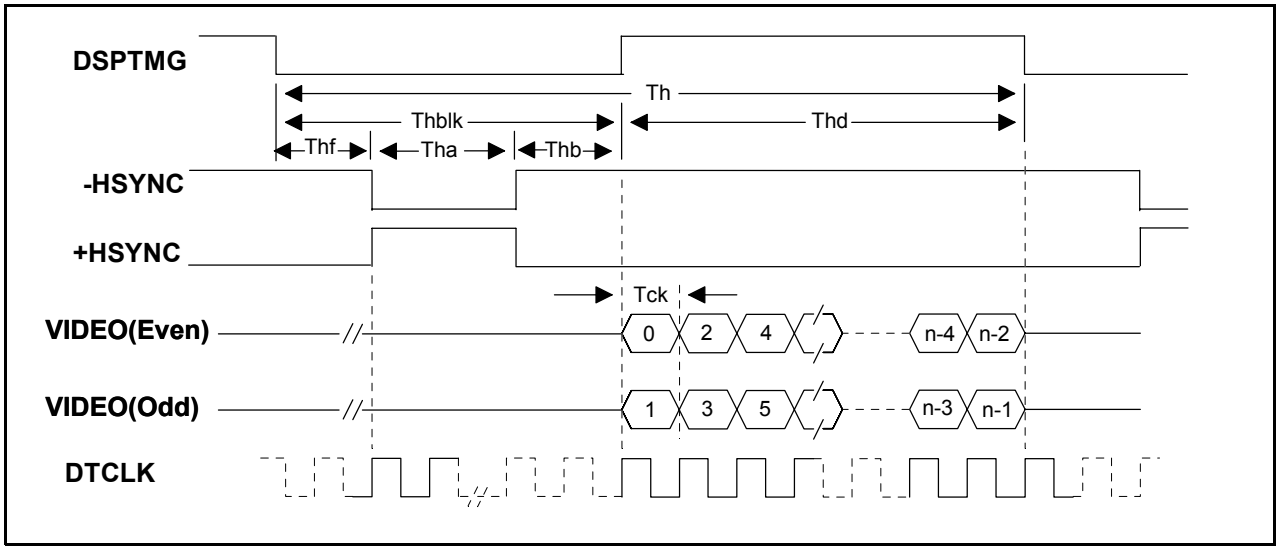
Vertical Timing

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1400 x 1050 at 60Hz (H line rate : 15.63 us)	0.250 ms (16 lines)	16.411 ms (1050 lines)	0.016 ms (1 line)	16.661 ms (1066 lines)	0.047 ms (3 lines)	0.188 ms (12 lines)



Horizontal Timing

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1400 x 1050 Dotclock : 108.000 MHz (54.000MHz x2)	2.667 us (288 dots)	12.963 us (1400 dots)	0.444 us (48 dots)	15.630 us (1688 dots)	1.037 us (112 dots)	1.185 us (128 dots)



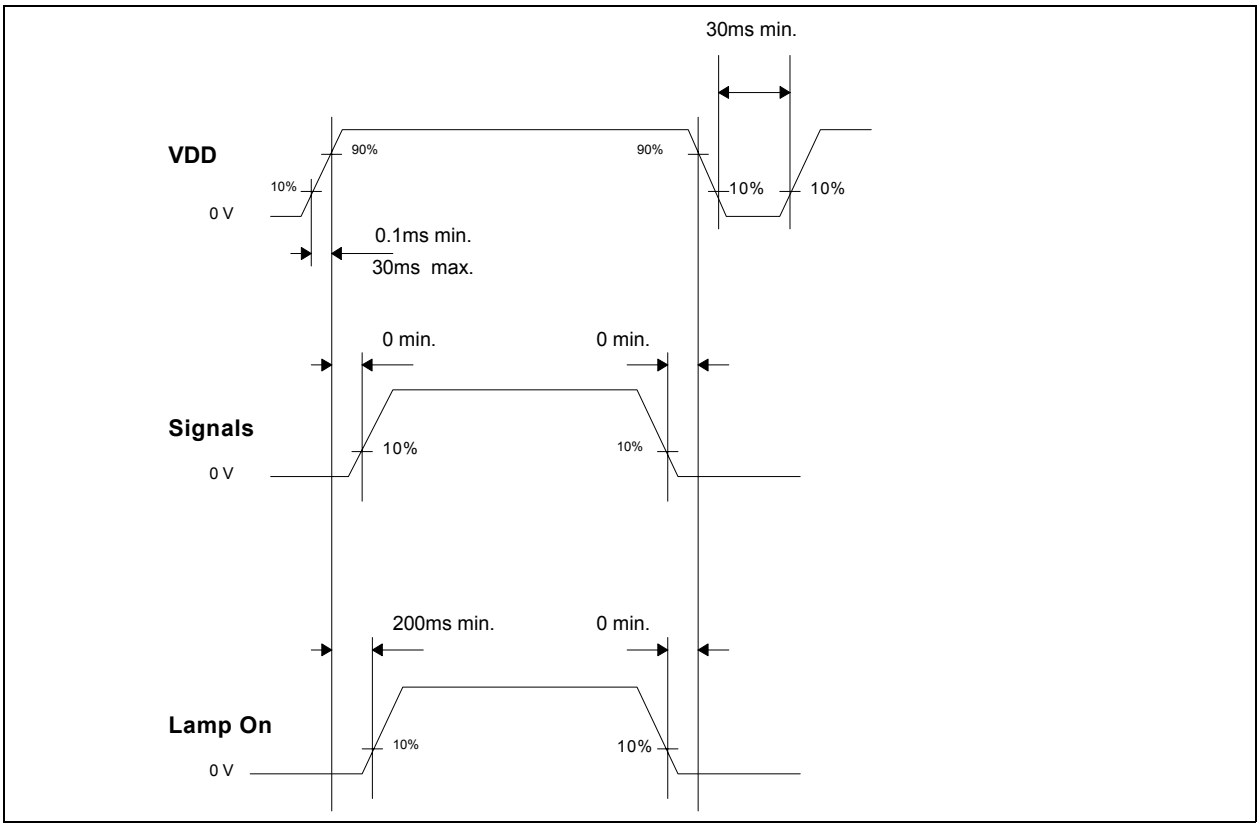
9.0 Power Consumption

Input power specifications are as follows;

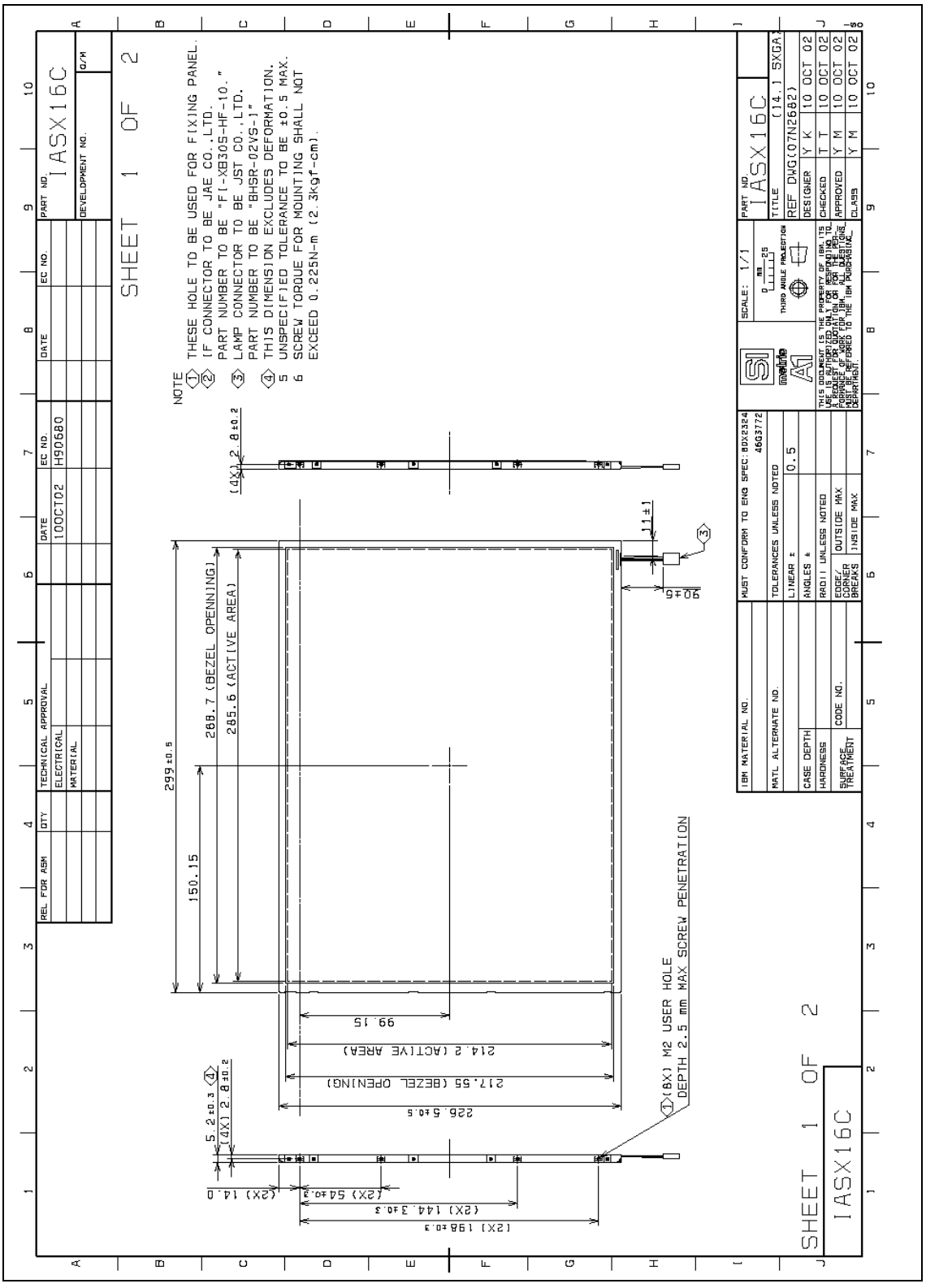
SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 20[uF]
PDD	VDD Power			3.1	[W]	Max. Pattern, VDD=3.6[V]
PDD	VDD Power		1.9		[W]	All Black Pattern, VDD=3.3[V]
IDD	VDD Current			940	[mA]	Max Pattern, VDD=3.3[V]
IDD	VDD Current		575		[mA]	All Black Pattern, VDD=3.3[V]
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	

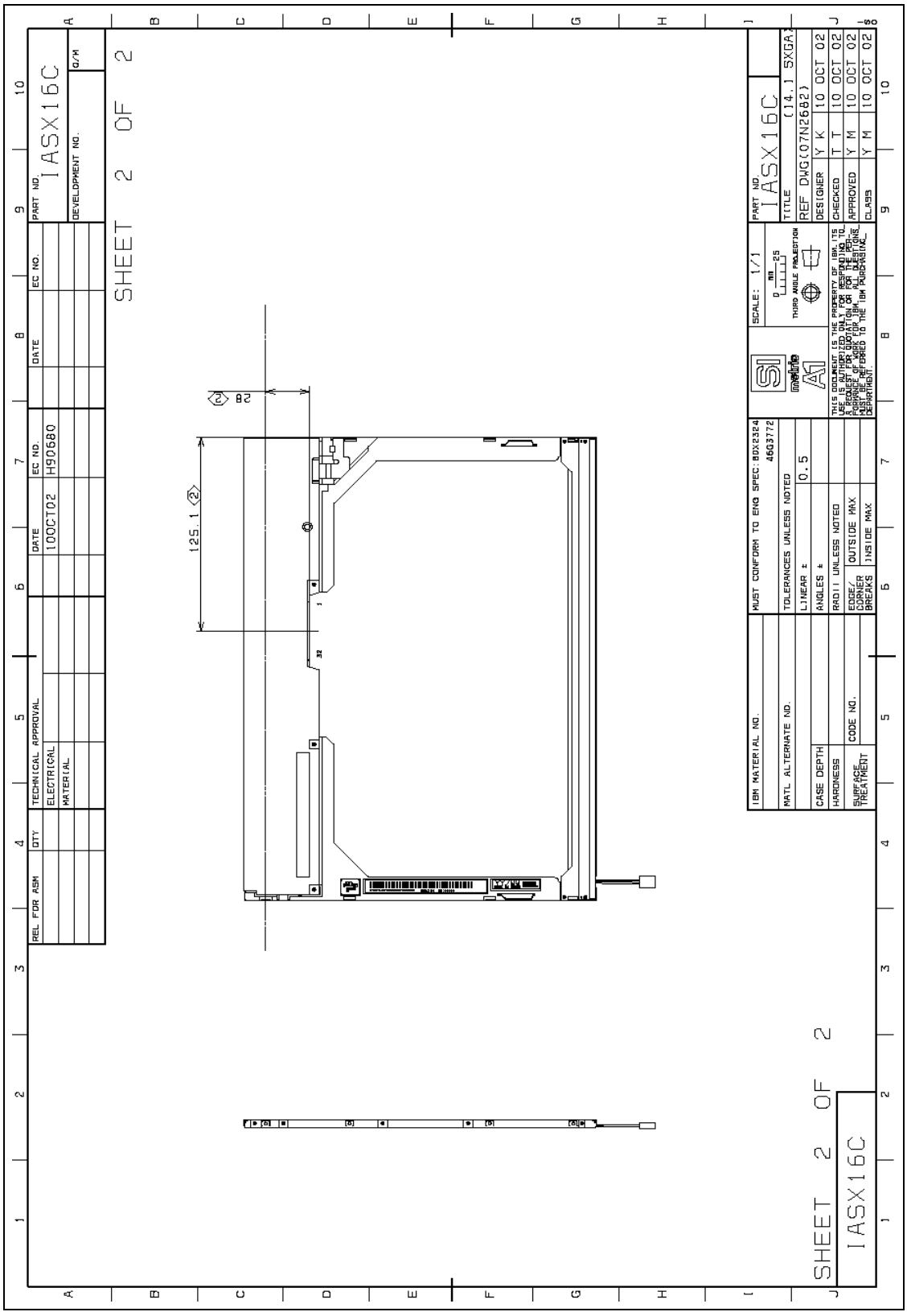
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics





12.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

Conditions of Acceptability - When installed in the end-product, consideration shall be given to the following;

1. This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, CSA/ UL60950, Third Edition, dated December 1, 2000, Sub-clause 2.10, which would cover the component itself if submitted for Listing.
2. The inverter output circuit is Limited Current Circuits.
3. The unit is intended to be supplied by SELV and Limited Power Source. Also separated from electrical parts, which may produce high temperature that could cause ignition by as least 13 mm of air or by a solid barrier of material of V-1 minimum.
4. The terminals and connectors are suitable for factory wiring only.
5. A suitable electrical enclosure shall be provided.

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