Engineering Specification

Type 19.6 UXGA Monochrome TFT/LCD Module
Model Name:IAUX61

Document Control Number : OEM I-961-01

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Sales Support
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
March 19,2003	OEM I-961-01	All	First Edition for customer. Based on Internal Spec as of January 16,2003.

1.0 Handling Precautions

- If any signal or power line deviates from the power on/off sequence, it may cause shortening the life of the LCD module and/or damage the electrical components. Also , hot plug-in operation may cause the similar damages as above.
- The LCD panel and CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may break or crack if dropped on a hand surface.Handling with care is necessary.
- The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be applied to exemption conditions of the flammability requirements (4.4.3.3, EN60950 or UL1950) in an end product.
- Please handle with care when mounted in the system cover. Mechanical damage for the lamp cable/ lamp connector may cause safety problems.
- After installation of the TFT Module into an enclosure (Monitor frame ,for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/ twisting forces are applied to the TFT Module from out side. Otherwise the TFT Module may be damaged.
- Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- Also, when removing a protection sheet from the module surface, please take some actions against static electricity, like earth band,ionic shower , etc.
- Since front polarizer is easily damaged, pay attention not to scratch it.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- Do not open nor modify the Module Assembly.
- Prevent continuous 10 hours or over same pattern displaying, to avoid image sticking.

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• The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the 49.8cm(19.6") Monochrome TFT/LCD Module ; IAUX61.

This module is designed for a display unit of a monitor application.

The screen format and electrical interface are intended to support the UXGA (1600(H) x 1200(V)) screen.

Supported color is 8-bit gray scale per XYZ-subpixels. All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.

2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS		SPECIFICATIONS
Screen Diagonal [mm]		498
Pixels H x V		1600 x 1200
Active Area [mm]		398.4(H) x 298.8(V)
Pixel Pitch [mm]		0.249 x 0.249
Pixel Arrangement		XYZ-Subpixels per one Pixel, Vertical Stripe
Weight [K grams]		2.30 Typ. 2.5Max
Physical Size [mm]		427.0(W) x 322.4(H) x 30.0 Typ. 41 (D) Typ. for Inverter Cover Area
Surface Treatment		Anti-glare / Hard-coating
Display Mode		Dual Domain IPS, Normally Black
Supported Color		XYZ 8-bit per each subpixel
White Luminance [cd/m^2]	Operation	500 Target 900 Max
	Maximum	1140 Typ.
Contrast Ratio		600 : 1 Typ.
Optical Rise Time/Fall Time [msec]		40 Typ.
White Point(x,y)		P45 (0.250,0.305)
Luminance Uniformity [%]		70 min
Viewing Angle [degree]		+/- 85 Typ. (Horizontal, Vertical)
Logic Input Voitage [V]		12.0 Typ. 11.4 Min 12.6 Max
Logic Power Consumption [W]		7.5 Max **(TBD)**
B/L Inverter Input Voltage [V]		12.0 Typ. 11.0 Min 12.6Max

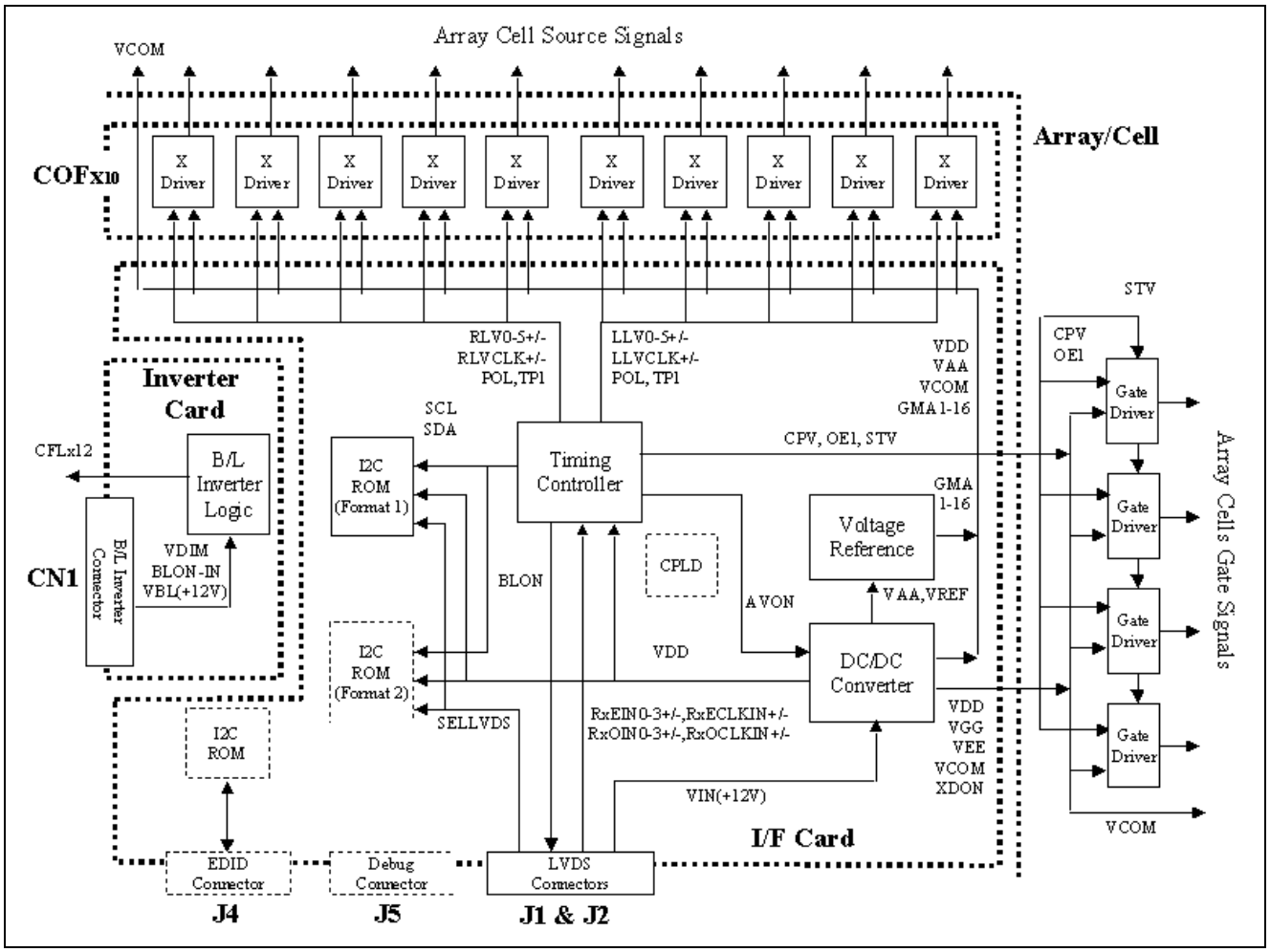
B/L Inverter Power Consumption [W]	50 MAX **(TBD)**
Electrical Interface	Dual LVDS
Operating Temperature [degree C]	0 to +50 **(*1)**
Storage Temperature [degree C]	-20 to +65
Humidity [%RH]	5 to 80 (Operating/Non-operating) Max wet bulb temp. 39deg.C, No condensation.
Lamp Quantity	12 Lamps
Lamp Life [hour]	50,000 (by Lamp Maker @ Ta=25degC) **(TBD)**
Module Backlight Life [hour]	30,000 (Backlight Unit replaceable) **(*2) (TBD)**

Note : (*1) Max. Operating Temperature 50 degree C in the Spec means the temperature measured at the point of the front surface of the LCD glass cell.

(*2) Can be replaced at IDT repair center.

2.2 Functional Block Diagram

The following diagram shows the functional block diagram for the IAUX61TFT-LCD Module.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VCC	-0.3	+17.6	V	
Backlight Voltage	VBL	-0.3	+17.6	V	
Brightness control	VDIM	-0.3	+5.3	V	
Backlight on signal	BLON	-1.0	+5.3	V	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Humidity	HOP	8	80	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	
Shock			50 11	G ms	Half sine wave

Note 1 : Max. Operating Temperature 50 degree C in the Spec means the temperature measured for the point of the front surface of the LCD glass cell.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item		Conditions	Specification	
			Typ.	Note
Viewing Angle (Degrees)		Horizontal (Right) K≥10 (Left)	85 85	-- -
K:Contrast Ratio		Vertical (Upper) K≥10 (Lower)	85 85	- -
Contrast ratio			600	-
Response Time (ms)		Rising+Falling	40	-
White Balance	IAUX61 P45	White x	0.250	-
		White y	0.305	-
Maximum White Luminance (cd/m^2)		VDIM-IN = 0V	1140	-
Minimum White Luminance (%)		VDIM-IN = 3.0V	10	20 Max.

Measure center of the screen.

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Signal Connectors

Connector	Function	Type	Manufacturer	Mating Connector
J1	I/F Connector-1	DF19G-20P-1H	HIROSE	DF19G-20S-1C DF19G-20S-1F
J2	I/F Connector-2	DF19G-20P-1H	HIROSE	DF19G-20S-1C DF19G-20S-1F
J3	(Not for customer)	FH12-20S0.5SH	HIROSE	
J4	(Optional)	SM05B-SRSS-TB	JST	05SR-3S
J5	(Not for customer)	SM03B-SRSS-TB	JST	03SR-3S

Backlight Connectors

Connector	Function	Connector Type	Manufacturer	Mating Connector
CN1	Inverter Input	B12B-PH-SM3-TB	JST	PHR-12

5.2 Interface Signal Connector

I/F Connector-1 Signals Pin Assignment (J1)

Pin #	Signal Name
1	VCC
2	VCC
3	GND
4	GND
5	RxEIN0-
6	RxEIN0+
7	GND
8	RxEIN1-
9	RxEIN1+
10	GND
11	RxEIN2-
12	RxEIN2+
13	GND
14	RxECLKIN-
15	RxECLKIN+
16	GND
17	RxEIN3-
18	RxEIN3+
19	GND
20	BLON

I/F Connector-2 Signals Pin Assignment (J2)

Pin #	Signal Name
1	VCC
2	VCC
3	GND
4	GND
5	RxOIN0-
6	RxOIN0+
7	GND
8	RxOIN1-
9	RxOIN1+
10	GND
11	RxOIN2-
12	RxOIN2+
13	GND
14	RxOCLKIN-
15	RxOCLKIN+
16	GND
17	RxOIN3-
18	RxOIN3+
19	GND
20	(N.C.)

Inverter Input Connector Signals Pin Assignment (CN1)

Pin #	Signal Name
1	VBL
2	VBL
3	VBL
4	VBL
5	VBL
6	GND
7	GND
8	GND
9	GND
10	GND
11	VDIM
12	BLON-IN

5.3 Interface Signal Description

The module uses a pair of LVDS receiver macro which is equivalent to THC63LVDF84A/R84A(THine Electronics, Inc.). LVDS is a differential signal transfer technology for LCD interface and high speed data transfer device. Transmitter shall be THC63LVDF83A/M83A(THine Electronics, Inc.) or equivalent.

Signal Description for J1,J2 and CN1

SIGNAL NAME	Description
VCC	+12V Power Supply for Logic
GND	Ground
RxEIN0-	Negative LVDS data 0 input for even pixel
RxEIN0+	Positive LVDS data 0 input for even pixel
RxEIN1-	Negative LVDS data 1 input for even pixel
RxEIN1+	Positive LVDS data 1 input for even pixel
RxEIN2-	Negative LVDS data 2 input for even pixel
RxEIN2+	Positive LVDS data 2 input for even pixel
RxEIN3-	Negative LVDS data 3 input for even pixel
RxEIN3+	Positive LVDS data 3 input for even pixel
RxECLKIN-	Negative LVDS clock input for even pixel
RxECLKIN+	Positive LVDS clock input for even pixel
RxOIN0-	Negative LVDS data 0 input for odd pixel
RxOIN0+	Positive LVDS data 0 input for odd pixel
RxOIN1-	Negative LVDS data 1 input for odd pixel
RxOIN1+	Positive LVDS data 1 input for odd pixel
RxOIN2-	Negative LVDS data 2 input for odd pixel
RxOIN2+	Positive LVDS data 2 input for odd pixel
RxOIN3-	Negative LVDS data 3 input for odd pixel
RxOIN3+	Positive LVDS data 3 input for odd pixel
RxOCLKIN-	Negative LVDS clock input for odd pixel
RxOCLKIN+	Positive LVDS clock input for odd pixel
BLON	Back-Light ON signal output. This signal turns high at XXX ms after VCC applied. 3.3V CMOS output.
VBL	+12V Power Supply for Back-Light Inverter
VDIM	Back-Light Dimension Control Input VDIM=0V, the brightness is maximum. VDIM=3.0V, the brightness is minimum. VDIM is set over 3.1V, Inverter protection logic works. This protection is cleared by Inverter power off.
BLON-IN	Back-Light ON signal input. High level input makes Back-Light On. 3.3V CMOS Input.

5.4 Interface Signal Electrical Characteristics

Each signal characteristics are as follows;

Electrical Characteristics

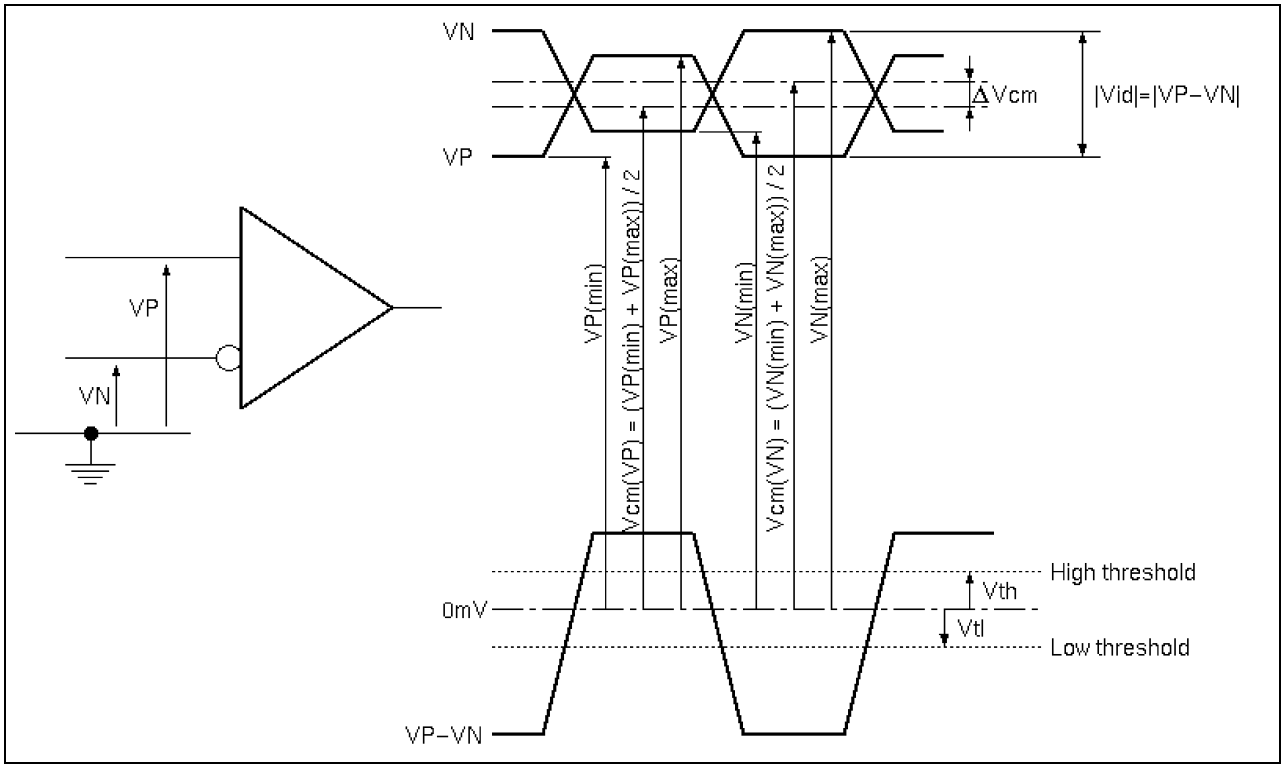
Parameter	Symbol	Min	Max	unit	Conditions
Differential Input High Threshold	Vth		+100	[mV]	Vcm=+1.2[V]
Differential Input Low Threshold	Vtl	-100		[mV]	Vcm=+1.2[V]
Magnitude Differential Input Voltage	|Vid|	100	600	[mV]	
Common Mode Input Voltage	Vic	$0.825+\frac{\|Vid\|}{2}$	$2.0-\frac{\|Vid\|}{2}$	[V]	Vth-Vtl=200[mV]
Common Mode Voltage Offset	ΔVcm	-50	+50	[mV]	Vth-Vtl=200[mV]

Note: 1. Input signals shall be low or Hi-Z state when VCC is off.

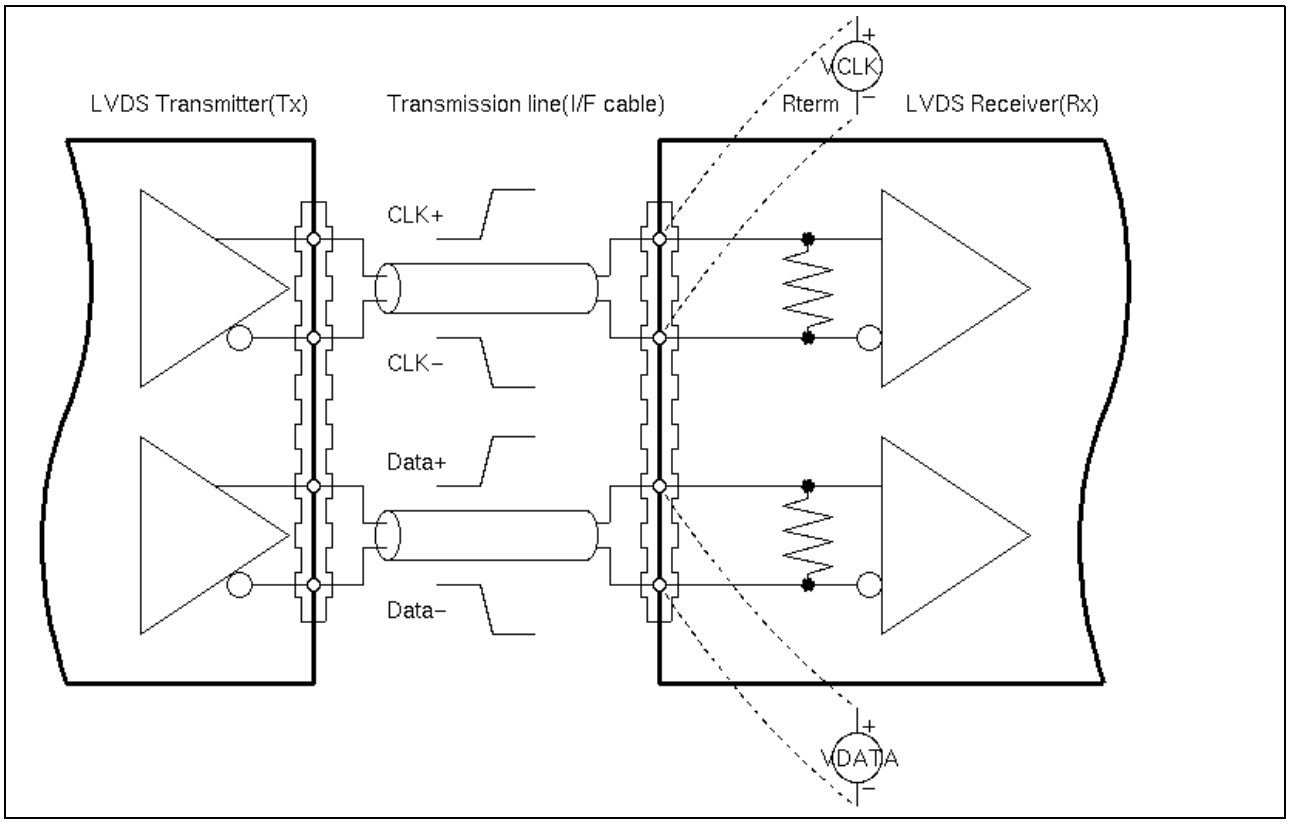
2. All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see Figure Measurement system) .

3. There is a 100-ohm resister between positive and negative lines of each LVDS signal input.

Voltage Definitions



Measurement system



LVDS Receiver AC Characteristics

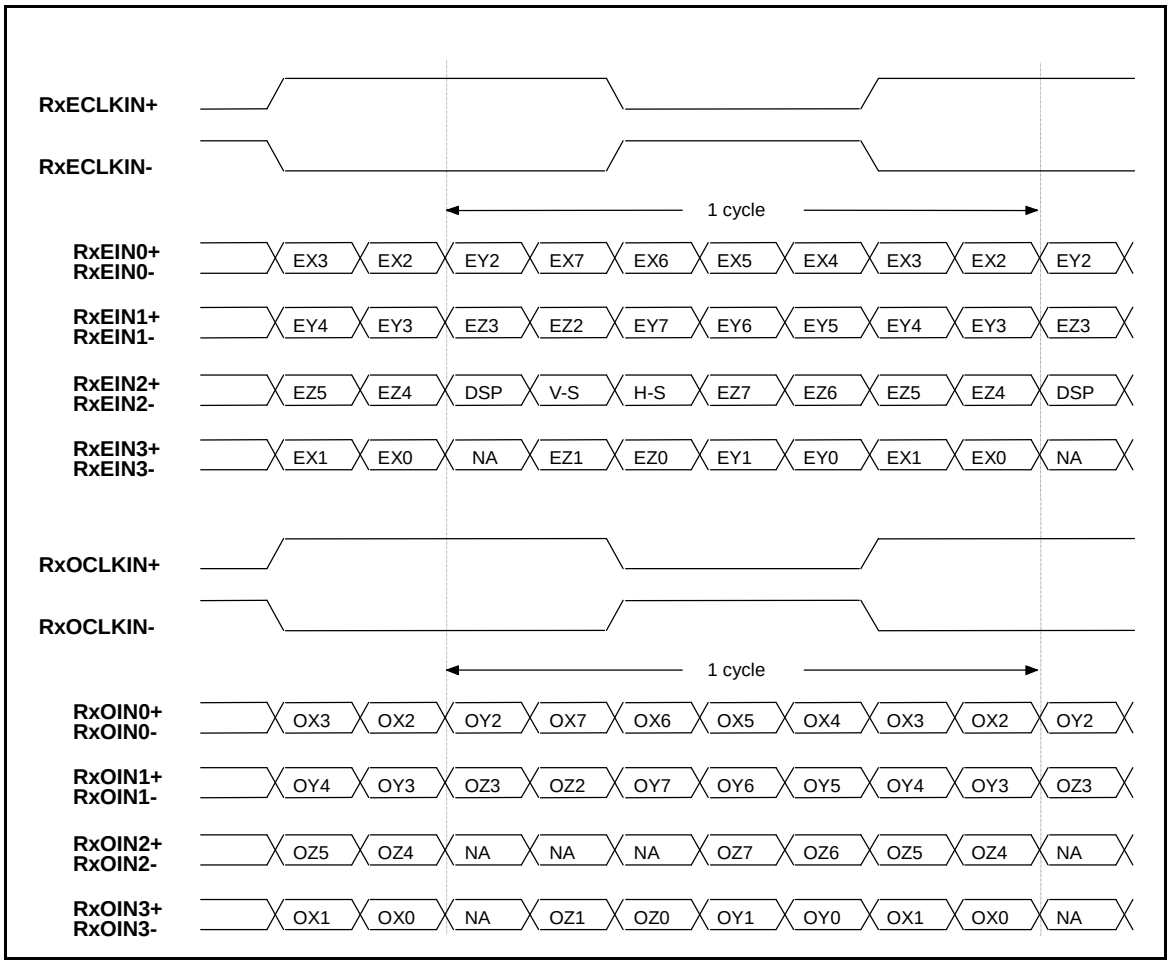
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	76.9	81.0	85.1	[MHz]	
Cycle Time	tc	11.7	12.3	13.0	[ns]	
Data Setup Time (*2)	Tsu	500 TBD			[ps]	fc = 81.0[MHz], tCCJ < 50[ps], Vth-Vtl=200[mV], Vcm=1.2[V], ∆Vcm=0[V]
Data Hold Time (*2)	Thd	500 TBD			[ps]	
Cycle-to-cycle jitter (*3)	TCCJ	-150 TBD		+150 TBD	[ps]	
Cycle Modulation Rate (*4)	tCJavg			20 TBD	[ps/clk]	

Note:

1. All values are at VCC=12.0[V], Ta=25[C deg.].
2. See figure "LVDS Format" and "Detail Timing Definition" for definition.
3. Jitter is the magnitude of the change in input clock period.
4. This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. Figure "Cycle Modulation Rate" illustrates a case against this requirement. This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

LVDS per each channel becomes as below. Each channel has Hsync (H-S), Vsync (V-S) and DSPTMG (DSP).

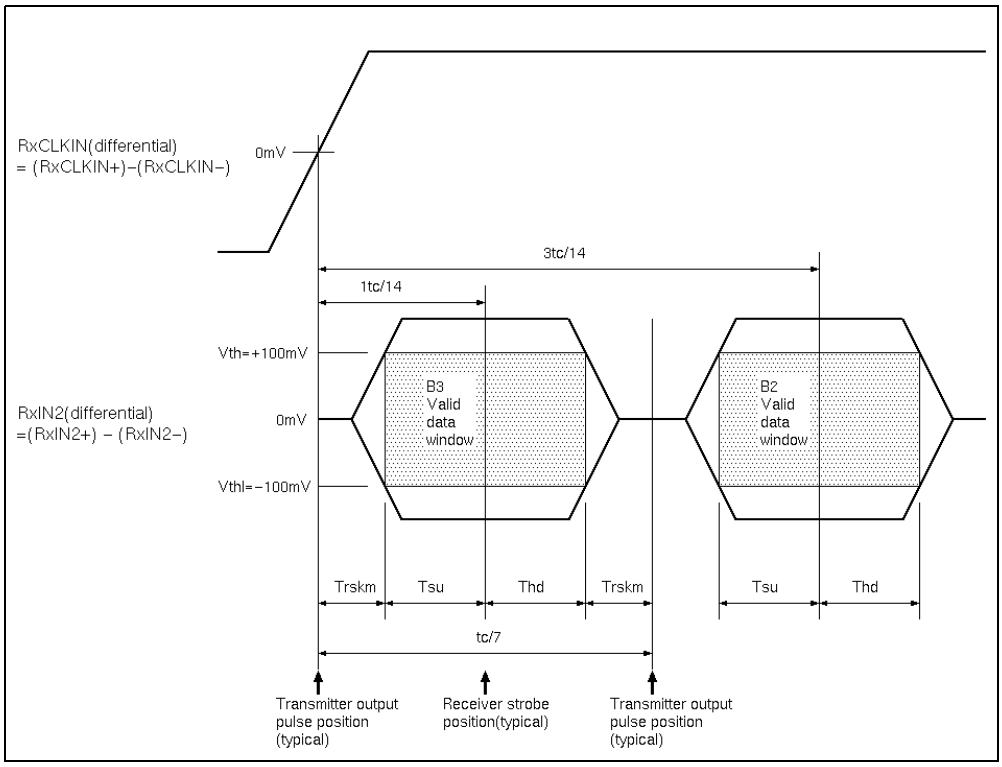
LVDS Format



Note: X/Y/Z data 7: MSB, X/Y/Z data 0: LSB, DSP = DSPTMG, V-S = Vsync, H-S = Hsync

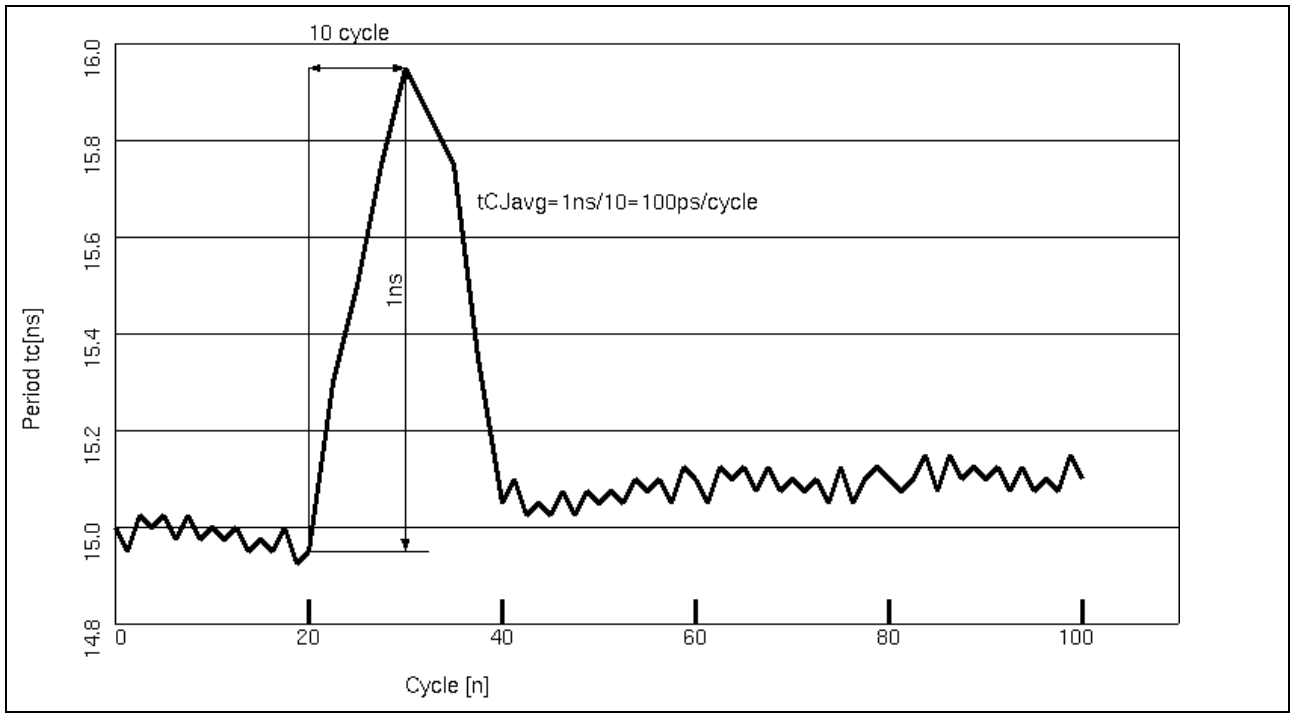
LVDS transmitter/receiver are Thine THC63LVD823/Texas Instruments TFP7x5 (1 chip each).

Detail Timing Definition



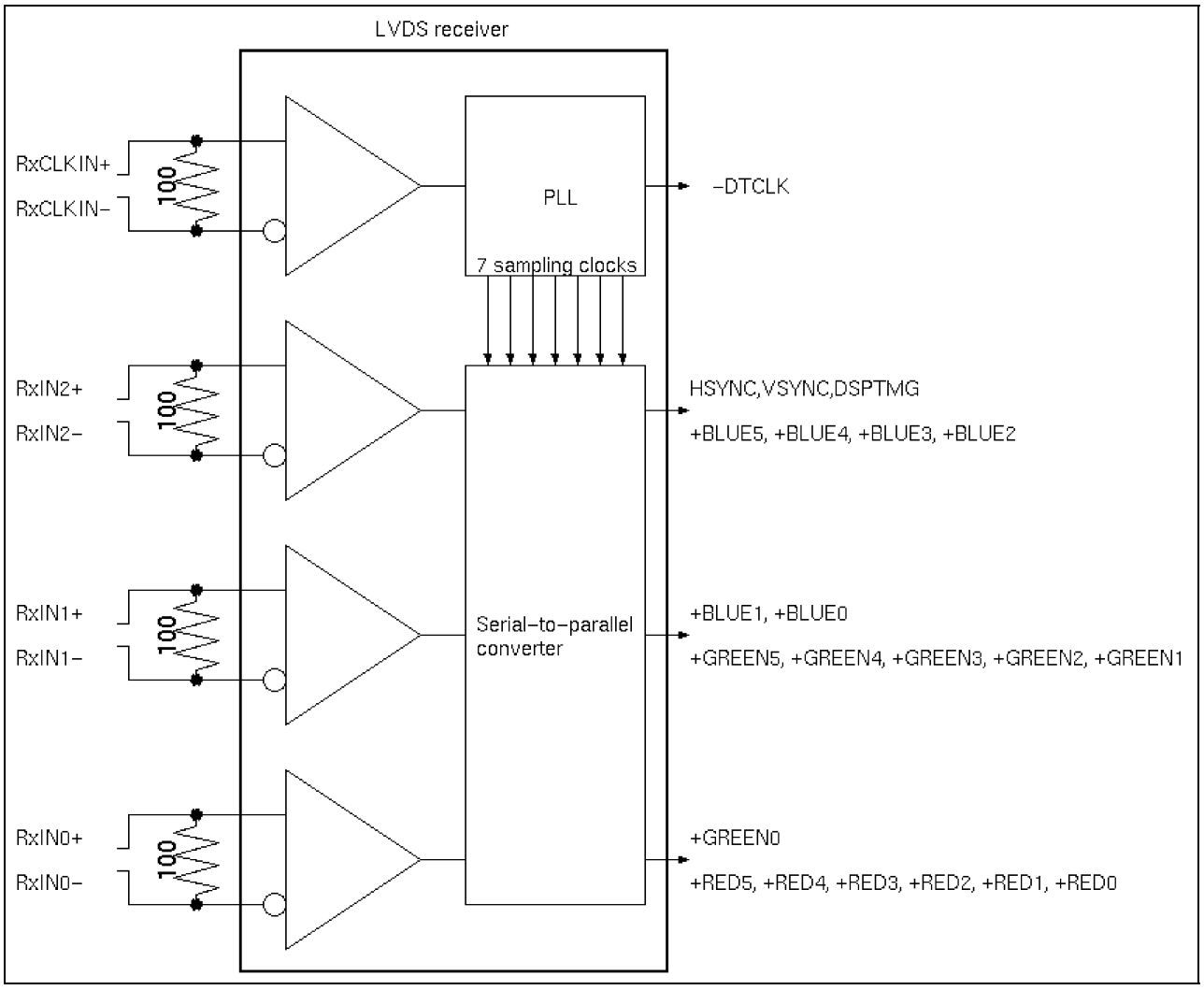
Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

Cycle Modulation Rate



5.4 1 LVDS Receiver Inverter Circuit

Internal circuit of LVDS inputs are as follows.



The module uses a 100ohm resistor between positive and negative lines of each LVDS signal input.

5.4.2 Recommended Guidelines for Motherboard PCB Design and Cable Selection

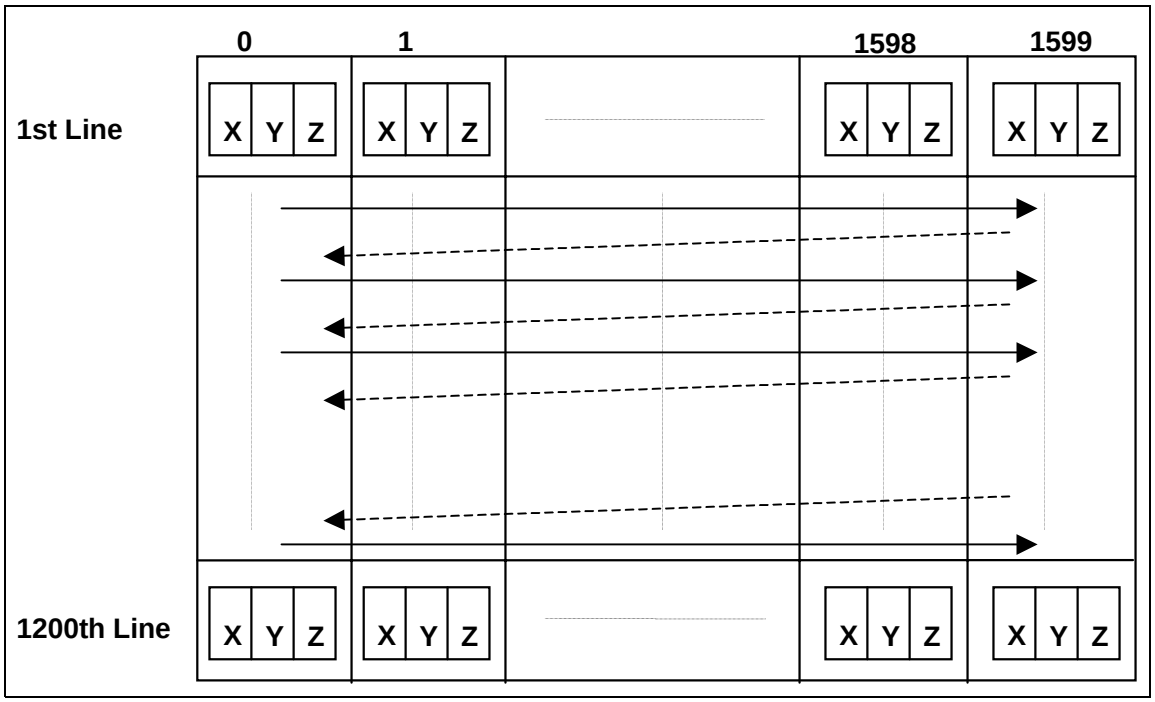
Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.

6.0 Pixel format image

Following figure shows the relationship between the input signals and the LCD pixel format image.
IAUX61 has a LVDS interface.Following figure shows the relationship of the input signals and LCD pixel format image.

Screen Format



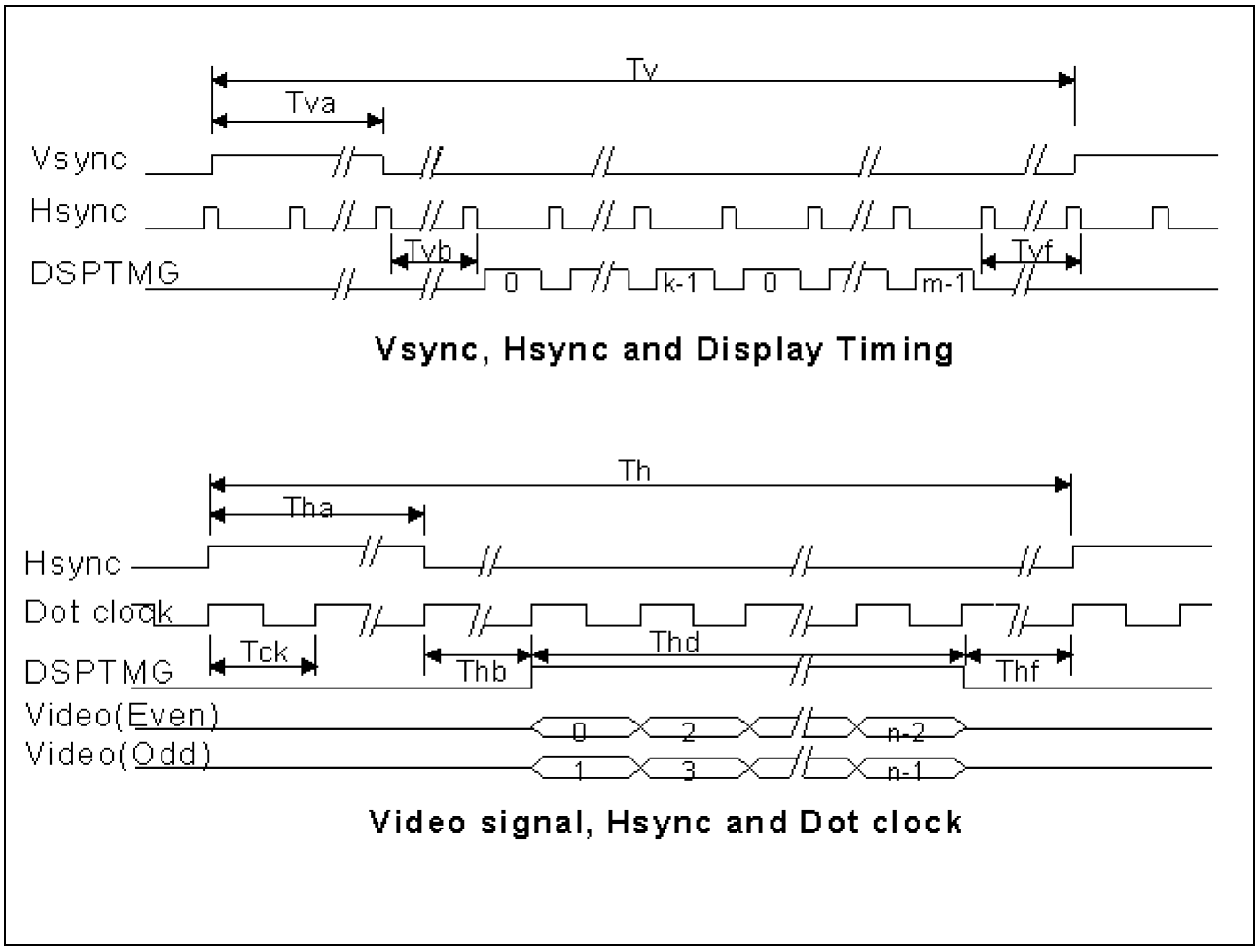
7.0 Interface Timings

Following is the Video timing per channel to be converted to/from LVDS interface .

7.1 Timing Characteristics

EVEN for LVDS-LE or LVDS-RE
ODD for LVDS-LO or LVDS-RO.

Interface Timing Definition



NOTE:

1. The sensor lines exist on top of screen, and it is recommended for this area to be filled with the same image of 1st line of actual displayed except for calibration time. And also these lines need DSPTMG.
2. Even dot for 1st dot, Odd dot for 2nd dot.

Timing Characteristics

Signal	Item	Symbol	Min.	Typ.	Max.	Unit
DTCLK	Dot Clock Freq.	Fdck	76.9	81.0	85.1	[MHz]
DTCLK	Dot Clock period	Tck	11.7	12.35	13.0	[ns]
+V-Sync	Refresh Rate	1/Tv		60		[Hz]
+V-Sync	Frame period	Tv		16.67		[ms]
+V-Sync	Total line	Tv		1250	1440	[lines]
+V-Sync	V-front porch	Tvf	1	1		[lines]
+V-Sync	V-active level	Tva	1	3		[lines]
+V-Sync	V-back porch	Tvb	28	46	200	[lines]
+V-Sync	V-Blank	Tvf+Tva+Tvb	30	50	240	[lines]
+DSPTMG	Display Lines / frame	k+m		1200		[lines]
+H-Sync	H-Scan Rate	1/Th		75.0		[kHz]
+H-Sync	H-Scan Rate	Th		13.3		[us]
+H-Sync	H-total period	n+Thf+Tha+Thb Th		1080	1130	[tck]
+H-Sync	H-front porch	Thf	16	32		[tck]
+H-Sync	H-active level	Tha	48	96		[tck]
+H-Sync	H-back porch	Thb	76	152		[tck]
+H-Sync	H-Blank	Thf+Tha+Thb	140	280		[tck]
+DSPTMG	Display Pixels	n		800		[pixels]

Note:

1. H/V sync Polarity will be acceptable both positive and negative. DSPTMG (Data Enable) should be Active High.
2. Vsync should not be changed at Hsync leading edge (+/- 6 [tck]). **(TBD)**
3. Even Dot clock and Odd Dot clock in each channel should have completely the same clock source. The skew should be within +/- 1.5 [ns]. **(TBD).**
4. All timing among channels should be synchronized (Vsync, Hsync, DSPTMG, video and clocks) and the skew of Vsync etc. among channels should be **within +/- 1 Tck (TBD)**.
5. All channels should be activated any time after Power On (because it does not have Auto Refresh protection.)

8.0 Power Consumption

Input power specifications are as follows;

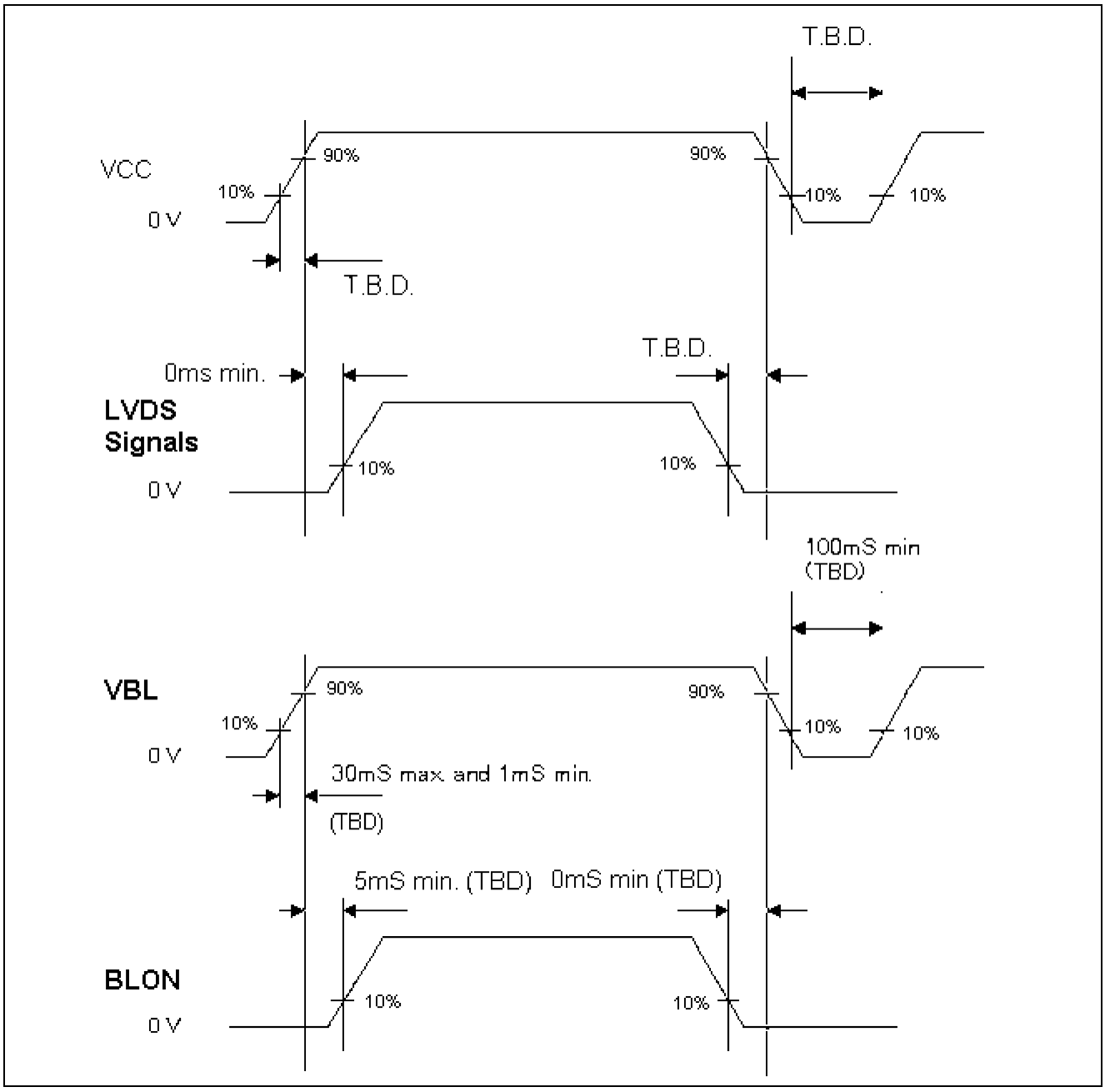
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNITS	CONDITION
VCC	Logic/LCD Drive Voltage	11.4	12.0	12.6	[V]	
Iin	Vcc Current	**TBD**	TBD	**TBD**	[A]	VCC=12.0[V]
Pin	Vcc Power	**TBD**	**TBD (*1)**	7.5 **(TBD) (*2)**	[W]	VCC=12.0[V]
VCC rp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	
VCC ns	Allowable Logic/LCD Drive Ripple Noise			100	[mVp-p]	
VBL	Backlight Power Voltage	11.0	12.0	12.6	[V]	
IBL	VBL Current	TBD	**TBD**	**TBD**	[A]	2 minutes after power ON
		TBD	**TBD**	**TBD**	[A]	30 minutes after Power ON
PBL	Backlight Power Consumption(*3)		TBD**)**	**50 (TBD)**	[W]	VBL=12.0[V] Max. bright.
			TBD	**TBD**	[W]	VBL=12.0[V] Min. bright.
				TBD	[W]	VBL=12.0[V] Stand-by
VBL rp	Allowable Backlight Drive Ripple Voltage			100	[mVp-p]	
VBL ns	Allowable Backlight Drive Ripple Noise			100	[mVp-p]	

Note (*1): = Vertical Gray Bar (Left =black, Right = White), (*2): Sub Pixel Checker
(*3): Measurement after CCFL luminance saturation. (minimum 60 minutes.)

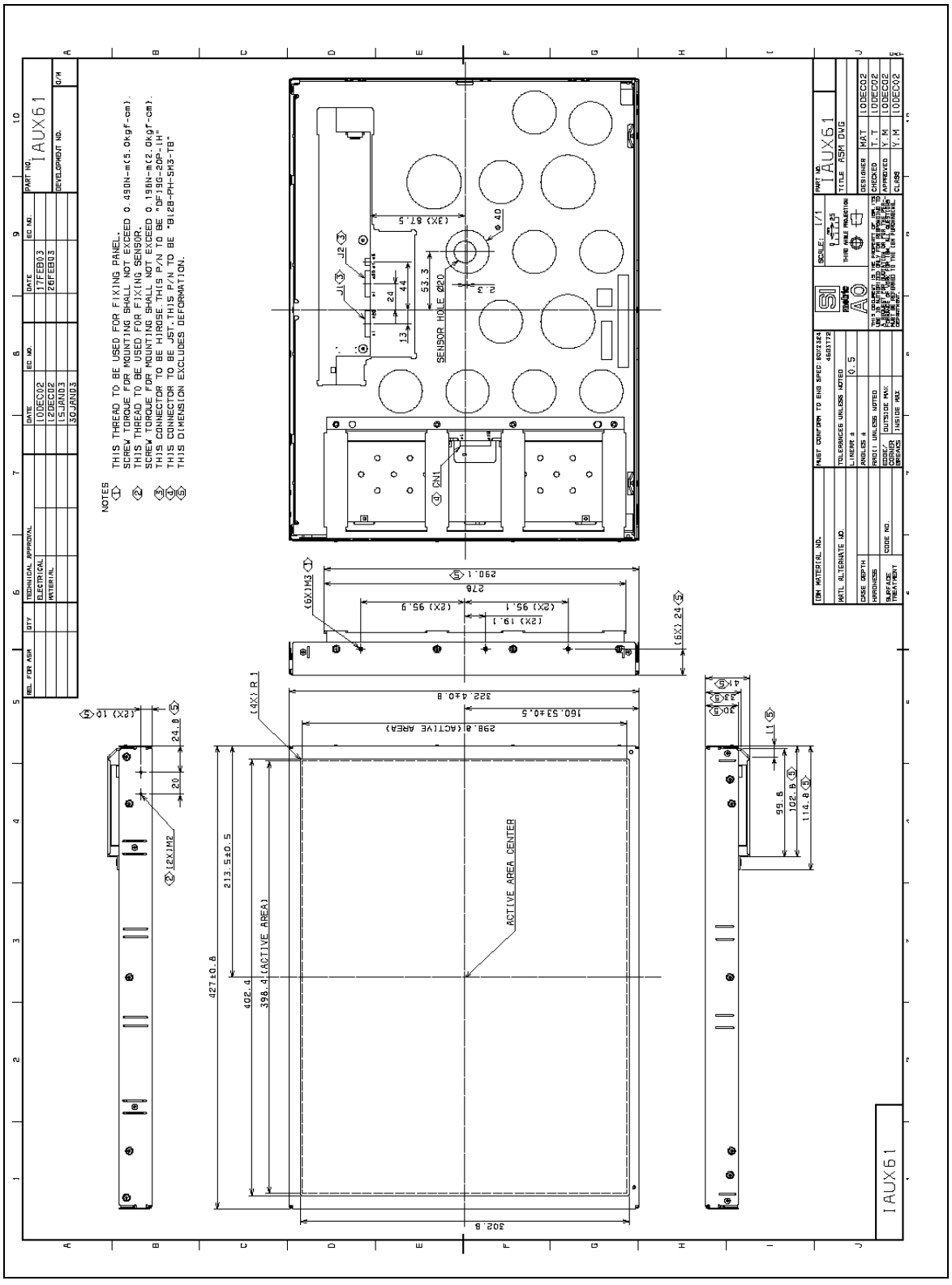
9.0 Power ON/OFF Sequence

VCC power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VCC is off.

Signals from any system shall be Hi-Z state or low level when VCC is off.



10.0 Mechanical Characteristics



11.0 National Test Lab Requirement

The LCD module will comply with the the following requirements when housed in a suitable enclosure.

UL 60950, 3rd Edition	U.S.A. Information Technology Equipment
CAN/CSA-C22.2 No.60950-00	Canada, Information Technology Equipment
IEC 60950 (3rd Ed.)	International, Information Technology Equipment
EN 60950 (3rd Ed.)	International, Information Technology Equipment (European Norm for IEC 60950)

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