TO: Apple Computer Inc.

Accepted By: Date:

Customer's Acceptance Specification

Type 20.12 WSXGA+ Color TFT/LCD Module
Model Name:IAWS64C

Document Control Number: CAS I-964C-A01

Issued By: T. Tokuda **Date: August 25,2003**

Sales Support
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
June 17,2003	CAS I-964C-A01 (Preliminary)	All	Preliminary Edition for Apple Computer Inc.
August 25, 2003	CAS I-964C-A01	All	First Edition for Apple Computer Inc.

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1.0 Handling Precautions

- If any signal or power line deviates from the power on/off sequence, it may cause shortening the life of the LCD module and/or damage the electrical components. Also, hot plug-in operation may cause the similar damages as above.
- The LCD panel and the CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may break or crack if dropped on a hard surface. Handling with care is necessary.
- The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be applied to exemption conditions of the flammability requirements (4.4.3.3, EN60950 or UL1950) in an end product.
- Please handle with care when mounted in the system cover. Mechanical damage for the lamp cable / lamp connector may cause safety problems.
- After installation of the TFT Module into an enclosure (Monitor frame, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/ twisting forces are applied to the TFT Module from out side. Otherwise the TFT Module may be damaged.
- Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- Also, when removing a protection sheet from the module surface, please take some actions against static electricity, like earth band, ionic shower, etc.
- Since front polarizer is easily damaged, pay attention not to scratch it.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- Do not open nor modify the Module Assembly.
- Prevent continuous 10 hours or over same pattern displaying, to avoid image sticking.

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2.0 General Description

This specification applies to the Type 20.12 Color TFT/LCD Module 'IAWS64C'.

This module is designed for a display unit of a monitor application.

The screen format and electrical interface are intended to support the WSXGA+ (1680(H) x 1050(V)) screen.

Supported color is native 24bit colors (8-bit per RGB-sub pixels data driver).

All input signals are TMDS (Transition Minimized Differential Signaling) interface compatible.

This module does not contains an inverter card for backlight.

2.1 Characteristics

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [cm]	51.11 (16:10)
Pixels	1680(H) x 1050(V)
Active Area [mm]	433.44(H) x 270.90(V)
Pixel Pitch [mm]	0.258 x 0.258
Pixel Arrangement	RGB-sub pixels per one Pixel, Vertical Stripe
Weight [K grams]	3.25 Typ., 3.40 Max.
Physical Size [mm]	486.2(W) x 307.0(H) x 24.8 Typ./ 25.3 Max. (D)
Surface Treatment	Low Refrection (<80 G.U.), Anti-glare, Hard-Coating (3H)
Display Mode	Dual Domain IPS, Normally Black
Supported Color	Native 24bit colors (RGB 8-bits per each sub pixel)
White Luminance [cd/m^2] (5 Points Average)	240 Typ., 205 Min. (ICFL = 6.0[mA])
Contrast Ratio	350:1 Typ. 250:1 Min. (In the Dark room)
Optical Rise Time+Fall Time [msec]	25 Typ., 40 Max.
Input Voltage [V]	+18 +5/-5% (Logic)
Power Consumption [W]	Logic 5.1 Typ., Backlight 32 Typ.
Electrical Interface	Single Link TMDS (Clock Freq.:117.13 [MHz])
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 **(Note)** -20 to +65

Note: Max. Operating Temperature 50 deg.C in the spec means the temperature measured at the point of the front surface of the LCD glass cell.

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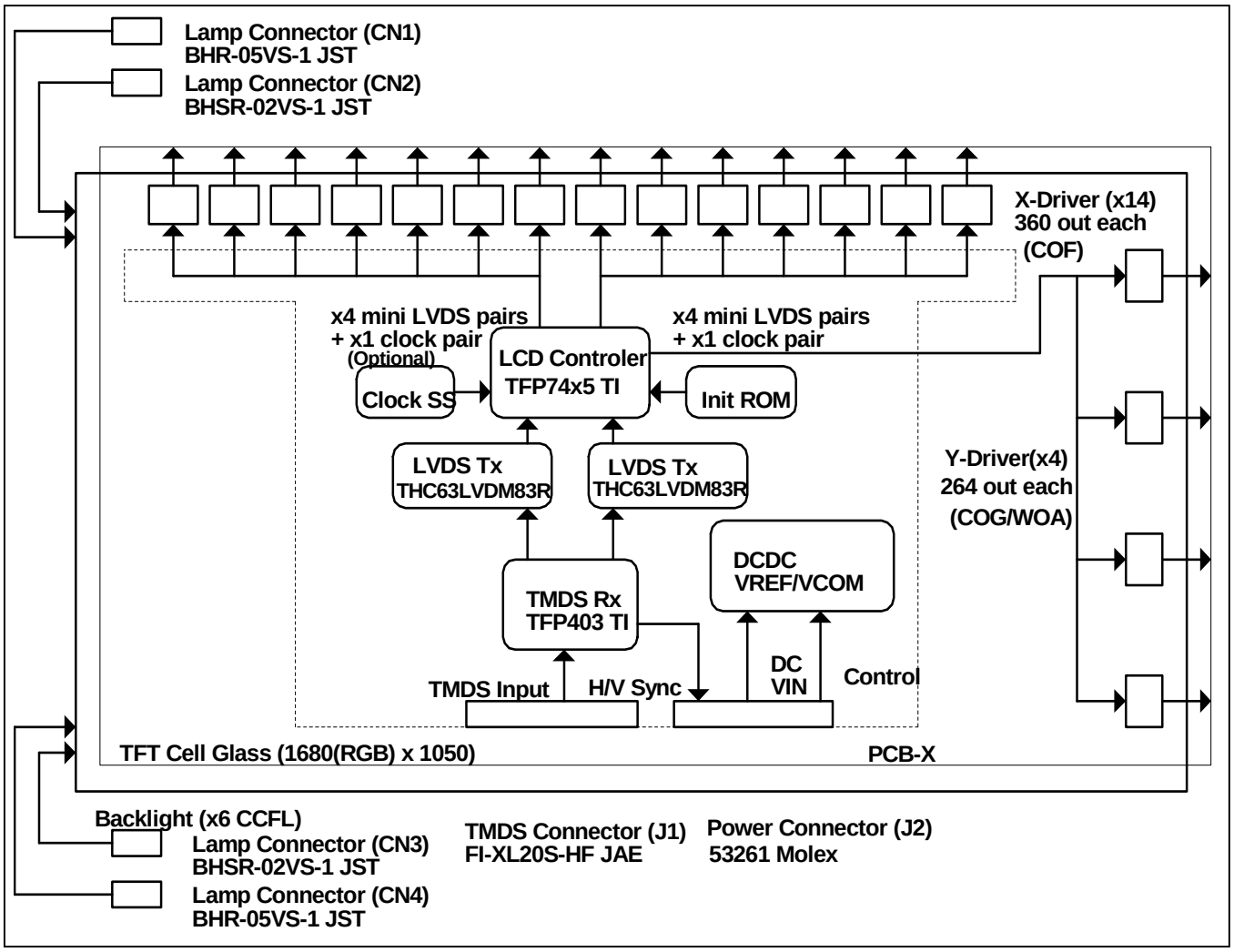
2.2 Functional Block Diagram

The following diagram shows the functional block diagram for the Type 20.12 Color TFT/LCD Module.



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3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module are as follows;

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vcc	-0.3	+21.0	V	
Input Voltage of Signal		-0.3	+4.0	V	(TMDS pins)
Input Voltage of Signal		-0.3	+5.3	V	(PWR_CTRL)
Input Signal Current		-75	75	mA	(TMDS pins)
CFL Ignition Voltage	Vinv	-	2,000	Vrms	**(Note 1)**
CFL Current	ICFL	-	7.0	mArms	
CFL Peak Current	ICFLP	-	20	mArms	**(Note 1)**
Operating Temperature	TOP	0	+50	deg.C	**(Note 2)**
Operating Relative Humidity	HOP	8	80	%RH	**(Note 2)**
Storage Temperature	TST	-20	+65	deg.C	**(Note 2)**
Storage Relative Humidity	HST	5	95	%RH	**(Note 2)**
Vibration			1.5 10-200	G Hz	**(Note 3)**
Shock			50 11	G ms	Half sine wave **(Note 3)**

Note:

1. Duration : 50[mS] Max.
2. Maximum Wet-Bulb should be 39 degree C and No condensation. Max. Operating Temperature 50 deg. C in the spec means the temperature measured for the point of the front surface of the LCD glass cell.
3. Vibration Specification
   - Sine Vibration:10-200-10Hz, 1.5G, 30 min, X, Y, Z Axis, Each One Time.

   Shock Specification
   - Half sine wave:50G 11msec. -X+/-, -Y+/-, -Z+/- (Total 6 directions), Each one time Shock.

3.1 Component Temperature

The table below shows the maximum component temperature specifications.

Maximum Component Temperature

Component	Maximum Temperature Specifications [deg. C]
X-Driver	100
Gate Array	85
TMDS Receiver	94

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4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K: Contrast Ratio	Horizontal (Right) K≧10 (Left)	85 85	- -
	Vertical (Upper) K≧10 (Lower)	85 85	- -
Contrast ratio		350	250 Min.
Response Time (ms)	Rising	13	20 Max.
	Falling	13	20 Max.
	Rising + Falling	25	40 Max.
Color Chromaticity (CIE)	Red x	0.640	±0.030
	Red y	0.330	±0.030
	Green x	0.290	±0.030
	Green y	0.600	±0.030
	Blue x	0.150	±0.030
	Blue y	0.060	±0.030
	White x	0.313	±0.030
	White y	0.329	±0.030
White Luminance (cd/m^2)	ICFL = 6.0 [mA]	240 (5 Points Average)	205 Min. (5 Points Average)
White point tracking (K)	L64 - L255	Less than 600 **(TBD)**	-

Gamma Corrected Gray Scale

Following table shows the luminance for each gray level for reference.

Luminance of the Gray Level

i (gray level)	**L(i) [%]**		
	Min.	Typ.	Max.
L0	-	0.28	0.4
L31	0.6	1.00	1.4
L63	2.5	4.70	7.0
L95	6.5	11.4	17.0
L127	14.0	21.7	30.0
L159	27.0	36.1	48.0
L191	42.0	53.0	67.0
L223	62.0	73.4	86.0
L255	100.0	100.0	100.0

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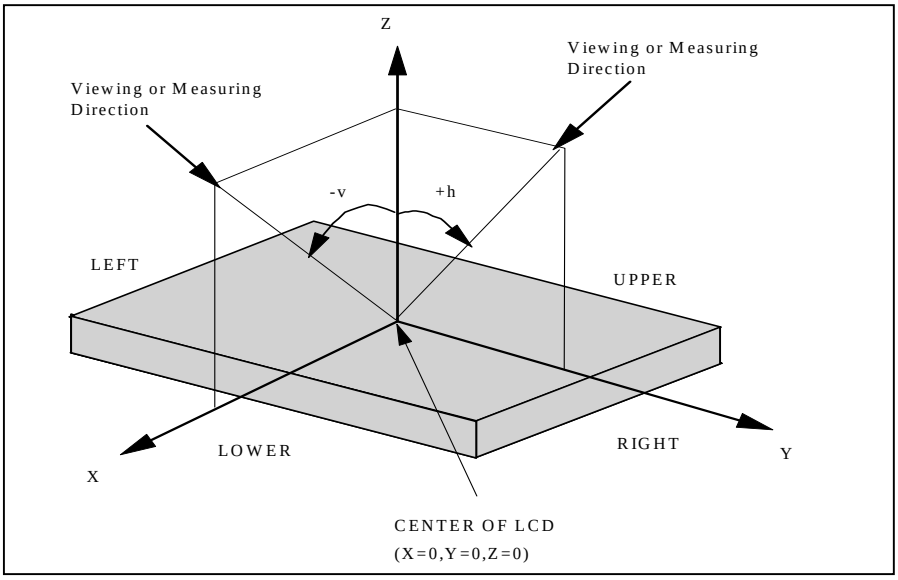
The following is the note for the Optical Characteristics:



- Chromaticity and White Balance are defined as the C.I.E. 1931 x,y coordinates at the center of LCD.The Standard Equipment are as shown below table.

Item	Standard Equipment
Viewing Angle	MCPD-7000 by Ohtsuka Elec
Contrast	MCPD-7000 by Ohtsuka Elec
Response Time	BM5A by TOPCON OPTICAL Co.,Ltd.
White Luminance	MCPD-7000 by Ohtsuka Elec
Luminance Uniformity	MCPD-7000 by Ohtsuka Elec
Chromaticity	MCPD-7000 by Ohtsuka Elec
White Balance	MCPD-7000 by Ohtsuka Elec

The measurement is to be done after 60 minutes of Power-on of BackLight.

Unless otherwise specified, the ambient conditions are as following.

Ambient Temperature	:	25 + 2	(degreeC)
Ambient Humidity	:	25 - 85	(%)
Atmospheric Pressure	:	86.0 - 104.0	(kPa)

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4.1 Luminance Uniformity

When the backlight is on with all the pels in the white (maximum gray) level, the luminance uniformity is defined as follows;

Where:

L_{bright} : The luminance of the brightest data from $L_{(p1)}$ to $L_{(p13)}$.

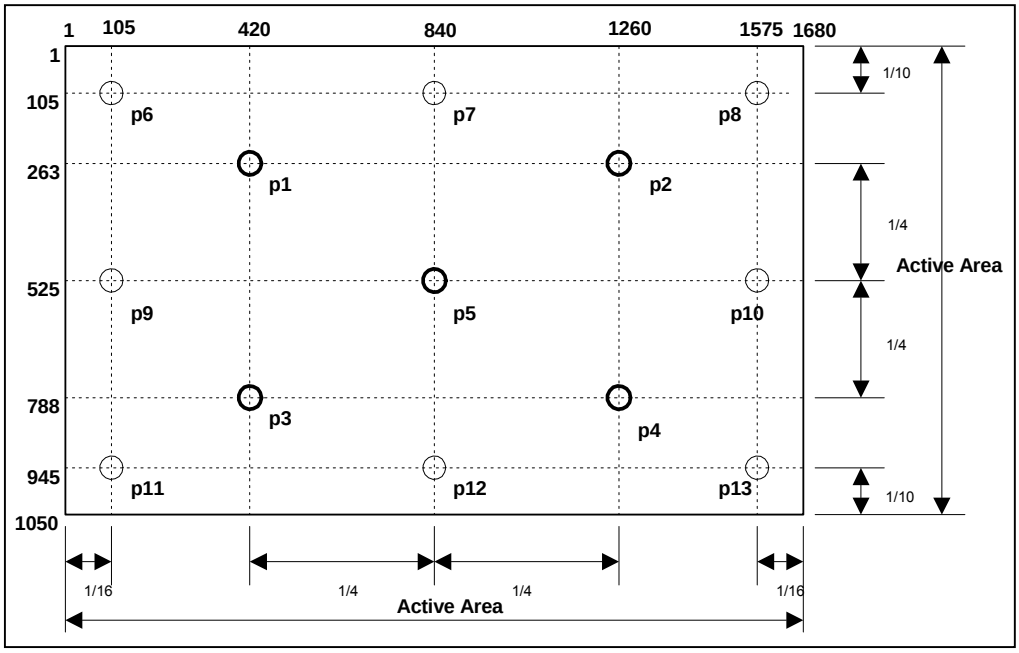
L_{dark} : The luminance of the darkest data from $L_{(p1)}$ to $L_{(p13)}$.

$L_{average}$: The average luminance of all data form $L_{(p1)}$ to $L_{(p13)}$.

$$L_{average} = \frac{L_{(p1)} + L_{(p2)} + L_{(p3)} + L_{(p4)} + L_{(p5)} + L_{(p6)} + L_{(p7)} + L_{(p8)} + L_{(p9)} + L_{(p10)} + L_{(p11)} + L_{(p12)} + L_{(p13)}}{13}$$

$$\text{Luminance Uniformity} = \frac{L_{bright} - L_{dark}}{L_{average}} X100 < 30\ [\%]$$

Optical Measurement Point for Luminance Uniformity (5points/13points)



The luminance data from $L_{(p1)}$ to $L_{(p5)}$ are used for the White luminance Measurement.

The luminance data from $L_{(p1)}$ to $L_{(p13)}$ are used ofr the Luminance Variation Measurement.

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5.0 Signal Interface

Physical interface is described in accordance with the connectors on the LCD module.

These connectors are capable of accommodating the following signals and will be the following components or IDT approved types.

5.1 Connectors

All video signals are provided through the TMDS cable from Monitor Card. These connectors are the input connector of video signals. The TMDS signals, which are provided from monitor card, are described on the following table.

Signal Connectors

Connector	Function	Type	Manufacturer	Mating Connector
J1	TMDS Connector	FI-XL20S-HF	JAE	
J2	Power Connector	53261-1510	Molex	

Lamp Connectors

Connector	Function	Connector Type	Manufacturer	Mating Connector
CN1	Lamp Connector (Upper1)	BHR-05VS-1	JST	SM04 (9-E2)B-BHS-1
CN2	Lamp Connector (Upper2)	BHSR-02VS-1	JST	SM02B-BHSS-1
CN3	Lamp Connector (Lower1)	BHSR-02VS-1	JST	SM02B-BHSS-1
CN4	Lamp Connector (Lower2)	BHR-05VS-1	JST	SM04(9-E2)B-BHS-1

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5.2 Interface Signal Connector

TMDS Connector Signals Pin Assignment (J1)

Pin #	Signal Name
1	GND
2	GND
3	GND
4	GND
5	SHLD2
6	TX2+
7	TX2-
8	SHLD1
9	TX1+
10	TX1-
11	SHLD0
12	TX0+
13	TX0-
14	SHLDC
15	TXC+
16	TXC-
17	GND
18	GND
19	GND
20	GND

Voltage levels of all input signals are TMDS compatible in this connector, J1.

Power Connector Signals Pin Assignment (J2)

Pin #	Signal Name
1	GND
2	Reserved
3	PWR_CTRL
4	GND
5	Vcc
6	Vcc
7	Vcc
8	Vcc
9	GND
10	NC
11	NC
12	GND
13	HS_OUT
14	VS_OUT
15	GND

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Lamp Connectors Pin Assignment (CN1)

Pin #	Signal Name	CFL Position **(Note)**	Voltage	Wire Color
1	Lamp High	HIGH	HV	PINK
2	Lamp High	MID	HV	BLUE
3				
4	Lamp Low	HIGH	LV	YELLOW
5	Lamp Low	MID	LV	ORANGE

Lamp Connectors Pin Assignment (CN2)

Pin #	Signal Name	CFL Position **(Note)**	Voltage	Wire Color
1	Lamp High	LOW	HV	GRAY
2	Lamp Low	LOW	LV	WHITE

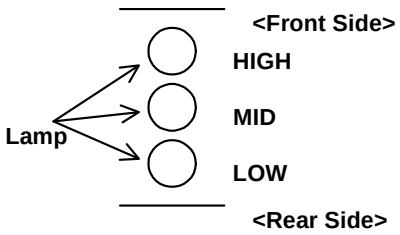
Lamp Connectors Pin Assignment (CN3)

Pin #	Signal Name	CFL Position **(Note)**	Voltage	Wire Color
1	Lamp High	LOW	HV	GRAY
2	Lamp Low	LOW	LV	WHITE

Lamp Connectors Pin Assignment (CN4)

Pin #	Signal Name	CFL Position **(Note)**	Voltage	Wire Color
1	Lamp High	HIGH	HV	PINK
2	Lamp High	MID	HV	BLUE
3				
4	Lamp Low	HIGH	LV	YELLOW
5	Lamp Low	MID	LV	ORANGE

Note: CFL Position is defined as follows.



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5.3 Interface Signal Description

TMDS Connector Signal Description (J1)

SIGNAL NAME	Description
TX0+	TMDS positive differential Input (Channel 0)
TX0-	TMDS negative differential Input (Channel 0)
TX1+	TMDS positive differential Input (Channel 1)
TX1-	TMDS negative differential Input (Channel 1)
TX2+	TMDS positive differential Input (Channel 2)
TX2-	TMDS negative differential Input (Channel 2)
TXC+	TMDS positive differential Input (Channel C)
TXC-	TMDS negative differential Input (Channel C)
SHLD0	Shield for TMDS channel 0
SHLD1	Shield for TMDS channel 1
SHLD2	Shield for TMDS channel 2
SHLDC	Shield for TMDS channel C
GND	Ground

Power Connector Signal Description (J2)

SIGNAL NAME	Description
Vcc	+18V Power Supply
GND	Ground
PWR_CTRL	LCD Module Power Control Signal Input **(Note)**
HS_OUT	Hsync Output
VS_OUT	Vsync Output
Reserved	No Connect LCD panel internal use

Note: PWR_CTRL is used to control the power to the LCD drivers.

The actual control circuit is on the LCD module.

Lamp Connector Signal Description (CN1, CN2, CN3,CN4)

SIGNAL NAME	Description
Lamp High	Lamp Electrode at High Voltage Side
Lamp Low	Lamp Electrode at Low Voltage Side

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Signal Description

SIGNAL NAME	Description
+Red7 (QE23, QO23)	Red Sub Pixel Data 7 (MSB)
+Red6 (QE22, QO22)	Red Sub Pixel Data 6
+Red5 (QE21, QO21)	Red Sub Pixel Data 5
+Red4 (QE20, QO20)	Red Sub Pixel Data 4
+Red3 (QE19, QO19)	Red Sub Pixel Data 3
+Red2 (QE18, QO18)	Red Sub Pixel Data 2
+Red1 (QE17, QO17)	Red Sub Pixel Data 1
+Red0 (QE16, QO16)	Red Sub Pixel Data 0 (LSB)
	Red Sub Pixel Data: Each Red Sub pixel's brightness data consists of these 8 bits pixel data.
+Green7 (QE15, QO15)	Green Sub Pixel Data 7 (MSB)
+Green6 (QE14, QO14)	Green Sub Pixel Data 6
+Green5 (QE13, QO13)	Green Sub Pixel Data 5
+Green4 (QE12, QO12)	Green Sub Pixel Data 4
+Green3 (QE11, QO11)	Green Sub Pixel Data 3
+Green2 (QE10, QO10)	Green Sub Pixel Data 2
+Green1 (QE9, QO9)	Green Sub Pixel Data 1
+Green0 (QE8, QO8)	Green Sub Pixel Data 0 (LSB)
	Green Sub Pixel Data: Each Green Sub pixel's brightness data consists of these 8 bits pixel data.
+Blue7 (QE7, QO7)	Blue Sub Pixel Data 7 (MSB)
+Blue6 (QE6, QO6)	Blue Sub Pixel Data 6
+Blue5 (QE5, QO5)	Blue Sub Pixel Data 5
+Blue4 (QE4, QO4)	Blue Sub Pixel Data 4
+Blue3 (QE3, QO3)	Blue Sub Pixel Data 3
+Blue2 (QE2, QO2)	Blue Sub Pixel Data 2
+Blue1 (QE1, QO1)	Blue Sub Pixel Data 1
+Blue0 (QE0, QO0)	Blue Sub Pixel Data 0 (LSB)
	Blue Sub Pixel Data: Each Blue Sub pixel's brightness data consists of these 8 bits pixel data.
DTCLK	Data Clock: The typical frequency is 117.13MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.

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5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for TMDS Receiver

Please refer to TI TFP403 datasheet (SLDS 125 December 2000)10

5.4.2 Recommended Guidelines for Motherboard PCB Design and Cable Selection

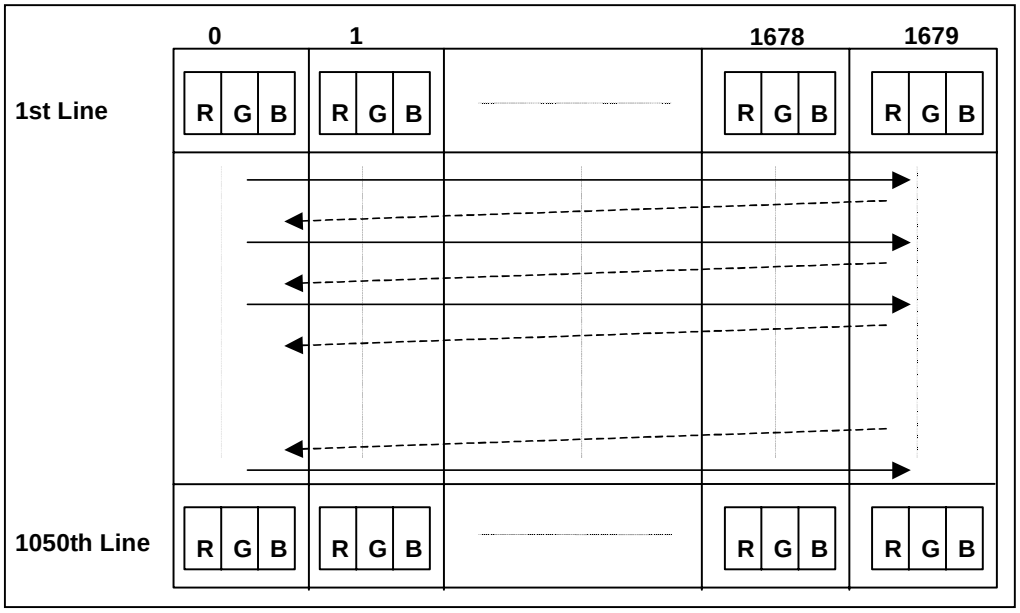
Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for TMDS signals.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from TMDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

6.0 Pixel format image

Following figure shows the relationship between the input signals and the LCD pixel format image.
IAWS64C has a TMDS interface. Following figure shows the relationship of the input signals and LCD pixel format image.

Screen Format



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7.0 Interface Timings

7.1 Timing Characteristics

Timing Characteristics

Signal	Item	Symbol	Min.	Typ.	Max.	Unit
DTCLK	Dot Clock Freq.	Fdck	111.0	117.13	124.0	[MHz] +/- 5%
DTCLK	Dot Clock period	Tck	8.06	8.54	9.01	[ns]
+V-Sync	Refresh Rate	1/Tv		59.94		[Hz]
+V-Sync	Frame period	Tv		16.68		[ms]
+V-Sync	Total line	Tv		1062	1305	[lines]
+V-Sync	V-front porch	Tvf	1	3		[lines]
+V-Sync	V-active level	Tva	1	3		[lines]
+V-Sync	V-back porch	Tvb	6	6	127	[lines]
+V-Sync	V-Blank	Tvf+Tva+Tvb	8	12	255	[lines]
+DSPTMG	Display Lines / frame	m	-	1050	-	[lines]
+H-Sync	H-Scan Rate	1/Th		63.7		[kHz]
+H-Sync	H-Scan Rate	Th		15.71		[us]
+H-Sync	Cycle	Th		1840	2048	[tck]
+H-Sync	H-front porch	Thf	64	64		[tck]
+H-Sync	H-active level	Tha	8	32		[tck]
+H-Sync	H-back porch	Thb	8	64		[tck]
+H-Sync	H-Blank	Thf+Tha+Thb	80	160		[tck]
+DSPTMG	Display clocks	Thd	-	1680	-	[tck]
+DSPTMG	Display Pixels	n	-	1680	-	[pixels]

Note:

1. H/V sync Polarity will be acceptable both positive and negative. DSPTMG (Data Enable) should be Active High.
2. Vsync should not be changed at Hsync leading edge (+/- 6 [tck]).
3. All channels should be activated any time after Power On (because it does not have Auto Refresh protection).

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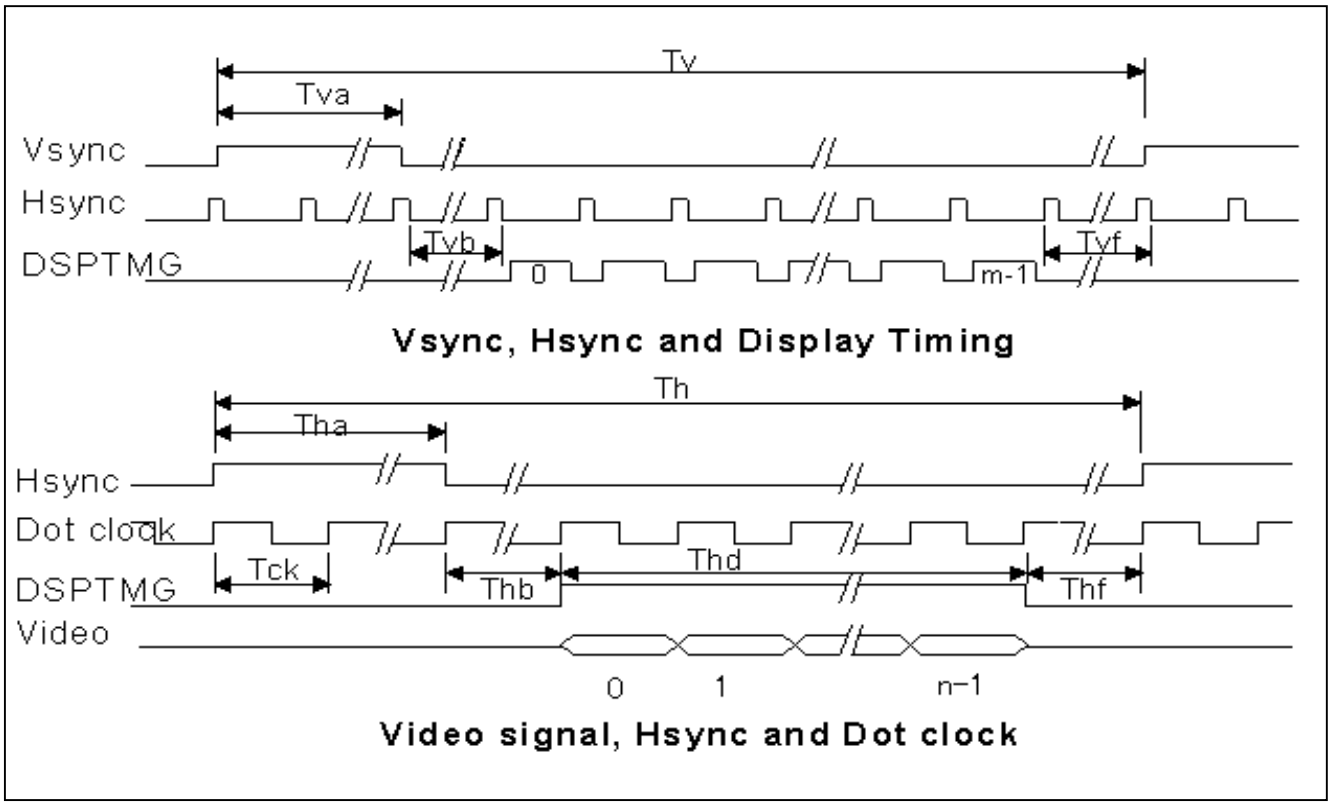
Following is the Video timing per channel to be converted to/from TMDS interface.



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8.0 Power Supply Requirement

8.1 Logic / LCD Power Requirement

8.1.1 Logic / LCD Power Specification

Power Characteristics

SYMBOL	PARAMETER	Min.	Typ.	Max.	UNITS	CONDITION
Vcc	Logic/LCD Drive Voltage	17.0	18.0	19.0	[V]	
Pin (1)	Vcc Power (1)		5.1		[W]	Vcc=18.0[V] Horizontally Gray Bar
Pin (2)	Vcc Power (2)			7.3	[W]	Vcc=17.0[V]~19.0[V] Horizontally-Sub-Pixel/ Vertically-Double-Pixel Checker
Pin (3)	Vcc Stand By Power			0.5	[W]	Vcc=17.0[V]~19.0[V] PWR CTRL=Inactive. No TMDS input.
Icc	Vcc Current			0.43	[A]	Vcc=17.0[V]~19.0[V] Horizontally-Sub-Pixel/ Vertically-Double-Pixel Checker
Icc (p)	Vcc Peak Current			1.4	[A]	Vcc=17.0[V]~19.0[V] **(Note)**
Vcc rp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	
Vcc ns	Allowable Logic/LCD Drive Ripple Noise			100	[mVp-p]	

Note:

Horizontally-Sub-Pixel/Vertically-Double-Pixel Checker

Each "Vcc" and "GND" are connected through quad 100[mm] length AWG28 wires to DC source.

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8.1.2 Input Low Voltage Detection

IAWS64C power supply circuit is equipped with low voltage detection mechanism to avoid the LCD module from operating in abnormal condition.
Threshold voltage of the low voltage detection mechanism is a function of time duration of voltage drop. The following table shows several condition of allowable dip voltage and duration.

Input voltage dip condition

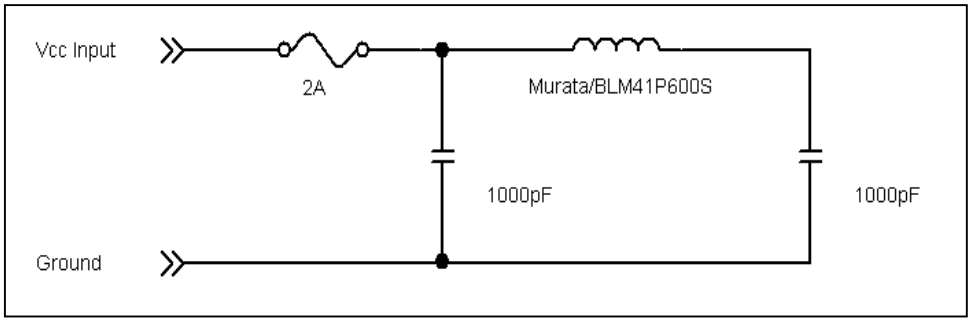
Voltage dip (Bottom of dip) [V]	Maximum Allowable Duration
17.0V	Infinity
16.0V	100 [uS]
15.0V	0 [S]

8.1.3 Inrush Current

Inrush condition occurs;

1. At Vcc starting time if the Vcc voltage is turned on by very high speed switching device. This inrush current is resulted from an EMI reduction filter circuit equipped at the Vcc input stage in the LCD module and DC source characteristics including the wiring characteristics. Please refer to Figure shown below for equivalent circuit of the Vcc input stage. Magnitude and waveform of the peak current depends on the combination of the characteristics of the Vcc input stage and Vcc source characteristics. Evaluating the inrush current/voltage waveform with the actual sample is recommended.
2. Approximately 800uS after Vcc comes active, maximum of 3A inrush peak current occurs for charging DC/DC converters input bulk capacitor. Peak current of this inrush current is controlled by slow-turn-on device equipped in the LCD module.
3. When PWR_CTRL signal comes active, maximum of 3A inrush current occurs.

Equvalent circuit of Vcc Input stage for initial inrush condition



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8.2 CFL Specification

8.2.1 CFL Characteristics

Symbol	Parameter	Min.	Max.	Units	Conditions
ICFL	CFL Current	2.0	6.5	[mArms]	Ta=25 [deg. C] **(Note 1)**
FCFL	CFL Frequency	35	80	[kHz]	Ta=25 [deg. C] **(Note 2)**
Vinv	CFL Ignition Voltage	-	1350	[Vrms]	Ta=25 [deg. C]
		-	1650	[Vrms]	Ta=0 [deg. C]

Note:

1. CFL current exceeds Min./Max. values, then "CFL life", "ON/OFF Cycle" and "Safety" will not be guaranted.
2. CFL frequency should be carefully determined to avoid interference between inverter and TFT LCD.

8.2.2 Inverter Design Point

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
(L255)	White Luminance (5 Points Average)	205	240	-	[cd/m^2]	Ta=25 [deg. C]
ICFL	CFL Current **(Note 5)**	2.0	6.0	6.5	[mArms]	Ta=25 [deg. C] **(Note 1)**
ICFLP	CFL Peak Inrush Current			20	[mA]	Ta=25 [deg. C] **(Note 1, 6)**
FCFL	CFL Frequency	35		60	[kHz]	Ta=25 [deg. C] **(Note 2)**
Vinv	Inverter Ignition Voltage *5	1500			[Vrms]	Ta=25 [deg. C]
		1700			[Vrms]	Ta=10 [deg. C]
		1850			[Vrms]	Ta=0 [deg. C]
VCFL	CFL Voltage (Reference)		860		[Vrms]	Ta=25 [deg. C]
PCFL	CFL Power Consumption		5.2	5.6	[W]	Ta=25 [deg. C] **(Note 3)**
	Total CFL Power Consumption (6 lamps)		32	34	[W]	Ta=25 [deg. C]

Note:

1. If it exceeds Min./Max. values, then "CFL Life", "ON/OFF Cycle" and "Safety" will not be guaranted.
2. CFL Frequency should be carefully determind to avoid interference between inverter and TFT LCD.
3. Caliculated value for reference (ICFL x VCFL = PCFL)
4. It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4.0 [mA].
5. Please keep balancing of all CFL currents.
6. Duration : 50[mS] Max.

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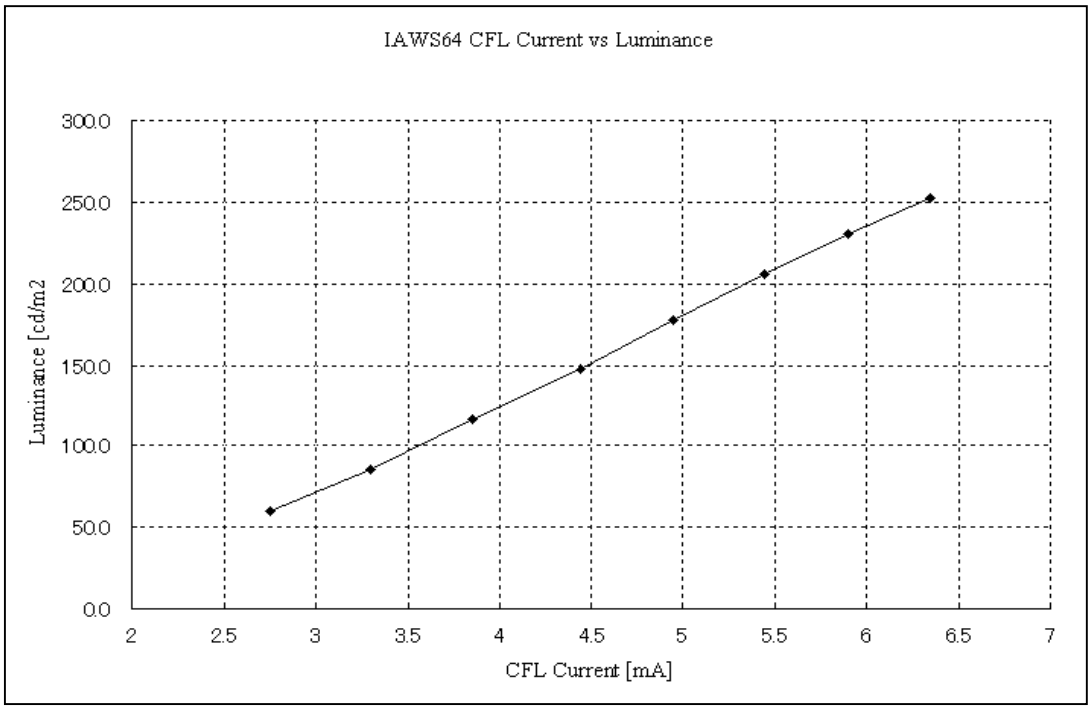
The following chart is the ICFL versus Brightness for your reference.



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9.0 Power ON/OFF Sequence

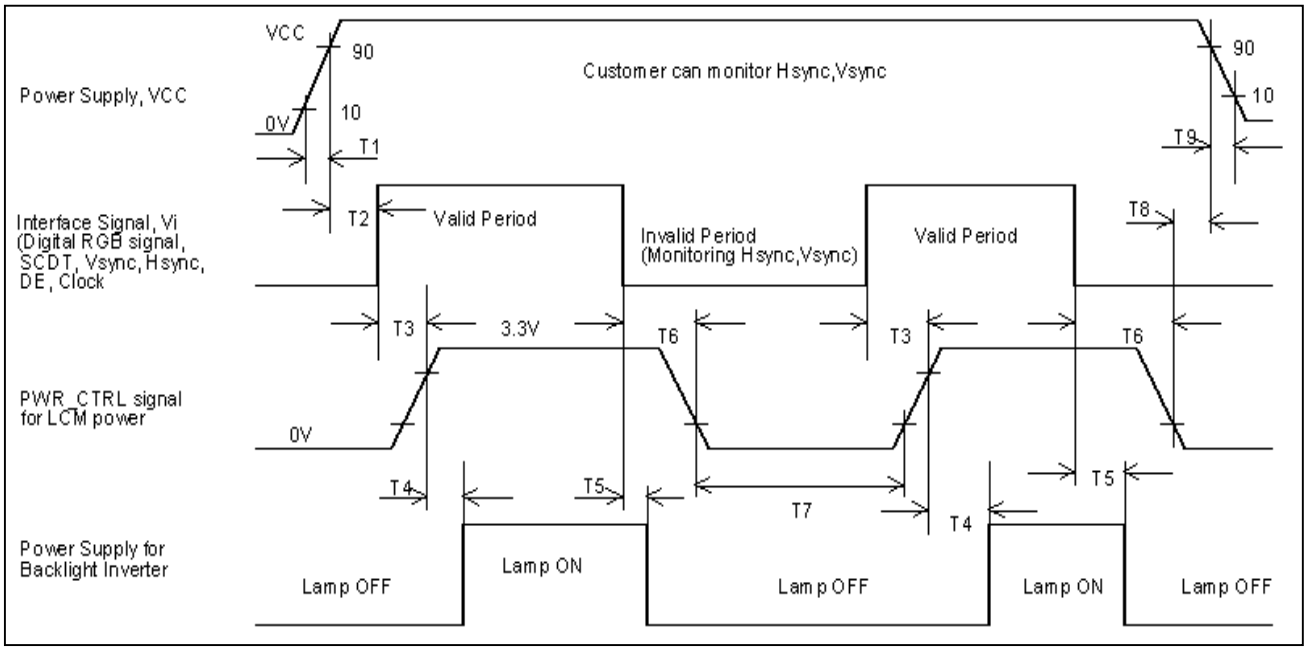
Vcc power and lamp on/off sequence is as follows. Interface signals are also shown in the chart.

Signals from any system shall be Hi-Z state or low level when Vcc is off.

Power On/Off Sequence

Parameter	Min.	Typ.	Max.	Unit
T1	-		10	[ms]
T2	0		-	[ms]
T3	-		50	[ms]
T4	100		-	[ms]
T5	-		50	[ms]
T6	-		80	[ms]
T7	400		-	[ms]
T8	0		-	[ms]
T9	-		10	[ms]

Vcc/TMDS Signals/Lamp Voltage On/Off Sequence Requirements



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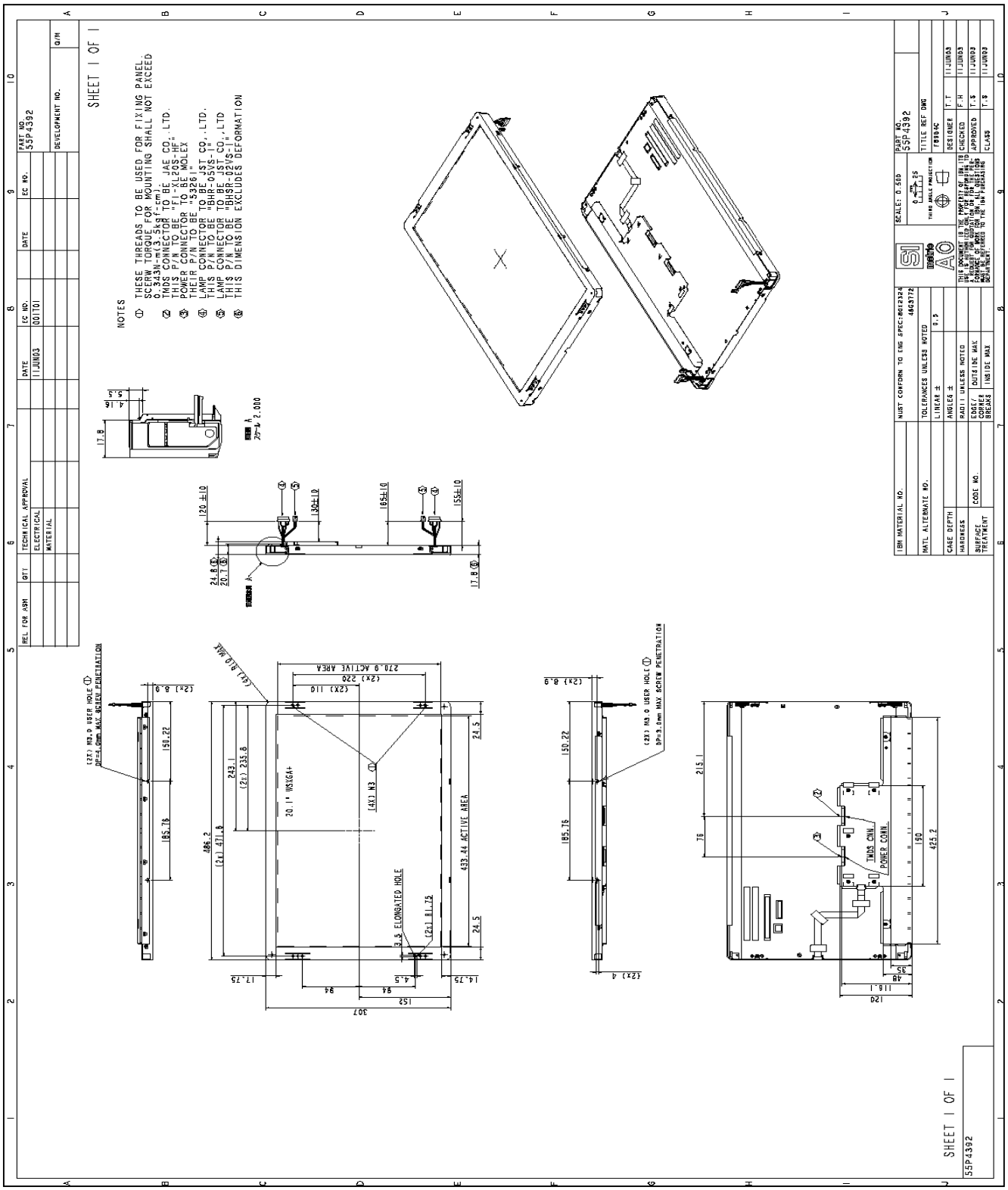
10.0 Mechanical Characteristics



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Dimension

	Min.	Typ.	Max.	Unit
Width	485.7	486.2	486.7	[mm]
Hight	306.5	307.0	307.5	[mm]
Depth (High)	24.3	24.8	25.3	[mm]
Depth (Low)	17.3	17.8	18.3	[mm]
Lamp Cable (CN1)	125	135	145	[mm]
Lamp Cable (CN2)	125	135	145	[mm]
Lamp Cable (CN3)	125	135	145	[mm]
Lamp Cable (CN4)	155	165	175	[mm]

Weight

Min.	Typ.	Max.	Unit
3.10	3.25	3.40	[k grams]

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11.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

Conditions of Acceptability - When installed in the end-product, consideration shall be given to the following;

1. This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, CSA / UL60950, Third Edition, dated December 1, 2000, Sub-clause 2.10, which would cover the component itself if submitted for Listing.
2. The unit is intended to be supplied by SELV and Limited Power Source. Also separated form electrical parts, which may produce high temperature that could cause ignition by as least 13mm of air or by a solid barrier of material of V-1 minimum.
3. The terminals and connectors are suitable for factory wiring only.
4. A suitable Electrical enclosure shall be provided.
5. ISO13406

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12.0 Qualifications and CFL Life

This Quality Specification is for the WSXGA+ TFT-LCD module IAWS64C supplied from International Display Technology to the customer.

Please pay attention the following items, when this LCD Module is checked in your inspection.

1. You should consider the LCD Module to mount that uneven force is not applied to this LCD Module.

2. Do not push and put a label on the rear side that is located backlight.

3. Do not joggle the LCD Module, there will be some ripple on the screen.

4. Display qualifications depend on the power on time.
   The visual screen quality is applied the state since 30 seconds after power on.

12.1 Visual Screen Quality (*)

12.2 Line Defect (*)

12.3 Bright and Black Dots (*)

(*) Refer to the "Cosmetic Specification for 20.1" WSXGA+ TFT-LCD".
Title: SPEC. COSM. DSPL, 20.1" TFFLCD
DWG Number: 062-9932 Rev. 1.0
Apple Computer, Inc.

12.4 CCFL Life

CCFL Life Time	50,000 Hours (Typ.) 30,000 Hours (Min.)	condition 25 deg.C

The assumed CCFL life will be until the luminance becomes 90 cd/m^2 (equivalent of the module value) or more the general test condition (7[mA] Max.).

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12.5 CCFL Information

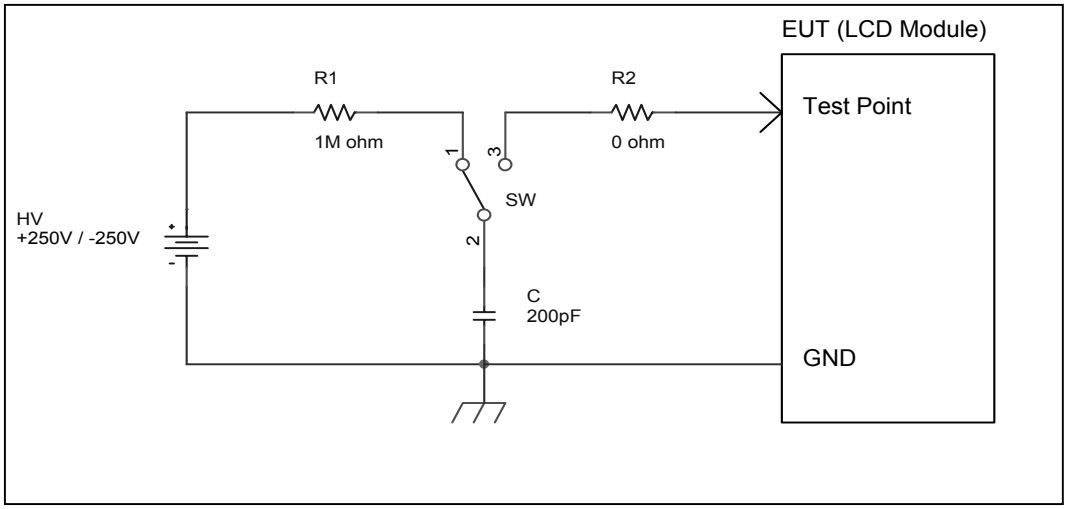
Supplier Name	Harison Toshiba Lighting
Part Number	MBTM24J**(*)** x 450NCRBU / CD
Outer / Inner diameter [□]	2.4 / 2.0
Length [mm]	450
Mercury contain [mg]	3.5 Max. / 2.7 Typ. / 1.9 Min.

(*) color code

The TFT-LCD module contains of six lamps.

12.6 ESD Spec.

The LCD module shall withstand against electrostatic discharge applied by the following test circuit in.



Test points are all non-ground conductors on the interface and power connectors.

Five shots of positive and negative each positive and five negative

Tests are performed in non-operating condition.

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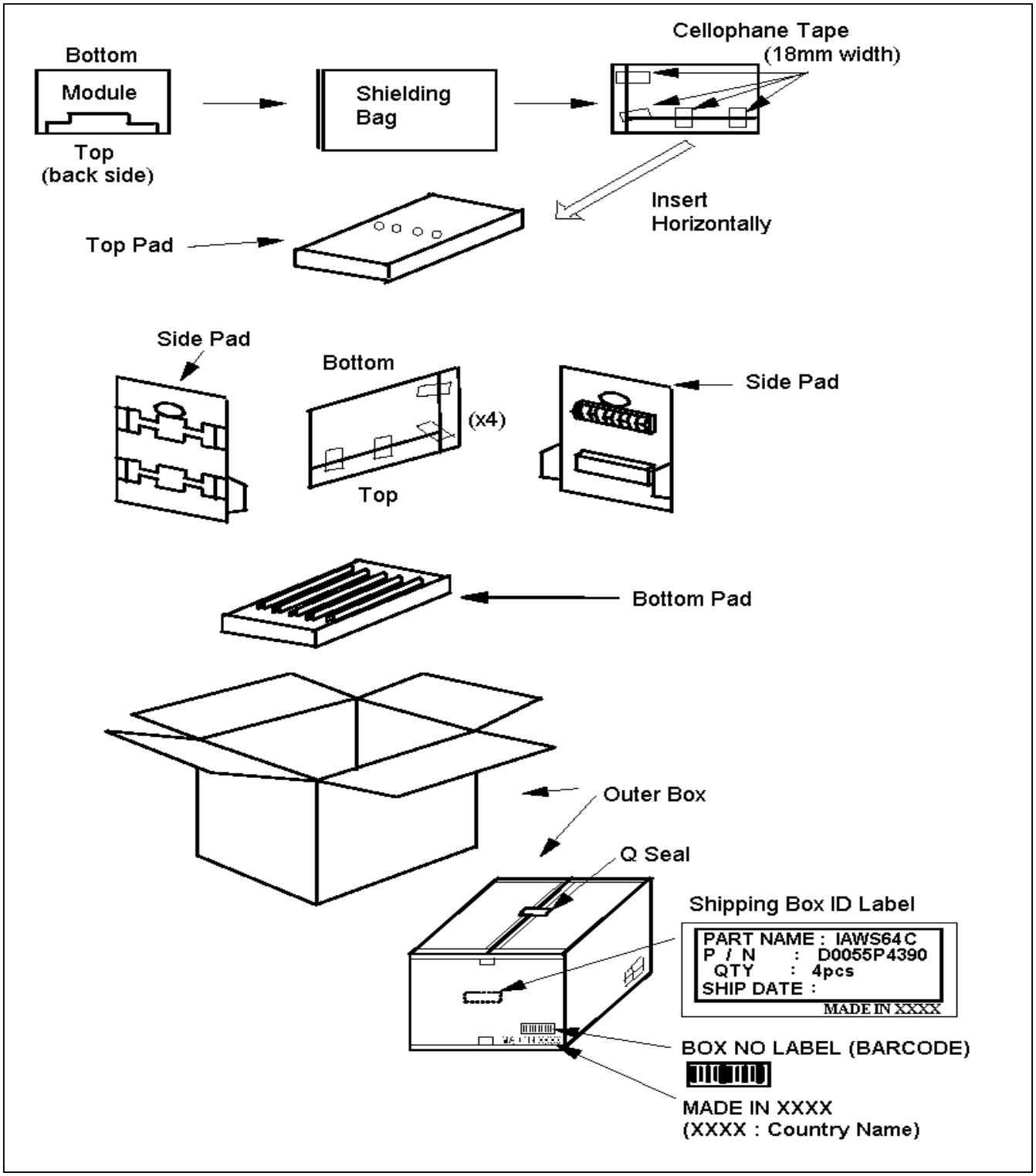
13.0 Packaging Specification

The following is the drawing of the package.



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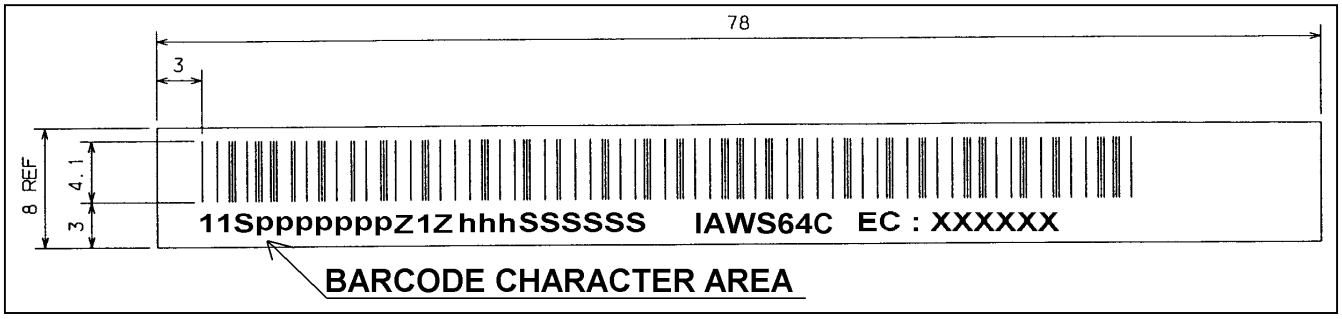
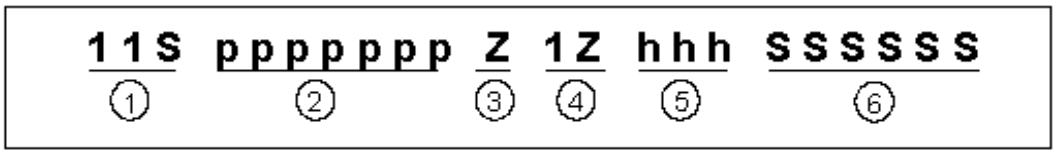
14.0 Label

There are labels on the rear side of the Module.



Serial Number Label

BARCODE CHARACTER AREA



① 11S = FIXED
Starting identifier which is common to component level serial numbers.

② Seven digit IDT part number
Assigned by the IDT development releasing the part

③ Z = FIXED
Automatically given when using the 11S-Z format

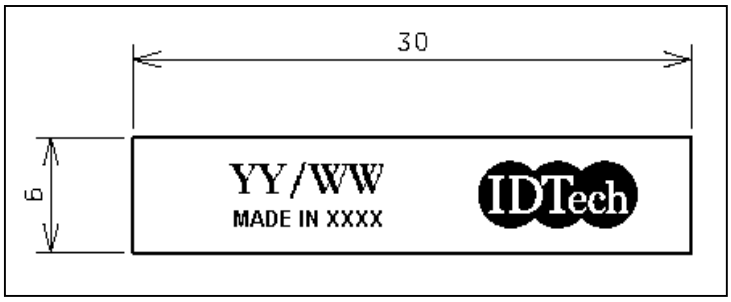
④ 1Z = FIXED
Location code

⑤ hhh = Header code
(Depend on EC Level and Manufacturing Location)

⑥ SSSSSS = Serial Number

Date Label

YY and WW of the Week Code stand for the Year and the Week of the Year of manufacturing of the Module respectively.



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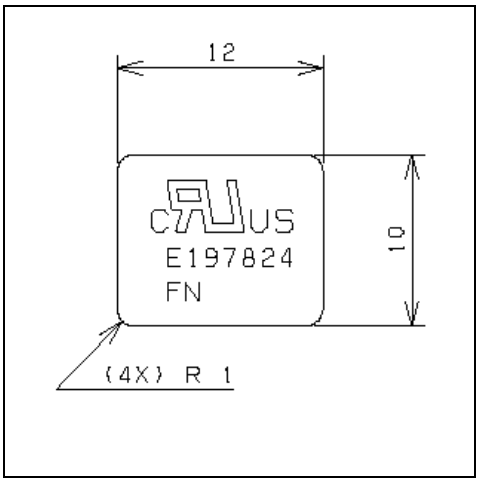
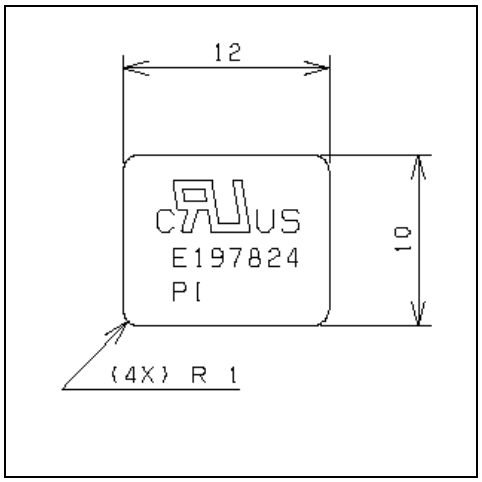
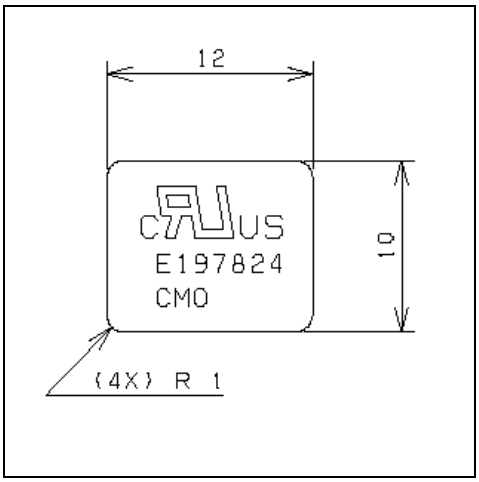
UL Label (TBD)







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