Engineering Specification

Type 15.0 UXGA Color TFT/LCD Module
Model Name:ITUX97C

Document Control Number : OEM I-97C-02

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Product Development
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
January 10,2001	OEM97C-01	All	First Edition for customer. ITUX97C is based on ITUX97S. The difference is Cable Length only. Cable Length : 125mm
May 14,2001	OEM97C-02	 1,5,6,7 4 8 11 12,13 14,15,16,17,18	Based on Internal Spec. EC F79475 as of January 31,2001. To avoid using "inch" indication. To update Handling Precautions. To update Absolute Maximum Ratings. To update Interface Signal Connector. To update Interface Signal Description. To update Interface Signal Electrical Characteristics.
January 15,2002	OEM I-97C-02		Updated by establishment of the New Company as "International Display Technology".

1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
10) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
11) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
12) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
13) The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
14)Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL1950), or be applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL1950) in an end product.
15)The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the Type 15.0 Color TFT/LCD Module 'ITUX97C'.
This module is designed for a display unit of notebook style personal computer.
The screen format and electrical interface are intended to support the UXGA(1600(H) x 1200(V)) screen.
Support color is native 262K colors(RGB 6-bit data driver).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

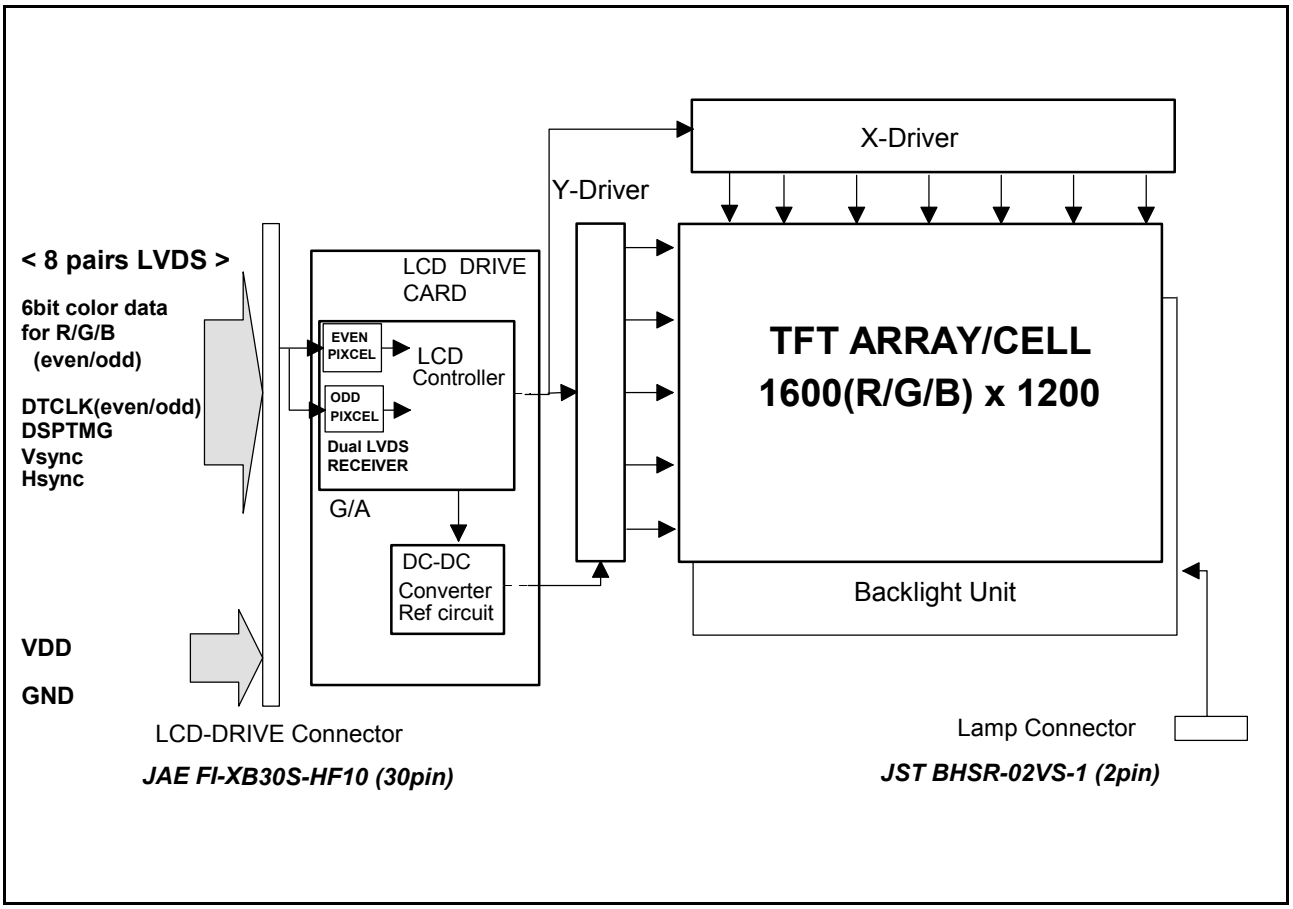
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	381(15.0")
Pixels H x V	1600(x3) x 1200
Active Area [mm]	304.8(H) x 228.6(V)
Pixel Pitch [mm]	0.1905(per one triad) x 0.1905
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	650Typ. 685Max.
Physical Size [mm]	317.3(W) x 242.0(H) x 6.7(D) typ.7.0(D)Max.
Display Mode	Normally White
Support Color	Native 262K colors(RGB 6-bit data driver)
White Luminance [cd/m^2] Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA)	 90 Typ(center) 85 Typ(5 points average) 150 Typ(center)140 Typ(5 points average)
Contrast Ratio	200 : 1 Typ.
Optical Rise Time/Fall Time [msec]	30Typ.,50 Max.
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt](VDD Line)	2.4 Typ.,3.4MAX.
Lamp Power Consumption [Watt] (VCFL Line) Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA)	 2.7Typ.,(W/o inverter loss) 4.4Typ.,(W/o inverter loss)
Typical Power Consumption [Watt] (VDD Line + VCFL Line) Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA)	 5.1Typ.6.1MAX,(W/o inverter loss) 6.8Typ.8.1MAX,(W/o inverter loss)
Electrical Interface	8 pairs LVDS(Even/Odd R/G/B Data(6bit), 3sync signals, Clock)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the Type 15.0 Color TFT/LCD Module.
The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Signal Voltage	VIN	-0.3	VDD+0.3	V	
CFL Ignition Voltage	Vs	-	+1,600	Vrms	Note 2
CFL Current	ICFL	-	7	mAms	
CFL Peak Inrush Current	ICFLP	-	20	mA	
Operating Temperature	TOP	0	+50	deg.C	Note 1
Operating Relative Humidity	HOP	8	95	%RH	Note 1
Storage Temperature	TST	-20	+60	deg.C	Note 1
Storage Relative Humidity	HST	5	95	%RH	Note 1
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.
Note 2 : Duration : 50msec Max. Ta=0 degree C

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≥10 (Left) Vertical (Upper) K≥10 (Lower)	40 40 15 30	- - - -
Contrast ratio		200	-
Response Time	Rising	30	50Max
(ms)	Falling	30	50Max
Color	Red x	0.569	-
Chromaticity	Red y	0.332	-
(CIE)	Green x	0.312	-
	Green y	0.544	-
	Blue x	0.149	-
	Blue y	0.132	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2) ICFL 6.5 mA		150Typ. Center 140Typ. 5 points average	-

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30S-HF10
Mating Type / Part Number	FI-X30M

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Pin #	Signal Name
1	FG (GND)
2	GND
3	VDD
4	VDD
5	V_{EEDID} (Note 2,3)
6	Reserved (Note 1)
7	CLK_{EEDID} (Note 2,4)
8	$Data_{EEDID}$ (Note 2,4)
9	ReIN0-
10	ReIN0+
11	GND
12	ReIN1-
13	ReIN1+
14	GND
15	ReIN2-
16	ReIN2+

Pin #	Signal Name
17	GND
18	ReCLKIN-
19	ReCLKIN+
20	GND
21	RoIN0-
22	RoIN0+
23	GND
24	RoIN1-
25	RoIN1+
26	GND
27	RoIN2-
28	RoIN2+
29	GND
30	RoCLKIN-
31	RoCLKIN+
32	FG (GND)

Note:

1. 'Reserved' pins are not allowed to connect any other line.
2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3".
3. V_{EEDID} power source shall be the limited current circuit which has not exceeding 1A. (Reference Document : "Enhanced Display Data Channel (E-DDC™) Proposed Standard", VESA)
4. Both CLK_{EEDID} line and $DATA_{EEDID}$ line are pulled up with 10k ohm resistor to V_{EEDID} power source line at LCD panel, respectively.

5.3 Interface Signal Description

The module uses a pair of LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be a negative edge sampling type.

PIN #	SIGNAL NAME	Description
1	FG	Frame Ground
2	GND	Ground
3	VDD	+3.3V Power Supply
4	VDD	+3.3V Power Supply
5	V_{EEDID}	EEDID 3.3V Power Supply
6	Reserved	Reserved
7	CLK_{EEDID}	EEDID Clock
8	$Data_{EEDID}$	EEDID Data
9	ReIN0-	Negative LVDS differential data input (Even R0-R5, G0)
10	ReIN0+	Positive LVDS differential data input (Even R0-R5, G0)
11	GND	Ground
12	ReIN1-	Negative LVDS differential data input (Even G1-G5, B0-B1)
13	ReIN1+	Positive LVDS differential data input (Even G1-G5, B0-B1)
14	GND	Ground
15	ReIN2-	Negative LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
16	ReIN2+	Positive LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
17	GND	Ground
18	ReCLKIN-	Negative LVDS differential clock input (Even)
19	ReCLKIN+	Positive LVDS differential clock input (Even)
20	GND	Ground
21	RoIN0-	Negative LVDS differential data input (Odd R0-R5, G0)
22	RoIN0+	Positive LVDS differential data input (Odd R0-R5, G0)
23	GND	Ground
24	RoIN1-	Negative LVDS differential data input (Odd G1-G5, B0-B1)
25	RoIN1+	Positive LVDS differential data input (Odd G1-G5, B0-B1)
26	GND	Ground
27	RoIN2-	Negative LVDS differential data input (Odd B2-B5)
28	RoIN2+	Positive LVDS differential data input (Odd B2-B5)
29	GND	Ground
30	RoCLKIN-	Negative LVDS differential clock input (Odd)
31	RoCLKIN+	Positive LVDS differential clock input (Odd)
32	FG	Frame Ground

Note:
1. Input signals of odd and even clock shall be the same timing.
2. The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
3. Even: First Pixel , Odd: Second Pixel

SIGNAL NAME	Description
+RED 5 (ER5/OR5) +RED 4 (ER4/OR4) +RED 3 (ER3/OR3) +RED 2 (ER2/OR2) +RED 1 (ER1/OR1) +RED 0 (ER0/OR0) (EVEN/ODD)	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 (EG5/OG5) +GREEN 4 (EG4/OG4) +GREEN 3 (EG3/OG3) +GREEN 2 (EG2/OG2) +GREEN 1 (EG1/OG1) +GREEN 0 (EG0/OG0) (EVEN/ODD)	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 (EB5/OB5) +BLUE 4 (EB4/OB4) +BLUE 3 (EB3/OB3) +BLUE 2 (EB2/OB2) +BLUE 1 (EB1/OB1) +BLUE 0 (EB0/OB0) (EVEN/ODD)	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 81MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG (DSP)	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC (V-S)	Vertical Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
HSYNC (H-S)	Horizontal Sync: This signal is synchronized with DTCLK. Both active high/low signals are acceptable.
VDD	Power Supply
GND	Ground
V_{EEDID}	EEDID 3.3V Power Supply
CLK_{EDID}	EEDID Clock
$Data_{EEDID}$	EEDID Data

Note: Output signals except V_{EEDID} ,CLK_{EEDID} and $Data_{EEDID}$ from any system shall be Hi-Z state when VDD is off.

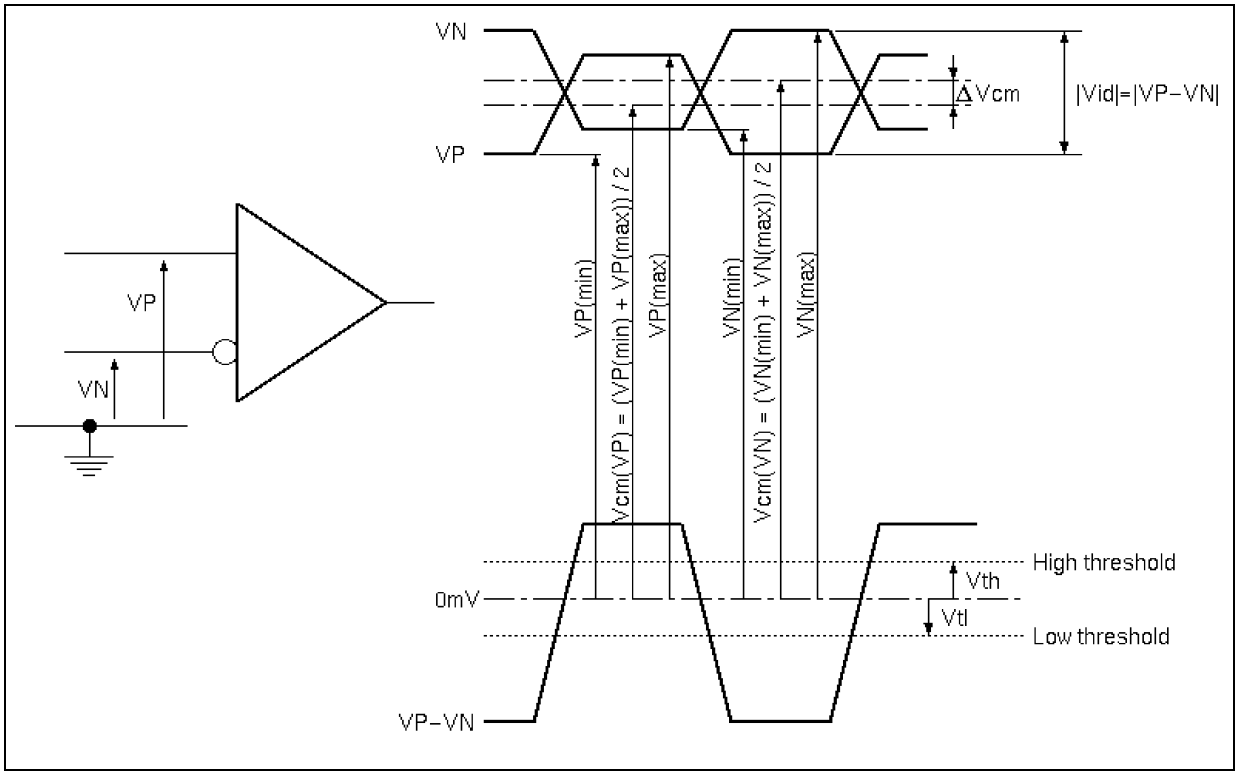
5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Electrical Characteristics

Parameter	Symbol	Min	Max	unit
Differential Input High Threshold	Vth		+100	[mV]
Differential Input Low Threshold	Vtl	-100		[mV]
Magnitude Differential Input Voltage	|Vid|	100	600	[mV]
Common Mode Input Voltage	Vic	$0.825+\frac{\lvert Vid \rvert}{2}$	$2.4-\frac{\lvert Vid \rvert}{2}$	[V]
Common Mode Voltage Offset	ΔVcm	-50	+50	[mV]

Note: Input signals shall be low or Hi-Z state when VDD is off.

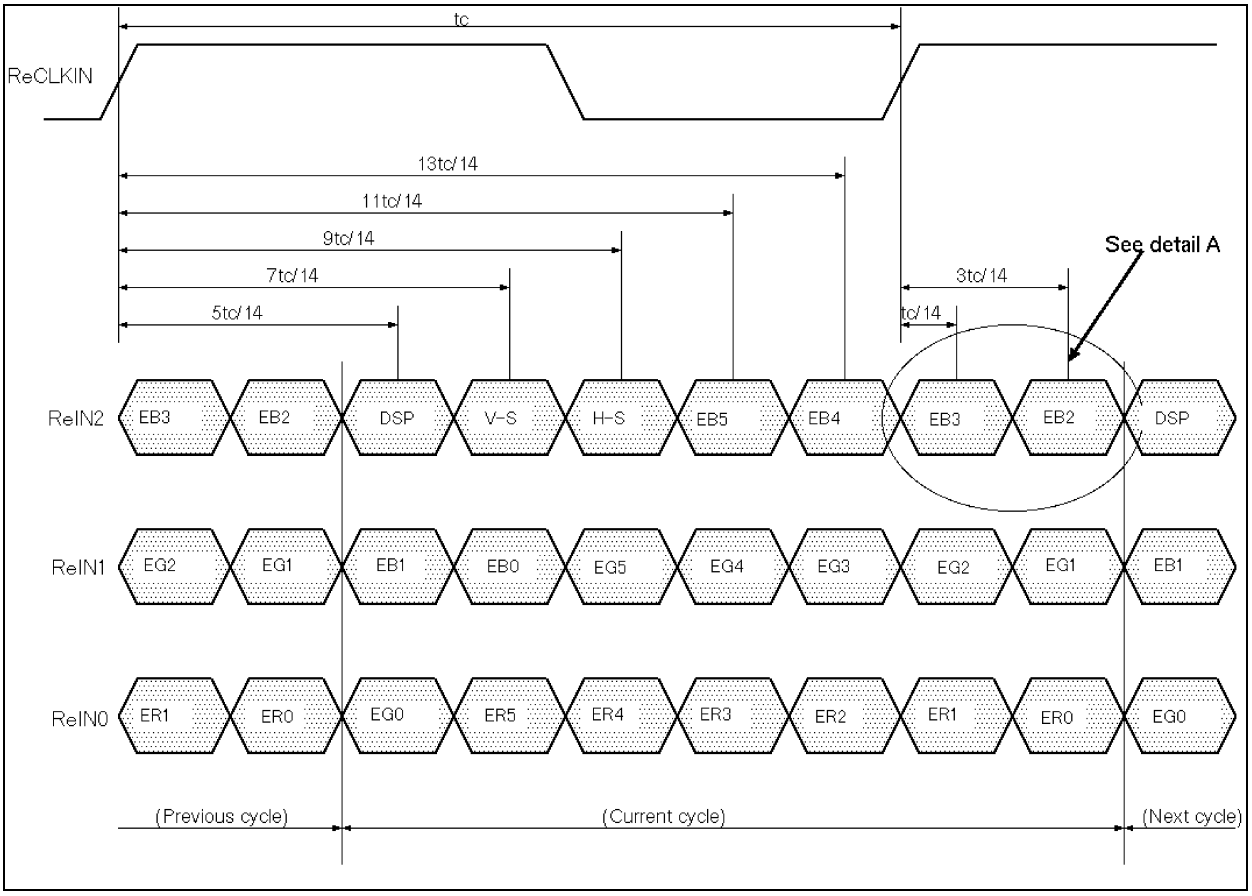


Voltage Definitions

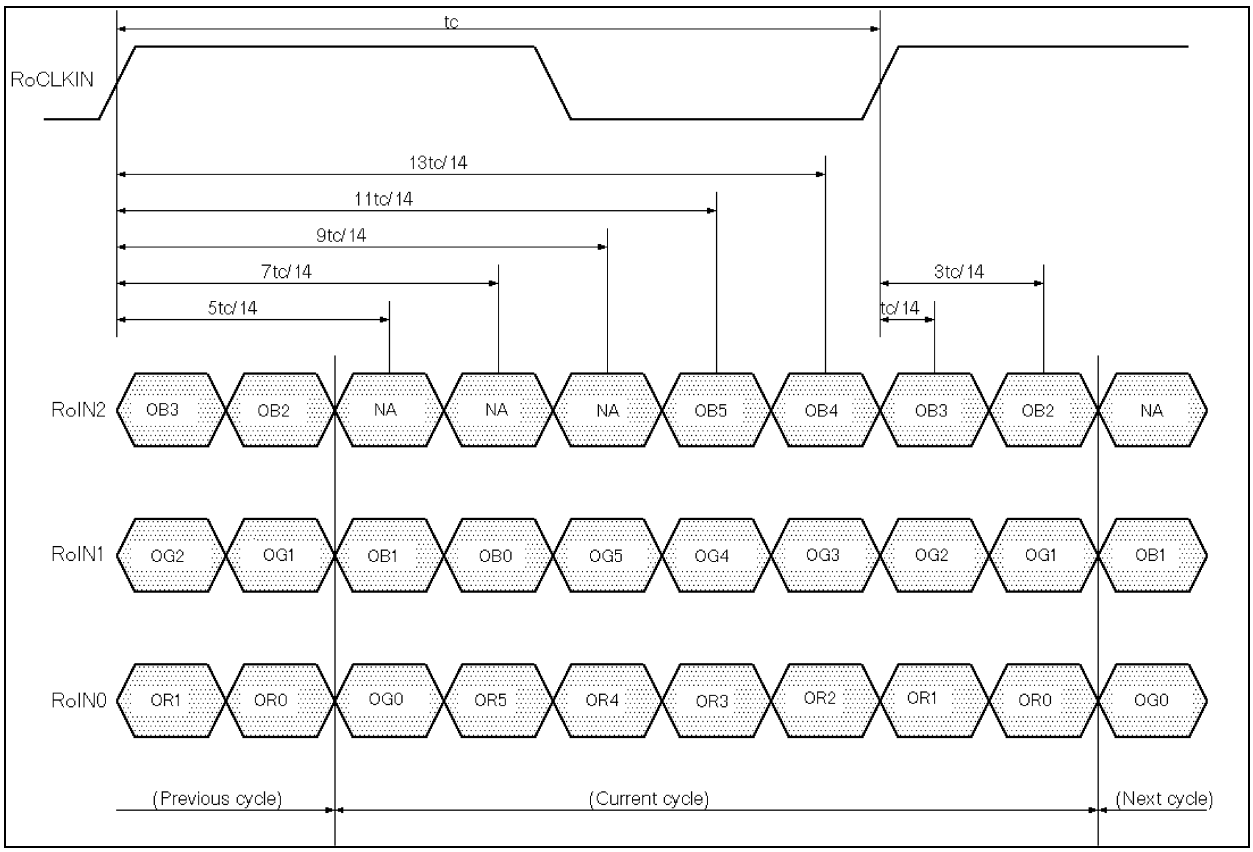
Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency (UXGA)	fc	75.0	81.0	83.0	MHz	
Clock Frequency (UXGA FPT)	fc	61.0	66.4	69.0	MHz	
Cycle Time (UXGA)	tc	12.0	12.3	13.3	ns	
Cycle Time (UXGA FPT)	tc	14.5	15.1	16.4	ns	
Data Setup Time (UXGA)	Tsu	500			ps	fc = 81.0MHz, jitter < 50ps
Data Setup Time (UXGA FPT)	Tsu	600			ps	
Data Hold Time (UXGA)	Thd	500			ps	fc = 66.4MHz, jitter < 50ps
Data Hold Time (UXGA FPT)	Thd	600			ps	
Cycle modulation rate(Note)	tCJavg			20	ps/clk	

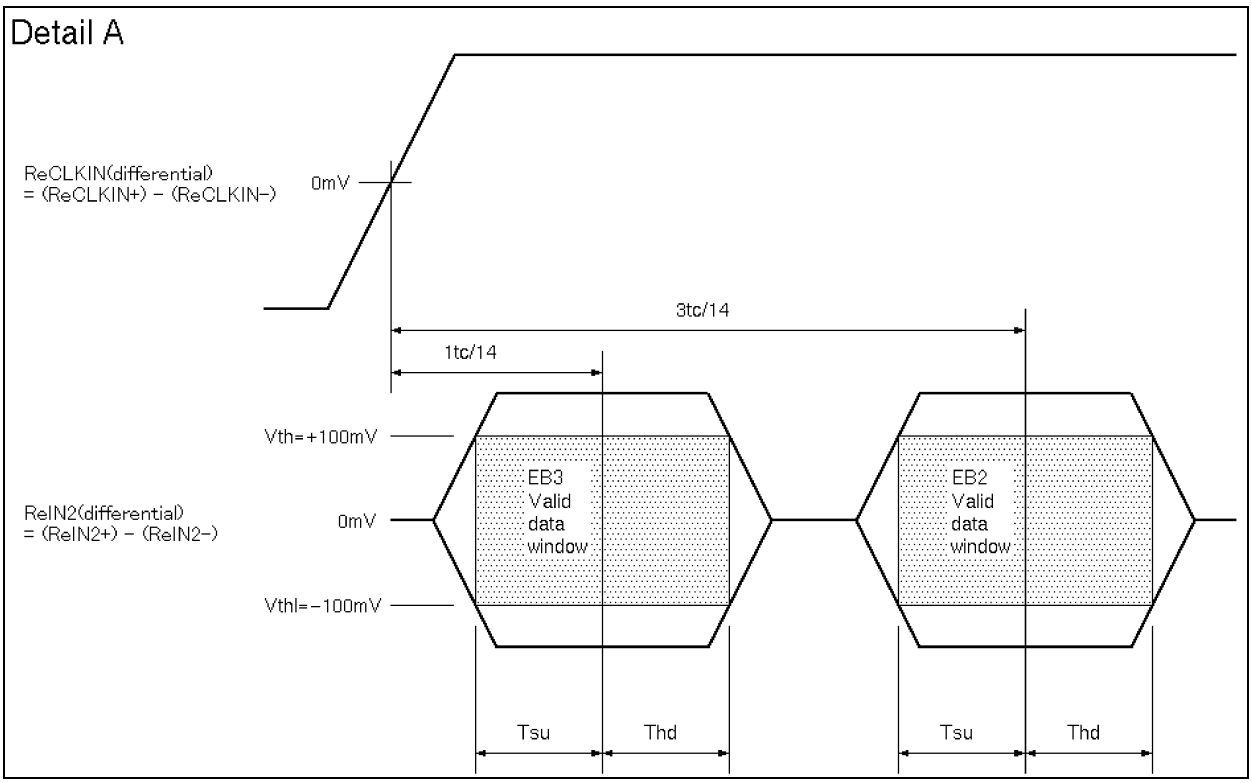
Note: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.



Timing Definition (Even)



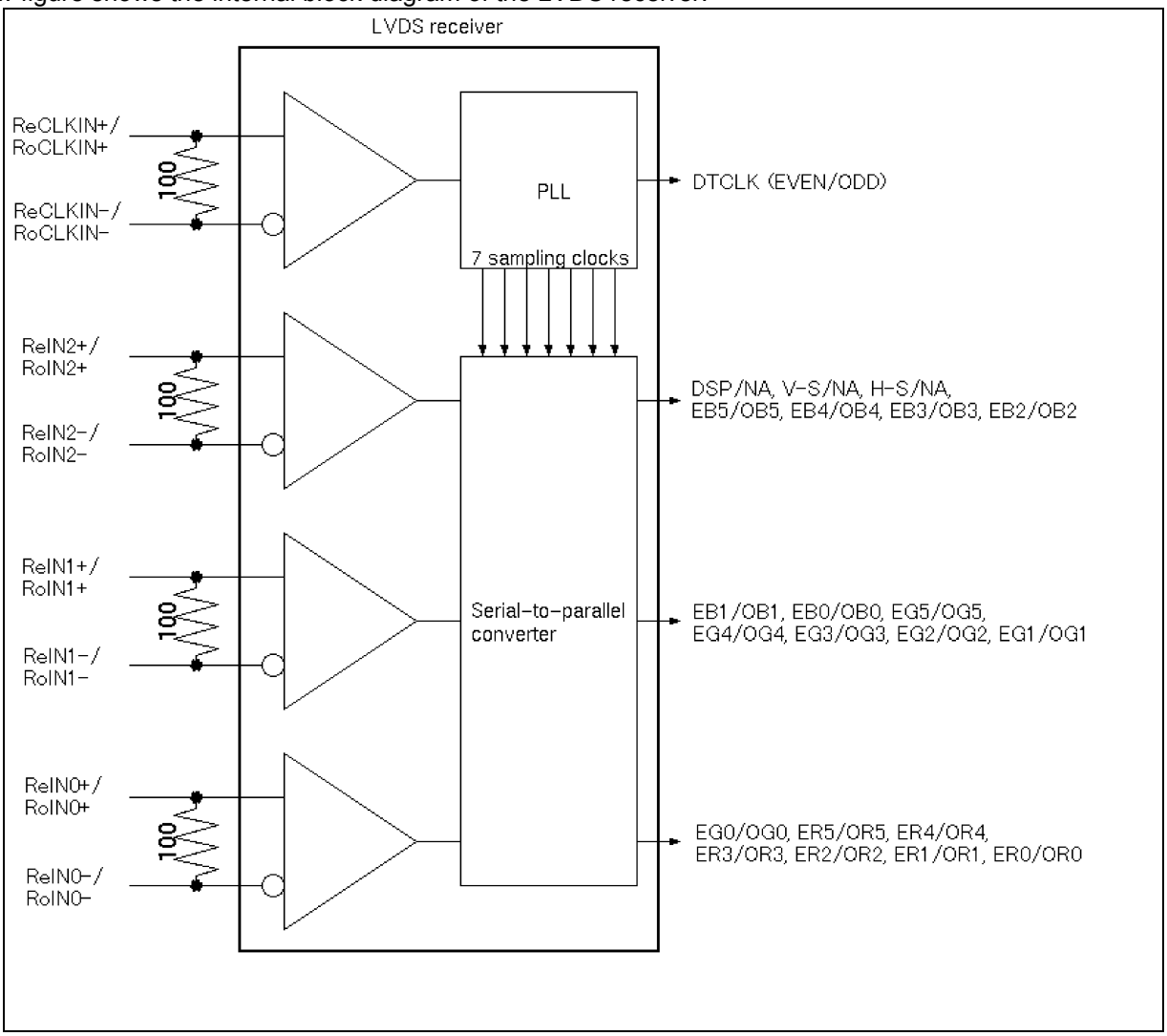
Timing Definition (Odd)



Timing Definition(detail A)

5.4.2 LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver.

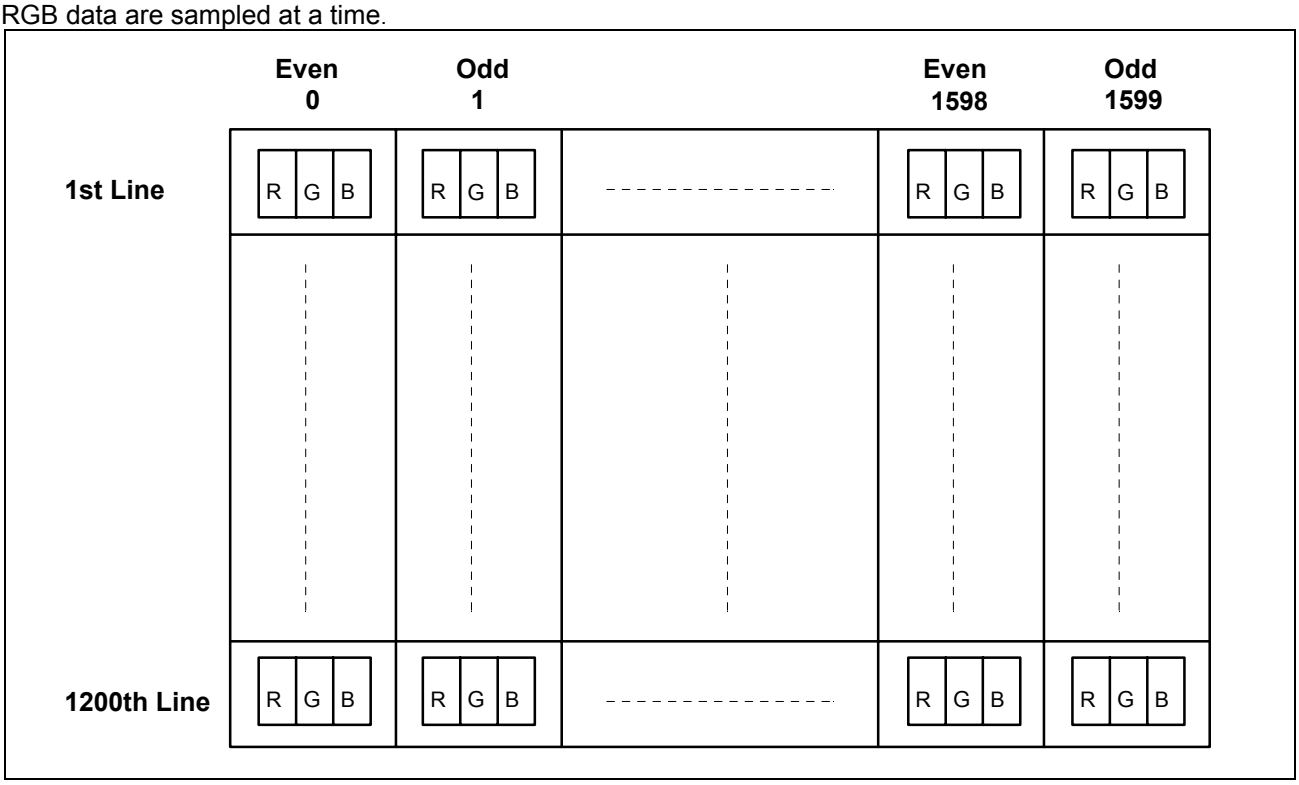


5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Even and odd pair of RGB data are sampled at a time.



7.0 Parameter guide line for CFL Inverter

PARAMETER	MIN	DP-1	DP-2	MAX	UNITS	CONDITION
White Luminance (Center) (5 Points average)	 - -	 90 85	 150 140	 - -	cd/m^2	(Ta=25 deg.C)
CFL current(ICFL)	3.0	3.5	6.5	7.0	mArms	(Ta=25 deg.C)
CFL Frequency(FCFL)	40	-	-	60	KHz	(Ta=25 deg.C) **Note 1**
CFL Ignition Voltage(Vs)	1,450	-	-	-	Vrms	(Ta= 0 deg.C) **Note 3**
CFL Voltage (Reference)(VCFL)	-	745	645	-	Vrms	(Ta=25 deg.C) **Note 2**
CFL Power consumption(PCFL)	-	2.7	4.4	-	W	(Ta=25 deg.C) **Note 2**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,450 voltage. Lamp units need 1,450 voltage minimum for ignition.

Note 4: DP-1 and DP-2 are recommended Design Points.

*1 All of characteristics listed are measured under the condition using the Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

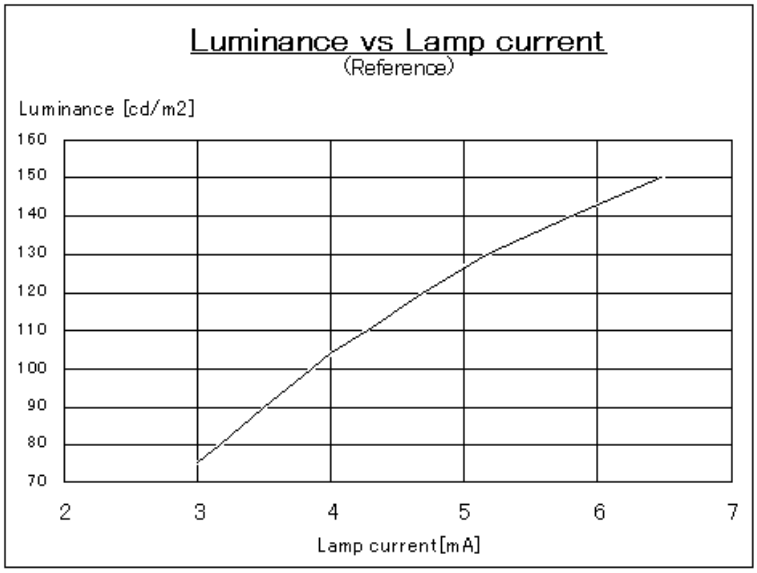
*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

*7 It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4mA.

The following chart is CFL current versus the luminance for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86(Texas Instruments) or equivalent.

8.1 Timing Characteristics

(VESA UXGA Mode)

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	75.0	81.0	83.0	[MHz]
		Tck	12.0	12.3	13.3	[ns]
+V-Sync	Frame Rate	Fv		60.0		[Hz]
		Tv		16.67		[ms]
		Nv	1208	1250	2046	[lines]
	V-Active Level	Tva	13.33	40.0	839.8	[us]
		Nva	1	3	63	[lines]
	V-Back Porch	Nvb	6	46	125	[lines]
	V-Front Porch	Nvf	1	1	125	[lines]
+DSPTMG	V-Line	m		1200		[lines]
+H-Sync	Scan Rate	Fh		75.0		[KHz]
		Th		13.33		[usec]
		Nh	1024	1080	2047	[Tck]
	H-Active Level	Tha		1.185		[usec]
		Tha	8	96	255	[Tck]
	H-Back Porch	Thb	8	152	511	[Tck]
	H-Front Porch	Thf	8	32		[Tck]
+DSPTMG	Display	Thd		9.877		[usec]
+DATA	Data Even/Odd	n		1600		[dots]

Note:Both positive Hsync and positive Vsync polarity is recommended.

(VESA UXGA FPT Mode)

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	61.0	66.4	69.0	[MHz]
		Tck	14.5	15.1	16.4	[ns]
+V-Sync	Frame Rate	Fv		60.0		[Hz]
		Tv		16.67		[ms]
		Nv	1208	1214	2046	[lines]
	V-Active Level	Tva	13.7	13.7		[us]
		Nva	1	1	63	[lines]
	V-Back Porch	Nvb	1	1	125	[lines]
	V-Front Porch	Nvf	3	12	125	[lines]
+DSPTMG	V-Line	m		1200		[lines]
+H-Sync	Scan Rate	Fh		73.0		[KHz]
		Th		13.74		[usec]
		Nh	873	912	1023	[Tck]
	H-Active Level	Tha		0.121		[usec]
		Tha	8	8	255	[Tck]
	H-Back Porch	Thb	8	56	511	[Tck]
	H-Front Porch	Thf	8	48		[Tck]
+DSPTMG	Display	Thd		12.053		[usec]
+DATA	Data Even/Odd	n		1600		[dots]

Note:Both positive Hsync and positive Vsync polarity is recommended.

8.2 Timing Definition

Basically, dor count described here is not actual input dot count of LCD module.

(VESA UXGA Mode)

Typical Vertical Timing Table

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1600 x 1200 at 60Hz (H line rate : 13.3 us)	0.667 ms (50 lines)	16.000 ms (1200 lines)	0.013 ms (1 line)	16.667 ms (1250 lines)	0.040 ms (3 lines)	0.613 ms (46 lines)

Typical Horizontal Timing Table

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1600 x 1200 Dotclock : 162.000 MHz (81.000MHz x2)	3.457 us (560 dots)	9.877 us (1600 dots)	0.395 us (64 dots)	13.333 us (2160 dots)	1.185 us (192 dots)	1.877 us (304 dots)

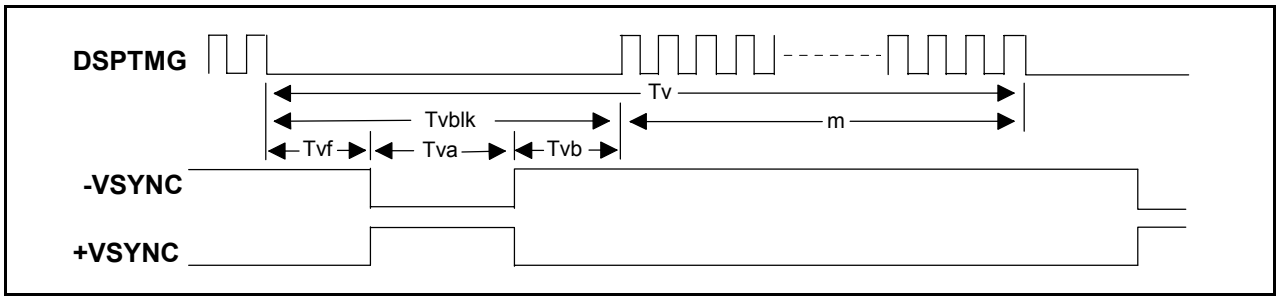
(VESA UXGA FPT Mode)

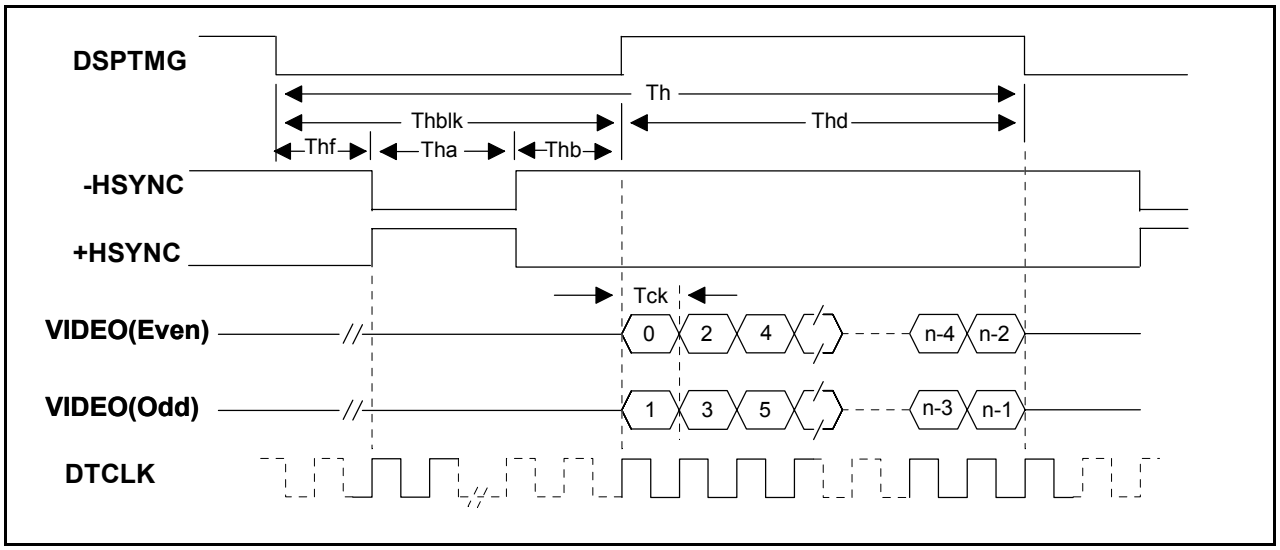
Typical Vertical Timing Table

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1600 x 1200 at 60Hz (H line rate : 13.7 us)	0.192 ms (14 lines)	16.440 ms (1200 lines)	0.164 ms (12 line)	16.632 ms (1214 lines)	0.014 ms (1 line)	0.014 ms (1 line)

Typical Horizontal Timing Table

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1600 x 1200 Dotclock : 132.75 MHz (66.375MHz x2)	1.687 us (224 dots)	12.053 us (1600 dots)	0.723 us (96 dots)	13.740 us (1824 dots)	0.121 us (16 dots)	0.844 us (112 dots)





9.0 Power Consumption

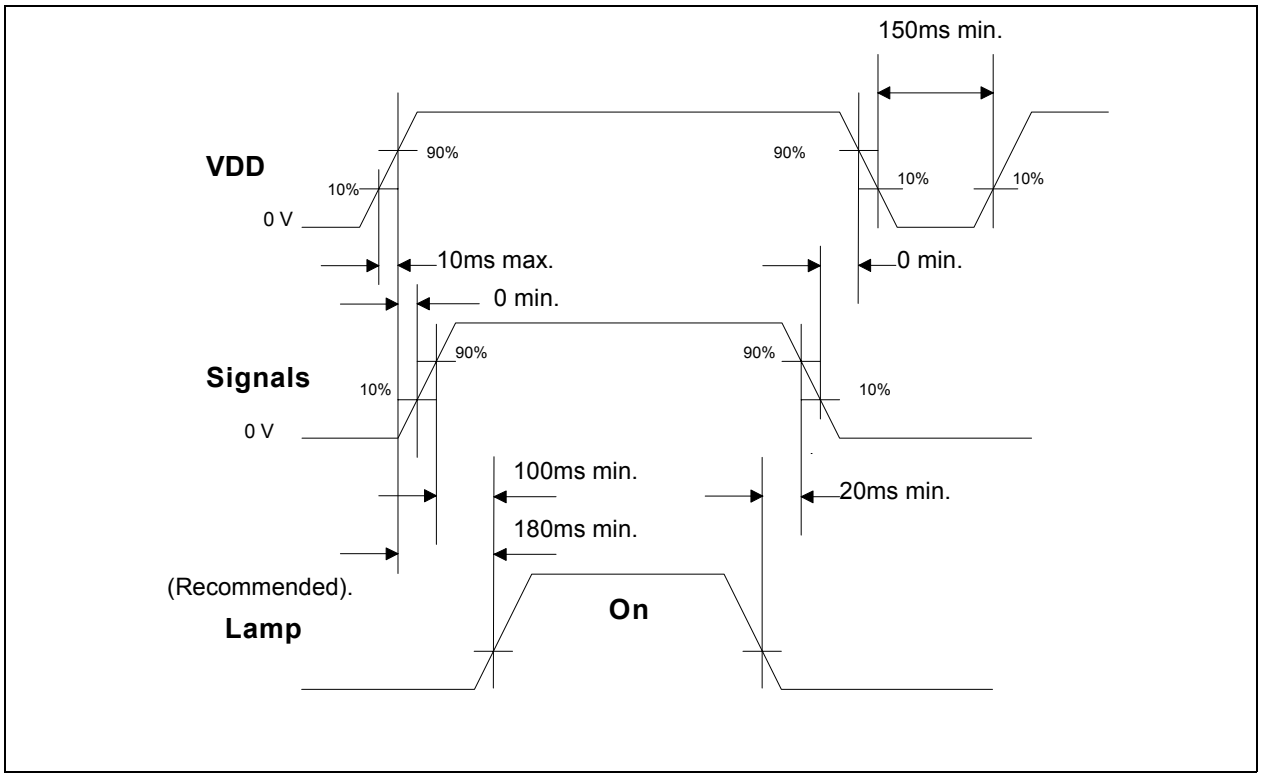
Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 68uF
PDD	VDD Power			3.4	[W]	MAX. Pattern, VDD=3.6[V]
PDD	VDD Power		2.4		[W]	All Black Pattern, VDD=3.3[V]
IDD	VDD Current			940	[mA]	MAX Pattern, VDD=3.0[V]
IDD	VDD Current		730		[mA]	All Black Pattern, VDD=3.3[V]
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mVp-p]	

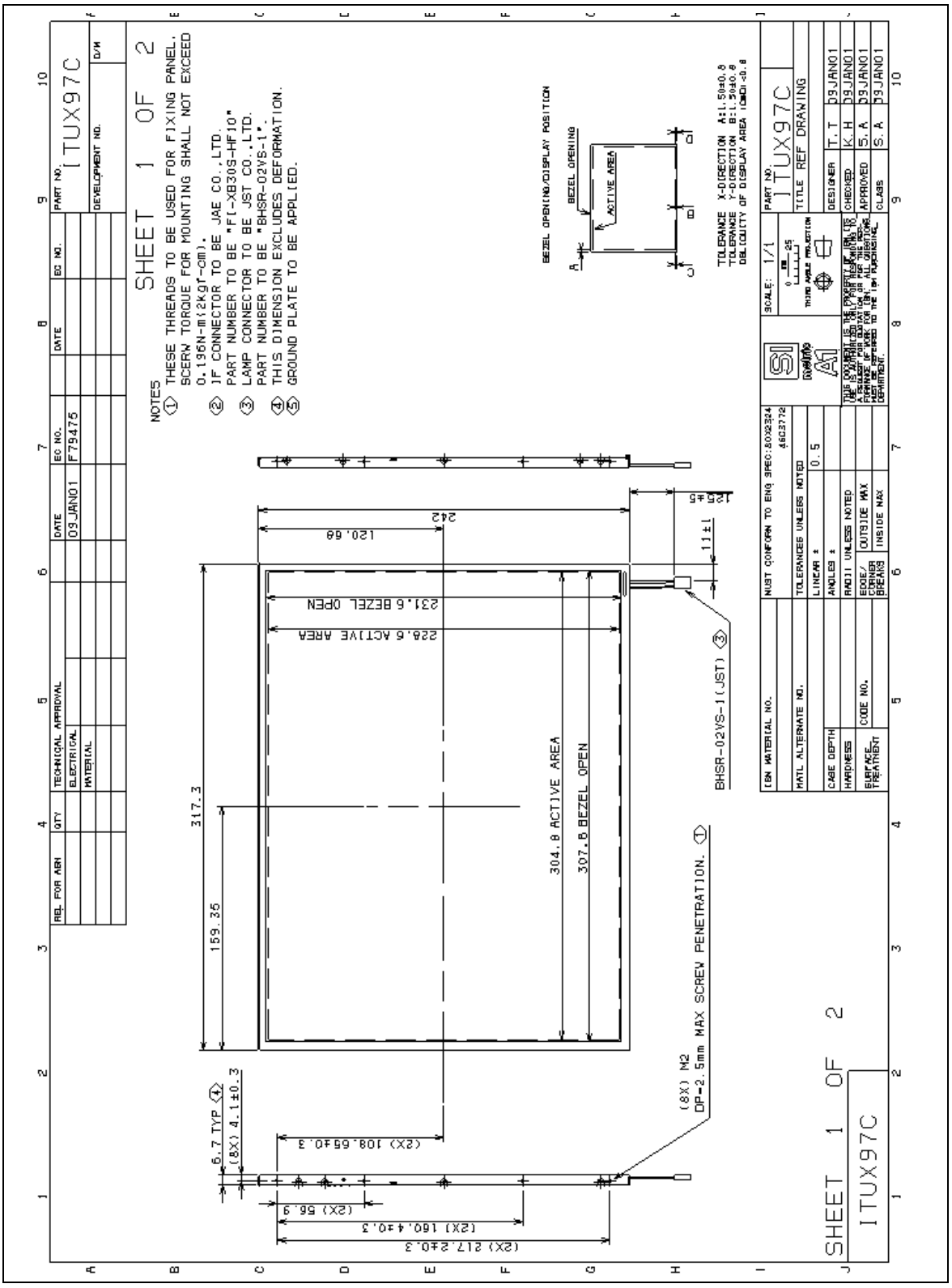
Note: Max Pattern:2 dot Vertical sub-pixel stripe.

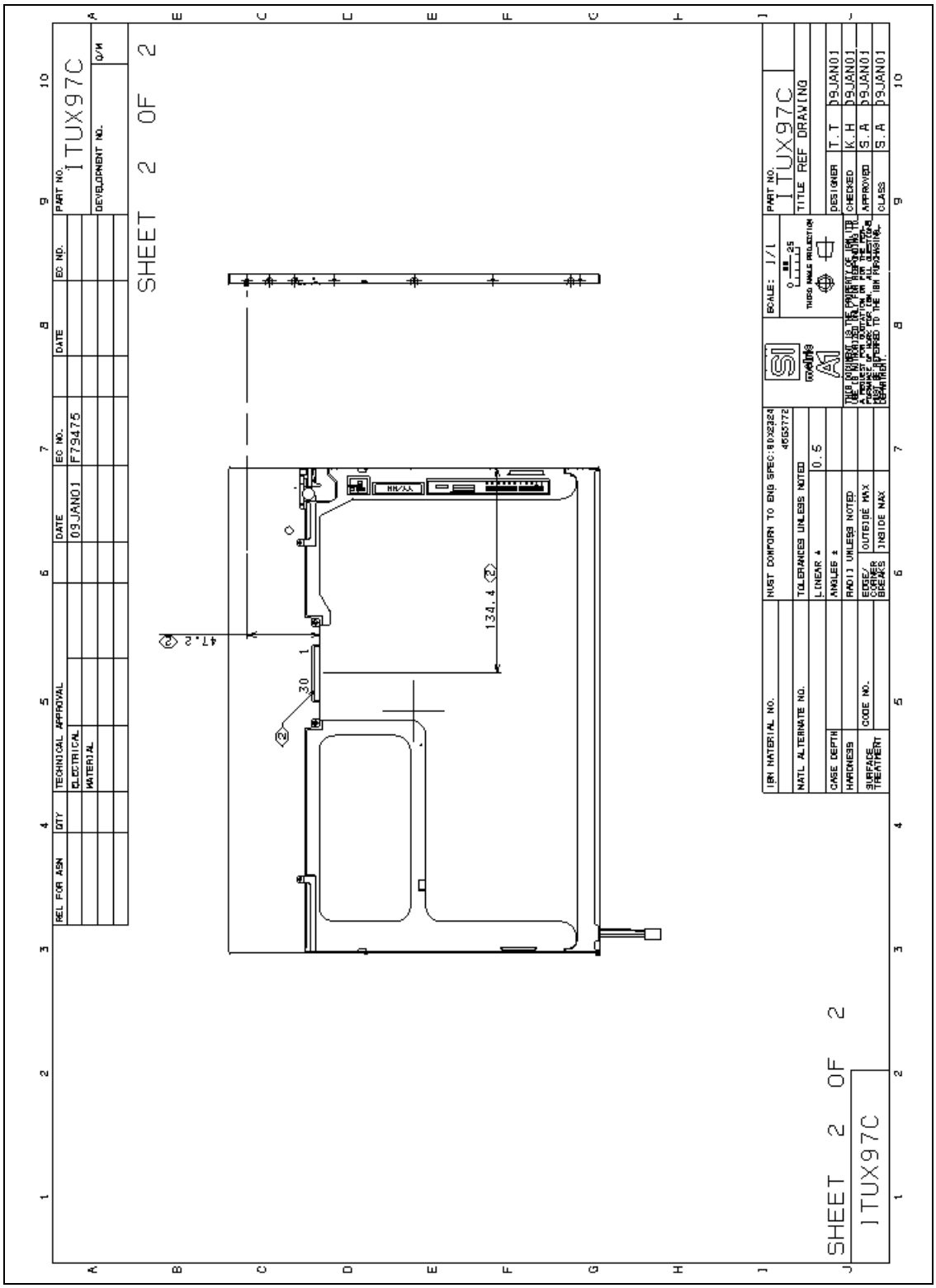
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics





12.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.950-95 *UL 1950, Third Edition, including revisions through revision date March 1,1998, which are based on the Fourth Amendment to IEC 950, Second Edition, which would cover the component itself if submitted for Listing.
- CF Lamp circuit for this model should be supplied from Limited Current Circuit.
- The units are supplied by Limited Power Sources.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.

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