ITXG60L (P/N 82H5200)

30.8cm(12.1 inch)XGA(1024x768)
IBM Color TFT LCD Module

OEM Specifications

OEM Spec.

2. Contents

3. Revision History

Date of Revision	Affected Pages	Reasons of Revision

4. Mechanical Characteristics Data

TFT Model	ITXG60L
Physical Size	278mm x 200mm x 6.8mm(Typ.)
Screen Diagonal	30.8cm(12.1")
Active Area	245.8mm(H) x 184.3mm(V)
Pixel Format	1024(x3) x 768
Pixel Pitch	0.240(per one triad) x 0.240 mm
Pixel Arrangement	R,G,B Vertical Stripe
Weight	470 grams Typ.
LCD Surface Treatment	Antiglare and Hard coat 3H
Backlight	Single cold-cathode fluorescent lamp

5. Absolute Maximum Ratings

Electrical Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	VDD	-0.3 to +6.0	V	
Signal Input Voltage	VIN	TBD	V	Refer DS90CF562 (NS) Spec.
Backlight Voltage	VBL	23	V	
CFL Discharge Current	Icfl	5	mArms	Exclude inrush current
CFL Inrush Current	IRcfl	30	mA0-p	With Max. duration = 50 (mSec)
CFL Driving Frequency	fCFL	30 to 70	kHz	At 25 degreeC
Static Electricity				Operators should be grounded in handling the TFT LCD Module

5. Absolute Maximum Ratings (continued)

Environmental Absolute Maximum Ratings

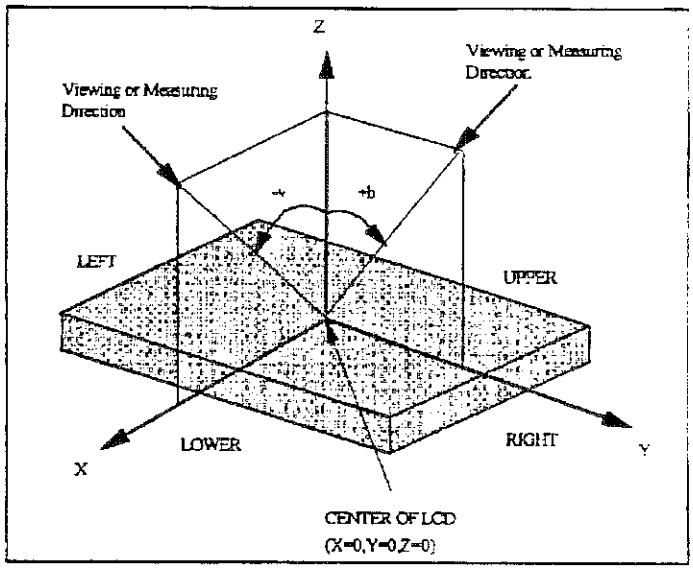
Rating	Symbol	Value	Unit	Conditions
Storage Temperature	TST	-20 to + 60	degC	At the glass surface
Operation Temperature	TOP	0 to +50	degC	At the glass surface
Operation Humidity		8 to 95	%RH	Max. wet bulb temp. 29 degC No condensation
Vibration		1	G	10 - 200 Hz, X,Y,Z (Note1)
Trapezoidal Shock		50	G	18 msec, +/- X,Y,Z (Note1)
Half-sine Shock		180	G	3 msec, +/- X,Y,Z (Note1)
Corrosive Gas		Not Acceptable		

Note 1 : At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

6. Optical Characteristics

Item	Conditions	Specification			Unit	Notes
		Min.	Typ.	Max.		
Viewing Angle	h = 0 ,v = + 20	5				In the unit of Contrast Ratio K
	h = 0 ,v = - 20	20				
	h = +/- 40 ,v = 0	10				
	h = +/- 20 ,v = 0	45				
Contrast	h = 0 ,v = 0	60	100			In the unit of Contrast Ratio K
Response Time	Both On/Off. From/To 10% luminance To/From 90% luminance level.		30	50	msec	Ambient Temperature 25degC. At Center of LCD. h = 0 ,v = 0
White Luminance	Gray Scale L= L63 h = 0 ,v = 0. CFL Power Consumption = 1.9W	57	70		cd/m^2	At Center of LCD
Luminance Uniformity	Adjacent Area	0.80				Ratio of (Ldark / Lbright) over a circular area of 10 mm diameter placed any one of 81 points of the screen.
	Screen Total	0.59				Ratio of (Ldark / Lbright) for any two of 81 measuring points of the screen
Chromaticity	Red x		0.54			+/- 0.04
	Red y		0.35			+/- 0.03
	Green x		0.31			+/- 0.03
	Green y		0.55			+/- 0.03
	Blue x		0.16			+/- 0.03
	Blue y		0.16			+/- 0.04
White Balance	x		0.31			+/- 0.03
	y		0.36			+/- 0.03

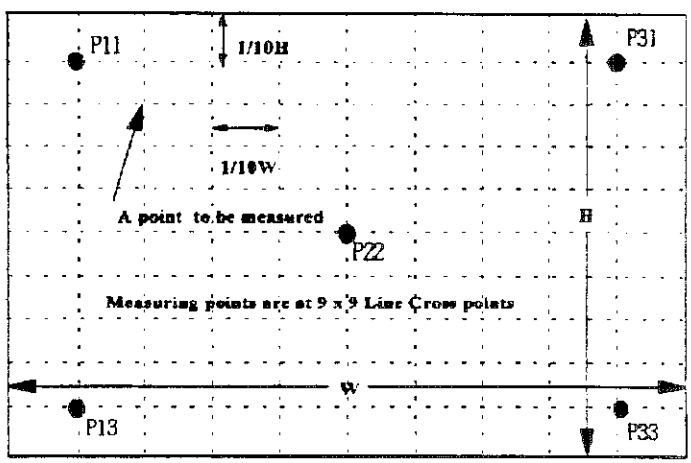
Notes for the Optical Characteristics :



- Gray Scale Level is denoted by Lxx. (ex. L00 means all Pels are in the selected state) .

(Uniformity Measurement)

- 'Lbright' represents the Luminance of the point that is brighter than the other point to be compared.
- 'Ldark' represents the Luminance of the point that is darker than the other point to be compared.
- Measuring points are at the following.



- Chromaticity and White Balance are defined as the C.I.E. 1931 x,y coordinates at the center of LCD.
- The Measurement Equipment are as shown below table.

Item	Measuring Equipment
Viewing Angle	Pritchard 1980A by Photo Research Corp.
Contrast	Pritchard 1980A by Photo Research Corp.
Response Time	LCD-5000 by Ohtsuka Elec
White Luminance	Pritchard 1980A by Photo Research Corp.
Luminance Uniformity	Pritchard 1980A by Photo Research Corp.
Chromaticity	LCD-5000 by Ohtsuka Elec
White Balance	LCD-5000 by Ohtsuka Elec

The measurement is to be done after 30 minutes of Power-on of BackLight.

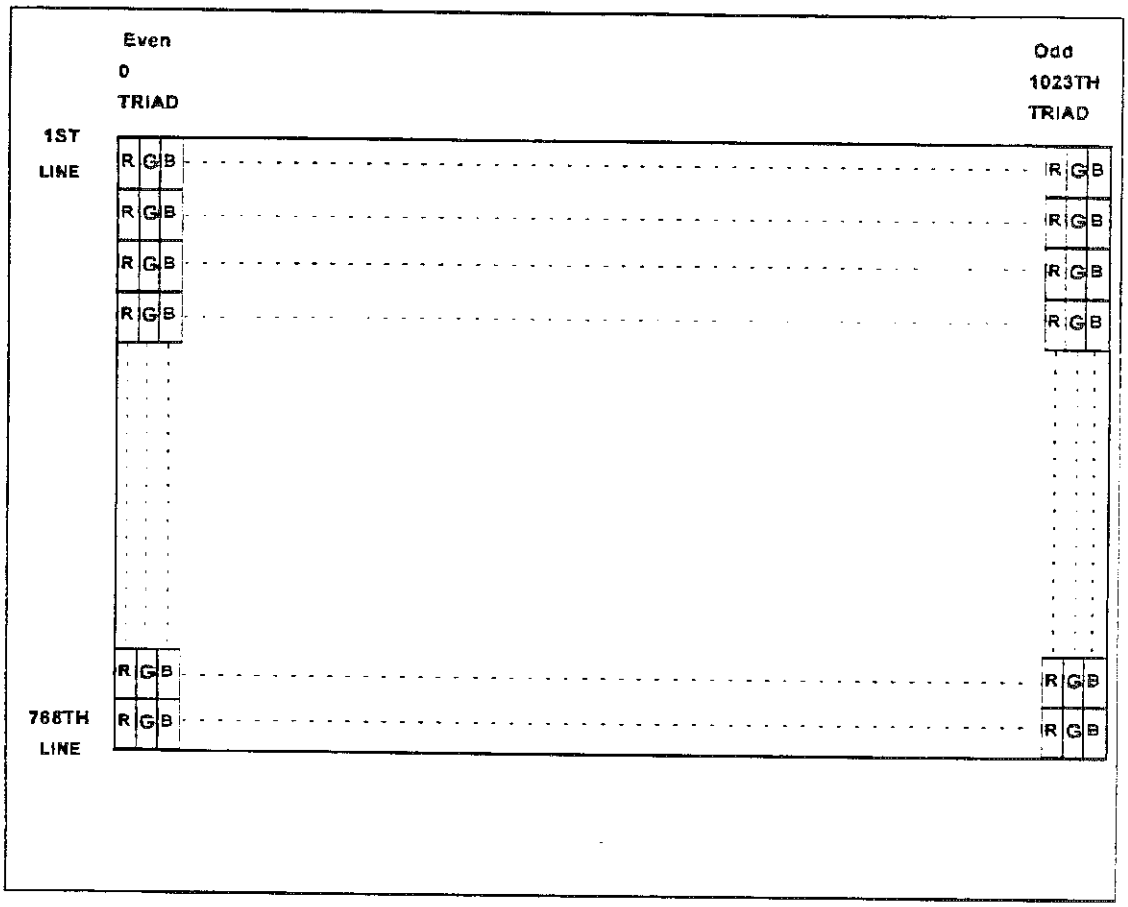
- Unless otherwise specified, the ambient conditions are as following.

Ambient Temperature : 25 ± 2 (degreeC)

Ambient Humidity : 25 - 85 (%)

Atmospheric Pressure : 86 - 106 (kPa)

7. Color Arrangement



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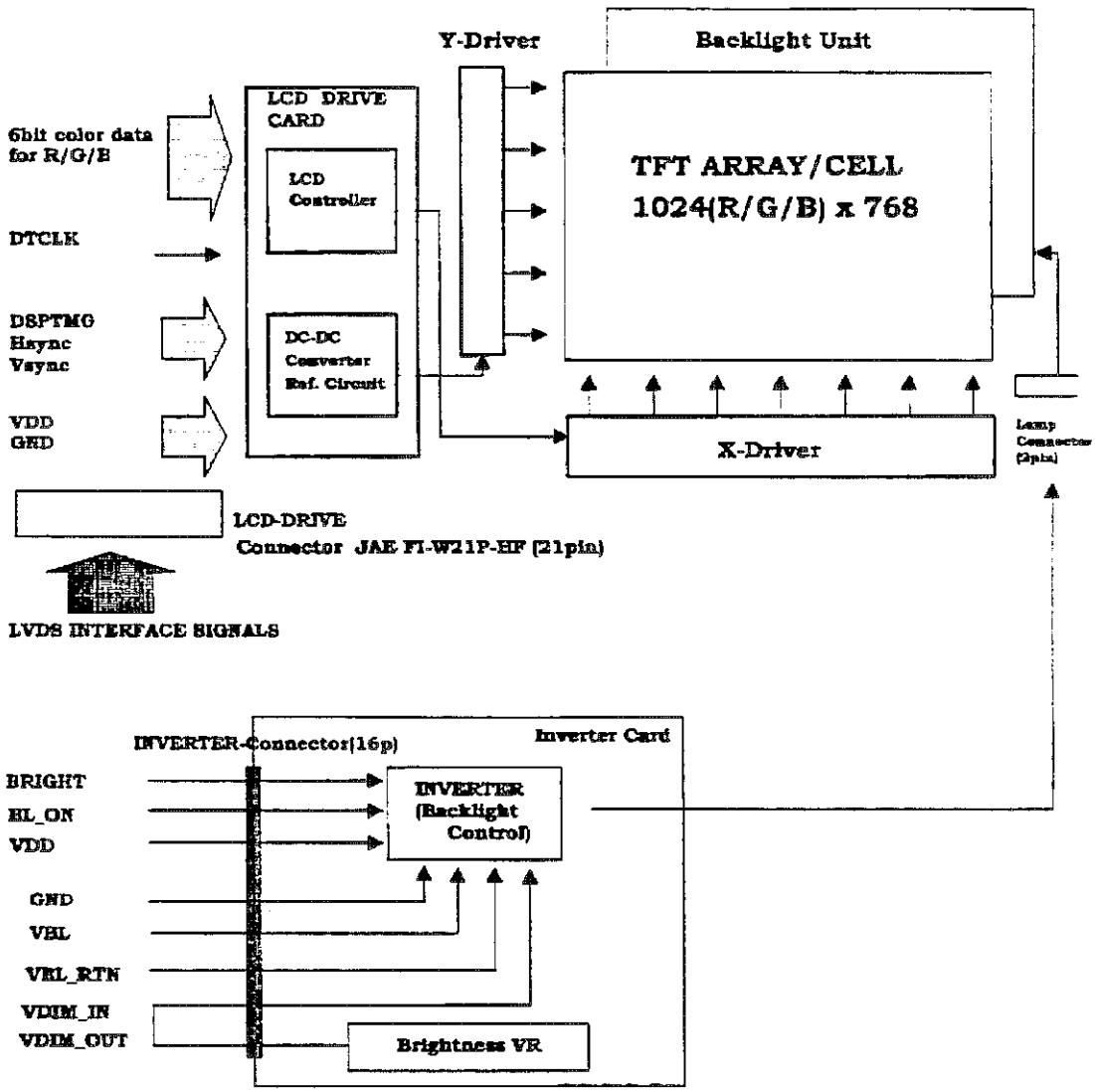
9. Block Diagram



10. Signal Interface

LCD Drive Connector	JAE	FI-W21P-HF
Corresponding Connector	JAE	FI-W21S
Contact / Part Number	JAE	FI-C3-1-0001

Pin No.	Signal Name	Description
1	RoCLKIN+	Positive LVDS differential clock input (Odd)
2	RoCLKIN-	Negative LVDS differential clock input (Odd)
3	RoIN2+	Positive LVDS differential data input (Odd B2 - B5)
4	RoIN2-	Negative LVDS differential data input (Odd B2 - B5)
5	RoIN1+	Positive LVDS differential data input (Odd G1 - G5, B0 - B1)
6	RoIN1-	Negative LVDS differential data input (Odd G1 - G5, B0 - B1)
7	RoIN0+	Positive LVDS differential data input (Odd R0 - R5, G0)
8	RoIN0-	Negative LVDS differential data input (Odd R0 - R5, G0)
9	VDD	+5V Power Supply
10	GND	
11	VDD	+5V Power Supply
12	GND	
13	ReCLKIN+	Positive LVDS differential clock input (Even)
14	ReCLKIN-	Negative LVDS differential clock input (Even)
15	ReIN2+	Positive LVDS differential data input (Even B2 - B5, HSYNC, VSYNC, DSPTMG)
16	ReIN2-	Negative LVDS differential data input (Even B2 - B5, HSYNC, VSYNC, DSPTMG)
17	ReIN1+	Positive LVDS differential data input (Even G1 - G5, B0 - B1)
18	ReIN1-	Negative LVDS differential data input (Even G1 - G5, B0 - B1)
19	ReIN0+	Positive LVDS differential data input (Even R0 - R5, G0)
20	ReIN0-	Negative LVDS differential data input (Even R0 - R5, G0)
21	Reserved	

Note: Input signals of odd and even clock shall be the same timing.

11. Signal Specification

Refer LVDS receiver Specification of DS90CF562 (National Semiconductor).

12. Inverter Connector Signal Specification

LCD Drive Connector		AMP	1-179369-6
Corresponding Connector		AMP	1-179373-6
Pin No.	Signal Name	Description	
1, 2, 3, 4	VBL		Battery Mode +8.4 or +10.8V Typ. AC Mode +16.0 or +20.0V Typ.
5, 6, 7, 8	VBL_RTN	VBL return	0V
9	+ BL_ON	Backlight ON	This signal is not synchronized to -DTCLK. When the signal is high, Backlight is Active. This signal is used to control the Backlight only.
10, 12		Reserved	No connection (Signal Reserved)
11	+ BRIGHT	Backlight Bright	This signal is not synchronized to -DTCLK. When the signal is low, the brightness shall be low to reduce power consumption. This signal is effective for battery operation.
13	GND	Signal Ground	
14	VDIM_IN	Brightness Control Input	0V (Brightness Max.) to +4V (Brightness Min.). This signal shall be connected to VDIM_OUT at user side connector when the brightness potentiometer on the inverter card isused.
15	VDD	+5V	
16	VDIM_OUT	Brightness Control Output	

Note: Output signals from system shall be low or Hi-Z state when VDD is off.

13. Lamp Charcteristics

Parameter Name	Symbol	Min.	Typ.	Max.	Unit	Note
CFL Kick-off Voltage	V_S	-	-	1,100	[V_{RMS}]	T_{amb}=25 degC *4
		-	-	1,500		T_{amb}= 0 degC *4
CFL Discharge Current	I_{CFL}	1.5 *6	-	5.0	[mA_{RMS}]	Total operating range
		-	3.1	-		Screen 70 [cd/m^2], T_{amb}=25degC
CFL Discharge Voltage	V_{CFL}	-	620	-	[V_{RMS}]	Screen 70 [cd/m^2], T_{amb}=25degC
CFL Power Consumption	P_{CFL}	-	1.9	-	[W]	Screen 70 [cd/m^2], T_{amb}=25degC
CFL Discharge Frequency	F_{CFL}	30	40	70*6	[kHz]	Reference*5

Note

*1 All of characteristics listed are measured under the condition using the IBM optional inverter (IBM P/N 46H3650).

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

14. Interface Timing defined at the LVDS Receiver Output

Basically ,interface timings should match the VESA 1024 x 768 60Hz manufacturing guideline timing.

Symbol	Signal Description	MIN.	TYP	MAX.	UNIT
f_{dck}	DTCLK Frequency		32.50	32.67	MHz
t_{ck}	DTCLK cycle time		30.77		nsec
t_{wcl}	DTCLK low width	4			nsec
t_{wch}	DTCLK high width	4			nsec
t_{ds}	Data set up time	3			nsec
t_{dh}	Data hold time	6			nsec
t_{dts}	DSPTMG set up time	3			nsec
t_{dth}	DSPTMG hold time	6			nsec
t_x	X total time	576	672		t_{ck}
t_{acx}	X active time		512		t_{ck}
t_{blkx}	X blank time		160		t_{ck}
H_{sync}	H-frequency		48.36		KHz
H_w	H-sync width	4			t_{ck}
t_y	Y total time		806		t_x
t_{acy}	Y active time		768		t_x
V_{sync}	Frame rate	(55)	60.00	61.00	Hz
V_w	V-sync width	2	4		t_x
V_{fp}	V-sync front porch	1	1		t_x
V_{bp}	V-sync back porch	6	29	63	t_x

Note: t_x (X total time) should be the same total time during 1 frame.

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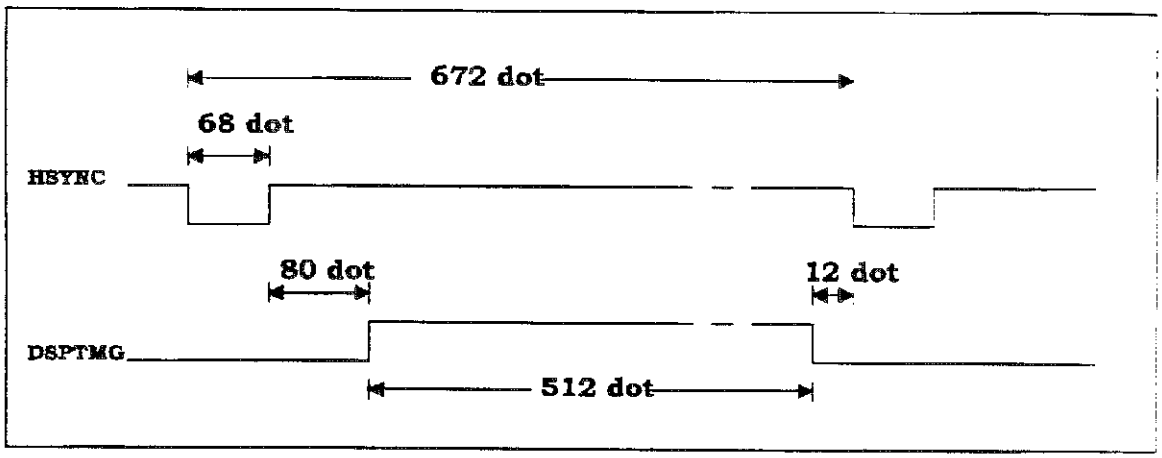
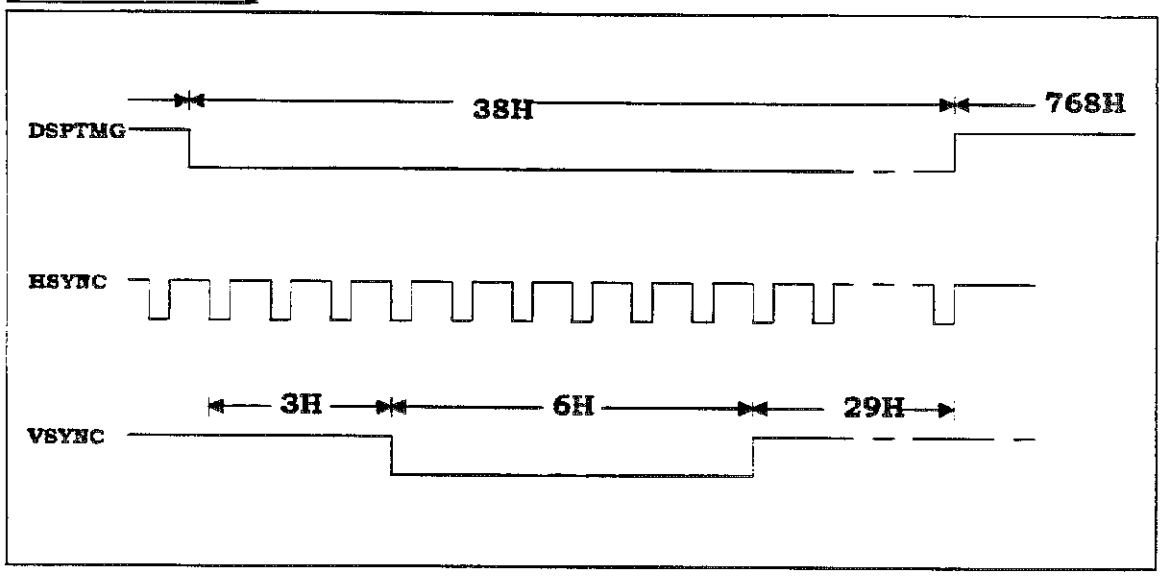
15. Horizontal Timing



16. Vertical Timing

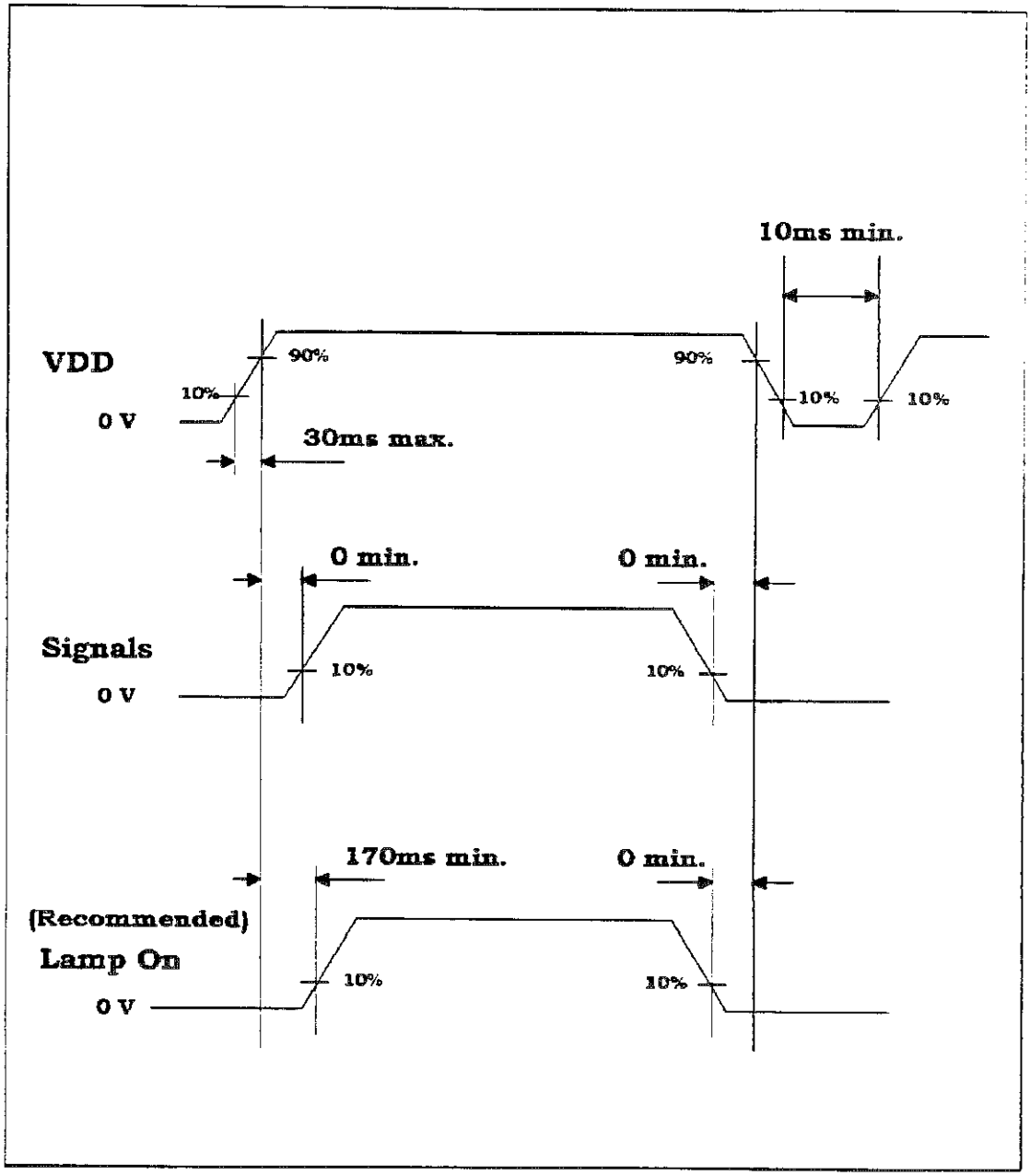


17. Power Requirement

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit	CONDITION
VDD	Logic/LCD Drive Voltage	+4.75	+5.0	+5.25	V	Load Capacitance 20uF
PDD	VDD Power		1.4		W	VDD=+5.0V
PL	Lamp Power(w/o inverter)		2.8		W	
PDD+PL	Total Power(w/o inverter)		4.2		W	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

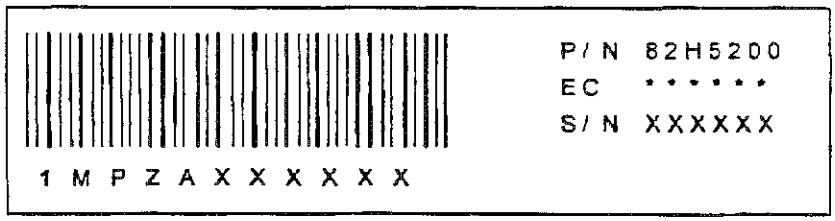
Note: This requirements shall be met with 'All black pattern'.

18. Power ON/OFF sequence



19. Product Label

Serial Number Label



Week Code Label

There are two labels at the front limb of the Module Frame.

One is the Serial Number Label and the other is the Week Code Label.

The first 4 digits of the Bar code shows the Module Type ITXG60L.

The fifth digit is for the manufacturing location code.

YY and WW of the Week Code stand for the Year and the Week of the Year of manufacturing of the Module respectively.

20. Handling Precautions

(REFER ALSO THE FIGURES ON NEXT PAGE)

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or creak if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

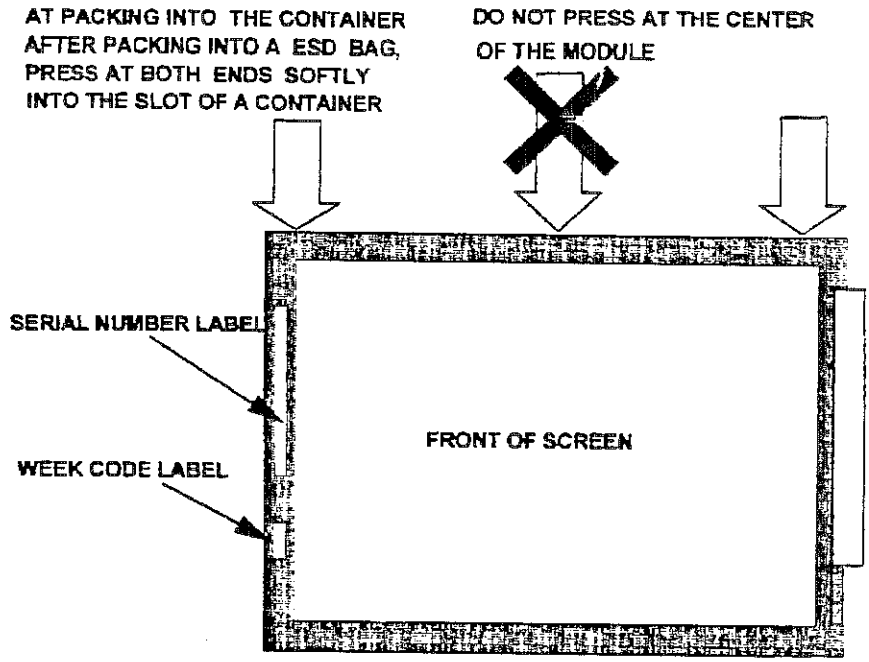
7) Do not open nor modify the Module Assembly.

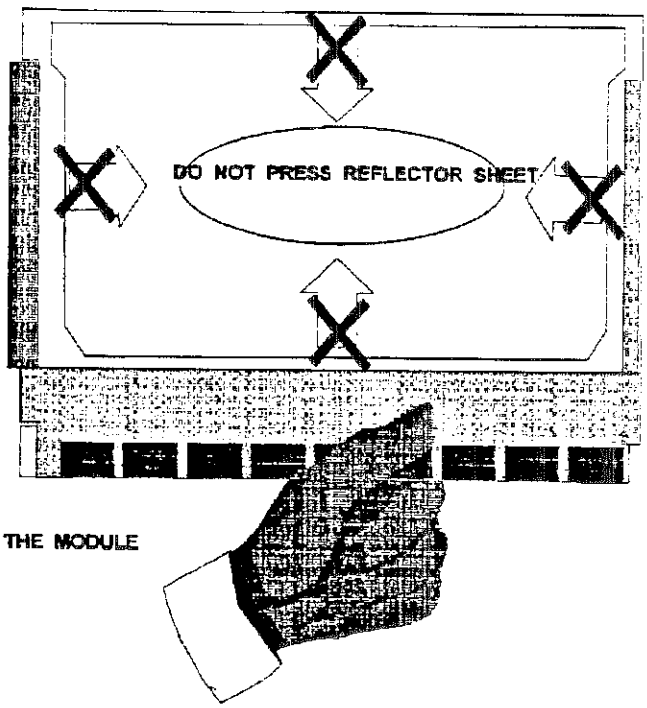
8) Do not press the reflector sheet at the back of the module to any directions.

9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.

10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module. Also be sure to support the metal frame of the TFT Module (by hand, for example) just at the reverse side of the Connector so that the Module itself is not twisted nor bent. Otherwise the TFT Module may be damaged.

11) At and after installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.





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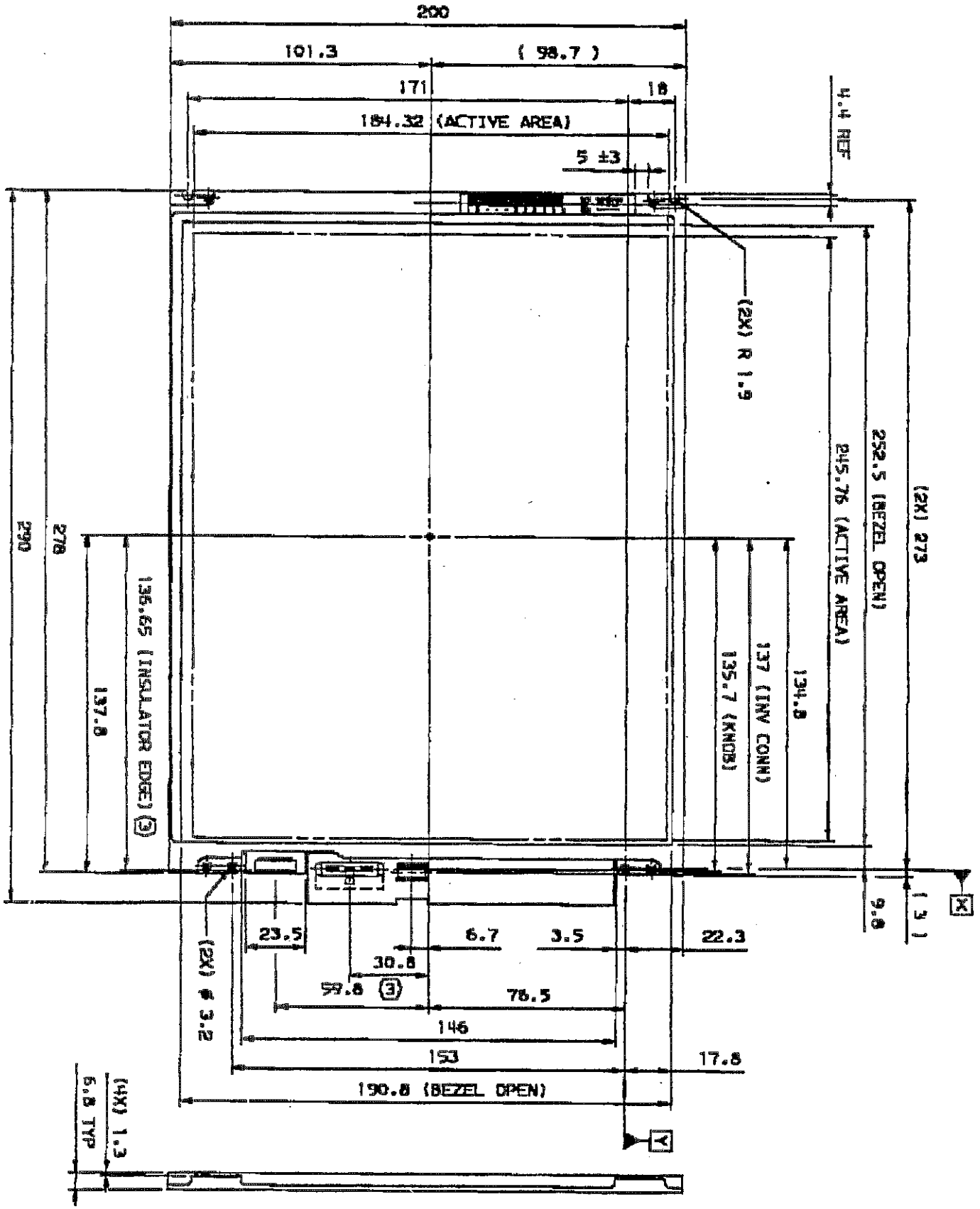
200
101.3
(98.7)
171
18
184.32 (ACTIVE AREA)
5 ±3
4.4 REF
(2X) R 1.9
252.5 (BEZEL OPEN)
245.76 (ACTIVE AREA)
(2X) 273
290
278
135.65 (INSULATOR EDGE) (3)
137.8
137 (INV CONN)
135.7 (KNOB)
134.8
9.8
(3)
X
23.5
6.7
3.5
22.3
30.8
59.8 (3)
78.5
146
153
17.8
(2X) ø 3.2
190.8 (BEZEL OPEN)
Y
(4X) 1.3
6.8 TYP