ITXG71

35.8cm(14.1 inch) XGA(1024x768) Color TFT LCD Module

ITXG71 is a color TFT LCD module to be designed for the display of a notebook-style personal computer. In addition to its large screen,the characteristics of this module are light weight, slim/thin outline, low power consumption and high resolution of XGA(1024x768) capability.

Features

- 35.8cm(14.1 inch) diagonal
- Native 262k colors (R/G/B 6bit each)
- XGA 1024 x 768 pixels
- Low Reflection (Black Matrix)
- 304mm x 230mm x 8.5mm typ. (without inverter)
- 655 g typ.(without inverter)
- 4.1 W typ.(without inverter)
- Single LVDS interface (TI SN75LVDS86 or Compatible)
- Side mount type

Applications

- Notebook PCs
- Monitors

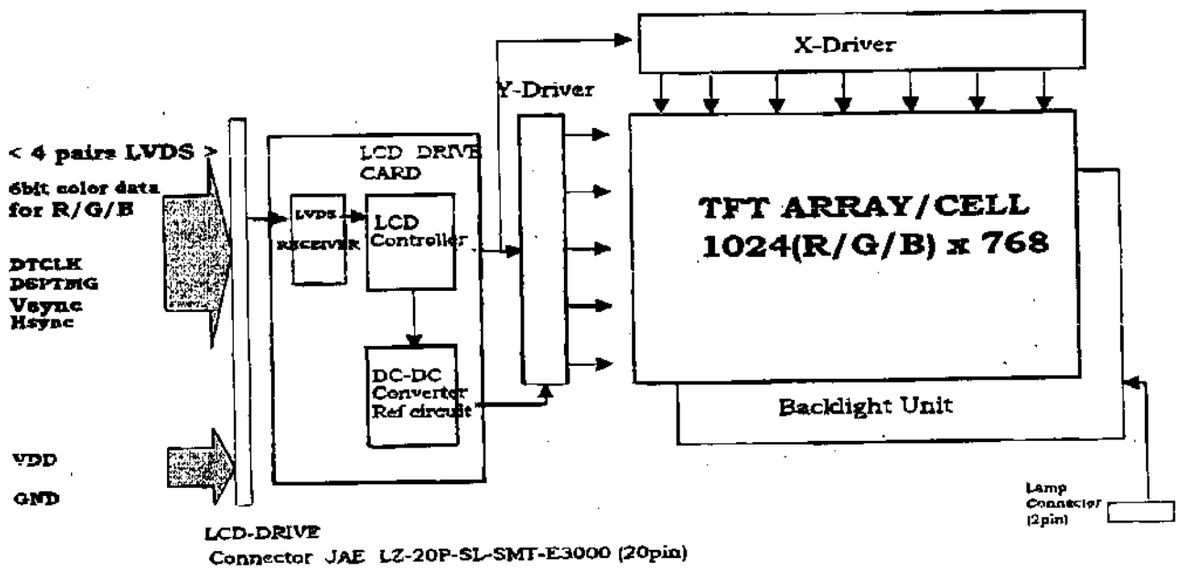
Characteristics Summary

Screen Diagonal	35.8cm(14.1")
Active Area	285.7mm(H) x 214.3mm(V)
Pixel Format	1024(x3) x 768
Pixel Pitch	0.279(per one triad) x 0.279
Pixel Arrangement	R,G,B Vertical Stripe
Display Mode	Normally White
White Luminance	90 cd/m^2 Typ. (CFL Dischsrge Current = 3.8 mA$_{rms}$)
Contrast Ratio	100 : 1 Typ.
Optical Rise Time/Fall Time	30 msec. Typ., 50msec. Max.
Nominal Input Voltage VDD	 +5.0V
Power Consumption (without inverter) (VDD line + Lamp input line)	4.1W Typ.
Weight	655 grams Typ. (w/o inverter)
Physical size	304mm x 230mm x 8.5mm typ. (w/o inverter)
Electrical Interface	R/G/B Data, 3 Sync signals, Clocks in 4 pairs LVDS and VDD, GND
Supported Colors	Native 262k colors
Temperature Range Operating Storage	 +0 to +50 degC -20 to +60 degC

Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	VDD	-0.3 to +6.0	V	
Lamp Current	Icfl	7	mArms	
Storage Temperature	TST	-20 to + 60	degC	At the glass surface
Operation Tempraute	TOP	0 to +50	degC	At the glass surface
Operation Humidity		8 to 95	%RH	Max wet bulb temp. 39 degC No condensation

Block Diagram



OEM Spec.

Signal Interface

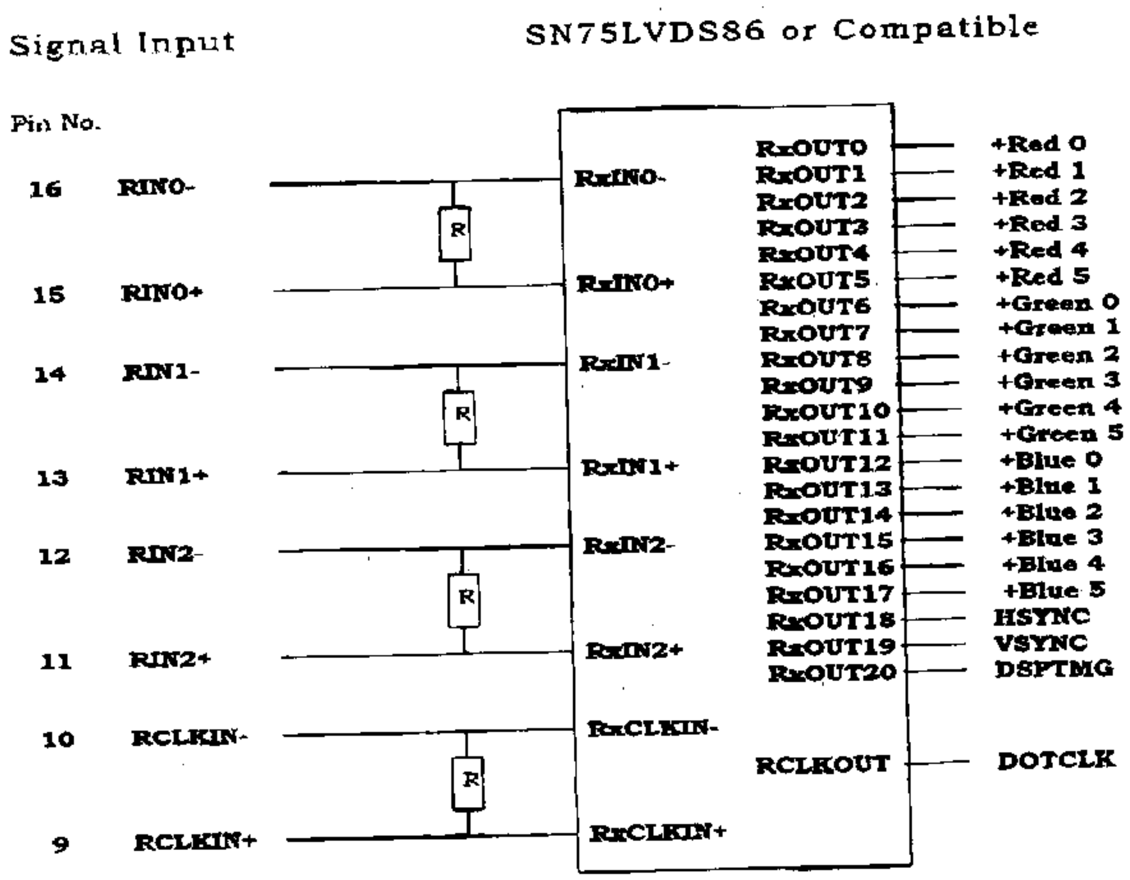
LCD Drive Connector	JAE	LZ-20P-SL-SMT-E3000
Corresponding Connector	JAE	LZ-20S-SC3
Corresponding Contact	JAE	LZ-SC-C3-A1-15000

Pin No.	Signal Name	Description
1		No Connection
2		No Connection
3		No Connection
4		No Connection
5		No Connection
6		No Connection
7		No Connection
8	-	No Connection
9	RCLKIN+	Positive LVDS differential clock input
10	RCLKIN-	Negative LVDS differential clock input
11	RIN2+	Positive LVDS differential data input (B2 - B5, HSYNC, VSYNC, DSPTMG)
12	RIN2-	Negative LVDS differential data input (B2 - B5, HSYNC, VSYNC, DSPTMG)
13	RIN1+	Positive LVDS differential data input (G1 - G5, B0 - B1)
14	RIN1-	Negative LVDS differential data input (G1 - G5, B0 - B1)
15	RIN0+	Positive LVDS differential data input (R0 - R5, G0)
16	RIN0-	Negative LVDS differential data input (R0 - R5, G0)
17	GND	
18	GND	
19	VDD	+5.0V Power Supply
20	VDD	+5.0V Power Supply

Note: Above connection is applied for LVDS Single Channel interface.

Internal Circuit

Refer LVDS receiver Specification of SN75LVDS86 (Texas Instruments)for the details of the guidelines in developing the interface cable and systems.

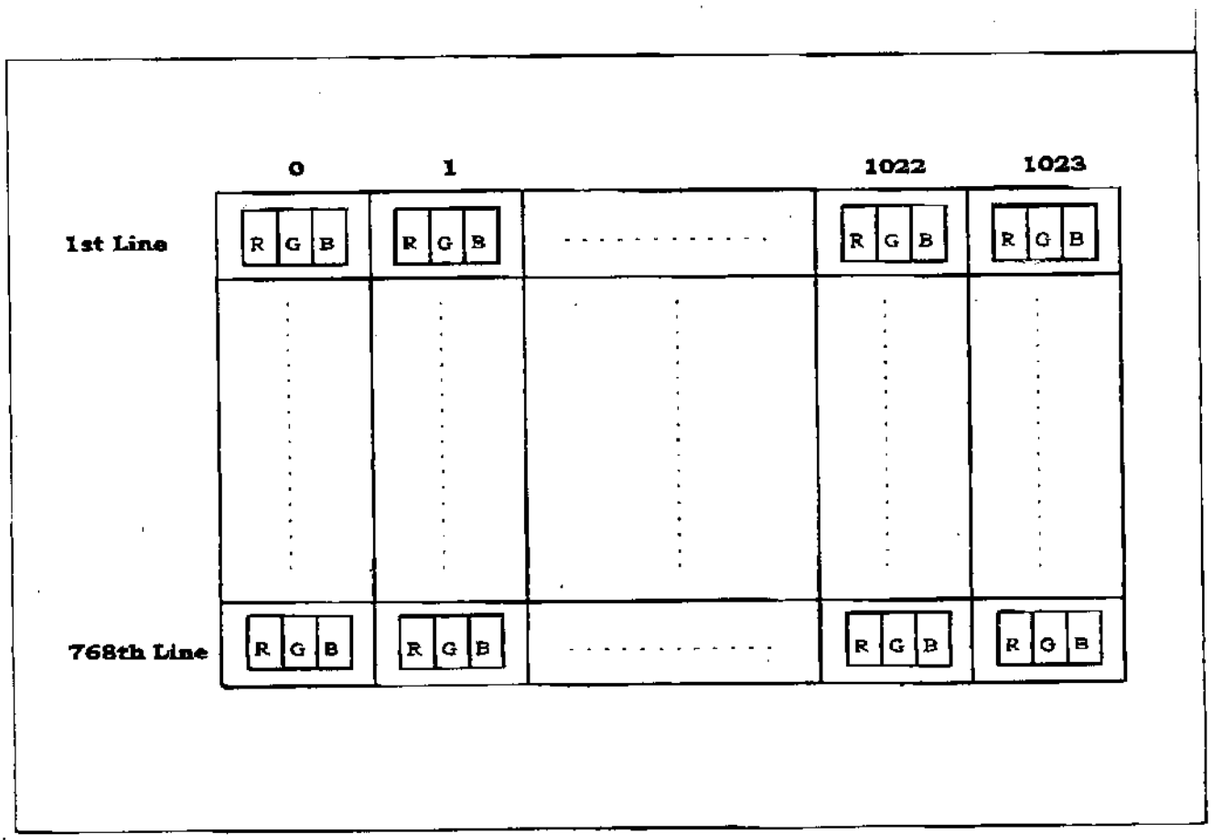


The LCD module uses a 100 ohm resistor between positive and negative lines of each receiver input.

Note : It is recommended that two Ground Wires and two Power Wires in the interface cables are with AWG#28. (Data wires can be AWG#32.)

Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.



Signal Description

Signal Name	Description	
+RED5	Red Data 5	(MSB)
+RED4	Red Data 4	
+RED3	Red Data 3	
+RED2	Red Data 2	
+RED1	Red Data 1	
+RED0	Red Data 0	(LSB)
	Red-Pixel-Data	Each red pixel's data consists of these 6 bits pixel data
+GREEN5	Green Data 5	(MSB)
+GREEN4	Green Data 4	
+GREEN3	Green Data 3	
+GREEN2	Green Data 2	
+GREEN1	Green Data 1	
+GREEN0	Green Data 0	(LSB)
	Green-Pixel-Data	Each green pixel's data consists of these 6 bits pixel data
+BLUE5	Blue Data 5	(MSB)
+BLUE4	Blue Data 4	
+BLUE3	Blue Data 3	
+BLUE2	Blue Data 2	
+BLUE1	Blue Data 1	
+BLUE0	Blue Data 0	(LSB)
		Each blue pixel's data consists of these 6 bits pixel data
-DTCLK	Data Clock	The typical frequency is 65MHz.The signal is used to strobe the pixel data and +DSPTMG signals.All pixel data shall be valid at the falling edge when the +DSPTMG signal is high.
+DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK.When the signal is high,the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK. Sync Polarity : Negative
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK. Sync Polarity : Negative

Note: Output signals from system shall be low or Hi-Z state when VDD is off.

Signal Interface for Lamp

Lamp Connector		JST	BHSR-02VS-1
Mating Connector		JST	SM02B-BHSS-1-TB
Pin No.	Signal Name	Description	
1	Lamp High		
2	Lamp Low	(GND)	

Signal Specification

Differential Input Voltage for LVDS Receiver Threshold *1

Parameter	Condition	Min.	Max.	Unit
Vih	Differential Input High Threshold (VCM = +1.2V)		+100	mV
Vil	Differential Input Low Threshold (VCM = +1.2V)	-100		mV

Note *1 It is recommended to refer the specifications of SN75LVDS86 (Texas Instruments).

Lamp Interface Specification

Absolute Maximum Rating

Parameter Name	Symbol	Value	Unit	Note
CFL Discharge Current	I_{CFL}	7.5 Max	[mA_{RMS}]	Exclude inrush current
CFL Inrush Current	IR_{CFL}	30 Max	[mA_{0-P}]	T = 50 Max. [mSec]

Lamp Charcteristics

Parameter Name	Symbol	Min.	Typ.	Max.	Unit	Note
CFL Kick-off Voltage	V_S	-	-	1,100	[V_{RMS}]	T_{amb}=25 degC *1
		-	-	1,500		T_{amb}= 0 degC *1

*1 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until dischargement.

Parameter Guideline for CFL Inverter*1

Parameter Name	Symbol	Min.	Typ.	Max.	Unit	Note
CFL Discharge Current	I_{CFL}	-*6	-	7.0	[mA_{RMS}]	Total operating range
		-	3.8	-		Screen 90 [cd/m^2],25degC
CFL Discharge Voltage	V_{CFL}	-	640	-	[V_{RMS}]	Screen 90 [cd/m^2], T_{amb}=25 degC
CFL Power Consumption	P_{CFL}	-	2.4	-	[W]	Screen 90 [cd/m^2], T_{amb}=25 degC
CFL Discharge Frequency	F_{CFL}	30	40	70*5	[KHz]	Reference*5,6

Note

*1 All of characteristics listed are measured under the condition using IBM Test Inverter.

*2 In case of using an inverter , it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 The minimum CFL current varies depending on the dimming methdology (PWM or Duty) and also on the electrical characteristics of the inverter used.

Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

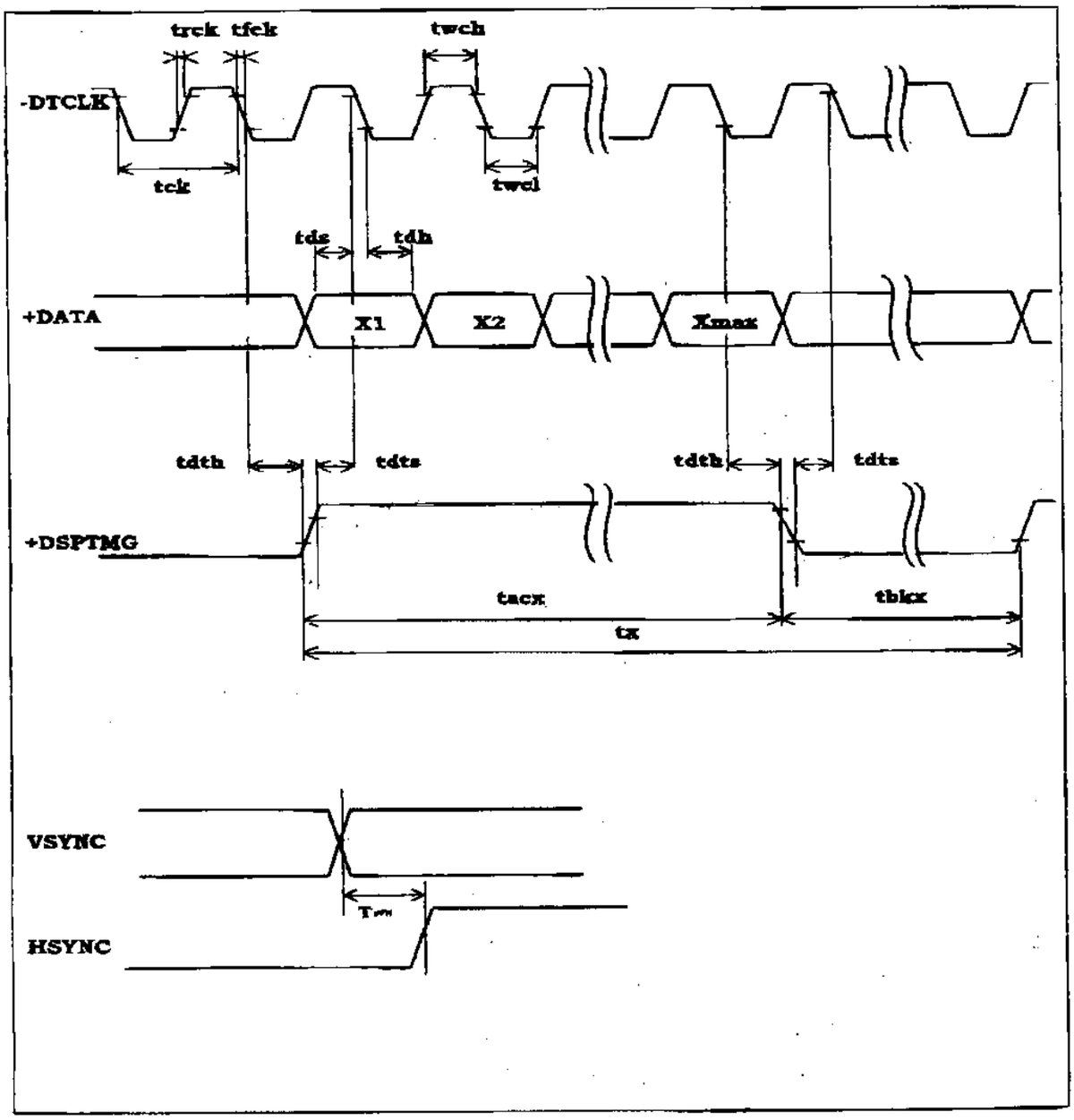
Interface Timings

Basically, interface timings should match the VESA 1024 x 768 Hz manufacturing guide line timing.

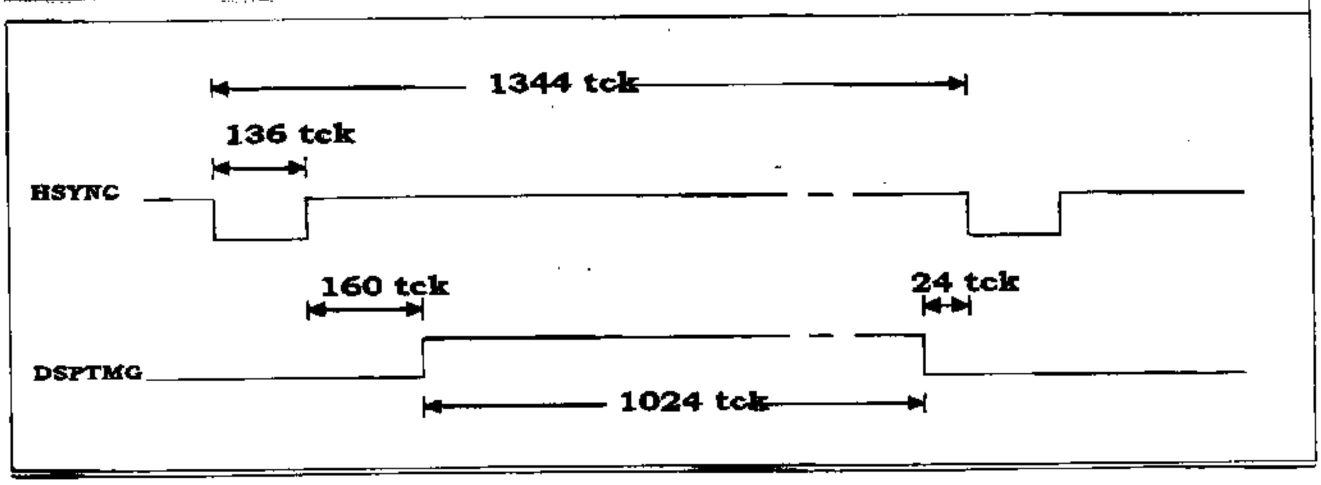
Symbol	Signal Description	MIN	TYP	MAX	UNIT
f_{dck}	DTCLK Frequency		65.00	65.34	MHz
t_{ck}	DTCLK cycle time		15.38		nsec
t_{wcl}	DTCLK low width	5			nsec
t_{wch}	DTCLK high width	6			nsec
t_{ds}	Data set up time	4			nsec
t_{dh}	Data hold time	4			nsec
t_{dts}	DSPTMG set up time	4			nsec
t_{dth}	DSPTMG hold time	4			nsec
t_x	X total time	1206	1344	(2047)	t_{ck}
t_{acx}	X active time	129	1024		t_{ck}
t_{blcx}	X blank time	90	320		t_{ck}
Hfp	H-sync front porch	0	24		t_{ck}
Hbp	H-sync back porch	1	160		t_{ck}
H_{sync}	H-frequency		48.36		KHz
H_w	H-sync width	4	68	$t_x/2$	t_{ck}
t_y	Y total time	771	806	1023	t_x
t_{acy}	Y active time	1	768		t_x
t_{bly}	Y blank time	1	38		t_x
V_{sync}	Frame rate		60.00	61.00	Hz
V_w	V-sync width	1	6	$t_y/2$	t_x
V_{fp}	V-sync front porch	0	3		t_x
V_{bp}	V-sync back porch	1	29		t_x
T_{pvh}	Vsync - Hsync Phase difference	1			t_{ck}

Note: t_x (X total time) should be the same total time during 1 frame.

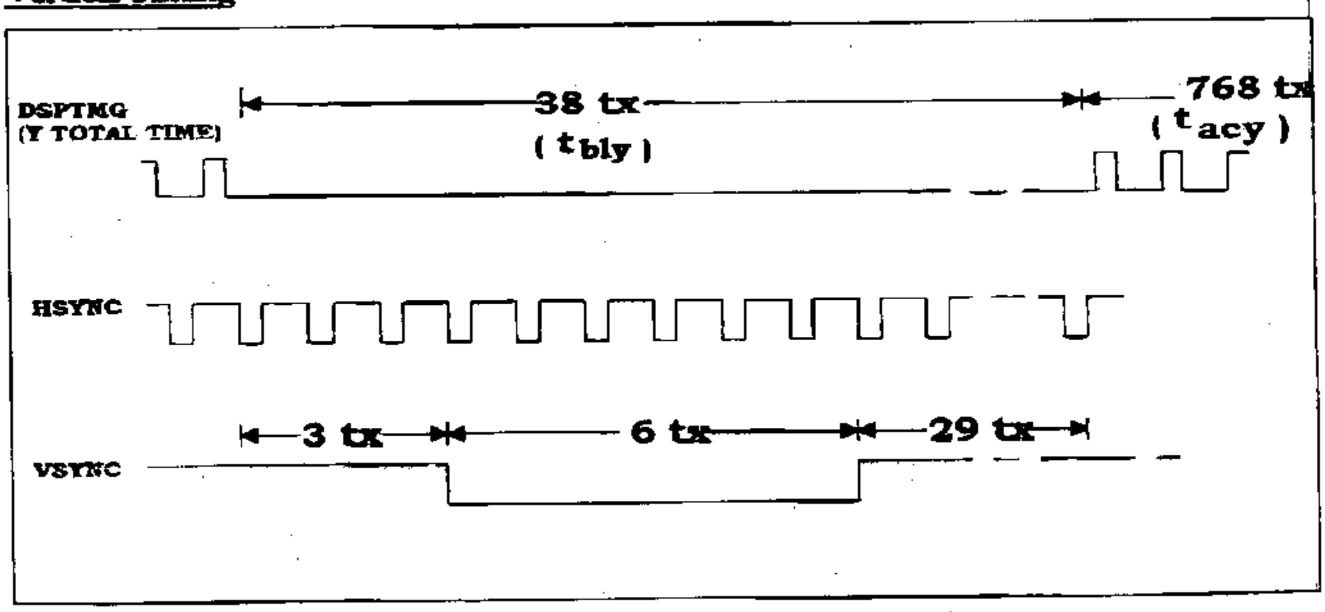
Interface Timings Defenition



Horizontal Timing



Vertical Timing



OEM Spec.

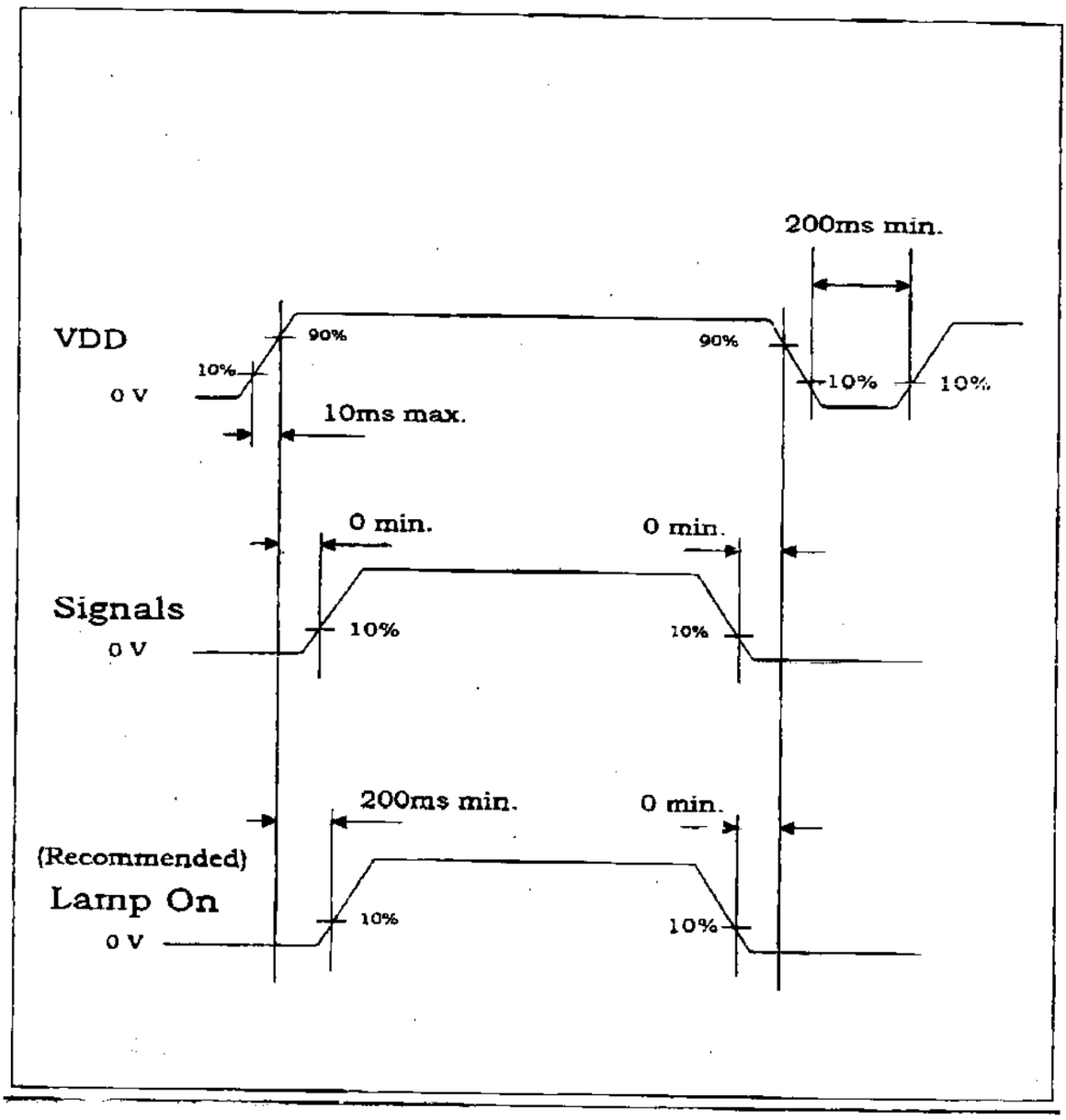
Power Requirement

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit	CONDITION
VDD	Logic/LCD Drive Voltage	+4.75	+5.0	+5.25	V	Load Capacitance 20uF
PDD	VDD Power		1.7		W	VDD= +5.0V All black pattern
				TBD		VDD= +5.0V Sub-pixel vertical stripe
PL	Lamp Power(w/o inverter)		2.4		W	90 nit (25 degC)
PDD+PL	Total Power(w/o inverter)		4.1		W	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

Note 1: This requirements shall be met with 'All black pattern' unless otherwise specified.

Note 2: The Sub-pixel vertical stripe is the vertical stripe pattern where sub-pixels are On and Off at every other vertical line.

Power ON/OFF sequence



Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or creak if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) At and after installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

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OEM Spec.

Reference Drawing For details refer Drawing P/N 09J0932

Note : Patens are under application for the design and the mounting mechanism of this panel.

OEM Spec.

PRELIMINARY

REL FOR ASM	QTY	TECHNICAL APPROVAL				DATE	EC NO.		DATE	EC NO.
		ELECTRICAL				06NOV96	961106		21APR97	
		MATERIAL				13NOV96	961113		15MAY97	E67806
					ET	20DEC96	961220			
					DAT	07MAR97	E67805			

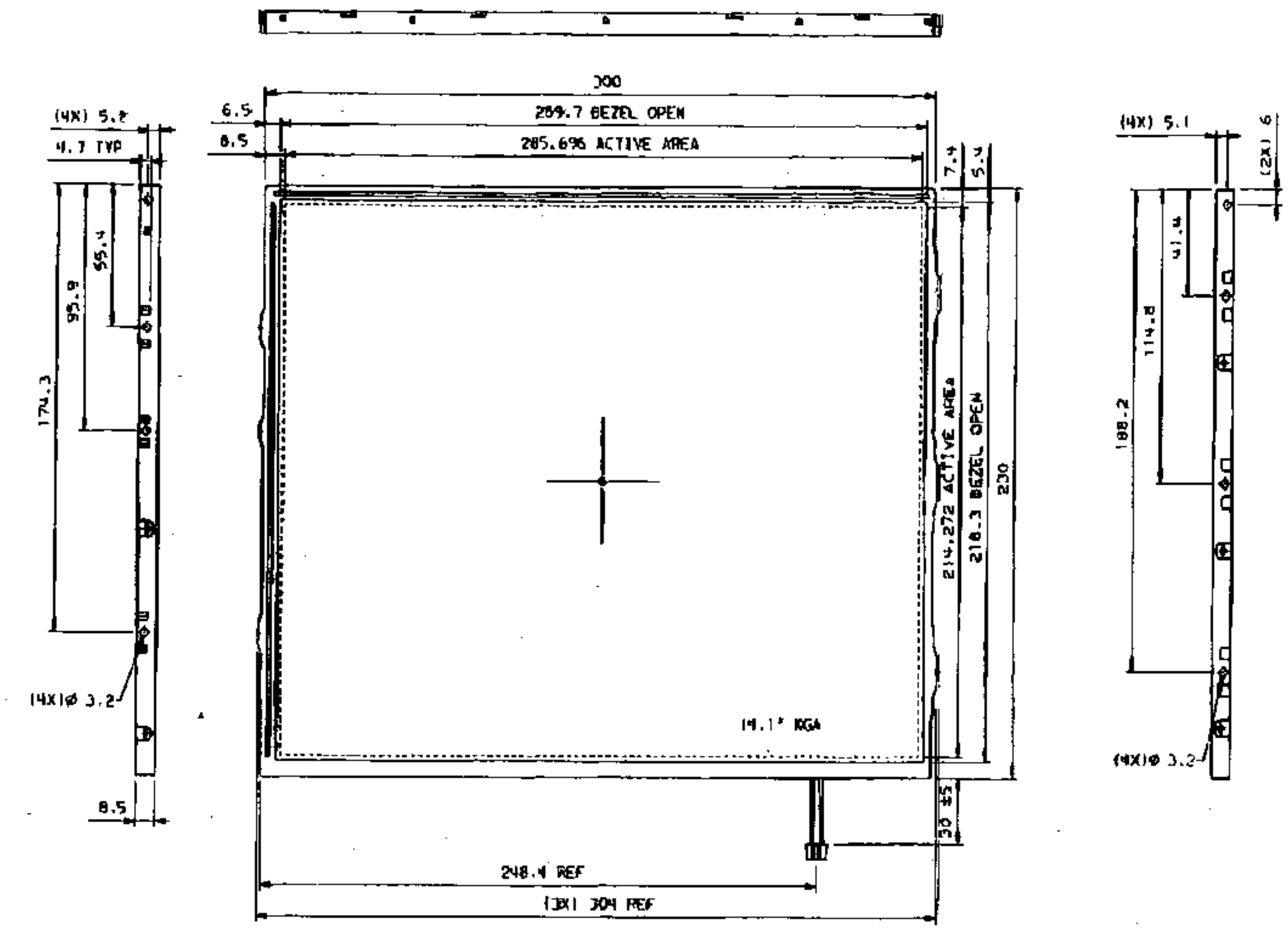
PART NO. ITXG71

DEVELOPMENT NO. | Q/N

USAGE CODE

SHE 1 - 2

NOTE
① CONNECTOR TO BE JAE INDUSTRY LTD. "LZ-20P-SL-SMT".



SHE 1 - 2

ITXG71

IBM MATERIAL NO.		MUST CONFORM TO ENG SPEC: 80X2324		
MATL ALTERNATE NO.		TOLERANCES UNLESS NOTED		
		LINEAR ±		0.3
CASE DEPTH		ANGLES ±		
HARDNESS		RADII UNLESS NOTED		
SURFACE TREATMENT	CODE NO.	EDGE/CORNER BREAKS	OUTSIDE MAX	
			INSIDE MAX	

SCALE: 1/1

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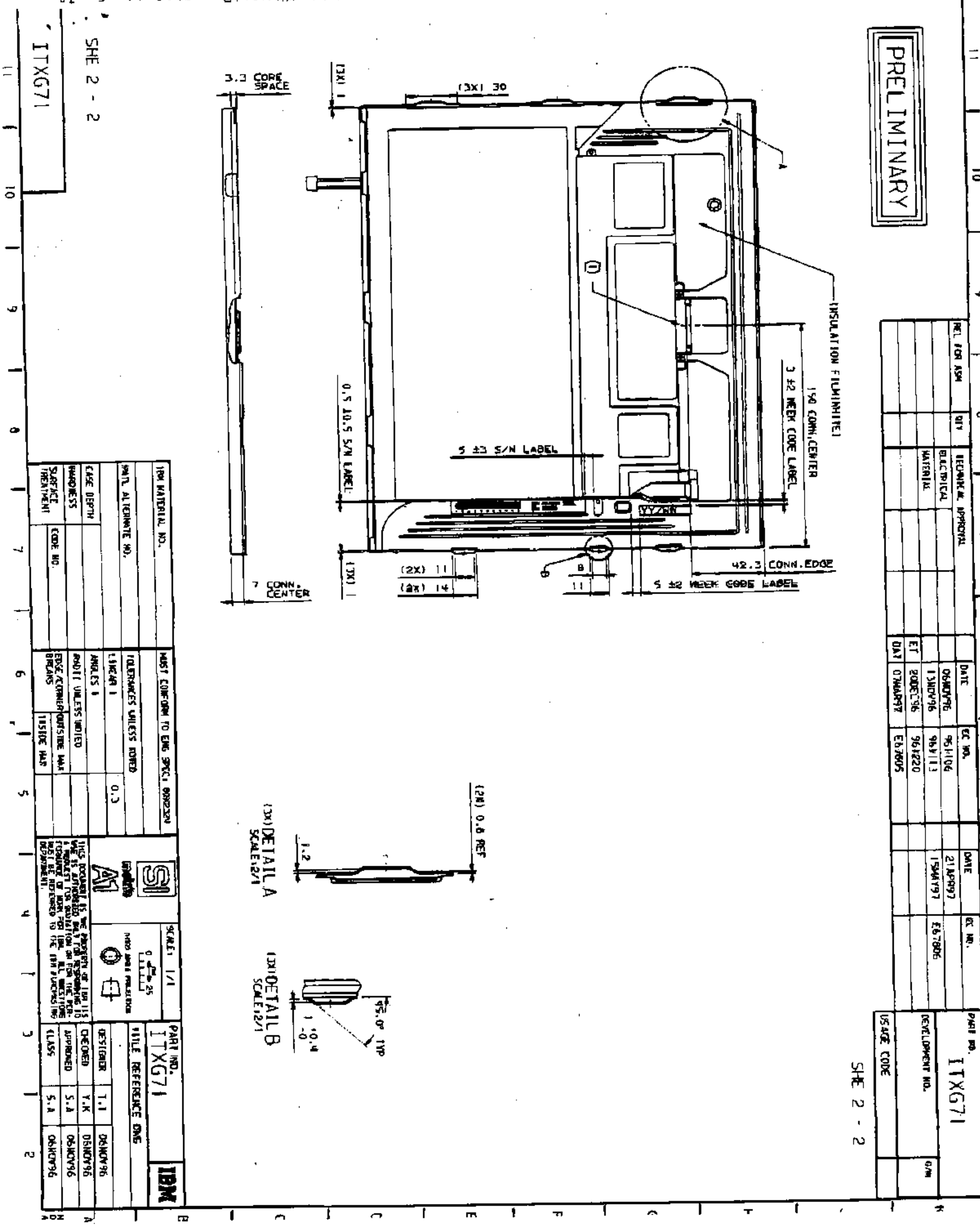
PART NO. ITXG71 IBM

TITLE REFERENCE DWG

DESIGNER	T.F	06NOV96
CHECKED	Y.K	06NOV96
APPROVED	S.A	06NOV96
CLASS	S.A	06NOV96


PRELIMINARY
ITXG71
SHE 2 - 2
3.3 CORE SPACE
(3X) 30
(3X) 1
INSULATION FILM(WHITE)
150 CONN.CENTER
3 ±2 WEEK CODE LABEL
0.5 ±0.5 S/N LABEL
5 ±3 S/N LABEL
42.3 CONN.EDGE
5 ±2 WEEK CODE LABEL
(2X) 11
(2X) 14
7 CONN. CENTER
(2X) 0.6 REF
(3X) DETAIL A
SCALE 2/1
(3X) DETAIL B
SCALE 2/1
45.0° TYP
IBM MATERIAL NO.
MATL ALTERNATE NO.
CASE DEPTH
HARDNESS
SURFACE TREATMENT
CODE NO.
MUST CONFORM TO ENG SPEC
TOLERANCES UNLESS NOTED
LINEAR ±
ANGLES ±
0.3
EDGE/CORNER/OUTSIDE MAX BREAKS
INSIDE MAX
SCALE 1/1
PART NO.
ITXG71
TITLE REFERENCE DWG
DESIGNER T.I 06NOV96
CHECKED Y.K 06NOV96
APPROVED S.A 06NOV96
CLASS S.A 06NOV96
IBM
REL FOR ASM
QTY
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ELECTRICAL
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96X220
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DEVELOPMENT NO.