SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**
(◆) **Final Specification**

Title	14.1" WXGA TFT LCD

Customer	DELL
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP141WX3
Suffix	TLQ1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
K. J. Kwon / G.Manager	
REVIEWED BY	
S.R. Kim / Manager	
PREPARED BY	
K. T. Moon / Engineer	

Products Engineering Dept.
LG Display Co., Ltd

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RECORD OF REVISIONS

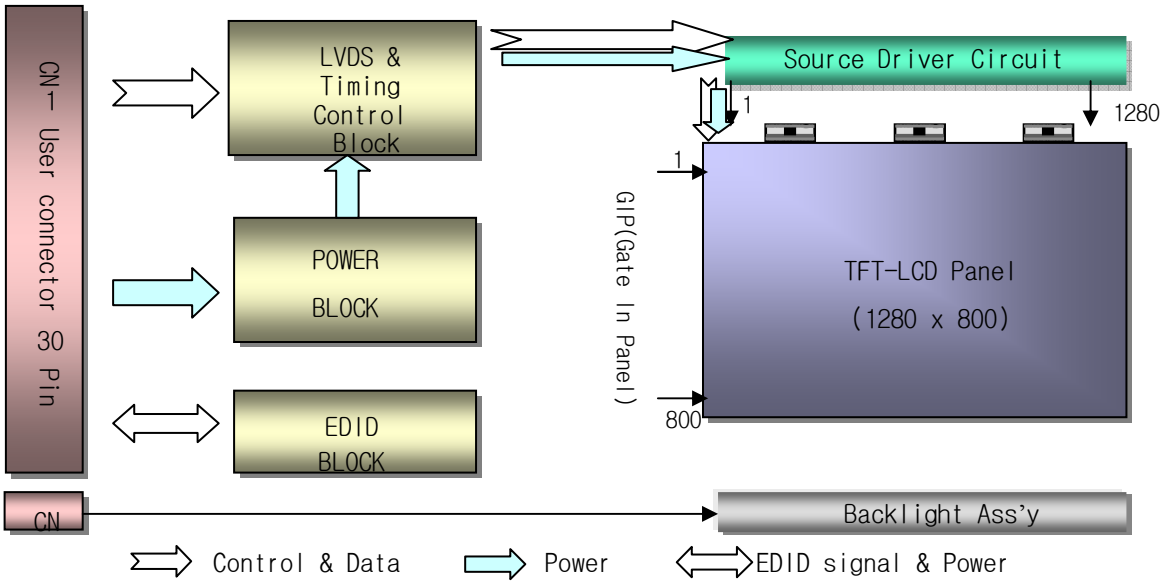
Revision No	Revision Date	Page	Description	EDID ver
0.0	Aug 30. 2007	-	First Draft (Preliminary Specification)	0.0
0.1	Mar 06. 2008	4, 6	Be updated Power Consumption	
			Logic 1.25W(Mosaic)	
		20	Be updated Label Code(2D drawing)	
		29~31	EDID update(be updated product code)	0.1
			page 29 Product code : 0000 → 2B01	
			page 29 Year of Manufacture : 11 → 12	
			page 31 Changed SMBUS Data : ** → 00	
			page 31 EDID check sum : 97 → 0E	
1.0	Mar. 28. 2008	All	Final specification	

1. General Description

The LP141WX3 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp (CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 14.1 inches diagonally measured active display area with WXGA resolution(800 vertical by 1280 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors.

The LP141WX3 has been designed to apply the interface method that enables low power, high speed, low EMI.

The LP141WX3 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP141WX3 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	14.1 inches diagonal
Outline Dimension	319.5(H,Typ.) × 205.5(V,Typ.) × 5.5(D,Max.) [mm]
Pixel Pitch	0.2373mm × 0.2373 mm
Pixel Format	1280 horiz. By 800 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	200 cd/m^2(Min.5 point)
Power Consumption	Total 5.45 Watt(Typ.) @ LCM circuit 1.25 Watt(Typ.), B/L input 4.2Watt(Typ.)
Weight	425g(Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Anti-glare treatment of the front polarizer
RoHS Comply	Yes

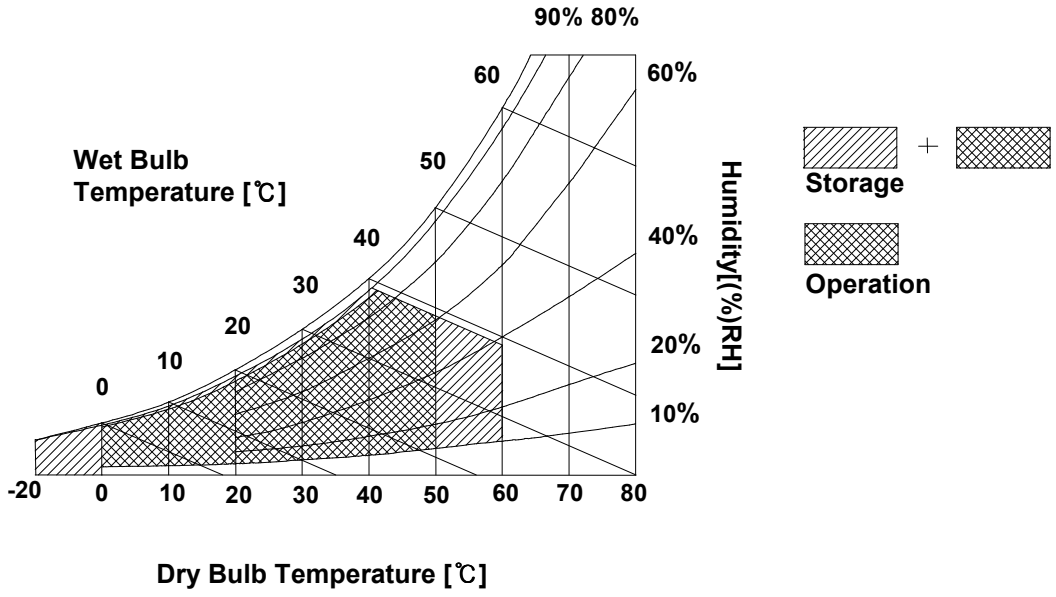
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

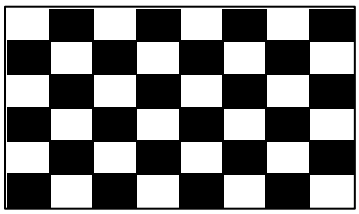
The LP141WX3 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
MODULE :						
Power Supply Input Voltage	VCC	3.0	3.3	3.6	V_{DC}	
	I_{CC} [Mosaic	320	380	440	mA	1
Power Consumption	Pc	-	1.25	1.6	Watt	1
Differential Impedance	Zm	90	100	110	Ohm	2
LAMP :						
Operating Voltage	V_{BL}	640(7.0mA)	667(6.3mA)	880(2.0mA)	V_{RMS}	
Operating Current	I_{BL}	2.0	6.3	7.0	mA_{RMS}	3
Power Consumption	P_{BL}	1.8	4.2	4.5	W	
Operating Frequency	f_{BL}	45	55	80	kHz	
Discharge Stabilization Time	Ts			3	Min	4
Life Time		15,000			Hrs	5
Established Starting Voltage at 25℃ at 0 ℃	Vs	 1180 1415			 V_{RMS} V_{RMS}	

Note)

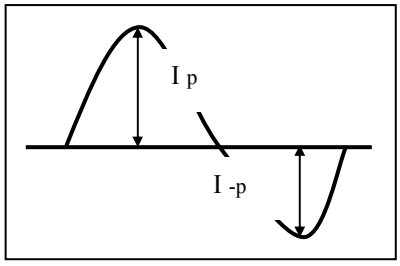
1. The specified current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition whereas Mosaic pattern is displayed and fv is the frame frequency.



2. This impedance value is needed to proper display and measured form LVDS Tx to the mating connector.
3. The typical operating current is for the typical surface luminance (L_{WH}) in optical characteristics.
4. Define the brightness of the lamp after being lighted for 5 minutes as 100%, Ts is the time required for the brightness of the center of the lamp to be not less than 95%.
5. The life time is determined as the time at which brightness of lamp is 50% compare to that of initial value at the typical lamp current.

Note)

6. The output of the inverter must have symmetrical(negative and positive) voltage waveform and symmetrical current waveform.(Asymmetrical ratio is less than 10%) Please do not use the inverter which has asymmetrical voltage and asymmetrical current and spike wave.
   Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.
7. It is defined the brightness of the lamp after being lighted for 5 minutes as 100%.
   T_S is the time required for the brightness of the center of the lamp to be not less than 95%.
8. The lamp power consumption shown above does not include loss of external inverter.
   The applied lamp current is a typical one.
9. Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.
   It shall help increase the lamp lifetime and reduce leakage current.
   a. The asymmetry rate of the inverter waveform should be less than 10%.
   b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.
   * Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

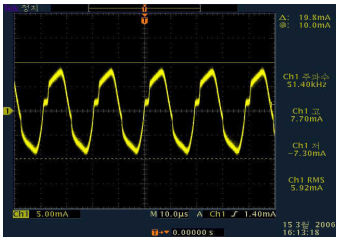
I_p (or I_{-p}) / I_{rms}

10. Inverter open voltage must be more than lamp voltage for more than 1 second for start-up. Otherwise, the lamps may not be turned on.
    ※ Do not attach a conducting tape to lamp connecting wire.
    If the lamp wire attach to a conducting tape, TFT-LCD Module has a low luminance and the inverter has abnormal action. Because leakage current is occurred between lamp wire and conducting tape.

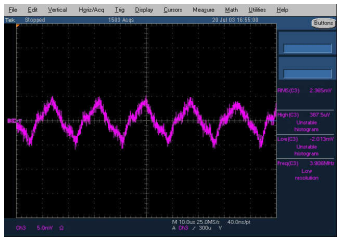
Ex of current wave)

Normal current wave - Standard

Abnormal current wave - Bad



Abnormal current wave - Bad



Abnormal current wave - Bad

3-2. Interface Connections

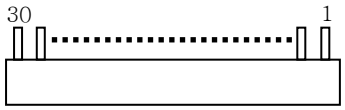
This LCD employs two interface connections, a 30 pin connector is used for the module electronics interface and the other connector is used for the integral backlight system.
The electronics interface connector is a model MDF76LBRW-30S-1 manufactured by HIROSE.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	GND	Ground	
2	VCC	Power Supply, 3.3V Typ.	
3	VCC	Power Supply, 3.3V Typ.	
4	V EEDID	DDC 3.3V power	
5	Test	Panel Self Test	
6	Clk EEDID	DDC Clock	
7	DATA EEDID	DDC Data	
8	R_{IN} 0-	Negative LVDS differential data input	
9	R_{IN} 0+	Positive LVDS differential data input	
10	GND	Ground	
11	R_{IN} 1-	Negative LVDS differential data input	
12	R_{IN} 1+	Positive LVDS differential data input	
13	GND	Ground	
14	R_{IN} 2-	Negative LVDS differential data input	
15	R_{IN} 2+	Positive LVDS differential data input	
16	GND	Ground	
17	CLKIN-	Negative LVDS differential clock input	
18	CLKIN+	Positive LVDS differential clock input	
19	GND	Ground	
20	NC	No Connect	
21	NC	No Connect	
22	GND	Ground	
23	NC	No Connect	
24	NC	No Connect	
25	GND	Ground	
26	NC	No Connect	
27	NC	No Connect	
28	GND	Ground	
29	NC	No Connect	
30	NC	No Connect	

1, Interface chips
1.1 LCD : SW, SW0612B (LCD Controller) including LVDS Receiver
1.2 System : THC63LVD823A or equivalent
* Pin to Pin compatible with LVDS

2. Connector
2.1 LCD : MDF76LBRW-30S ,HIROSE its compatibles
2.2 Mating : FI-X30M or equivalent.
2.3 Connector pin arrangement



[LCD Module Rear View]

The backlight interface connector is a model BHSR-02VS-1, manufactured by JST or Compatible.
The mating connector part number is AMP1674817-2 or equivalent.

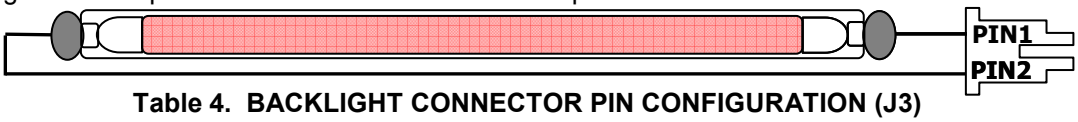


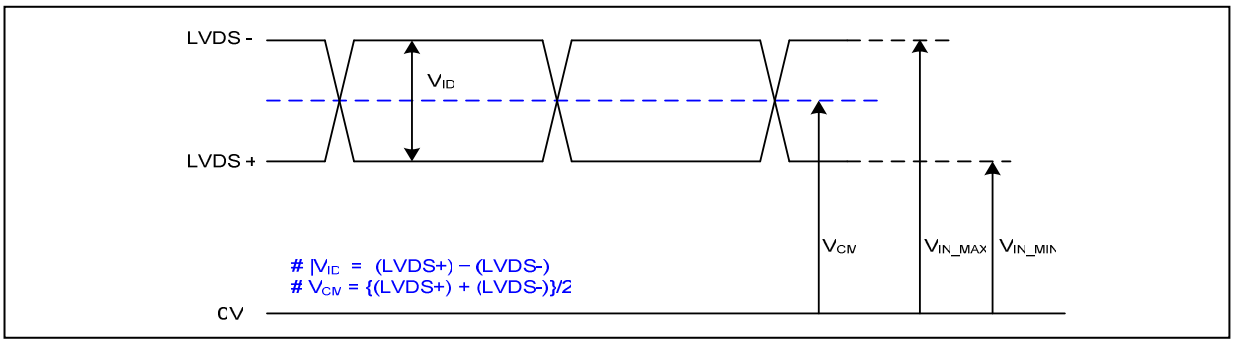
Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION (J3)

Pin	Symbol	Description	Notes
1	HV	Power supply for lamp (High voltage side)	1
2	LV	Power supply for lamp (Low voltage side)	1

Notes : 1. The high voltage side terminal is colored Pink and the low voltage side terminal is Yellow.

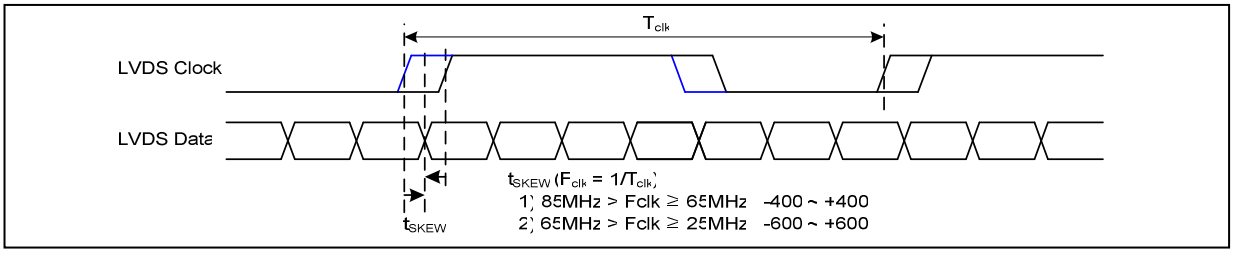
3-3. LVDS Signal Timing Specifications

3-3-1. DC Specification

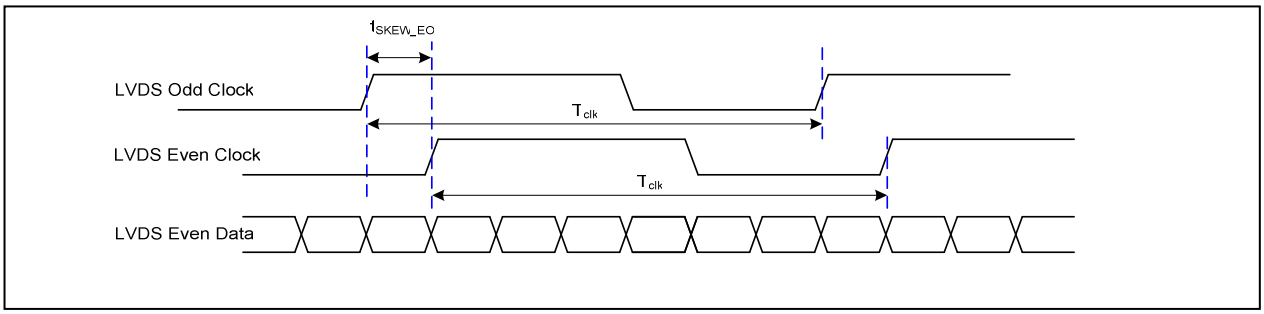


Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	100	600	mV	-
LVDS Common mode Voltage	V_{CM}	0.6	1.8	V	-
LVDS Input Voltage Range	V_{IN}	0.3	2.1	V	-

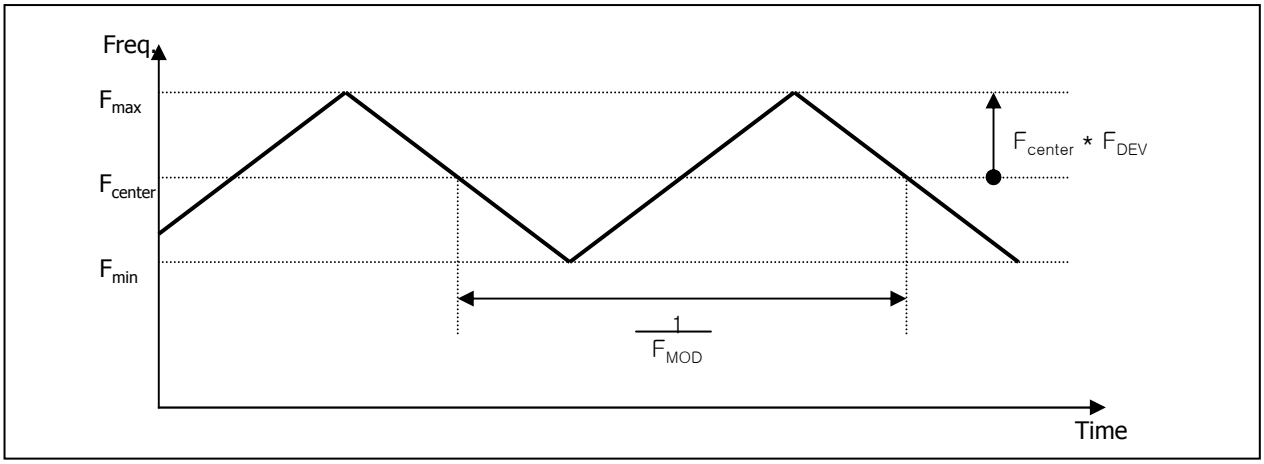
3-3-2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-



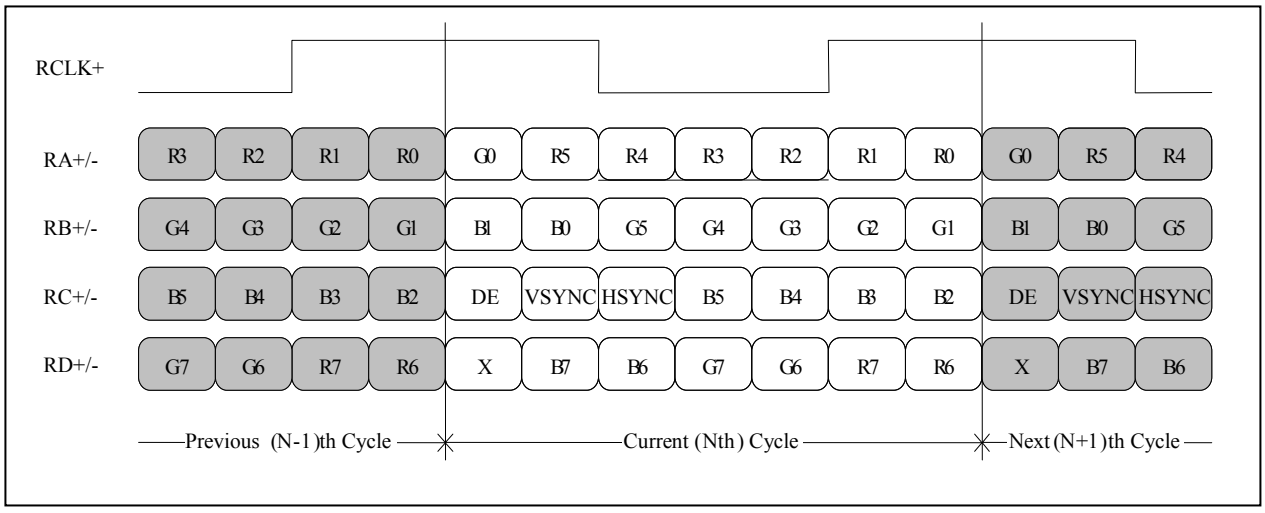
< Clock skew margin between channel >



< Spread Spectrum >

3-3-3. Data Format

1) LVDS 1 Port



< LVDS Data Format >

3-4. Signal Timing Specifications

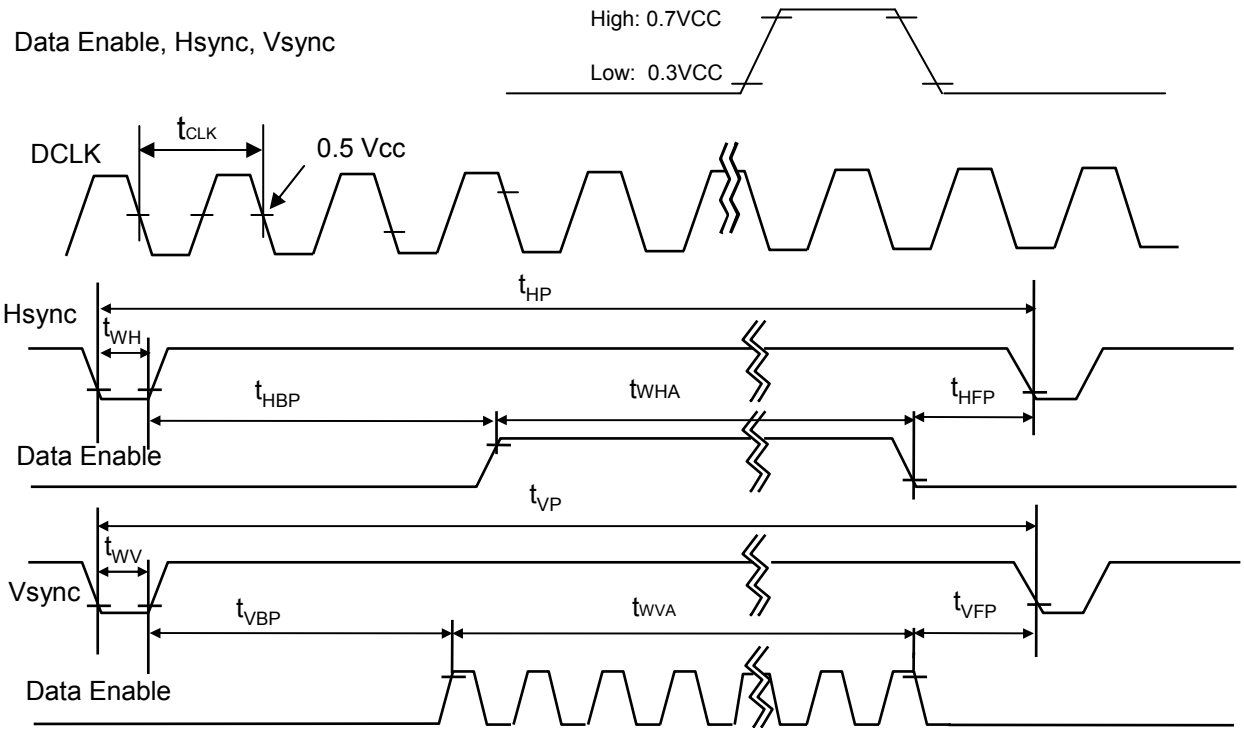
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 6. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	-	72.17	-	MHz	
Hsync	Period	Thp	1360	1432	1480	tCLK	
	Width	t_{WH}	16	32	48		
	Width-Active	t_{WHA}	1280	1280	1280		
Vsync	Period	t_{VP}	809	840	860	tHP	
	Width	t_{WV}	2	8	10		
	Width-Active	t_{WVA}	800	800	800		
Data Enable	Horizontal back porch	t_{HBP}	40	80	96	tCLK	
	Horizontal front porch	t_{HFP}	24	40	56		
	Vertical back porch	t_{VBP}	6	24	32	tHP	
	Vertical front porch	t_{VFP}	1	8	18		

3-5. Signal Timing Waveforms

Condition : VCC =3.3V



3-6. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 7. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	…			…						…						…			
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...			...						...						...			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…			…						…						…			
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-7. Power Sequence

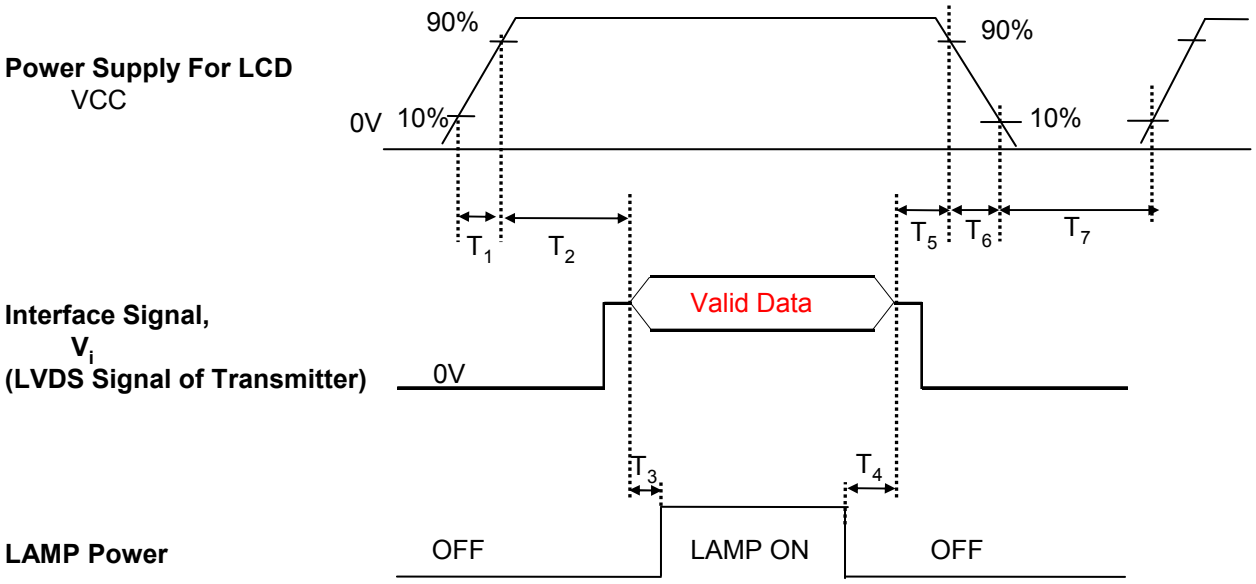


Table 8. POWER SEQUENCE TABLE

Parameter	Value			Units
	Min.	Typ.	Max.	
T_1	0.5	-	10	(ms)
T_2	0	-	50	(ms)
T_3	200	-	-	(ms)
T_4	200	-	-	(ms)
T_5	0	-	50	(ms)
T_6	0	-	10	(ms)
T_7	200	-	-	(ms)

Note)
1. Valid Data is Data to meet “3-3. LVDS Signal Timing Specifications”
2. Please avoid floating state of interface signal at invalid period.
3. When the interface signal is invalid, be sure to pull down the power supply for LCD VCC to 0V.
4. Lamp power must be turn on after power supply for LCD and interface signal are valid.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

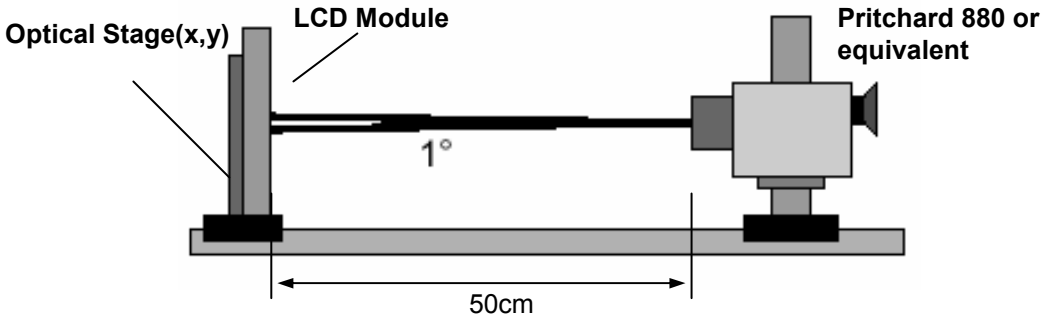


Table 9. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 72.17MHz, F_{BL} = 55kHz , I_{BL}= 6.3mA

Parameter	Symbol	Values			Units	Notes
		Min	Typ	Max		
Contrast Ratio	CR	400	-	-		1
Surface Luminance, white	L_{WH}	200	220	-	cd/m^2	2
Luminance Variation	δ_{WHITE}	-	1.8	2.0		3
Response Time	Tr_R+ Tr_D		16		ms	4
Color Coordinates						
RED	RX	0.554	0.584	0.614		
	RY	0.317	0.347	0.377		
GREEN	GX	0.294	0.324	0.354		
	GY	0.512	0.542	0.572		
BLUE	BX	0.128	0.158	0.188		
	BY	0.115	0.145	0.175		
WHITE	WX	0.283	0.313	0.343		
	WY	0.299	0.329	0.359		
Viewing Angle						5
x axis, right(Φ=0°)	Θr	40	-	-	degree	
x axis, left (Φ=180°)	Θl	40	-	-	degree	
y axis, up (Φ=90°)	Θu	15	-	-	degree	
y axis, down (Φ=270°)	Θd	35	-	-	degree	
Gray Scale						6

Note)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 1.

$$L_{WH} = \text{Average}(L_1, L_2, \ldots L_5)$$

3. The variation in surface luminance , The panel total variation (δ_{WHITE}) is determined by measuring L_N at each test position 1 through 13 and then defined as followed numerical formula.
For more information see FIG 2.

$$\delta_{WHITE} = \frac{\text{Maximum}(L_1, L_2, \ldots L_{13})}{\text{Minimum}(L_1, L_2, \ldots L_{13})}$$

4. Response time is the time required for the display to transition from white to black (rise time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

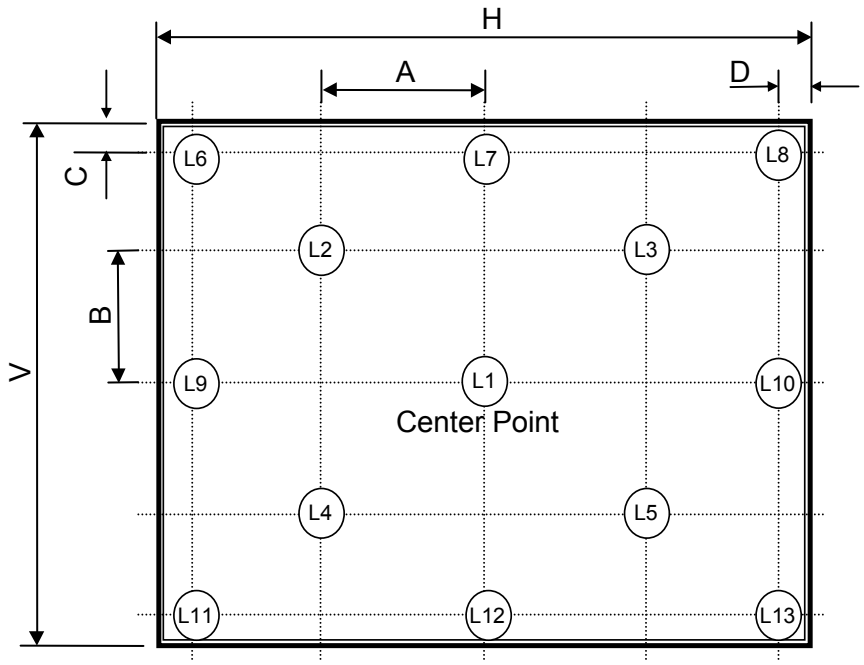
6. Gray scale specification

* f_V = 60Hz

Gray Level	Luminance [%] (Typ)
L0	0.12
L7	1.60
L15	5.80
L23	12.6
L31	20.4
L39	34.9
L47	55.2
L55	78.8
L63	100.0

FIG. 2 Luminance

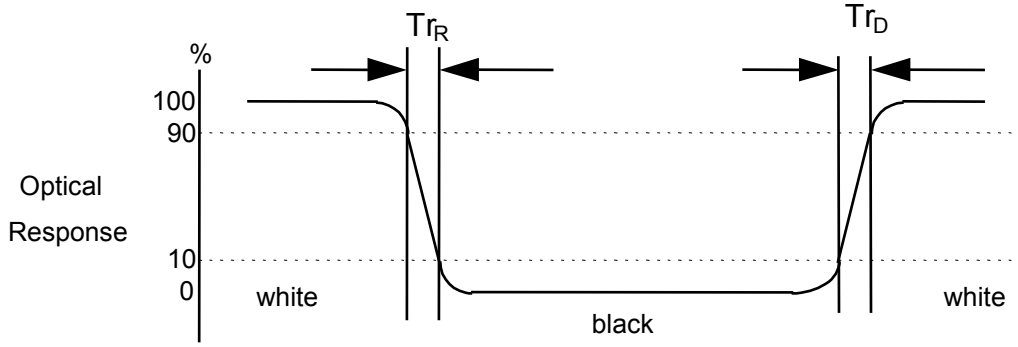
<measuring point for surface luminance & measuring point for luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
C : 10 mm
D : 10 mm
POINTS : 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.



5. Mechanical Characteristics

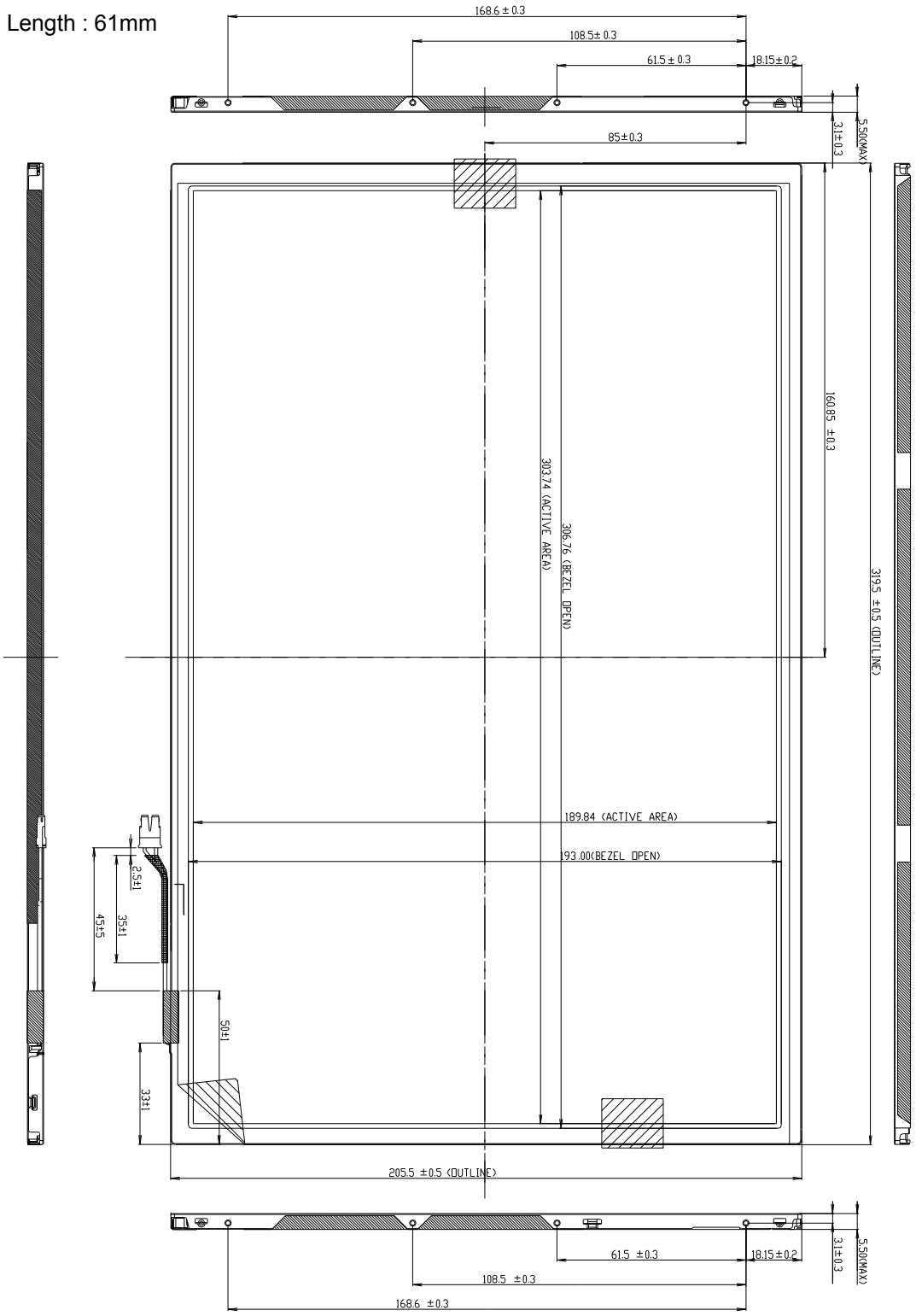
The contents provide general mechanical characteristics for the model LP141WX3. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	319.5 ± 0.5mm
	Vertical	205.5 ± 0.5mm
	Thickness	5.5mm (max)
Bezel Area	Horizontal	306.76 ± 0.5mm
	Vertical	193.00 ± 0.5mm
Active Display Area	Horizontal	303.74 mm
	Vertical	189.84 mm
Weight	425(Max)	
Surface Treatment	Anti-glare treatment of the front polarizer	

<FRONT VIEW>

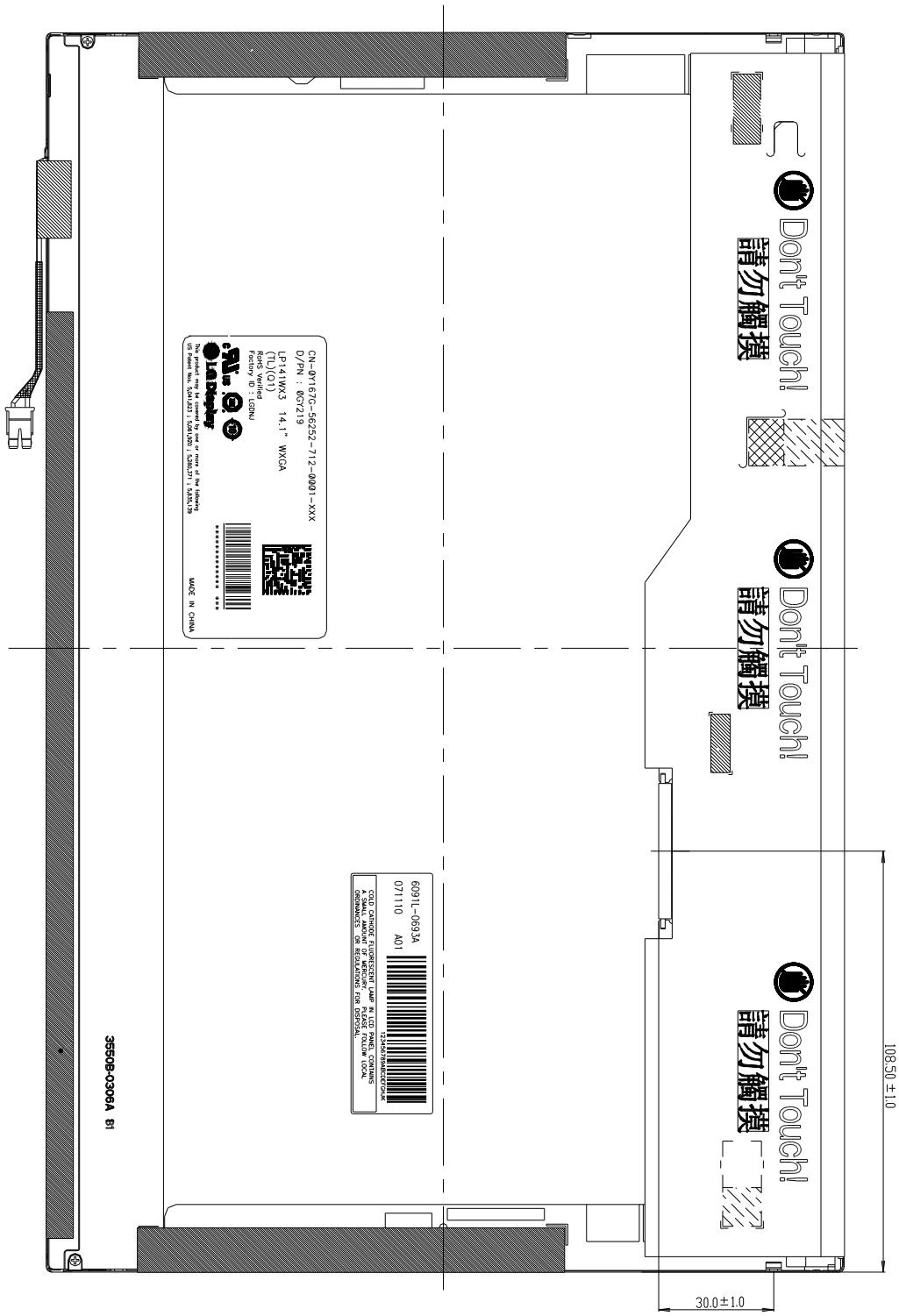
Note) Unit:[mm], General tolerance: ± 0.5mm

Wire Length : 61mm

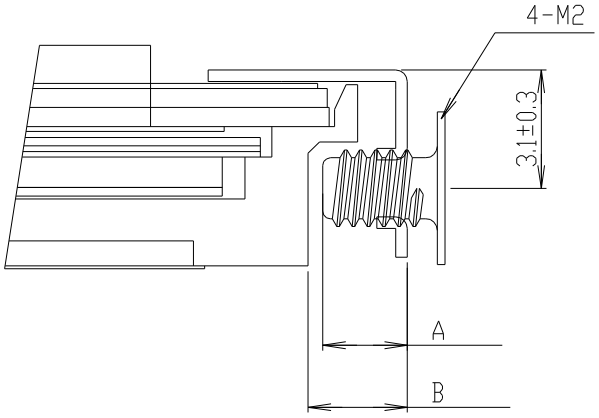


<REAR VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm



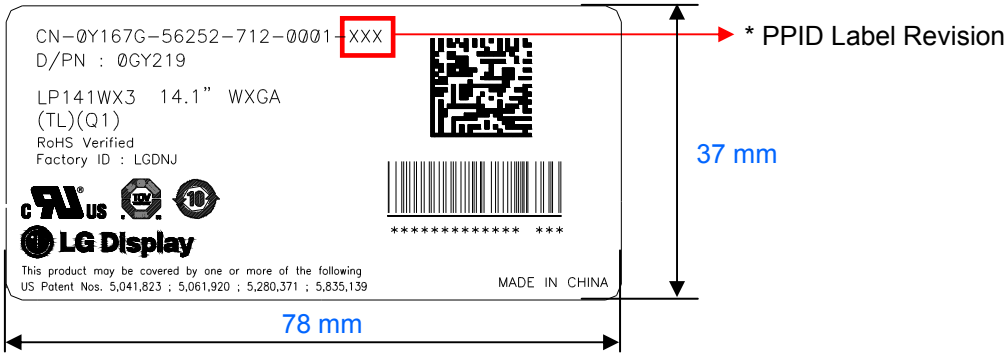
[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]



* Mounting Screw Length (A)
  = 2.0(Min) / 2.5(Max)
* Mounting Screw Hole Depth (B)
  = 2.5(Min)
* Mounting hole location : 3.7(typ.)
* Torque : 2.5 kgf.cm(Max)
  (Measurement gauge : torque meter)

Notes : 1. Screw plated through the method of non-electrolytic nickel plating is preferred to reduce possibility that results in vertical and/or horizontal line defect due to the conductive particles from screw surface.

[DETAIL INFORMATION OF PPID LABEL AND REVISION CODE]

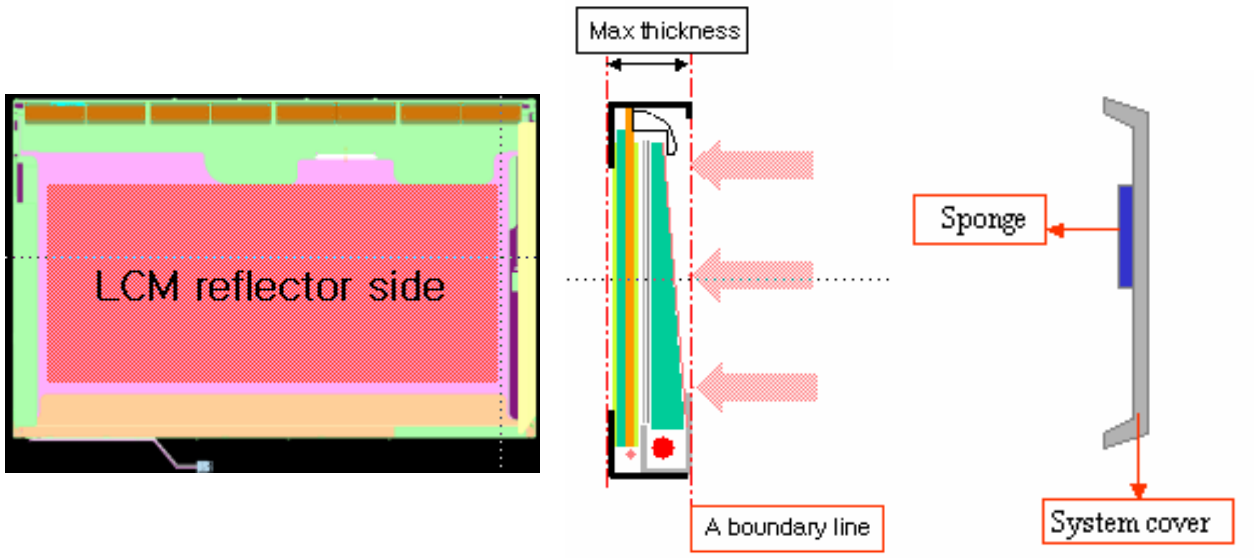


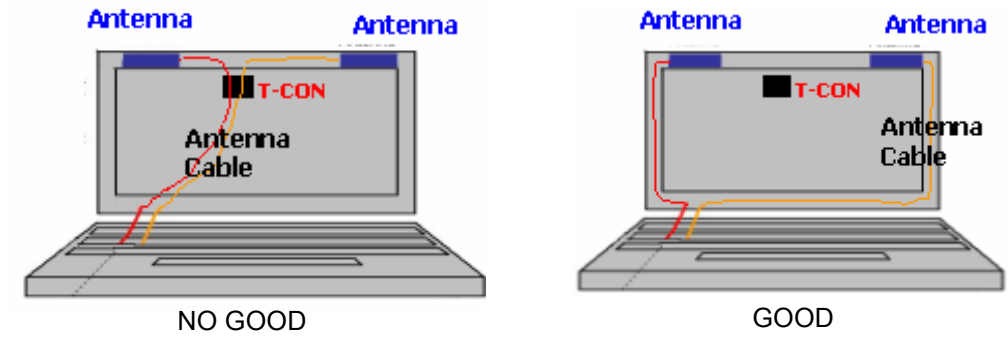
* PPID Label Revision :
  It is subject to change with Dell event. Please refer to the below table for detail.

Classification	No Change	1st Revision	2nd Revision	…	9th Revision	…
SST(WS)	X00	X01	X02	…	A09	…
PT(ES)	X10	X11	X12	…	A19	…
ST(CS)	X20	X21	X22	…	A29	…
XB(MP)	A00	A01	A02	…	A09	…

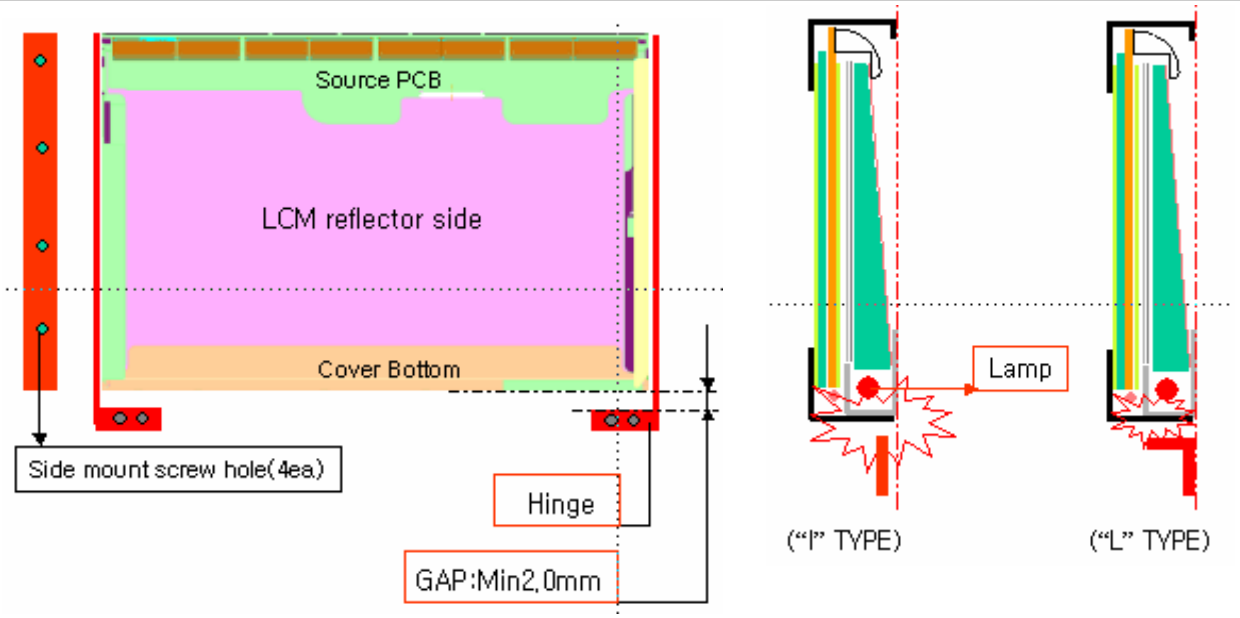
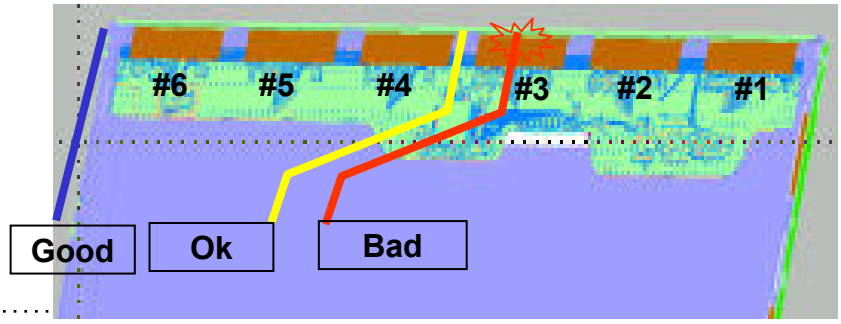
LPL Proposal for system cover design.(Appendix)

1	Gap check for securing the enough gap between LCM and System cover.	



Define	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.
Define	
	1.If system antenna is overlapped with T-CON,it might be cause the noise.

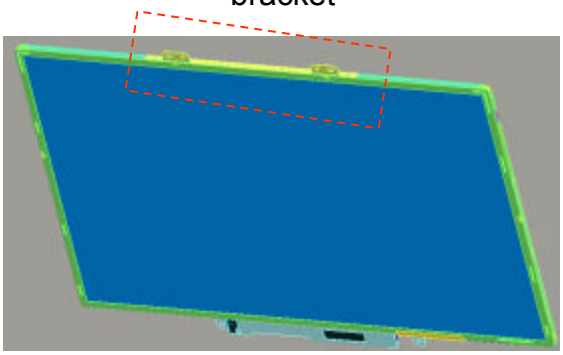
LPL Proposal for system cover design.

3	Gap check for securing the enough gap between LCM and System hinge.	
		
Define	1.At least 2.0mm of gap needs to be secured to prevent the shock related defects. 2."L" type of hinge is recommended than "I" type under shock test.	
4	Checking the path of the System wire.	
		
Define	1.COF area needs to be handled with care. 2.GOOD ➔Wire path design to system side. OK➔ Wire path is located between COFs. BAD➔Wire path overlapped with COF area.	

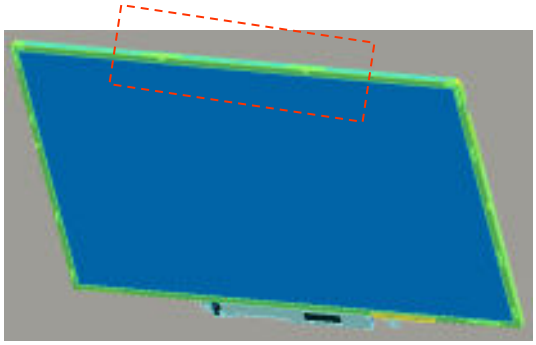
LPL Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	

bracket

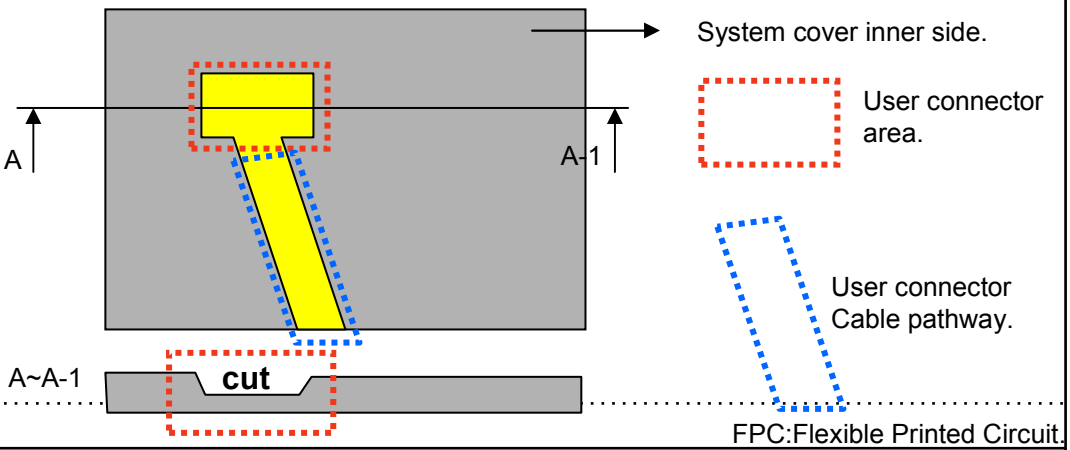


With bracket



Without bracket

Define	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.
6	Securing additional gap on CNT area..



Define	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 10 ~ 500 ~ 10Hz, 1.5G, 0.37oct/min 3 axis, 1hour/axis
6	Shock test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces(I.e. run 180G, 2ms for all six faces)
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Safety

a) UL 60950-1:2003, First Edition, Underwriters Laboratories, Inc.,
Standard for Safety of Information Technology Equipment.
b) CAN/CSA C22.2, No. 60950-1-03 1st Ed. April 1, 2003, Canadian Standards Association,
Standard for Safety of Information Technology Equipment.
c) EN 60950-1:2001, First Edition,
European Committee for Electrotechnical Standardization(CENELEC)
European Standard for Safety of Information Technology Equipment.

7-2. EMC

a) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. “American National Standards Institute(ANSI), 1992
b) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ International Special Committee on Radio Interference.
c) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ European Committee for Electrotechnical Standardization.(CENELEC), 1998
(Including A1: 2000)

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 30 pcs

b) Box Size : 490mm × 393mm × 287mm

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (hex)	Field Name and Comments	Value (hex)
Header	0	Header	00
	1	Header	FF
	2	Header	FF
	3	Header	FF
	4	Header	FF
	5	Header	FF
	6	Header	FF
	7	Header	00
Vendor / Product EDID Version	8	EISA manufacture code = LPL	32
	9	EISA manufacture code (Compressed ASCII)	0C
	0A	Panel Supplier Reserved – Product Code	2B
	0B	Panel Supplier Reserved – Product Code	01
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	10	Week of manufacture	00
	11	Year of manufacture = 2008	12
	12	EDID structure version # = 1	01
	13	EDID revision # = 3	03
Display Parameters	14	Video I/P definition = Digital I/P (80h)	90
	15	Max H image size = (Rounded to cm)	1E
	16	Max V image size = (Rounded to cm)	13
	17	Display gamma = (gamma ×100)-100 = Example: (2.2× 100) – 100 = 120	78
	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	B3
	1A	Blue/White Low bit (BxBy/WxWy)	85
	1B	Red X Rx = 0.584	95
	1C	Red Y Ry = 0.347	58
	1D	Green X Gx = 0.324	53
	1E	Green Y Gy = 0.542	8A
	1F	Blue X Bx = 0.158	28
	20	Blue Y By = 0.145	25
	21	White X Wx = 0.313	50
	22	White Y Wy = 0.329	54
Established Timings	23	Established timings 1 (00h if not used)	00
	24	Established timings 2 (00h if not used)	00
	25	Manufacturer’s timings (00h if not used)	00
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01
	27	Standard timing ID1 (01h if not used)	01
	28	Standard timing ID2 (01h if not used)	01
	29	Standard timing ID2 (01h if not used)	01
	2A	Standard timing ID3 (01h if not used)	01
	2B	Standard timing ID3 (01h if not used)	01
	2C	Standard timing ID4 (01h if not used)	01
	2D	Standard timing ID4 (01h if not used)	01
	2E	Standard timing ID5 (01h if not used)	01
	2F	Standard timing ID5 (01h if not used)	01
	30	Standard timing ID6 (01h if not used)	01
	31	Standard timing ID6 (01h if not used)	01
	32	Standard timing ID7 (01h if not used)	01
	33	Standard timing ID7 (01h if not used)	01
	34	Standard timing ID8 (01h if not used)	01
	35	Standard timing ID8 (01h if not used)	01

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (hex)	Field Name and Comments	Value (hex)
Timing Descripter #1	36	Pixel Clock/10,000 72.17MHz (LSB)	31
	37	Pixel Clock/10,000 (MSB)	1C
	38	Horizontal Active = 1280 pixels (lower 8 bits)	00
	39	Horizontal Blanking (Thbp) = 152 pixels (lower 8 bits)	98
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50
	3B	Vertical Active = 800 lines	20
	3C	Vertical Blanking (Tvbp) = 40 lines (DE Blanking typ. for DE only panels)	28
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
	3E	Horizontal Sync, Offset (Thfp) = 40 pixels	28
	3F	Horizontal Sync, Pulse Width = 32 pixels	20
	40	Vertical Sync, Offset (Tvfp) = 8 lines Sync Width = 8 lines	88
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	42	Horizontal Image Size =303.74 mm	30
	43	Vertical image Size = 189.84 mm	BE
	44	Horizontal Image Size / Vertical image size	10
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00
	46	Vertical Border = 0 (Zero for Notebook LCD)	00
	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition	1A
Timing Descripter #2	48	Pixel Clock/10,000 72.17MHz → **48.12MHz @ 40Hz (LSB)**	CC
	49	Pixel Clock/10,000 (MSB)	12
	4A	Horizontal Active = 1280 pixels (lower 8 bits)	00
	4B	Horizontal Blanking (Thbp) = 152 pixels (lower 8 bits)	98
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50
	4D	Vertical Active = 800 lines	20
	4E	Vertical Blanking (Tvbp) = 40 lines (DE Blanking typ. for DE only panels)	28
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
	50	Horizontal Sync, Offset (Thfp) = 40 pixels	28
	51	Horizontal Sync, Pulse Width = 32 pixels	20
	52	Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 8 lines	88
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	54	Horizontal Image Size =303.74 mm	30
	55	Vertical image Size = 189.84 mm	BE
	56	Horizontal Image Size / Vertical image size	10
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00
	58	Vertical Border = 0 (Zero for Notebook LCD)	00
	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition	1A
Timing Descripter #3 Dell specific information	5A	Flag	00
	5B	Flag	00
	5C	Flag	00
	5D	Dummy Descriptor	FE
	5E	Flag	00
	5F	Dell P/N 1st Character = G	47
	60	Dell P/N 2nd Character =Y	59
	61	Dell P/N 3rd Character = 2	32
	62	Dell P/N 4th Character = 1	31
	63	Dell P/N 5th Character = 9	39
	64	LCD Supplier EEDID Revision # = 0.0	00
	65	Manufacturer P/N = 1	31
	66	Manufacturer P/N = 4	34
	67	Manufacturer P/N = 1	31
	68	Manufacturer P/N = W	57
	69	Manufacturer P/N = X	58
	6A	Manufacturer P/N = 3	33
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (hex)	Field Name and Comments	Value (hex)
Timing Descripter #4	6C	Flag	00
	6D	Flag	00
	6E	Flag	00
	6F	Data Type Tag:	00
	70	Flag	00
	71	Flag	00
	72	Flag	00
	73	Flag	00
	74	Flag	00
	75	Flag	00
	76	Flag	00
	77	Flag	00
	78	Flag	00
	79	Number of LVDS receiver chips = '01' or '02'	01
	7A	BIST Enable: Yes = '01' No = '00'	01
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	7D