SAMSUNG ELECTRONICS

TO :

DATE : May. 10, 2010

SAMSUNG TFT-LCD

MODEL NO. : LTN121AP05-302

NOTE : Extension code [-302]
→ LTN121AP05-**302**
Surface type [**Anti-Glare**]

Any Modification of Spec is not allowed without SEC' permission.

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CONTENTS

REVISION HISTORY

Date	Revision No.	Page	Summary
May. 10, 2010	A00	All	The approval specification of LTN121AP05-302 was issued first. (LTN121AP05-302 is the solder crack improved version of LTN121AP05-301)

GENERAL DESCRIPTION

DESCRIPTION

LTN121AP05 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight unit. The resolution of a 12.1" contains 1280 x 800 pixels and can display up to 262,144 colors. 6 O'clock direction is the optimum viewing angle.

FEATURES

- High contrast ratio, Ultra wide viewing angle
- WXGA (1280 x 800 pixels) resolution
- Low power consumption
- Fast Response
- LED Back Light with embedded LED Driver
- DE (Data enable) only mode
- 3.3V LVDS Interface
- Onboard EEDID chip
- Green product (RoHS compliant)

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	261.12(H) x 163.2(V) (12.1” wide diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1280 x 800	pixel	
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.204(H) x 0.204(V) (TYP.)	mm	
Display Mode	Normally black		
Surface treatment	Haze 25% (inner 0%, outer 25%), Hard-Coating 3H		

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	276.5	276.8	277.1	mm	
	Vertical (V)	179.7	180.0	180.3	mm	
	Depth (D)	-	6.5	6.8	mm	(1)
Weight		-	270	275	g	

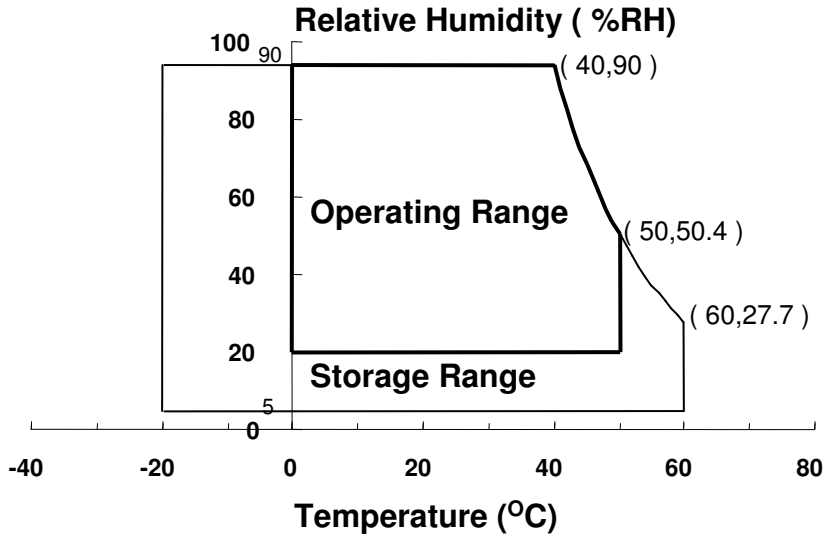
Note (1) Measurement condition of outline dimension
. Equipment : Bernier Calipers
. Push Force : 500g ·f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 °C ≥ Ta)
Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation



(2) 2ms, half sine wave, one time for ±X, ±Y, ± Z.
(3) 5 - 500 Hz, random vibration, 30min for X, Y, Z.
(4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

V_{DD} =3.3V, V_{SS} = GND = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	V_{DD} - 0.3	V_{DD} + 0.3	V	(1)
Logic Input Voltage	V_{IN}	V_{DD} - 0.3	V_{DD} + 0.3	V	(1)

Note (1) Within Ta (25 ± 2 °C)

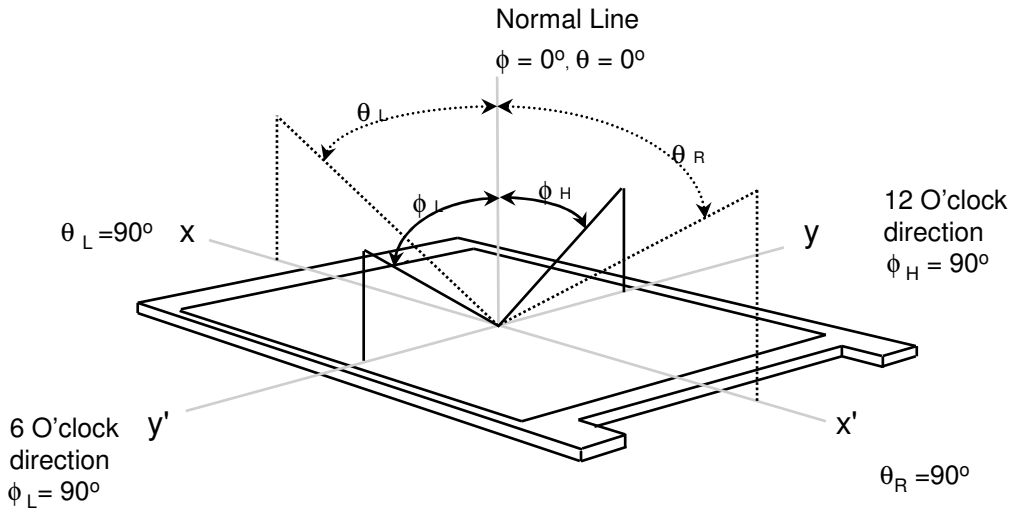
2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5). Measuring equipment : TOPCON BM-5A and PR-650

* Ta = 25 ± 2 °C, V_{DD}=3.3V, fv= 60Hz, f_{DCLK} = 69.3MHz, IF = 18.0 mA

Item		Symbol	Condition	Min.	Typ.	Max	Unit	Note
Contrast Ratio (5 Points)		CR	Normal Viewing Angle $\phi = 0$ $\theta = 0$	-	500	-	-	(1), (2), (5)
Response Time at Ta (Rising + Falling)		T_{RT}		-	25	35	msec	(1), (3)
Average Luminance of White (5 Points)		$Y_{L,AVE}$		170	200	-	cd/m^2	IF=18.0mA (1), (4)
Color Chromaticity (CIE)	Red	R_X		0.540	0.590	0.640	-	(1), (5) PR-650
		R_Y		0.310	0.360	0.410		
	Green	G_X		0.315	0.365	0.415		
		G_Y		0.520	0.570	0.620		
	Blue	B_X		0.110	0.160	0.210		
		B_Y		0.085	0.135	0.185		
	White	W_X		0.263	0.313	0.363		
		W_Y		0.279	0.329	0.379		
Viewing Angle	Hor.	θ_L	CR ≥ 10 At center	75	80		Degrees	(1), (5) BM-5A
		θ_H		75	80			
	Ver.	ϕ_H		75	80			
		ϕ_L		75	80			
13 Points White Variation		δ_L		-	1.4	1.6	-	(6)

Note 1) Definition of Viewing Angle : Viewing angle range($10 \leq C/R$)

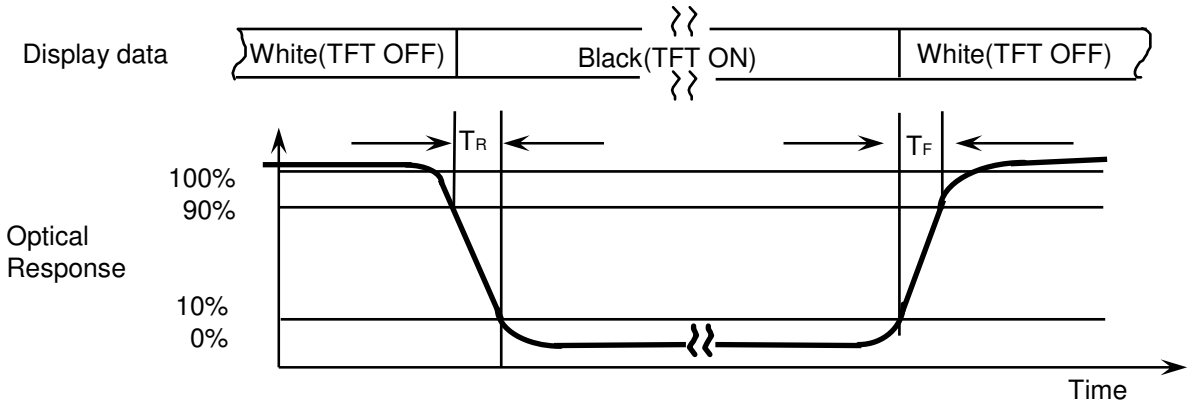


Note 2) Definition of Contrast Ratio (CR) : Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points(4, 5, 7, 9, 10)

$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

Points : ④ , ⑤ , ⑦ , ⑨ , ⑩ at the figure of Note (6).

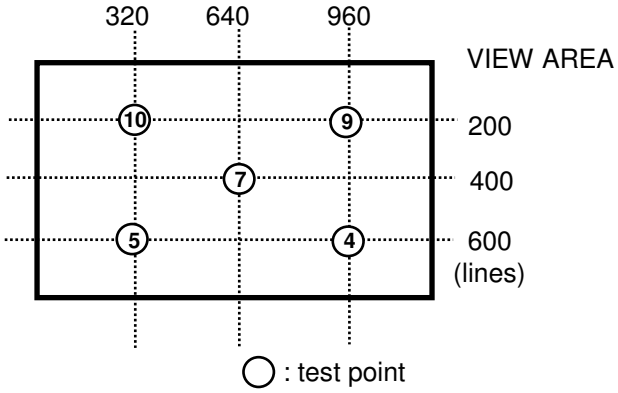
Note 3) Definition of Response time :



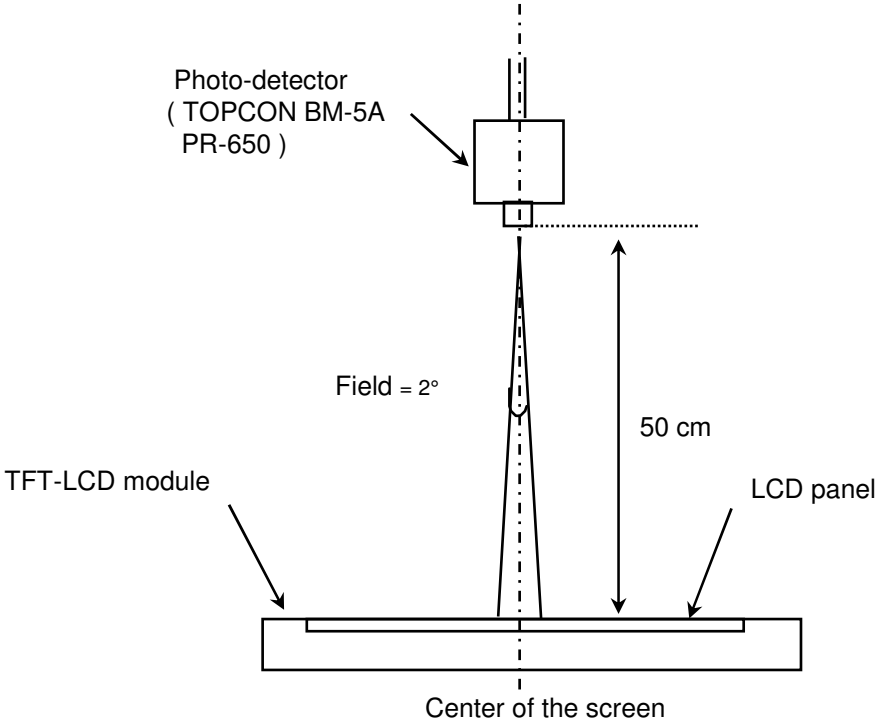
Note 4) Definition of Average Luminance of White : measure the luminance of white at 5 points.

Average Luminance of White ($Y_{L,AVE}$)

$$Y_{L,AVE} = \frac{Y_{L4} + Y_{L5} + Y_{L7} + Y_{L9} + Y_{L10}}{5}$$



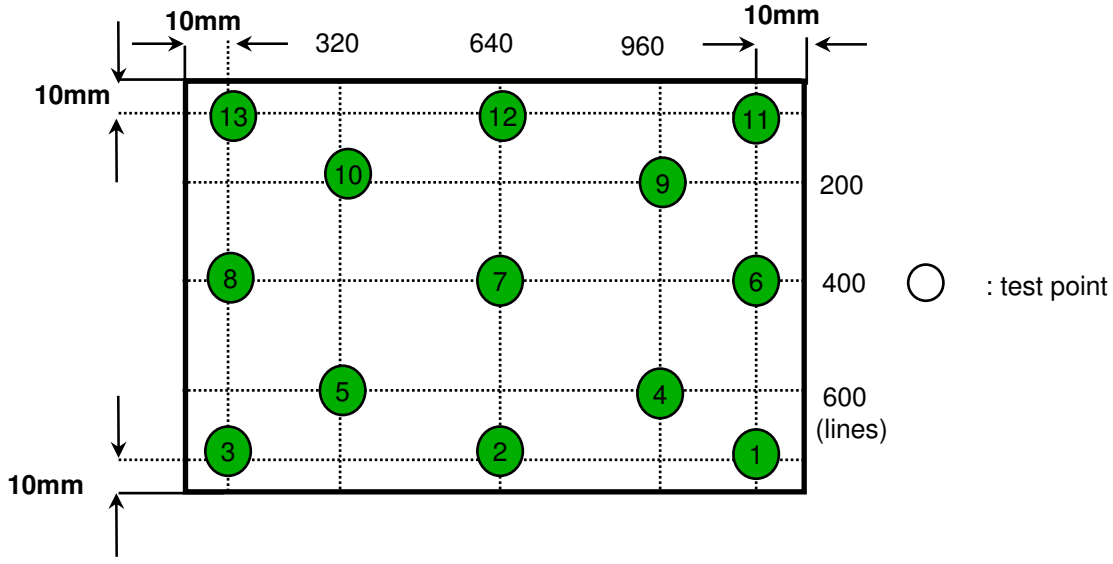
Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless,and dark room. 30 min after lighting the backlight. This should be measured in the center of screen.
Environment condition : Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

Note 6) Definition of 13 points white variation (δ_L), CR variation(C_{VER}) [① ~ ⑬]

$$\delta_L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$$



3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta= 25 ± 2°C

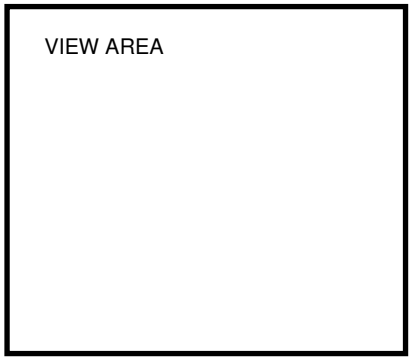
Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		V_{DD}	3.0	3.3	3.6	V	
Interface Type		eDP	eDP V1(D11) Va(Rx/Tx)				(1)
Vsync Frequency		fv	-	60	-	Hz	
Hsync Frequency		f_H	-	48.96	-	KHz	
Main Frequency		f_{DCLK}	67.2	69.3	70.6	MHz	
Rush Current		I_{RUSH}	-	-	1.5	A	(4)
Current of Power Supply	White	I_{DD}	-	335	-	mA	(2),(3)*a
	Mosaic		-	320	-	mA	(2),(3)*b
	V. stripe		-	370	400	mA	(2),(3)*c

Note (1) Display Port interface characteristics should be based on VESA standard (eDP V1 draft11)

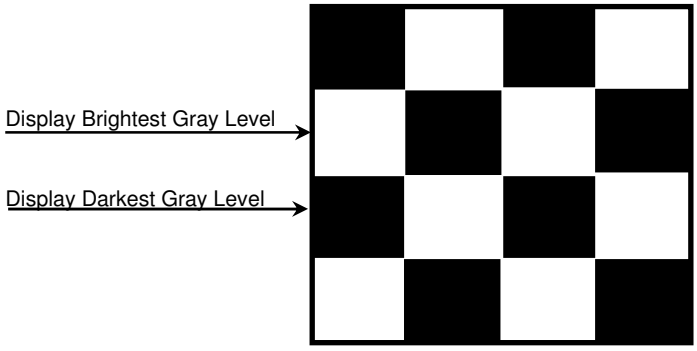
(2) f_V = 60Hz, f_{DCLK} = 69.3MHZ, V_{DD} = 3.3V , DC Current.

(3) Power dissipation pattern

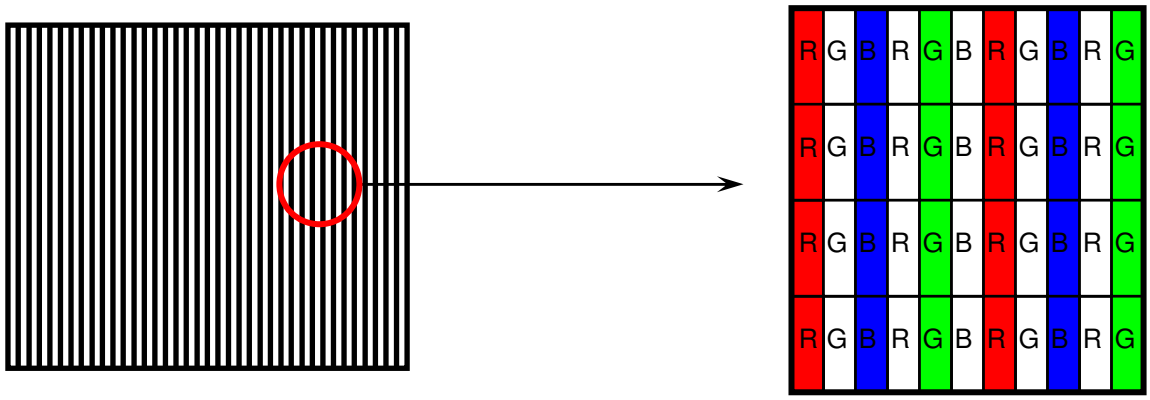
*a) White Pattern



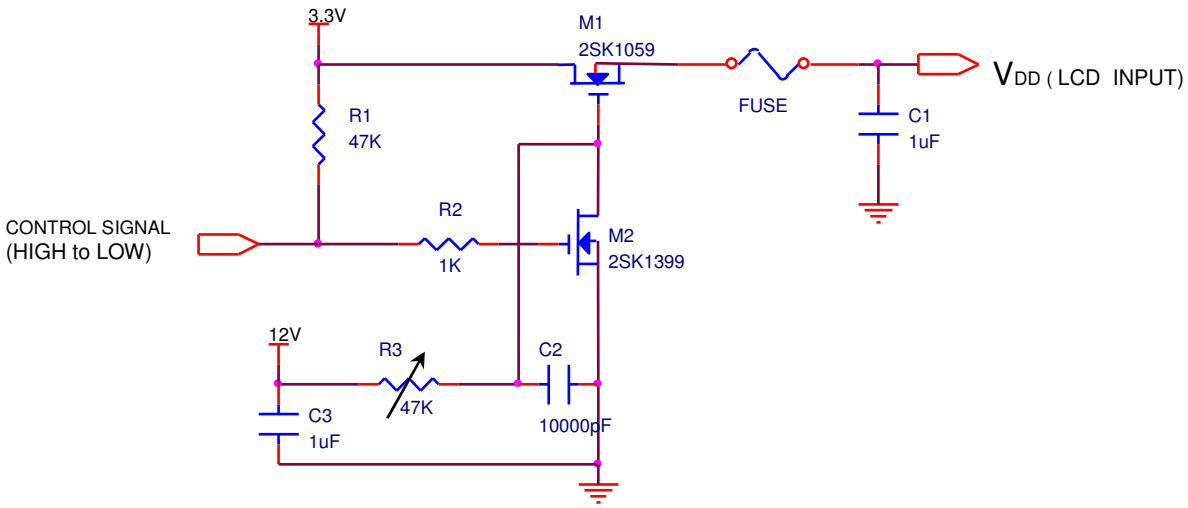
*b) Mosaic Pattern



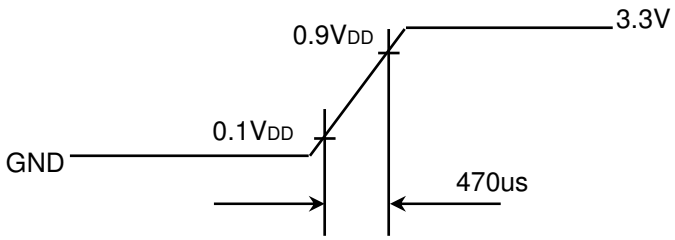
*c) 1dot Vertical stripe pattern



4) Rush current measurement condition



VDD rising time is 470us



3.2 BACK-LIGHT UNIT

Ta= 25 ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Forward Current	IF	-	18	-	mA	
LED Forward Voltage	VF	-	3.2	-	V	
LED Array Voltage	VP	-	32	-	V	VF X 10 LEDs
Power Consumption	P	-	-	3.5	W	IF X VF X 48 LEDs
Operating Life Time	Hr	12,000	-	-	Hour	(1)

Note (1) Life time (Hr) of LEDs can be defined as the time in which it continues to operate under the condition Ta= 25 ± 2 °C and IF = 18.0 mA rms until one of the following event occurs.
1. When the brightness becomes 50% or lower than the original.

3.3 LED Driver

- On board LED Driver (Manufacturer : SEC)

Ta= 25 ± 2 °C

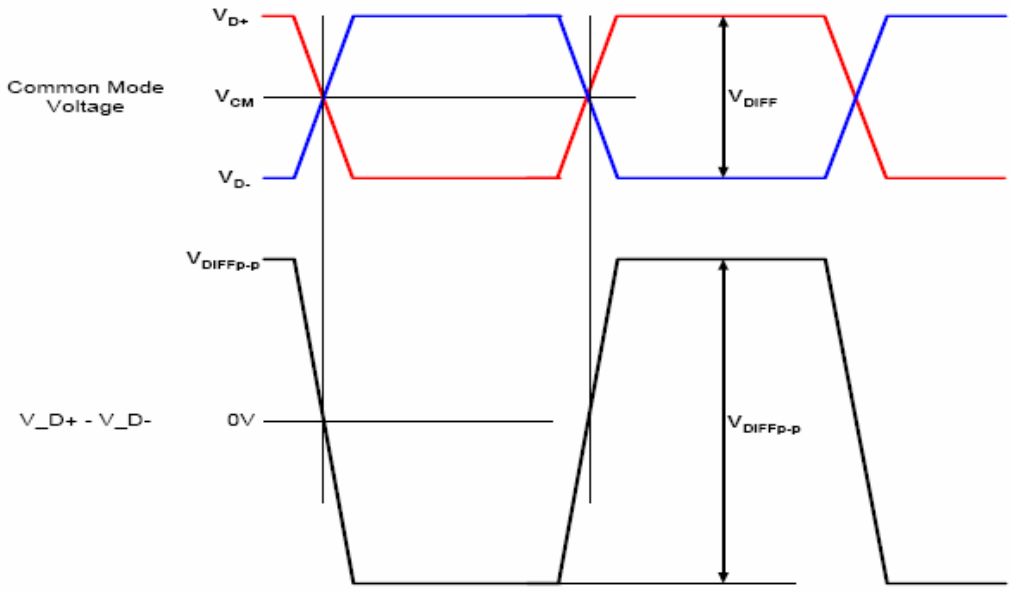
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage	V_{in}	6	12	20	V_{LED}	
Input Current	I	-	-	(2)	mA	RMS
Enable Control Level	V	0	-	3.3	V	ON Level : 2V~3.3V OFF Level : 0V ~ 0.5V
External PWM Dimming Control Frequency (BLIM)	F_{BLIM}	0.2	-	1	kHz	High Level : 1.5V~3.3V Low Level : 0V ~ 0.1V
PWM Control Duty Ratio	%	10	-	100	%	(1)
Operating Frequency	Hz	0.2	-	1	KHz	

Note (1) The operation of Led Driver below minimum dimming ratio may cause flicking or reliability issue.

3.4 DisplayPort Main RX Specifications (compliant to DP spec v1.1a & eDP spec v1.1)

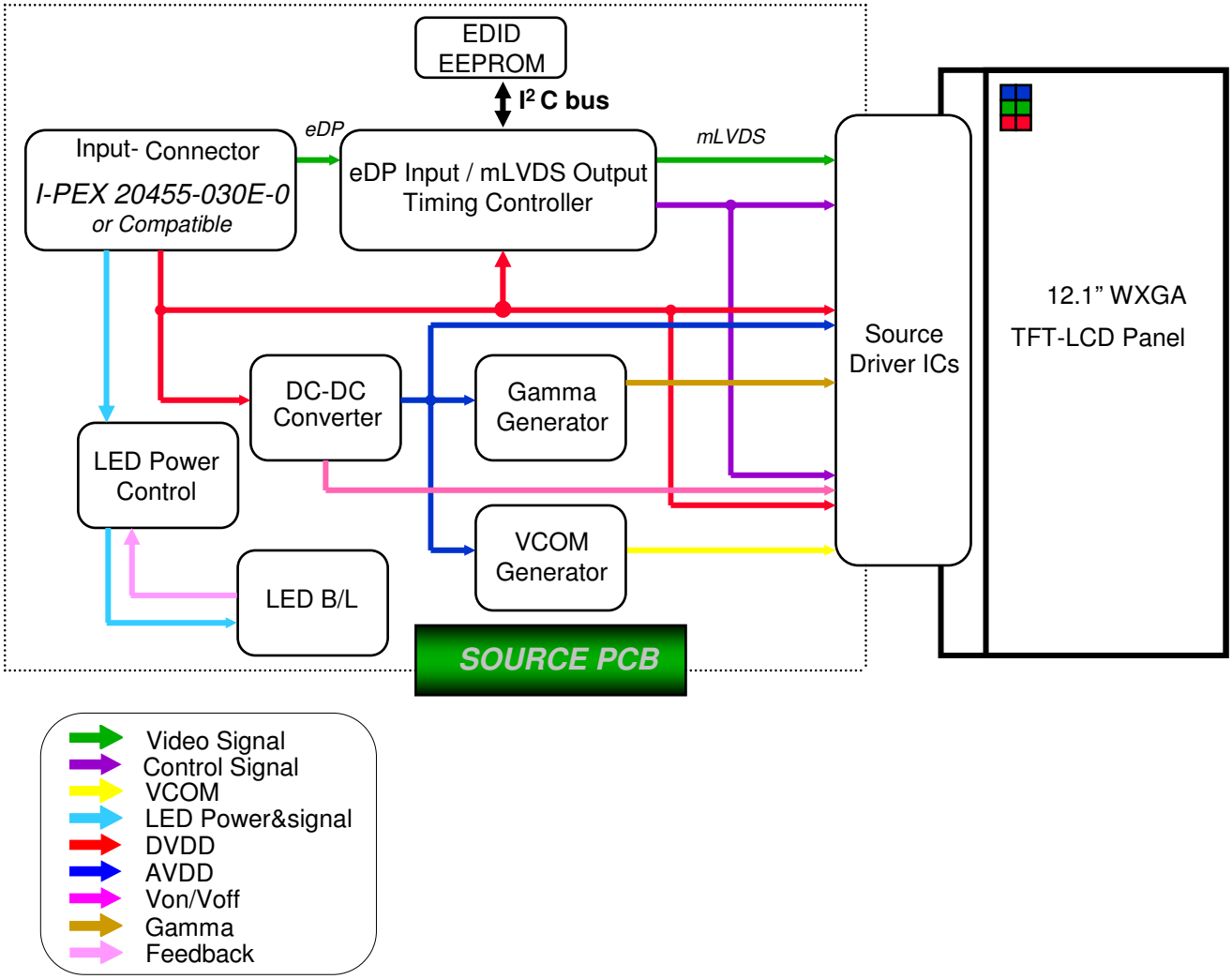
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
UI_High_Rate	Unit Interval for high bit rate (2.7 Gbps / lane)	-	370	-	ps	Range is nominal ±350ppm. DisplayPort Link Rx does not require local crystal for link clock generation
UI_Low_Rate	Unit Interval for low bit rate (1.62 Gbps / lane)	-	617	-	ps	
$V_{RX-DIFFp-p}$	Differential Peak-to-peak Input Voltage at RX package pins	120	-	-	mV	For High Bit Rate (2.7 Gbps / lane) Refer to note(1)
$V_{RX-DIFFp-p}$	Differential Peak-to-peak Input Voltage at RX package pins	40	-	-	mV	For Low Bit Rate (1.62 Gbps / lane) Refer to note(1)
$V_{RX-DC-CM}$	RX DC Common Mode Voltage	0	-	20	V	Common mode voltage is equal to Vbias_Rx voltage shown in note(1)
$L_{RX-SKEW-INTER\_PAIR}$	Lane-to-Lane Skew at RX package pins	-	-	5200	ps	Maximum skew limit between different RX lanes of a DisplayPort link
$L_{RX-SKEW-INTRA\_PAIR\_High-Bit-Rate}$	Lane Intra-pair Skew at RX package pins	-	-	100	ps	For High Bit Rate Maximum skew limit between D+ and D- of the same lane
$L_{RX-SKEW-INTRA\_PAIR\_Reduced-Bit-Rate}$	Lane Intra-pair Skew at RX package pins	-	-	300	ps	For Reduced Bit Rate Maximum skew limit between D+ and D- of the same lane

Note (1) Definition of differential voltage and differential voltage peak-to-peak



4. BLOCK DIAGRAM

4.1 TFT LCD Module

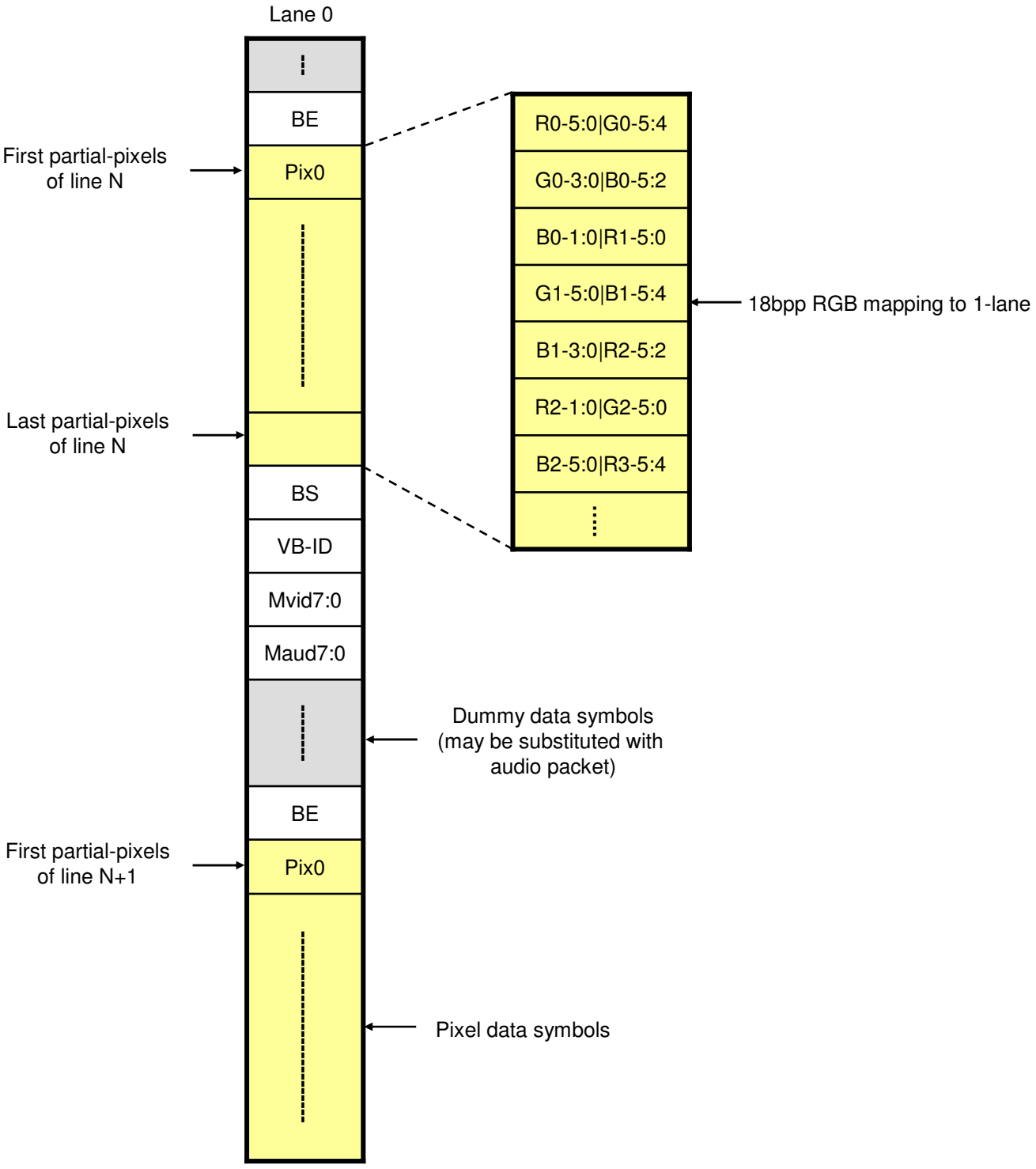


5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (1-Lane eDP, Connector : 20455-030E-02 by I-PEX or equivalent)

No.	Symbol	Function
1	NC	No Connection (Reserved)
2	NC	No Connection (Reserved)
3	NC	No Connection (Reserved)
4	NC	No Connection (Reserved)
5	H_GND	High Speed (Main Link) Ground
6	ML_Lane 0 (n)	Complement Signal-Main Link Lane
7	ML_Lane 0 (p)	True Signal-Main Link Lane
8	H_GND	High Speed (Main Link) Ground
9	AUX_CH (p)	True Signal-Auxiliary Channel
10	AUX_CH (n)	Complement Signal-Auxiliary Channel
11	H-GND	High Speed (Main Link) Ground
12	VCC	VCC for Module (3.3V)
13	VCC	VCC for Module (3.3V)
14	BIST	Build-In Self Test (active high)
15	GND	Ground
16	GND	Ground
17	HPD	Hot Plug Defect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL-EN	BL On/Off (On: 2.0~3.3V, Off: 0~0.5V) / NC (100K pull-up) / 5V tolerant
23	BL_PWM	PWM for luminance control (200~1KHz, 3.3V, 10~100%, 0V=off) 5V tolerant
24	NC	No Connection (Reserved)
25	NC	No Connection (Reserved)
26	VBL	BL Power 6V~20V
27	VBL	BL Power 6V~20V
28	VBL	BL Power 6V~20V
29	VBL	BL Power 6V~20V
30	NC	Vendor Reserved (DVR write protection)

5.2 eDP Interface (compliant to DP spec v1.1a & eDP spec v1.1)

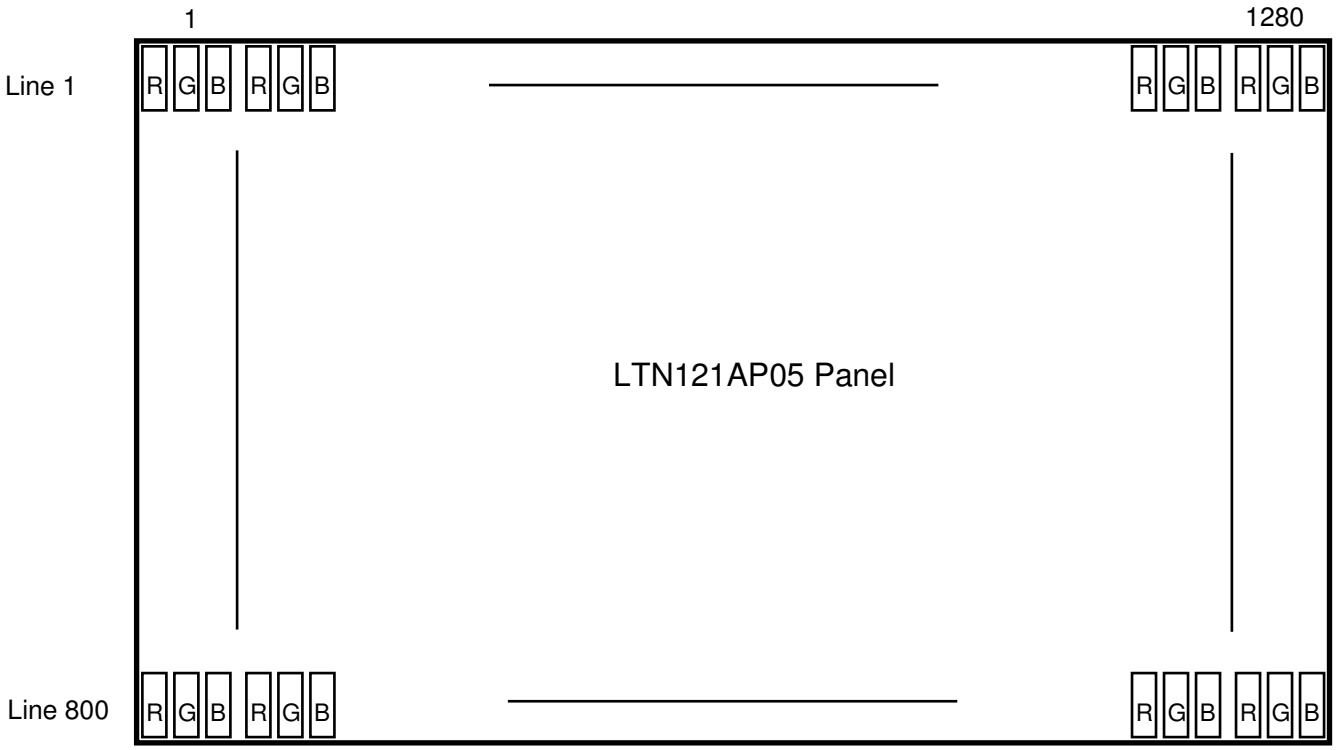


5.3 Input Signals, Basic Display Colors and Gray Scale of Each Color

Color	Display	Data Signal																		Gray Scale Level
		Red						Green						Blue						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	45	B5	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note 1) Definition of gray :
Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level)
Note 2)Input signal: 0 =Low level voltage, 1=High level voltage

5.4 Pixel Format in the display

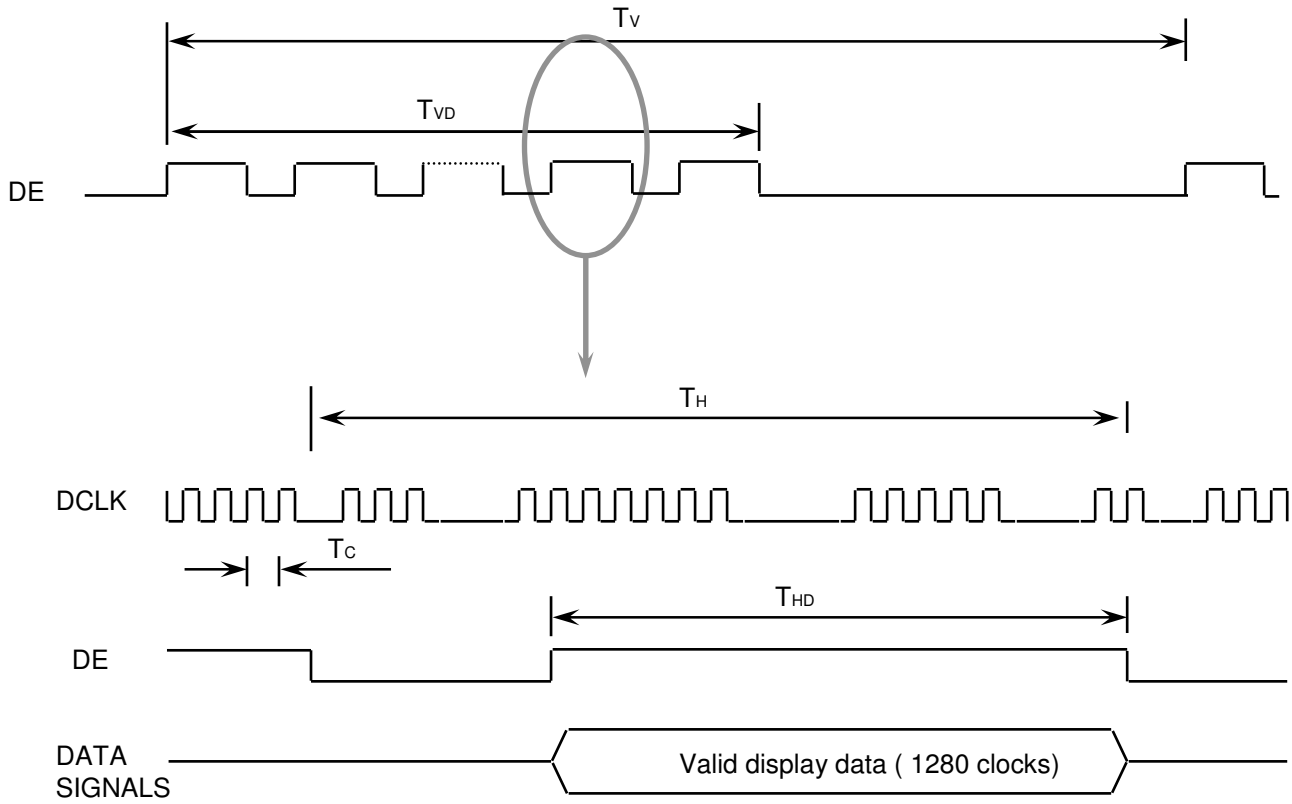


6. INTERFACE TIMING

6.1 Timing Parameters

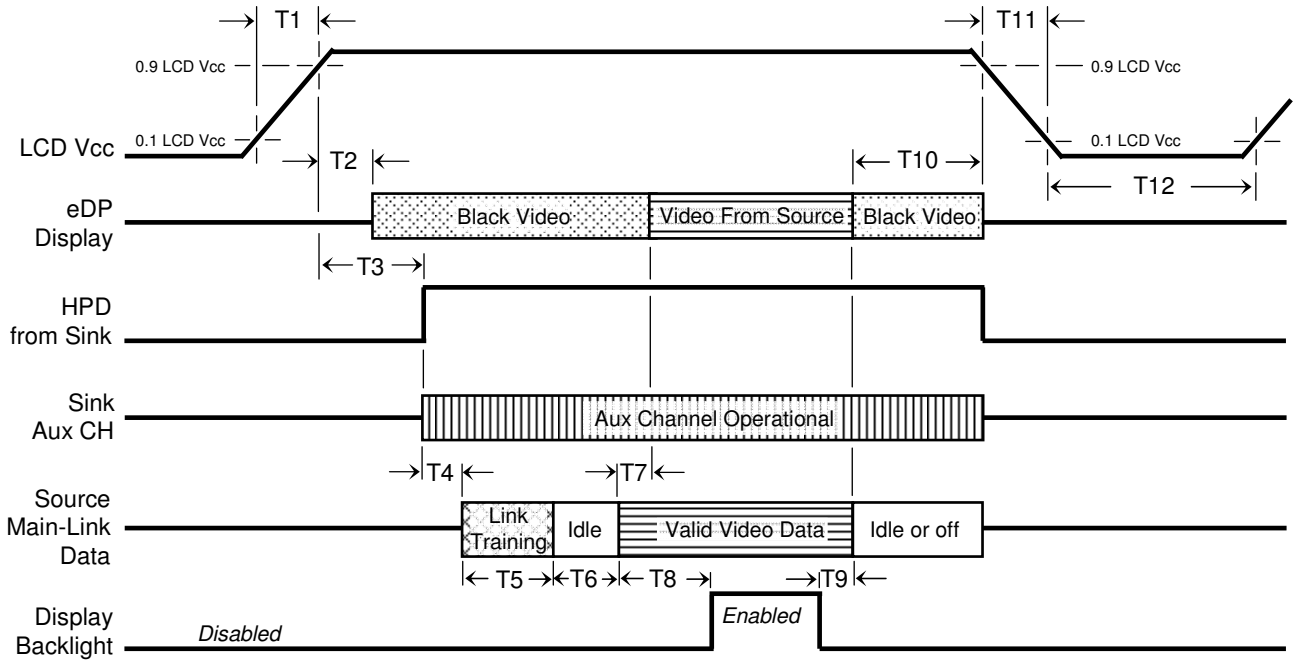
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	TV	804	816	860	Lines	
Vertical Active Display Term	Display Period	TVD	-	800	-	Lines	
One Line Scanning Time	Cycle	TH	1350	1415	1460	Clocks	
Horizontal Active Display Term	Display Period	THD	-	1280	-	Clocks	

6.2 Timing diagrams of interface signal

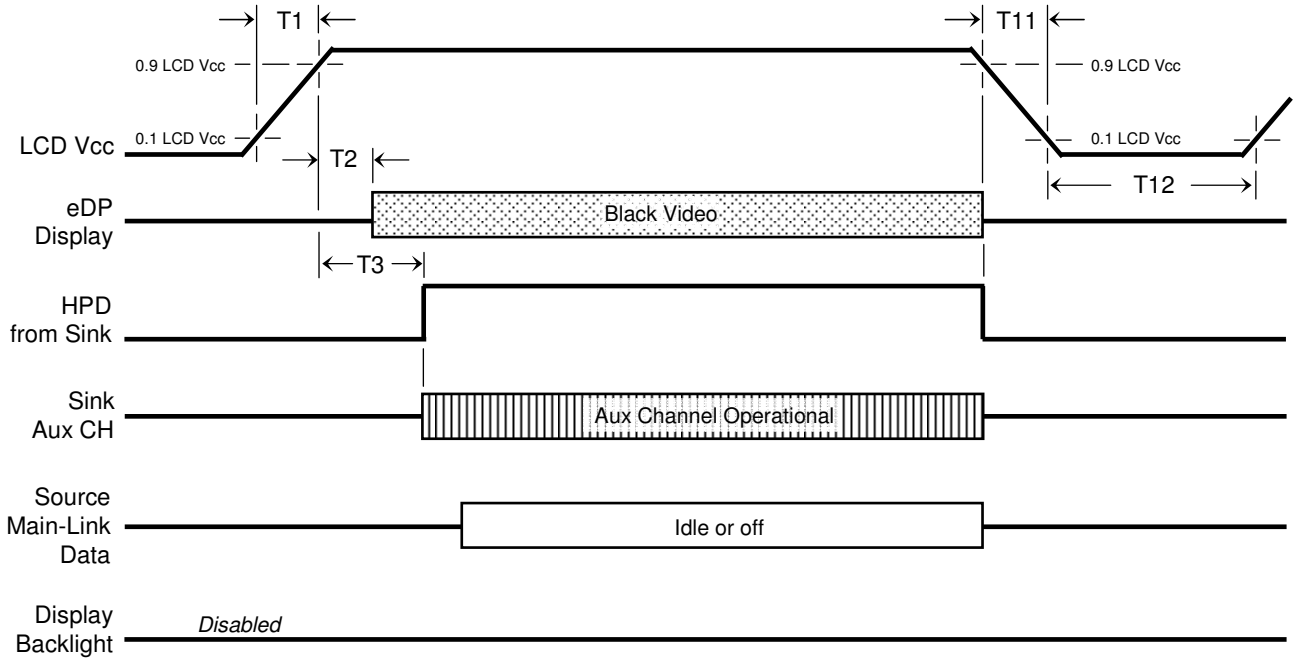


6.3 Power ON/OFF Sequence

: The Power ON/OFF sequence is described as follows :



Power ON/OFF Sequence, Normal System Operation



Power ON/OFF Sequence, Aux Channel Transaction Only

Timing Parameter	Description	Reqd. By	Limits (ms)		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5	10	
T2	Delay from LCD Vcc to black video generation	Sink	0	200	Prevents display noise until valid video data is received from Source (see note1 below)
T3	Delay from LCD Vcc to HPD high	Sink	0	200	Sink Aux Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization
T7	Delay from valid video data from Source to video on display	Sink	0	50	Max allows Sink validate video data and timing
T8	Delay from valid video data from Source to backlight	Source	-	-	Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	Source mush assure backlight is no longer illuminated (see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	0	500	
T11	Power rail fall time, 90% to 10%	Source		10	
T12	Power off time	Source	500	-	

Power Sequence Timing Parameters

Note 1) The Sink must include the ability to generate black video autonomously. The Sink must automatically enable black video under the following conditions:
- Upon LCD Vcc power-on (within T2 max)
- When the “NoVideoStream_Flag” (VB-ID Bit 3) is received from the Source (at the end of T9)
- When no Main Link data, or invalid video data, is received from the Source. Black video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

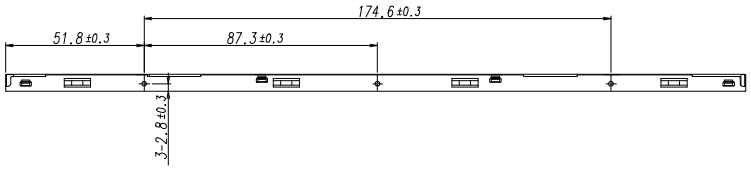
Note 2) The Sink may implement the ability to disable the black video function, as described in Notes 1, above, for system development and debugging purposes.

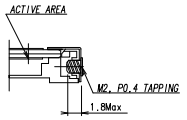
Note 3) The Sink must support Aux Channel polling by the Source immediately following LCD Vcc power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to respond to an Aux Channel transaction with the time specified within T3 max.

7. Mechanical Outline Dimension

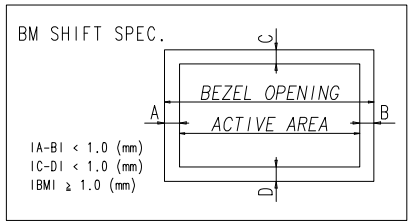
Refer to the next page

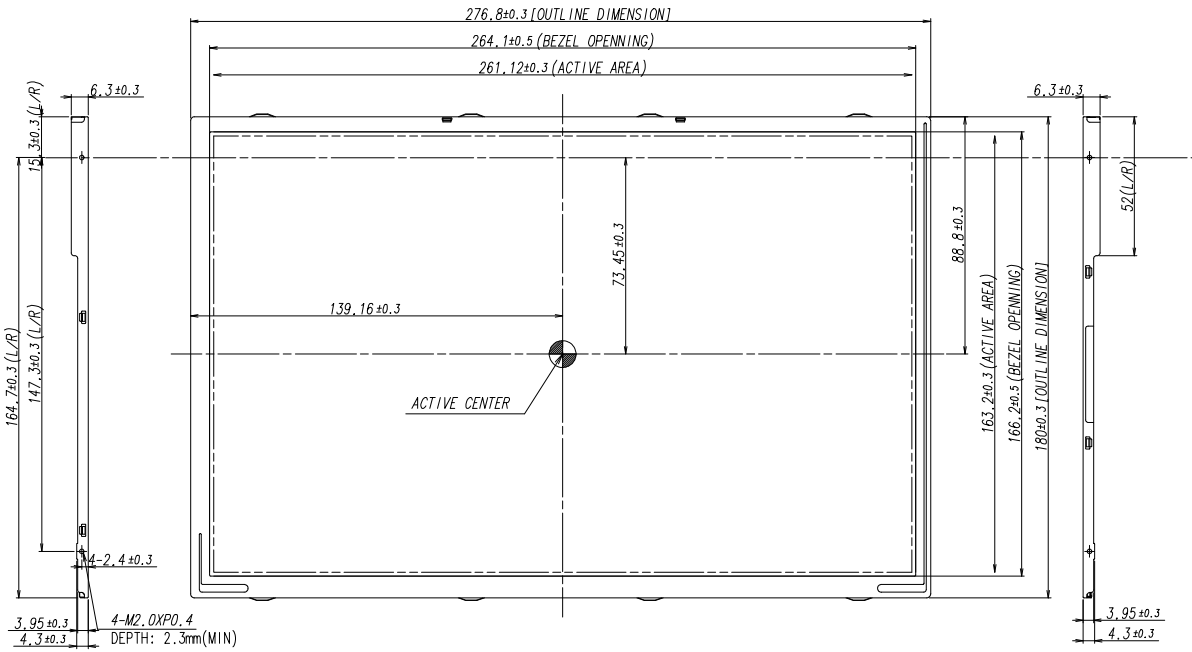
NO	PART NAME	CODE NO	SPECIFICATION	Q'TY	WEIGHT FINISH	WEIGHT MATERIAL	UNFOLDED DIM. OF. MATERIAL	REMARK

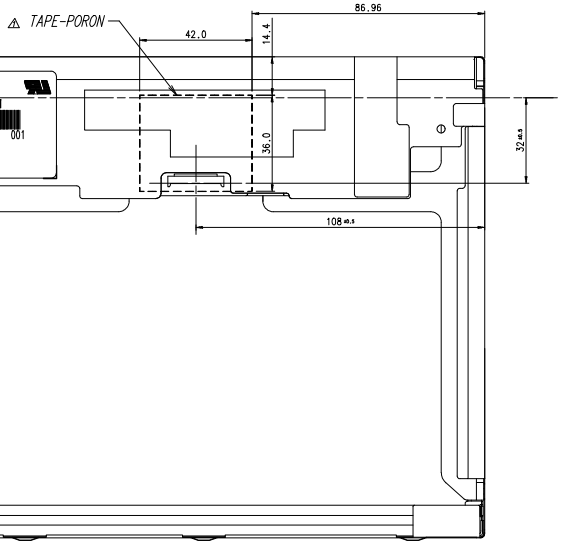


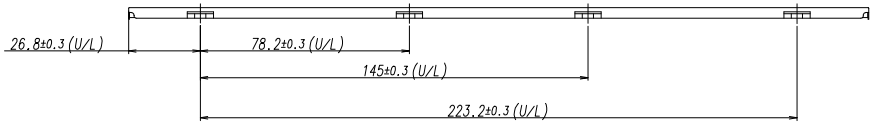


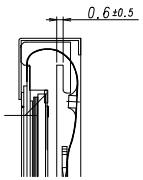
SCREW PENETRATION DEPTH











* NOTE

1. ***ALLOWED DEPTH OF USERHOLE SCREW INSERTION IS 1.8mm MAX.***
2. *MEASURING FORCE : 750gf-cm*
3. *USER HOLE TORQUE SPEC : 2.0kgf-cm Max(5times)*
4. *WEIGHT : 275 Max*
5. *SIGNAL INTERFACE CONNECTOR TO BE SPECIFIELD AS BELOW*
   - *MAKER : JAE*
   - *PART NO : 20455-030E-02R, I-PEX*

REVISION

REV.	DATE	DESCRIPTION OF REVISION	REASON	CHG'D BY
001	10.05.10	ADD TAPE-PORON	To Improve PCB	S.W.Jung

UNIT	mm	DRA'N BY	DES'D BY	CHK'D BY	APP'D BY
SCALE	1/1		J.E.YOO	S.H.LEE	D.C.YANG
TOLERANCE			09.04.06	09.04.06	09.04.06

SAMSUNG ELECTRONICS

SPEC. NO

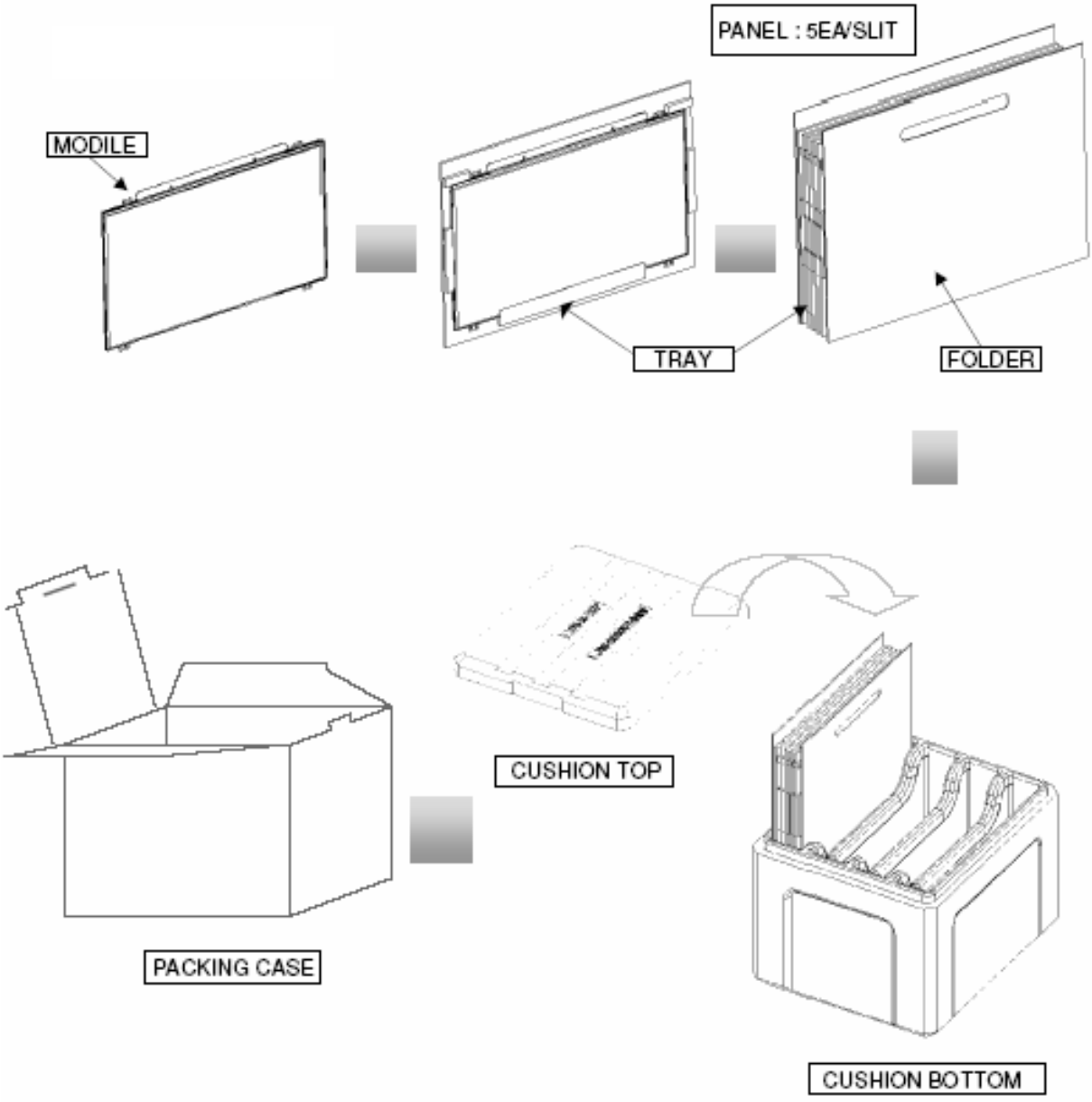
MODEL NAME	LTN121AP05-001	
PART/SHEET NAME	OUTLINE DIMENSION	SHEET 1/1
CODE NO.		VER. 001

8. PACKING

1. CARTON(Internal Package)

(1) Packing Form
Corrugated Cardboard box and Corrupad form as shock absorber

(2) Packing Method



Note 1)Total Weight : Approximately 9.46kg
2) Acceptance number of piling : 20 sets
3) Carton size : 495(W) × 423(D) × 320(H)
4) MAX accumulation quantity : 12 cartons

(3)Packing Material

No	Part name	Quantity
1	Static electric protective sack	20
2	Packing case (Inner box) included shock absorber	1 set
3	Pictorial marking	2 pcs
4	Carton	1 set

9. MARKINGS & OTHERS

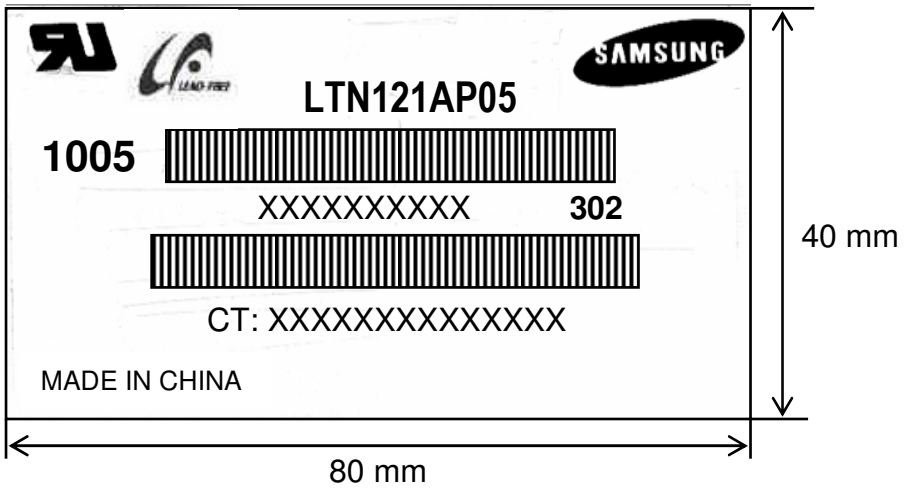
A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

(1)Parts number : LTN121AP05-302
(2)Revision : Three letters
(3)Lot number : X X X X XXX XX X **302**

Revision code

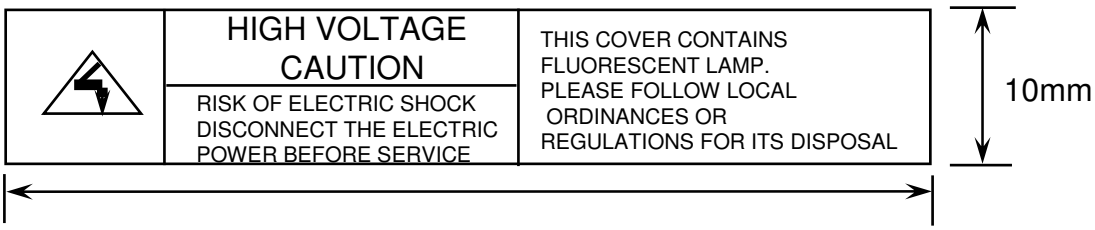
- Cell Position No.(In the one Glass)
- Glass No.(In the one Lot)
- Lot No.(Glass)
- Month
- Year(Note 1)
- Product Code
- Line

(4) Nameplate Indication

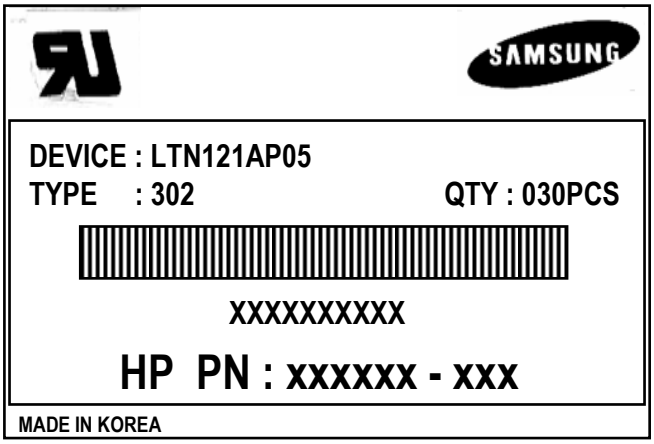


Parts name : LTN121AP05-301
Lot number : XXXXXXXXXX
Inspected work week : 1005 (2010 year 5th week)
Product Revision Code : **302**
CT code : XXXXXXXXXXXXX (Released after HP's approval)

High voltage caution label



(5) Packing small box attach



(6) Packing box Marking : Samsung TFT-LCD Brand Name

10. GENERAL PRECAUTIONS

1. Handling

(a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and LED back-light.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA (Isoprophyl Alcohol) or Hexane.
Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the C-MOS Gate Array IC.

(i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Do not pull or fold the lamp wire.

(l) Do not adjust the variable resistor which is located on the back side.

(m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(n) Pins of I/F connector shall not be touched directly with bare hands.

2. STORAGE

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module in direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

(a) Do not connect,disconnect the module in the " Power On" condition.

(b) Power supply should always be turned on/off by following item 6.3 " Power on/off sequence ".

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

4. OTHERS

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image "sticks" to the screen.

(e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

11. EDID

Address (HEX)	FUNCTION	Value HEX	BIN	DEC	ASCII or Data	Notes
00	Header	00	00000000	0		EDID Header
01		FF	11111111	255		
02		FF	11111111	255		
03		FF	11111111	255		
04		FF	11111111	255		
05		FF	11111111	255		
06		FF	11111111	255		
07		00	00000000	0		
08	ID Manufacturer Name	4C	01001100	76	S	3 character ID
					E	
09		A3	10100011	163	C	"SEC"
0A	ID Product Code	41	01000001	65	[A]	
0B		4C	01001100	76	[L]	
0C	32-bit serial no.	00	00000000	0		
0D		00	00000000	0		
0E		00	00000000	0		
0F		00	00000000	0		
10	Week of manufacture	00	00000000	0		
11	Year of manufacture	13	00010011	19	2009	2008
12	EDID Structure Ver.	01	00000001	1	1	EDID Ver. 1.0
13	EDID revision #	04	00000100	4	4	EDID Rev. 4
14	Video input definition	80	10000000	128		
15	Max H image size	1A	00011010	26	26	26 cm(approx)
16	Max V image size	10	00010000	16	16	16 cm(approx)
17	Display Gamma	78	01111000	120	2.2	Gamma 2.2
18	Feature support	0A	00001010	10		
19	Red/green low bits	87	10000111	135		10000111
1A	Blue/white low bits	F5	11110101	245		11111110
1B	Red x/ high bits	94	10010100	148	0.580	Red x 0.580=
						1001010010
1C	Red y	57	01010111	87	0.340	Red y 0.340=
						0101011100
1D	Green x	4F	01001111	79	0.310	Green x 0.310=
						0100111101
1E	Green y	8C	10001100	140	0.550	Green y 0.550=
						1000110011
1F	Blue x	27	00100111	39	0.155	Blue x 0.155=
						001001111
20	Blue y	27	00100111	39	0.155	Blue y 0.155=
						001001111
21	White x	50	01010000	80	0.313	White x 0.313=
						0101000001
22	White y	54	01010100	84	0.329	White y 0.329=
						0101010001
23	Established timing 1	00	00000000	0		
24	Established timing 2	00	00000000	0		
25	Established timing 3	00	00000000	0		

26	Standard timing #1	01	00000001	1		not used
27		01	00000001	1		
28	Standard timing #2	01	00000001	1		not used
29		01	00000001	1		
2A	Standard timing #3	01	00000001	1		not used
2B		01	00000001	1		
2C	Standard timing #4	01	00000001	1		not used
2D		01	00000001	1		
2E	Standard timing #5	01	00000001	1		not used
2F		01	00000001	1		
30	Standard timing #6	01	00000001	1		not used
31		01	00000001	1		
32	Standard timing #7	01	00000001	1		not used
33		01	00000001	1		
34	Standard timing #8	01	00000001	1		not used
35		01	00000001	1		
36	Detailed timing/monitor descriptor #1	12	00010010	18	69.3	Main clock= 69.3 MHz
37		1B	00011011	27		
38		00	00000000	0	1280	Hor active=640*2 pixels
39		49	01001001	73	73	Hor blanking=135 pixels
3A		50	01010000	80		4bit : 4bit
3B		20	00100000	32	800	Vertcal active=800 lines
3C		36	00110110	54	54	Vertical blanking=16 lines
3D		30	00110000	48		4bit : 4bit
3E		10	00010000	16	16	Hor sync. Offset=16 pixels
3F		30	00110000	48	48	H sync. Width=48 pixels
40		13	00010011	19	1 3	V sync. Offset=1 lines V sync. Width=3 lines
41		00	00000000	0		2bit : 2bit :2bit :2bit
42		05	00000101	5	261	H image size= 261 mm(approx)
43		A3	10100011	163	163	V image size = 163 mm(approx)
44		10	00010000	16		
45		00	00000000	0		No Horizontal Border
46		00	00000000	0		No Vertical Border
47		19	00011001	25		
48	Detailed timing/monitor descriptor #2 (sDRRS 40Hz)	0C	00001100	12	46.2	Main clock= 46.2 MHz
49		12	00010010	18		
4A		00	00000000	0	1280	Hor active=1280 pixels
4B		49	01001001	73	73	Hor blanking=135 pixels
4C		50	01010000	80		4bit : 4bit
4D		20	00100000	32	800	Vertcal active=800 lines
4E		36	00110110	54	54	Vertical blanking=16 lines
4F		30	00110000	48		4bit : 4bit
50		10	00010000	16	16	Hor sync. Offset=16 pixels
51		30	00110000	48	48	H sync. Width=48 pixels
52		13	00010011	19	1 3	V sync. Offset=1 lines V sync. Width=3 lines
53		00	00000000	0		2bit : 2bit :2bit :2bit
54		05	00000101	5	261	H image size= 261 mm(approx)
55		A3	10100011	163	163	V image size = 163 mm(approx)
56		10	00010000	16		
57		00	00000000	0		No Horizontal Border
58		00	00000000	0		No Vertical Border
59		19	00011001	25		

5A	Detailed timing/monitor descriptor #3(None)	00	00000000	0		
5B		00	00000000	0		
5C		00	00000000	0		
5D		00	00000000	0		
5E		00	00000000	0		
5F		00	00000000	0		
60		00	00000000	0		
61		00	00000000	0		
62		00	00000000	0		
63		00	00000000	0		
64		00	00000000	0		
65		00	00000000	0		
66		00	00000000	0		
67		00	00000000	0		
68		00	00000000	0		
69		00	00000000	0		
6A		00	00000000	0		
6B		00	00000000	0		
6C	Header	00	00000000	0		Detailed Timing Description#4
6D		00	00000000	0		Flag
6E		00	00000000	0		Reserved
6F		02	00000010	2		For Brightness Table and Power consumption
70		00	00000000	0		Flag
71	Brightness Table	0C	00001100	12		Step 0 = 5%, 10nits
72		3F	00111111	63		Step 5 = 25%, 60nits
73		F4	11110100	244		Step 10 = 96%, 220nits
74		0A	00001010	10		
75		3C	00111100	60		
76		6E	01101110	110		
77	Power Consumption	18	00011000	24		984mW
78		15	00010101	21		868mW
79		27	00100111	39		3144mW
7A		6E	01101110	110		220nits
7B	Flags	00	00000000	0		
7C	Flags	00	00000000	0		
7D	Flags	00	00000000	0		
7E	Extension Flag	00	00000000	0		
7F	Checksum	7A	01111010	122		