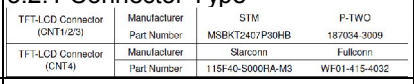
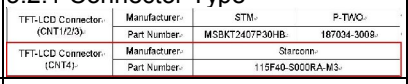
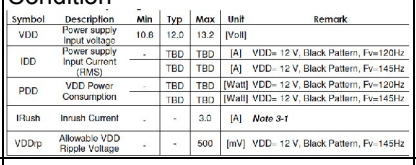
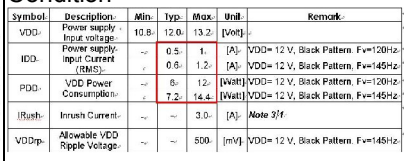
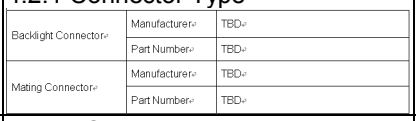
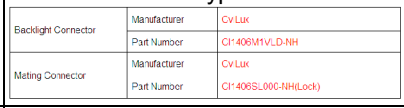
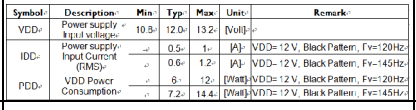
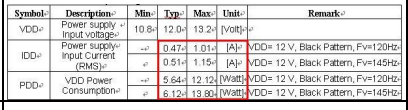
() Preliminary Specification
(V) Final Specification

Module	**23.8” Color TFT-LCD**
Model Name	**M238DTN01.2**

Customer	**Date**	**Approved by**	**Date**
		Howard Lee	Jan. 15, 2016
Approved by		**Prepared by**	**Date**
		Cherrychiu	Jan. 15, 2016
Note: This Specification is subject to change without notice.		AU Optronics corporation	

Contents

Record of Revision

Version	Date	Page	Old description	New Description	Remark
0.0	2015/11/06	All	First version release	-	
0.1	2015/12/14	P.6	Power Consumption **22.4 (Typ.)** LCD module : PDD (Typ.)=**6.5 W** @ Black pattern,Fv=144Hz Backlight unit : P_{BLU} (Typ.) =15.9 @Is=80mA	Power Consumption **22.4 (Typ.)** LCD module : PDD (Typ.)=**7.2 W** @ Black pattern,Fv=144Hz Backlight unit : P_{BLU} (Typ.) =15.9 @Is=80mA	
		P.15	3.2.1 Connector Type 	3.2.1 Connector Type 	
		P.20	3.3.2 Recommended Operating Condition 	3.3.2 Recommended Operating Condition 	
		P.32	4 Backlight Unit And it includes **60 pcs** LED in the LED light bar. (4 strings and **15 pcs** LED of one string).	4 Backlight Unit And it includes **60 pcs** LED in the LED light bar. (4 strings and **16pcs** LED of one string).	
		P.33	4.2.1 Connector Type 	4.2.1 Connector Type 	
1.1	2015/01/15	P.6	Power Consumption **22.4 (Typ.)** LCD module : PDD (Typ.)=**7.2 W** @ Black pattern,Fv=144Hz Backlight unit : P_{BLU} (Typ.) =15.9 @Is=80mA	Power Consumption **22.02 (Typ.)** LCD module : PDD (Typ.)=**6.12 W** @ Black pattern,Fv=144Hz Backlight unit : P_{BLU} (Typ.) =15.9 @Is=80mA	
		P.20	**3.3.2 Recommended Operating Condition** 	**3.3.2 Recommended Operating Condition** 	
		P.40	back side 圖面	back side 圖面 新增 cell 與 BLU 組裝規格	

1 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
12) Please avoid touching COF position while you are doing mechanical design.
13) When storing modules as spares for a long time, the following precaution is necessary:
    Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5□ and 35□ at normal humidity.

2 General Description

This specification applies to the 23.8 inch wide Color a-Si TFT-LCD Module M270DTN01.2. The display supports the QHD - 2560(H) x 1440(V) screen format and 16.7M colors (RGB 8-bit data). The input interface is 8 port LVDS and this module doesn't contain an driver board for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25□ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	23.8"
Active Area	[mm]	526.85 (H) x 296.35 (V)
Pixels H x V	-	2560(x3) x 1440
Pixel Pitch	[um]	205.8 (per one triad) ×205.8
Pixel Arrangement	-	R.G.B. Vertical Stripe
Display Mode	-	TN Mode, Normally White
White Luminance (Center)	[cd/m^2]	350 (Typ.)
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	5 (Typ., on/off)
Power Consumption (LCD Module + Backligh unit)	[Watt]	22.02 (Typ.) LCD module : PDD (Typ.)=6.12 W @ Black pattern,Fv=144Hz Backlight unit : P_{BLU} (Typ.) =15.9 @Is=80mA
Weight	[Grams]	2270 (typ.)
Outline Dimension	[mm]	536.7(H) x 313.89(V) x 12.3 (D)typ.
Electrical Interface	-	8 port LVDS
Support Color	-	16.7M colors (RGB 8-bits)
Surface Treatment	-	Anti-Glare, 3H
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance
TCO Compliance	-	TCO 6.0 Compliance

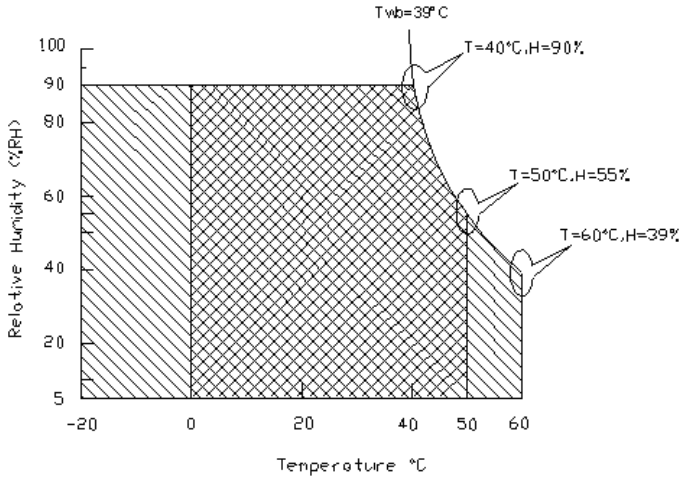
2.2 Absolute Maximum Rating of Environment

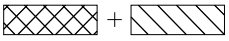
Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	***Note 2-1***
TGS	Glass surface temperature (operation)	0	+65	[°C]	***Note 2-1*** *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	***Note 2-1***
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta ≦39°C)
2. Max wet-bulb temperature at 39°C or less. (Ta ≦39°C)
3. No condensation



Operating Range  Storage Range 

2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

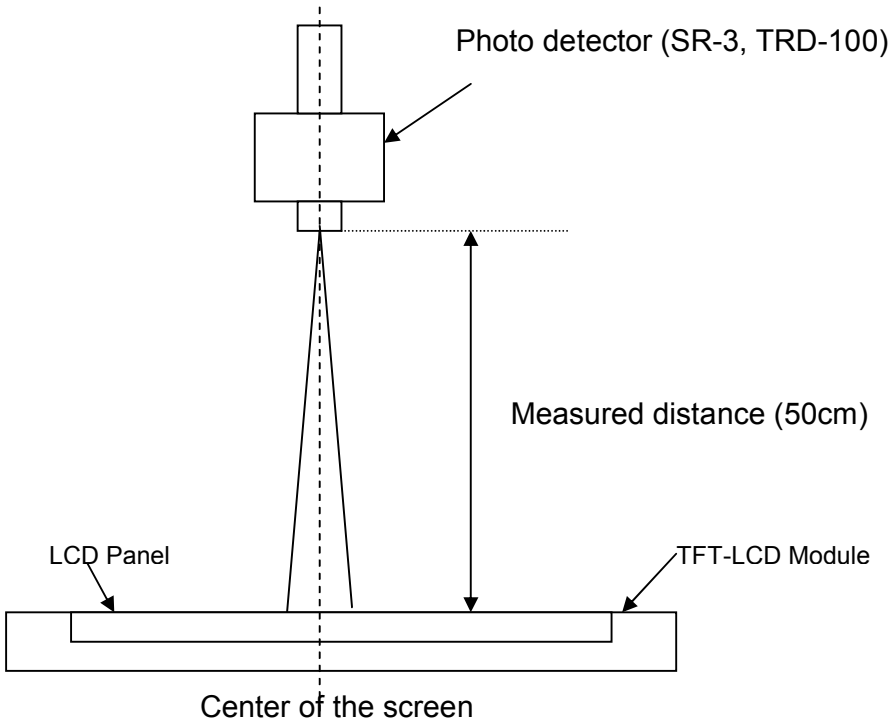
Test Condition:

1. Equipment setup: Please refer to ***Note 2-2***.
2. Panel Lighting time: 30 minutes
3. VDD=12.0V, Fv=120Hz, **Is=80mA**,Ta=25□

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_w	White Luminance (Center of screen)		300	350	-	[cd/m2]	***Note 2-2*** *By SR-3*
L_{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	***Note 2-3*** *By SR-3*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	***Note 2-4*** *By SR-3*
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	85	-	[degree]	***Note 2-5*** *By SR-3*
θ_L		Left	75	85	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	70	80	-		
Φ_L		Down	70	80	-		
θ_R	Horizontal Viewing Angle (CR=5)	Right	75	88	-		
θ_L		Left	75	88	-		
Φ_H	Vertical Viewing Angle (CR=5)	Up	70	85	-		
Φ_L		Down	70	85	-		
T_R	Response Time	Rising Time	-	3.5	5.5	[msec]	***Note 2-6*** *By TRD-100*
T_F		Falling Time	-	1.5	2.5		
-		Rising + Falling	-	5	8		
R_x	Color Coordinates (CIE 1931)	Red x	0.614	0.644	0.674	-	*By SR-3*
R_y		Red y	0.312	0.342	0.372		
G_x		Green x	0.294	0.324	0.354		
G_y		Green y	0.596	0.626	0.656		
B_x		Blue x	0.123	0.153	0.183		
B_y		Blue y	0.023	0.053	0.083		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
NTSC				72		[%]	*By SR-3*
CT Crosstalk			-	-	1.5	[%]	***Note 2-7*** *By SR-3*

F_{dB}	Flicker (Center of screen)	-	-	-20	[dB]	***Note 2-8*** *By SR-3*

Note 2-2: Equipment setup :

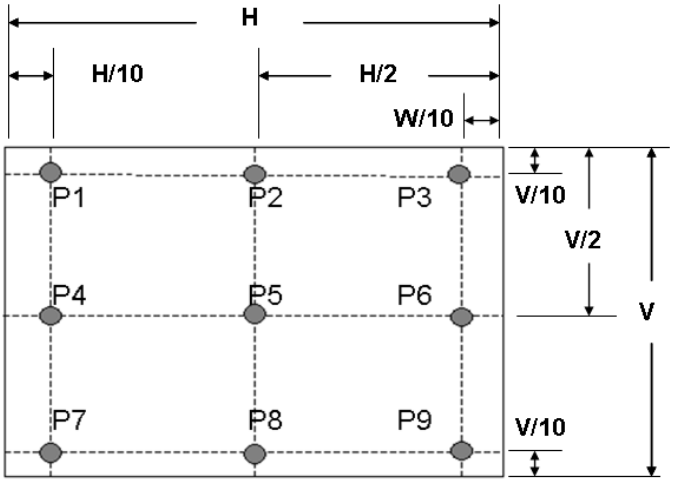


Note 2-3: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformity} = \frac{\text{Minimum Luminance of 9 Points (P1 ~ P9)}}{\text{Maximum Luminance of 9 Points (P1 ~ P9)}}$$

a. Test pattern: White Pattern



Note 2-4: Contrast Ratio Measurement

Definition:

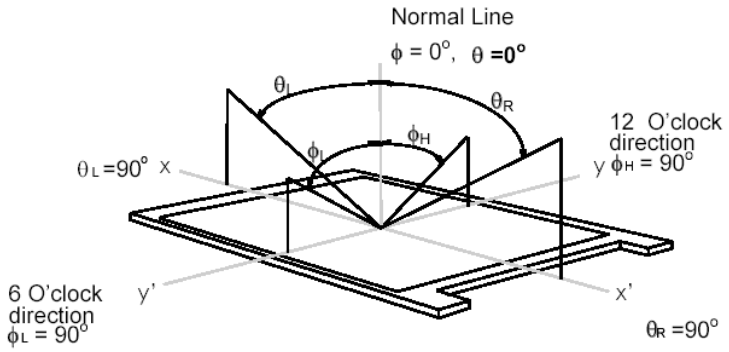
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

Note 2-5: Viewing angle measurement

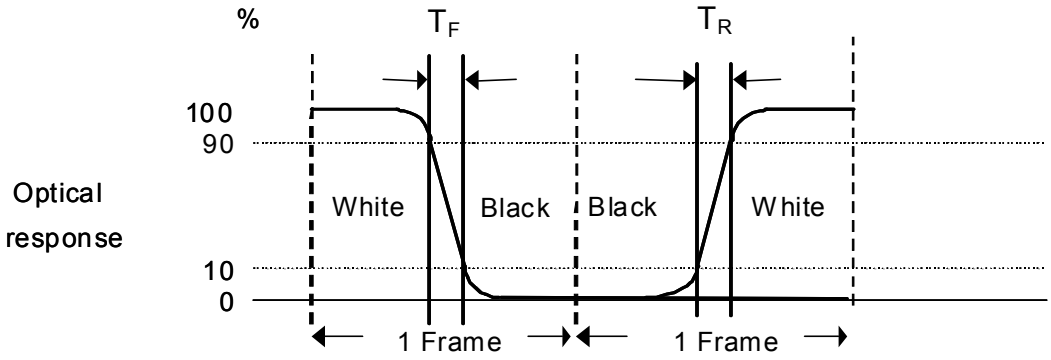
Definition: The angle at which the contrast ratio is greater than 10 & 5 .

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)



Note 2-6: Response time measurement

The output signals of photo detector are measured when the input signals are changed from “Black” to “White” (rising time, T_R), and from “White” to “Black” (falling time, T_F), respectively. The response time is interval between the 10% and 90% of optical response. (*Black & White color definition: Please refer section 3.4.3)*



Note 2-7: Crosstalk measurement

Definition:

$CT = Max. (CT_H, CT_V)$;

Where

a.Maximum Horizontal Crosstalk :

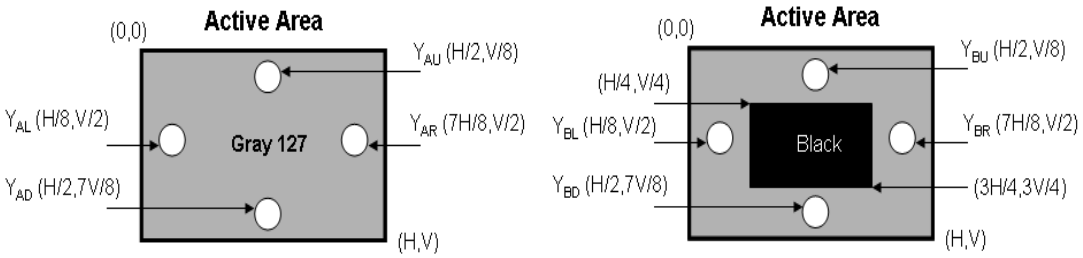
$CT_H = Max. (| Y_{BL} – Y_{AL} | / Y_{AL} \times 100\ \%, | Y_{BR} – Y_{AR} | / Y_{AR} \times 100\ \%)$;

Maximum Vertical Crosstalk:

$CT_V = Max. (| Y_{BU} – Y_{AU} | / Y_{AU} \times 100\ \%, | Y_{BD} – Y_{AD} | / Y_{AD} \times 100\ \%)$;

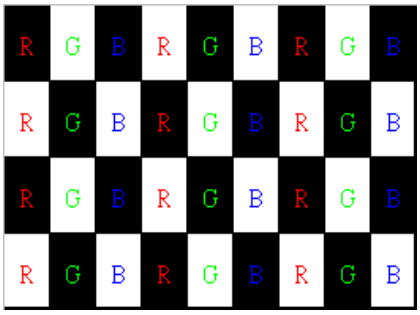
b. Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR} = Luminance of measured location without Black pattern

Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR} = Luminance of measured location with Black pattern



Note 2-8: Flicker measurement

a. Test pattern: It is listed as following.



Gray level = L0

Gray level = L127

R: Red, G: Green, B:Blue

b. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

2.4 Mechanical Characteristics

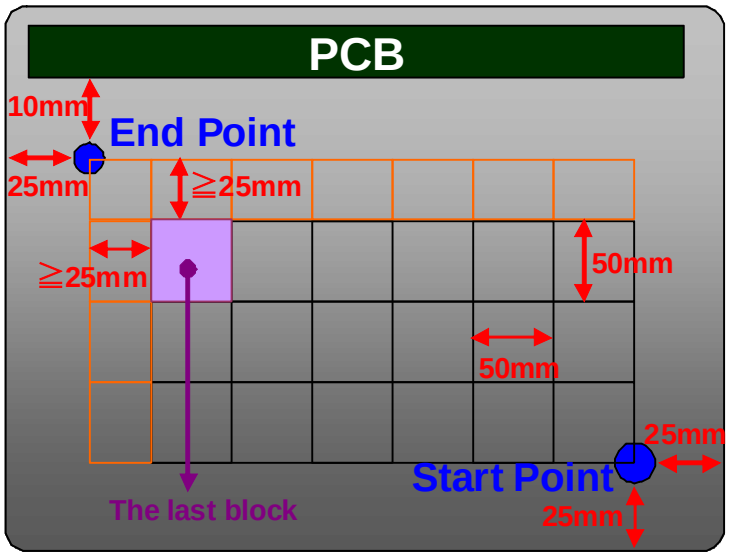
Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	*Note 2-9*

Note 2-9: Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

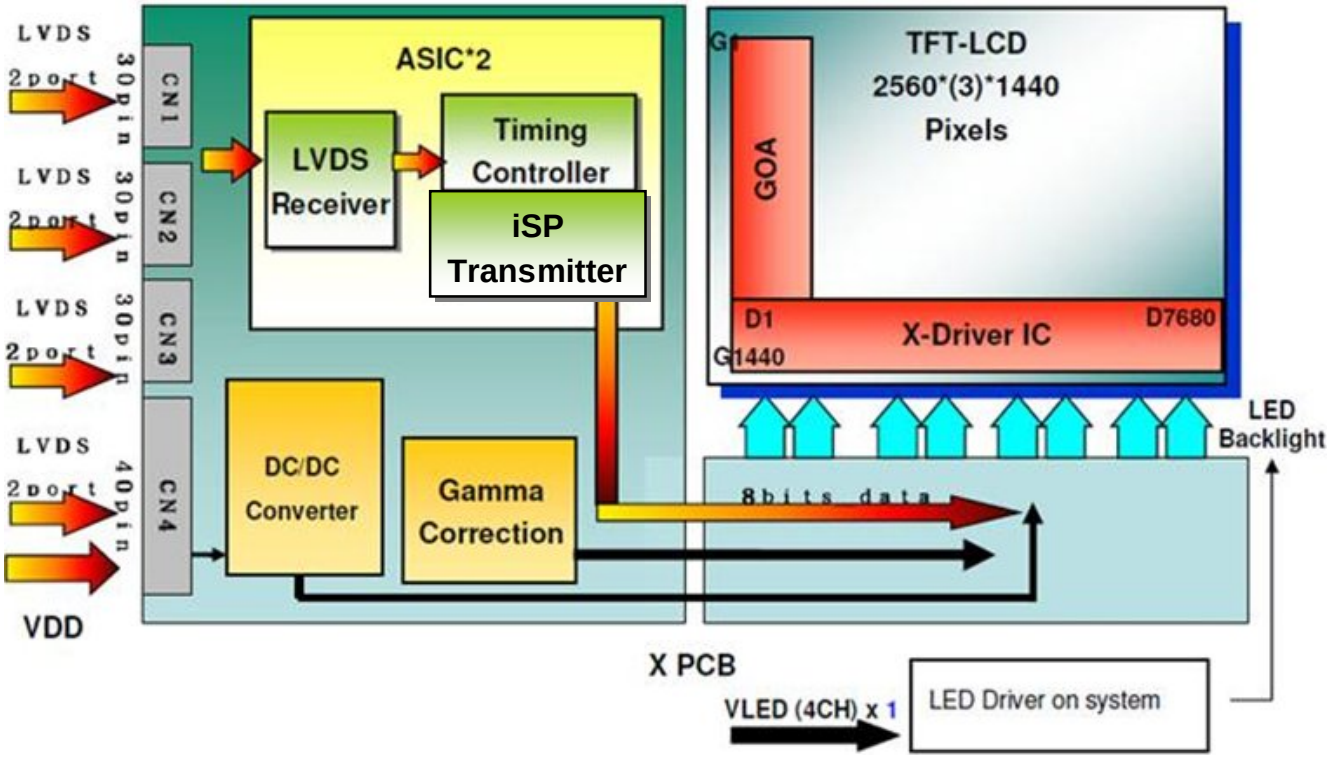
If the distance from the last block to each side of the End Point ≧ 25mm, add other blocks to make sure that most area of Bezel Back can be measured.



3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 23.8 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD Connector (CNT1/2/3)	Manufacturer	STM	P-TWO
	Part Number	MSBKT2407P30HB	187034-30091
TFT-LCD Connector (CNT4)	Manufacturer	Starconn	
	Part Number	115F40-S000RA-M3	
Mating Connector (CNT1/2/3)	Manufacturer	STM or Compatible	
	Part Number	PK2407P30V or Compatible	
Mating Connector (CNT4)	Manufacturer	JAE or Compatible	
	Part Number	FI-NX40HL or Compatible	

3.2.2 Connector Pin Assignment

CN 1

PIN #	Symbol	Description	Remark
1	R1_0N	Negative LVDS differential data input (Port1 data)	
2	R1_0P	Positive LVDS differential data input (Port1 data)	
3	R1_1N	Negative LVDS differential data input (Port1data)	
4	R1_1P	Positive LVDS differential data input (Port1 data)	
5	R1_2N	Negative LVDS differential data input (Port1 data)	
6	R1_2P	Positive LVDS differential data input (Port1 data)	
7	GND	Ground	
8	R1_CLKN	Negative LVDS differential clock input (Port1 clock)	
9	R1_CLKP	Positive LVDS differential clock input (Port1 clock)	
10	GND	Ground	
11	R1_3N	Negative LVDS differential data input (Port1 data)	
12	R1_3P	Positive LVDS differential data input (Port1 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R2_0N	Negative LVDS differential data input (Port2 data)	
17	R2_0P	Positive LVDS differential data input (Port2 data)	
18	R2_1N	Negative LVDS differential data input (Port2 data)	
19	R2_1P	Positive LVDS differential data input (Port2 data)	

20	R2_2N	Negative LVDS differential data input (Port2 data)	
21	R2_2P	Positive LVDS differential data input (Port2 data)	
22	GND	Ground	
23	R2_CLKN	Negative LVDS differential clock input (Port2 clock)	
24	R2_CLKP	Positive LVDS differential clock input (Port2 clock)	
25	GND	Ground	
26	R2_3N	Negative LVDS differential data input (Port2 data)	
27	R2_3P	Positive LVDS differential data input (Port2 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	NC	No connection (for AUO test only. Do not connect)	

CN 2

PIN #	Symbol	Description	Remark
1	R3_0N	Negative LVDS differential data input (Port3 data)	
2	R3_0P	Positive LVDS differential data input (Port3 data)	
3	R3_1N	Negative LVDS differential data input (Port3 data)	
4	R3_1P	Positive LVDS differential data input (Port3 data)	
5	R3_2N	Negative LVDS differential data input (Port3 data)	
6	R3_2P	Positive LVDS differential data input (Port3 data)	
7	GND	Ground	
8	R3_CLKN	Negative LVDS differential clock input (Port3 clock)	
9	R3_CLKP	Positive LVDS differential clock input (Port3 clock)	
10	GND	Ground	
11	R3_3N	Negative LVDS differential data input (Port3 data)	
12	R3_3P	Positive LVDS differential data input (Port3 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R4_0N	Negative LVDS differential data input (Port4 data)	
17	R4_0P	Positive LVDS differential data input (Port4 data)	
18	R4_1N	Negative LVDS differential data input (Port4 data)	
19	R4_1P	Positive LVDS differential data input (Port4 data)	
20	R4_2N	Negative LVDS differential data input (Port4 data)	
21	R4_2P	Positive LVDS differential data input (Port4 data)	
22	GND	Ground	
23	R4_CLKN	Negative LVDS differential clock input (Port4 clock)	
24	R4_CLKP	Positive LVDS differential clock input (Port4 clock)	

25	GND	Ground	
26	R4_3N	Negative LVDS differential data input (Port4 data)	
27	R4_3P	Positive LVDS differential data input (Port4 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	IMS_POL	Interlace Mode Selection Polarity (O)	

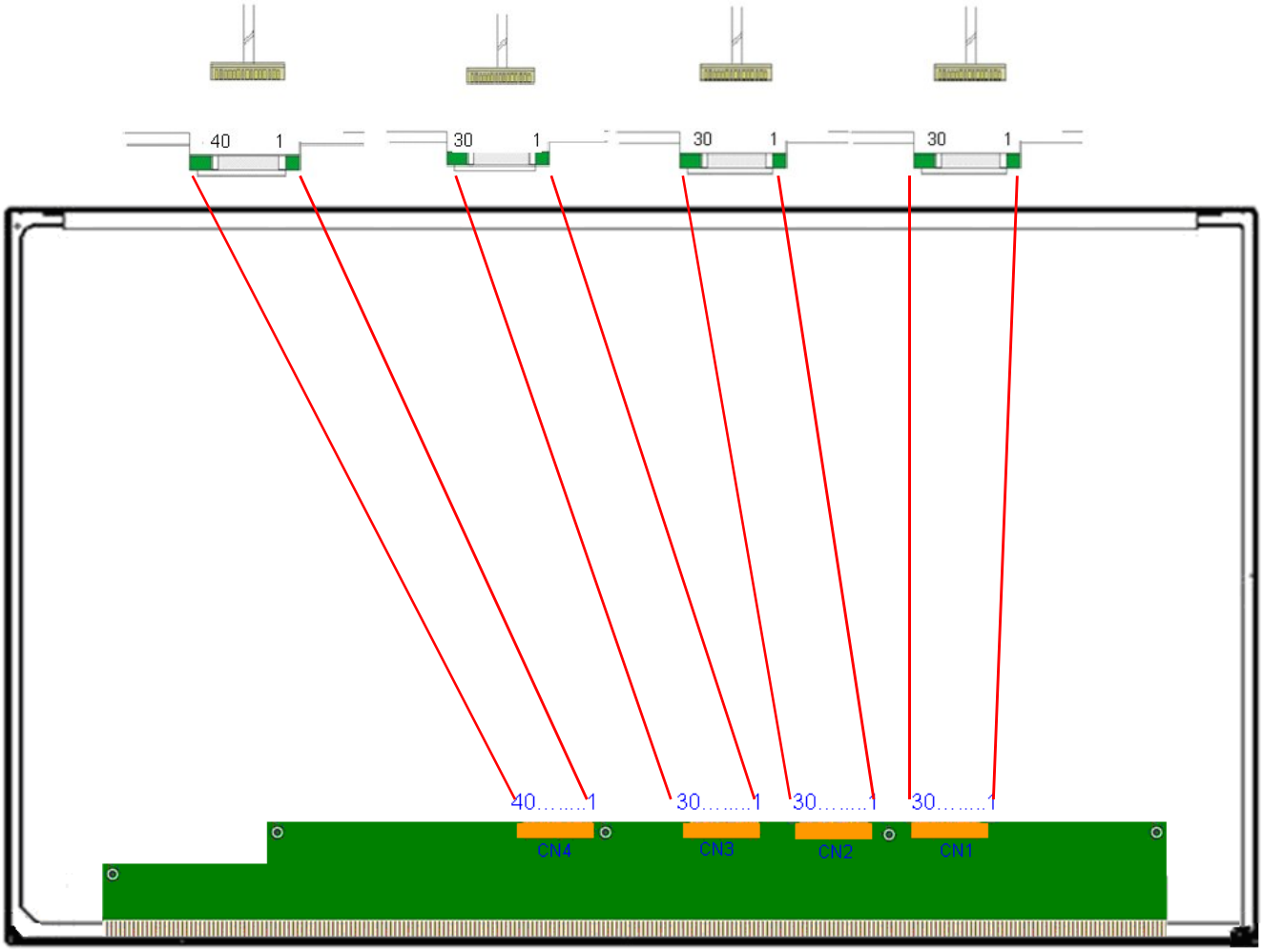
CN 3

PIN #	Symbol	Description	Remark
1	R5_0N	Negative LVDS differential data input (Port5 data)	
2	R5_0P	Positive LVDS differential data input (Port5 data)	
3	R5_1N	Negative LVDS differential data input (Port5 data)	
4	R5_1P	Positive LVDS differential data input (Port5 data)	
5	R5_2N	Negative LVDS differential data input (Port5 data)	
6	R5_2P	Positive LVDS differential data input (Port5 data)	
7	GND	Ground	
8	R5_CLKN	Negative LVDS differential clock input (Port5 clock)	
9	R5_CLKP	Positive LVDS differential clock input (Port5 clock)	
10	GND	Ground	
11	R5_3N	Negative LVDS differential data input (Port5 data)	
12	R5_3P	Positive LVDS differential data input (Port5 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R6_0N	Negative LVDS differential data input (Port6 data)	
17	R6_0P	Positive LVDS differential data input (Port6 data)	
18	R6_1N	Negative LVDS differential data input (Port6 data)	
19	R6_1P	Positive LVDS differential data input (Port6 data)	
20	R6_2N	Negative LVDS differential data input (Port6 data)	
21	R6_2P	Positive LVDS differential data input (Port6 data)	
22	GND	Ground	
23	R6_CLKN	Negative LVDS differential clock input (Port6 clock)	
24	R6_CLKP	Positive LVDS differential clock input (Port6 clock)	
25	GND	Ground	
26	R6_3N	Negative LVDS differential data input (Port6 data)	
27	R6_3P	Positive LVDS differential data input (Port6 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	IMS	Interlace Mode Selection (I)	

CN 4

PIN #	Symbol	Description	Remark
1	R7_0N	Negative LVDS differential data input (Port7 data)	
2	R7_0P	Positive LVDS differential data input (Port7 data)	
3	R7_1N	Negative LVDS differential data input (Port7 data)	
4	R7_1P	Positive LVDS differential data input (Port7 data)	
5	R7_2N	Negative LVDS differential data input (Port7 data)	
6	R7_2P	Positive LVDS differential data input (Port7 data)	
7	GND	Ground	
8	R7_CLKN	Negative LVDS differential clock input (Port7 clock)	
9	R7_CLKP	Positive LVDS differential clock input (Port7 clock)	
10	GND	Ground	
11	R7_3N	Negative LVDS differential data input (Port7 data)	
12	R7_3P	Positive LVDS differential data input (Port7 data)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	GND	Ground	
16	R8_0N	Negative LVDS differential data input (Port8 data)	
17	R8_0P	Positive LVDS differential data input (Port8 data)	
18	R8_1N	Negative LVDS differential data input (Port8 data)	
19	R8_1P	Positive LVDS differential data input (Port8 data)	
20	R8_2N	Negative LVDS differential data input (Port8 data)	
21	R8_2P	Positive LVDS differential data input (Port8 data)	
22	GND	Ground	
23	R8_CLKN	Negative LVDS differential clock input (Port8 clock)	
24	R8_CLKP	Positive LVDS differential clock input (Port8 clock)	
25	GND	Ground	
26	R8_3N	Negative LVDS differential data input (Port8 data)	
27	R8_3P	Positive LVDS differential data input (Port8 data)	
28	NC	No connection (for AUO test only. Do not connect)	
29	NC	No connection (for AUO test only. Do not connect)	
30	NC	No connection (for AUO test only. Do not connect)	
31	NC	No connection (for AUO test only. Do not connect)	
32	NC	No connection (for AUO test only. Do not connect)	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	GND	Ground	

36	NC	No connection (for AUO test only. Do not connect)	
37	VDD	Power Supply Input Voltage	
38	VDD	Power Supply Input Voltage	
39	VDD	Power Supply Input Voltage	
40	VDD	Power Supply Input Voltage	



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

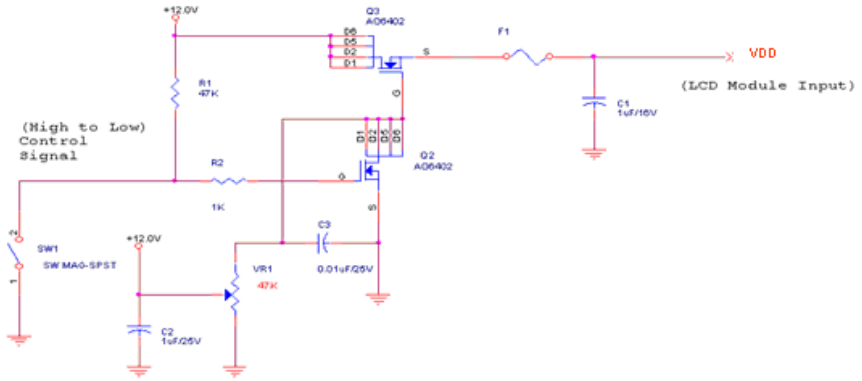
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25□

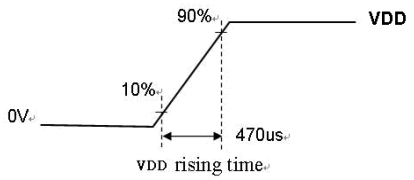
3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.47	1.01	[A]	VDD= 12 V, Black Pattern, Fv=120Hz
			0.51	1.15	[A]	VDD= 12 V, Black Pattern, Fv=145Hz
PDD	VDD Power Consumption	-	5.64	12.12	[Watt]	VDD= 12 V, Black Pattern, Fv=120Hz
			6.12	13.80	[Watt]	VDD= 12 V, Black Pattern, Fv=145Hz
IRush	Inrush Current	-	-	3.0	[A]	***Note 3-1***
VDDrp	Allowable VDD Ripple Voltage	-	-	500	[mV]	VDD= 12 V, Black Pattern, Fv=145Hz

Note 3-1: Inrush Current measurement:

Test circuit:

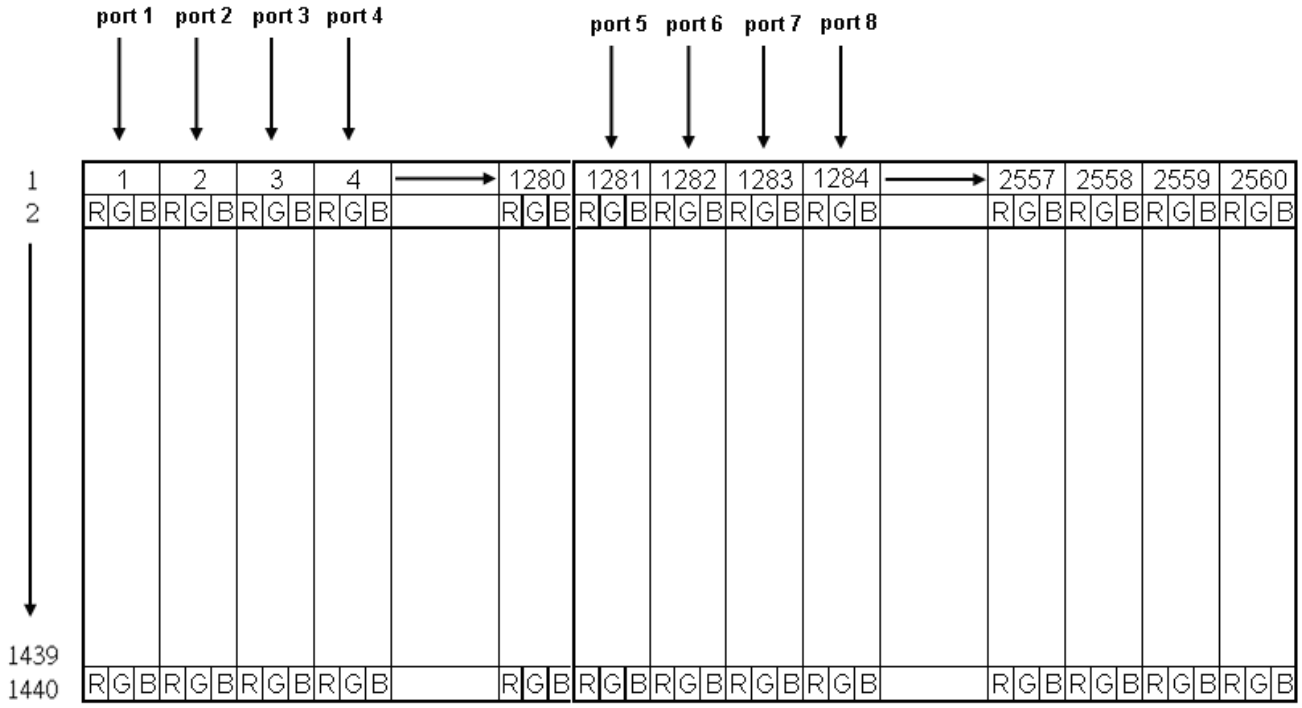




The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format



Note 3-2: The module use 8 port-LVDS interface.

Port 1：4N+1 N=0,~ 319 (1,5.. 1277pixel)

Port 2：4N+2 N=0,~ 319 (2,6.. 1278pixel)

Port 3：4N+3 N=0,~ 319 (3,7.. 1279pixel)

Port 4：4N+4 N=0,~ 319 (4,8.. 1280pixel)

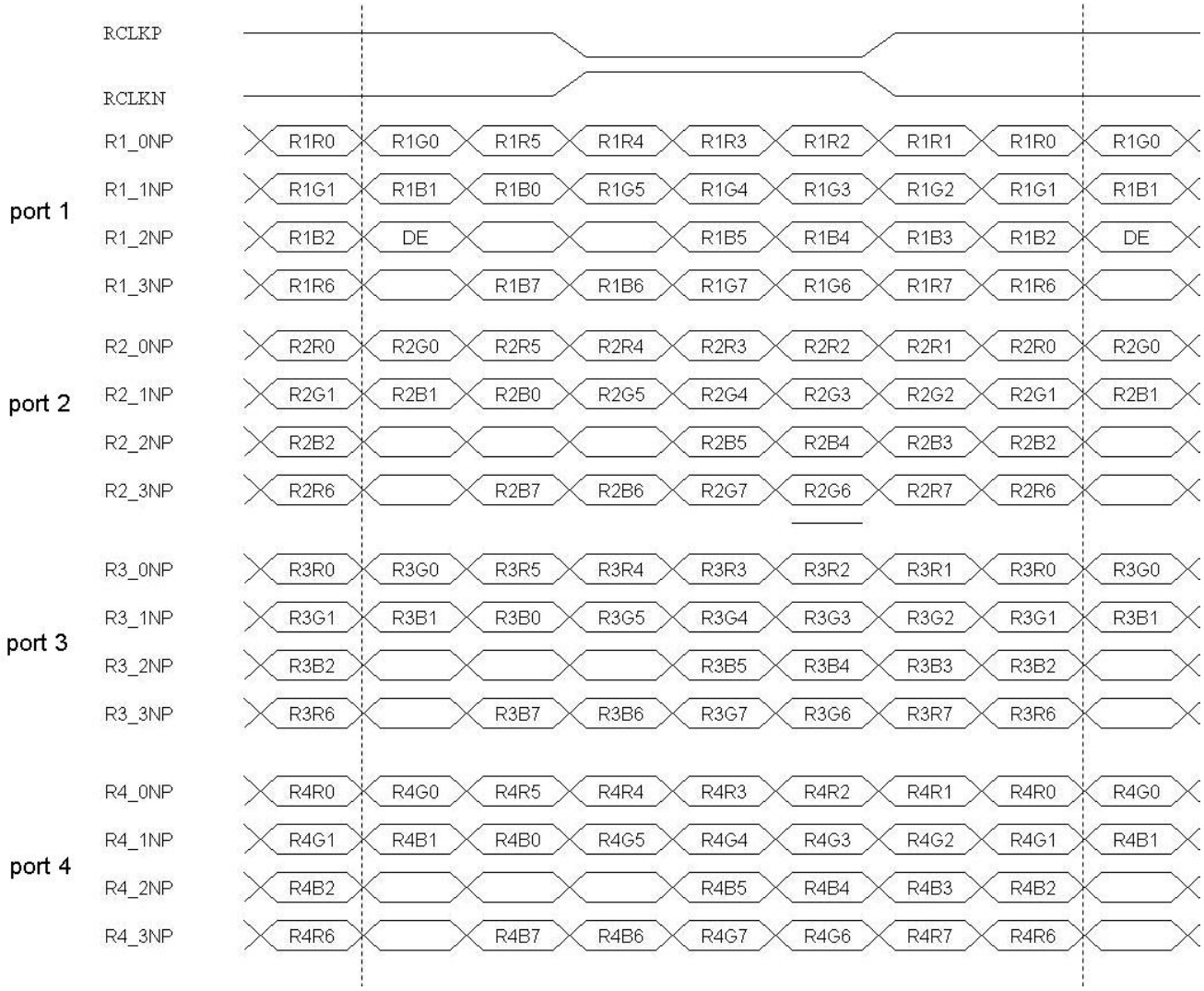
Port 5：4N+1281 N=0,~ 319 (1281,1285.. 2557pixel)

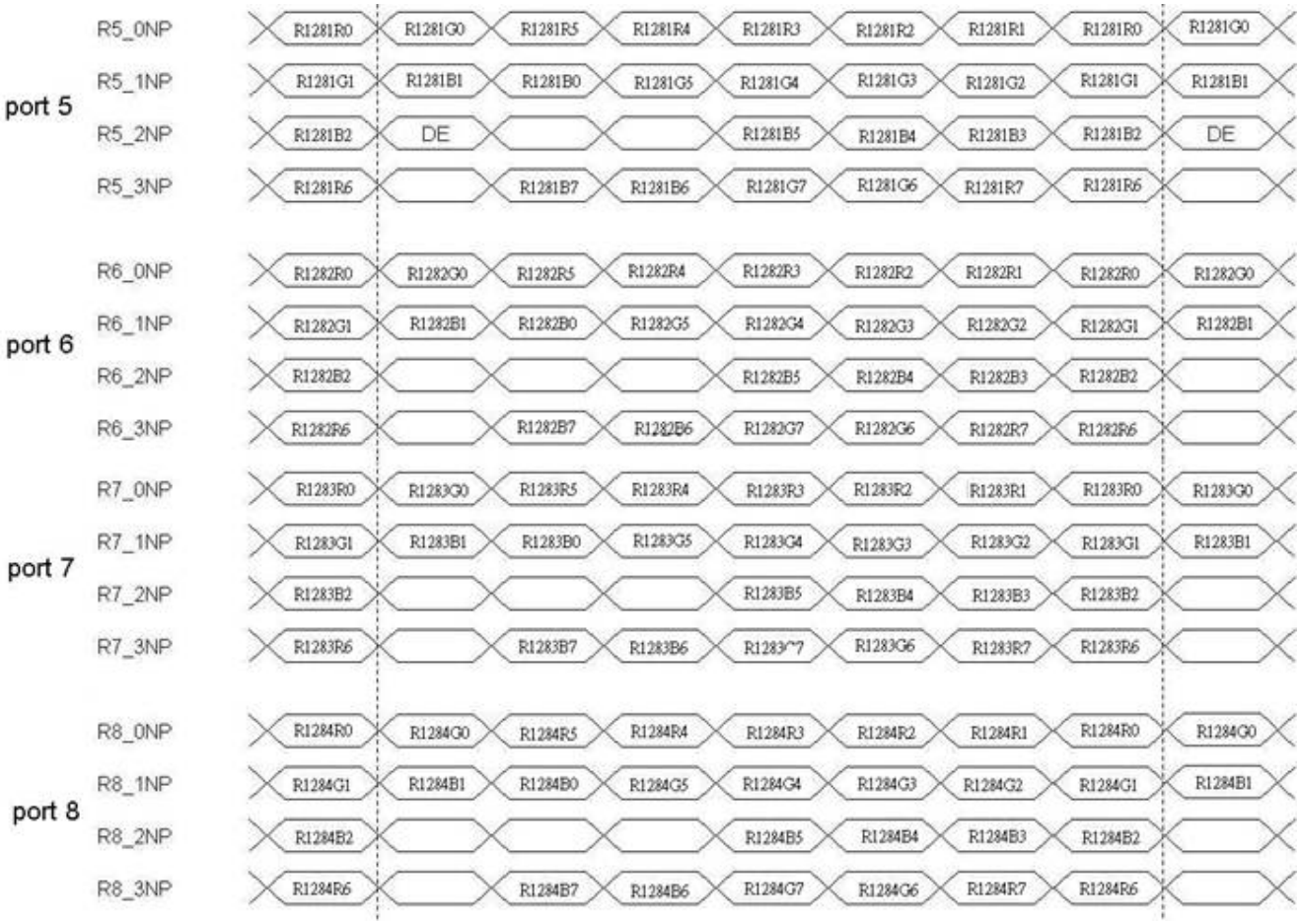
Port 6：4N+1282 N=0,~ 319 (1282,1286.. 2558pixel)

Port 7：4N+1283 N=0,~ 319 (1283,1287.. 2559pixel)

Port 8：4N+1284 N=0,~ 319 (1284,1288.. 2560pixel)

3.4.2 LVDS Data Format




port 5
R5_0NP
R5_1NP
R5_2NP
R5_3NP
R1281R0 R1281G0 R1281R5 R1281R4 R1281R3 R1281R2 R1281R1 R1281R0 R1281G0
R1281G1 R1281B1 R1281B0 R1281G5 R1281G4 R1281G3 R1281G2 R1281G1 R1281B1
R1281B2 DE R1281B5 R1281B4 R1281B3 R1281B2 DE
R1281R6 R1281B7 R1281B6 R1281G7 R1281G6 R1281R7 R1281R6
port 6
R6_0NP
R6_1NP
R6_2NP
R6_3NP
R1282R0 R1282G0 R1282R5 R1282R4 R1282R3 R1282R2 R1282R1 R1282R0 R1282G0
R1282G1 R1282B1 R1282B0 R1282G5 R1282G4 R1282G3 R1282G2 R1282G1 R1282B1
R1282B2 R1282B5 R1282B4 R1282B3 R1282B2
R1282R6 R1282B7 R1282B6 R1282G7 R1282G6 R1282R7 R1282R6
port 7
R7_0NP
R7_1NP
R7_2NP
R7_3NP
R1283R0 R1283G0 R1283R5 R1283R4 R1283R3 R1283R2 R1283R1 R1283R0 R1283G0
R1283G1 R1283B1 R1283B0 R1283G5 R1283G4 R1283G3 R1283G2 R1283G1 R1283B1
R1283B2 R1283B5 R1283B4 R1283B3 R1283B2
R1283R6 R1283B7 R1283B6 R1283G7 R1283G6 R1283R7 R1283R6
port 8
R8_0NP
R8_1NP
R8_2NP
R8_3NP
R1284R0 R1284G0 R1284R5 R1284R4 R1284R3 R1284R2 R1284R1 R1284R0 R1284G0
R1284G1 R1284B1 R1284B0 R1284G5 R1284G4 R1284G3 R1284G2 R1284G1 R1284B1
R1284B2 R1284B5 R1284B4 R1284B3 R1284B2
R1284R6 R1284B7 R1284B6 R1284G7 R1284G6 R1284R7 R1284R6

3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

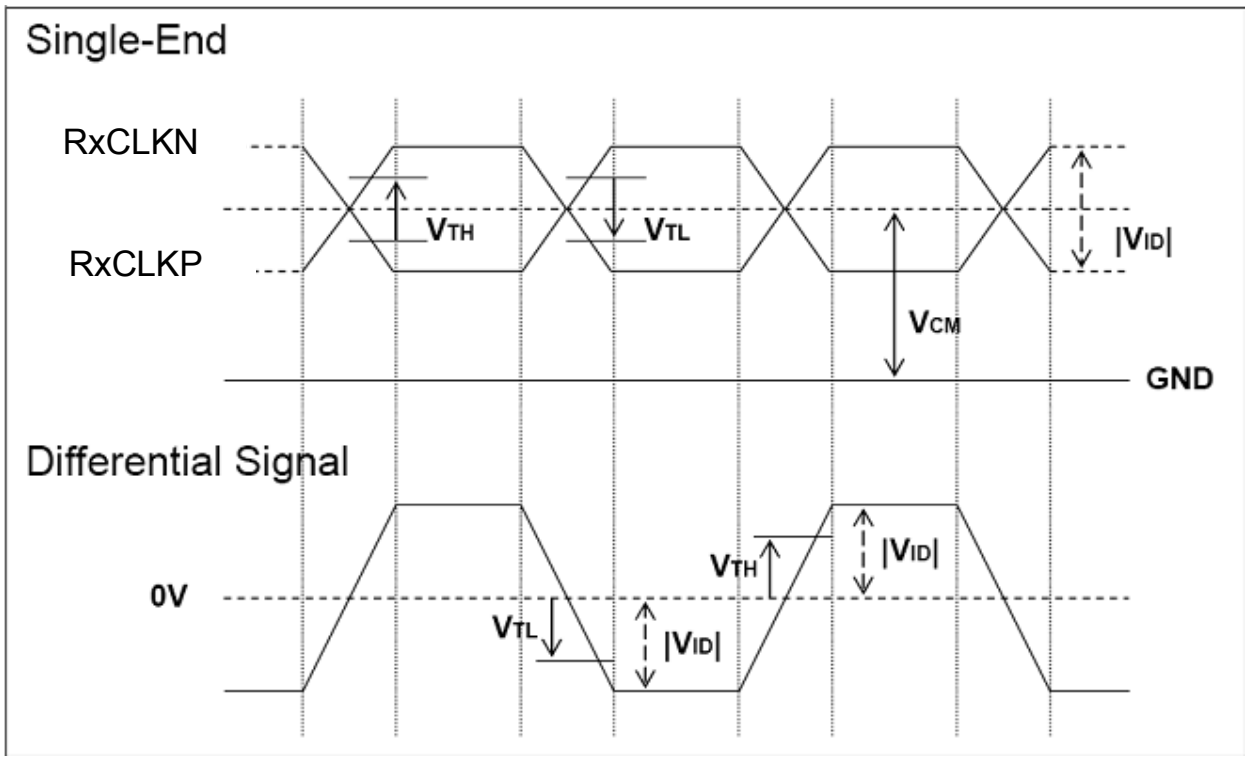
3.4.4 LVDS Specification

a. DC Characteristics:

Symbol	Description	Min	Typ	Max	Units	Condition
V_{TH}	LVDS Differential Input High Threshold	-	-	+100	[mV]	V_{CM} = 1.2V
V_{TL}	LVDS Differential Input Low Threshold	-100	-	-	[mV]	V_{CM} = 1.2V
$\lvert V_{ID} \rvert$	LVDS Differential Input Voltage	100	-	600	[mV]	
V_{CM}	LVDS Common Mode Voltage	+1.0	+1.2	+1.5	[V]	V_{TH}-V_{TL} = 200mV

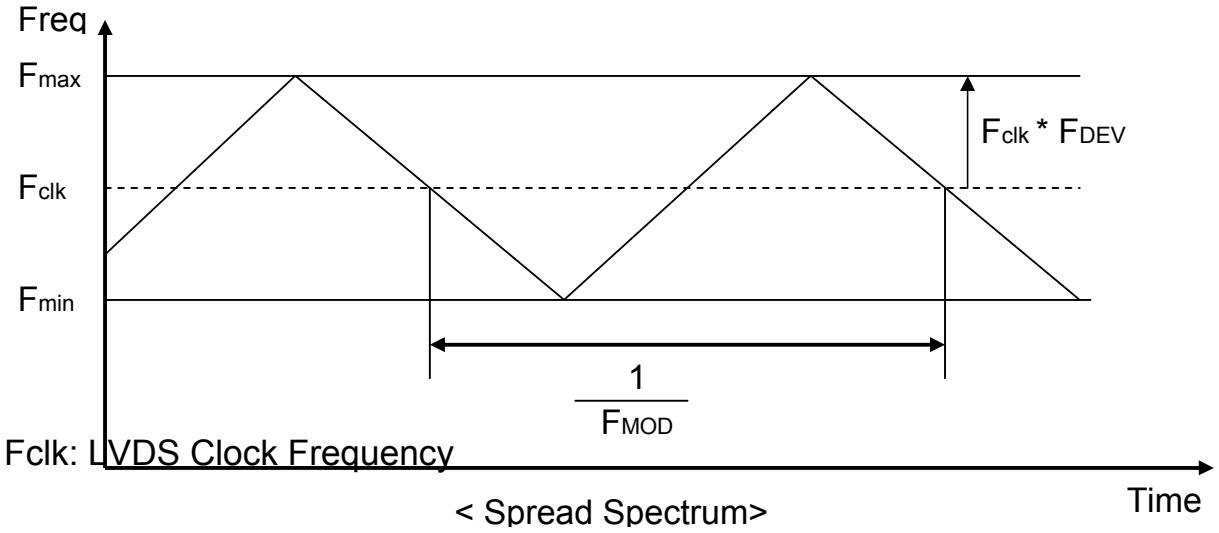
LVDS Signal Waveform:

Use RxCLKN & RxCLKP as example.



b. AC Characteristics:

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	100	KHz	



3.4.5 Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1452	1481	8192	Th	
Tdisp (v)		Active	1440	1440	1440	Th	
Tblk (v)		Blanking	12	41	6752	Th	
Fv		Frequency	30	120	145	Hz	***Note 3-3***
Th	Horizontal Section	Period	359	360	1023	Tclk	
Tdisp (h)		Active	320	320	320	Tclk	
Tblk (h)		Blanking	39	40	703	Tclk	
Fh		Frequency	69.7	177.7	250.6	KHz	***Note 3-4***
Tclk	LVDS Clock	Period	11.1	15.6	39.9	ns	1/Fclk
Fclk		Frequency	25	64	90	MHz	***Note 3-5***

Note 3-3: The optimal Vertical Frequency is 119~145 Hz for best picture quality

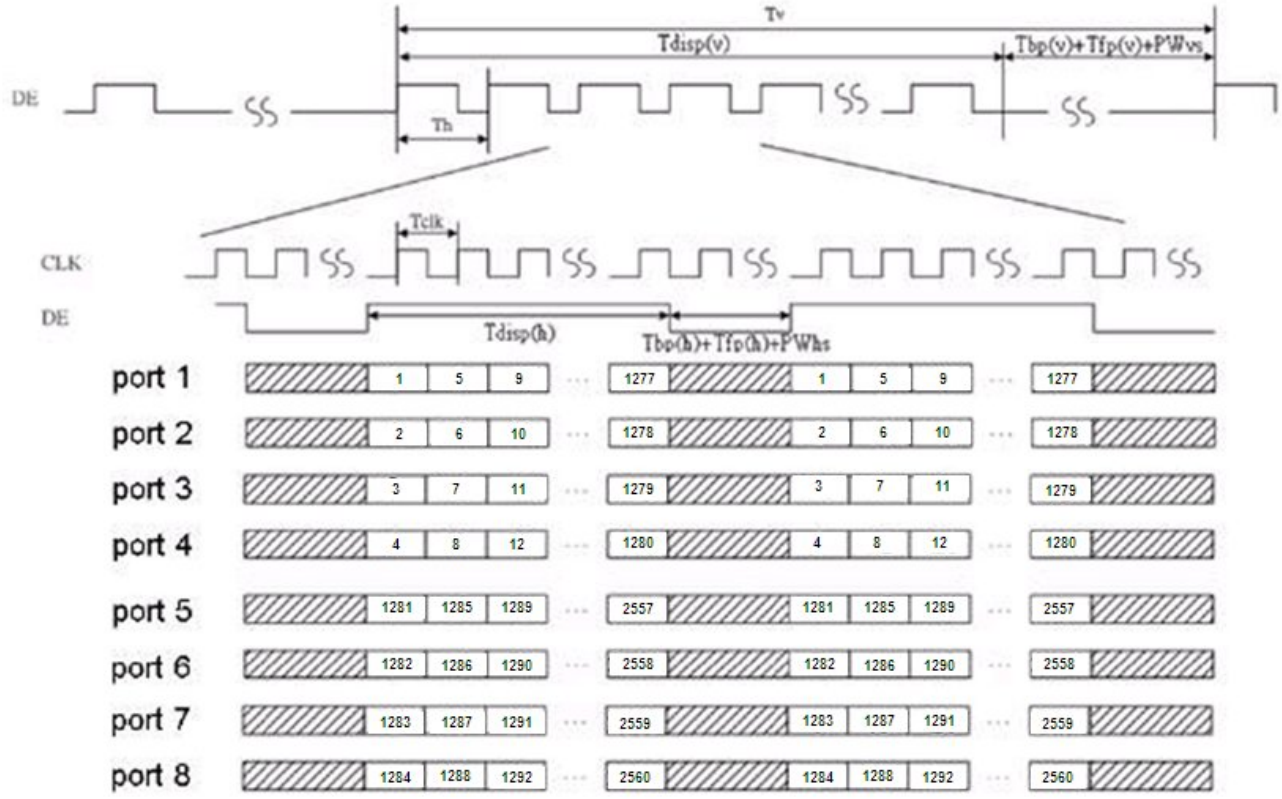
Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.);
Fh (Typ.) = Fclk (Typ.) / Th (Typ.);
Fh (Max.)= Fclk (Max.) / Th (Min.);

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.);
Fclk (Min.) < Fv x Th x Tv < Fclk (Max.)

3.4.6 Input Timing Diagram



3.4.7 3D Control

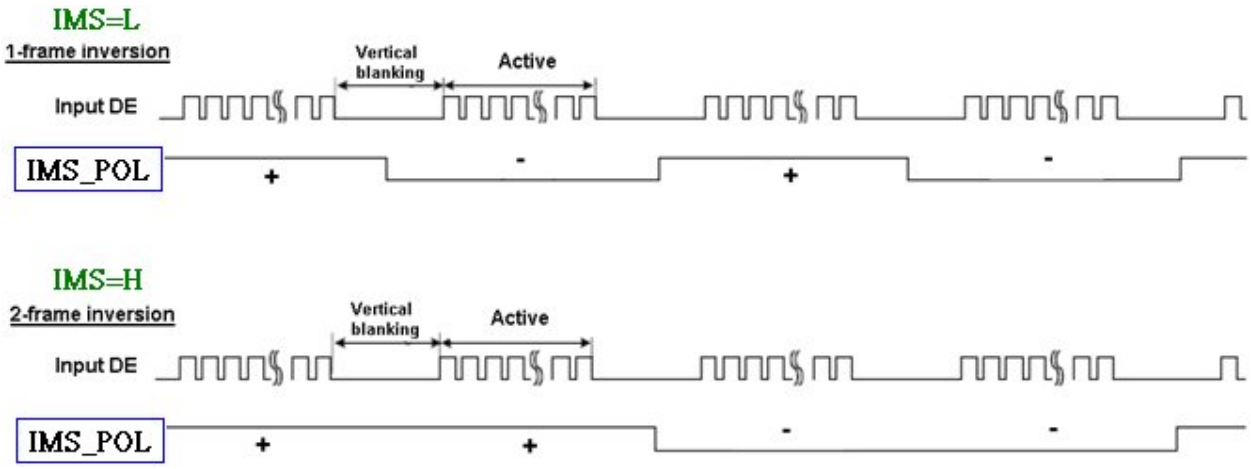
.

3.4.7.1. 3D control I/O Characteristics

Pin #	Symbol	I/O	Buffer	Description	Remark
CN2_pin 30	IMS_POL	O	4mA	Frame Inversion polarity Index IMS=L :1-frame inversion IMS=H :2-frame inversion	***Note 3-6***
CN3_pin 30	IMS	I	IPL*	3D enable control signal	

* IPL : internal pull low

Note 3-6



3.4.7.2. Absolute Maximum Rating

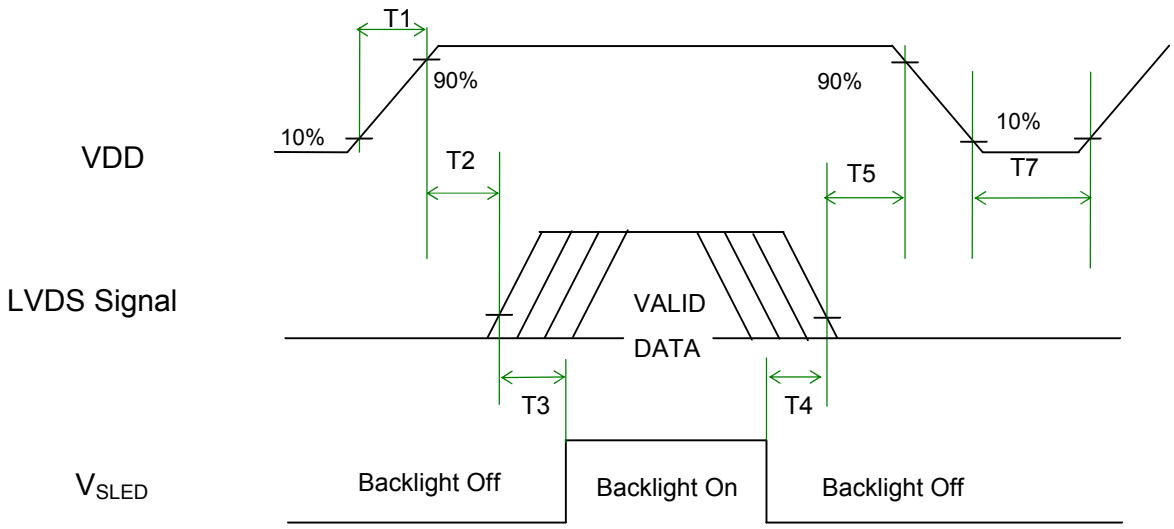
Symbol	Description	Min	Max	Unit	Remark
IMS	3D enable control signal	GND-0.3	5.0	[Volt]	Ta=25□

3.4.7.3. Recommended Operating Condition

Symbol	Parameter	Condition	Rating			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage	-	2.0	-	3.6	V
V_{IL}	Input Low Voltage	-	0	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = 4mA	2.4	-	3.4	V
V_{OL}	Output Low Voltage	I_{OL} = -4mA	0	-	0.4	V

3.5 Power ON/OFF Sequence

VDD power,LVDS signal and backlight on/off sequence are as following. LVDS signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	50	[ms]	
T3	500	-	-	[ms]	
T4	100	-	-	[ms]	
T5	0		50	[ms]	***Note 3-7*** ***Note 3-8***
T7	1000	-	-	[ms]	

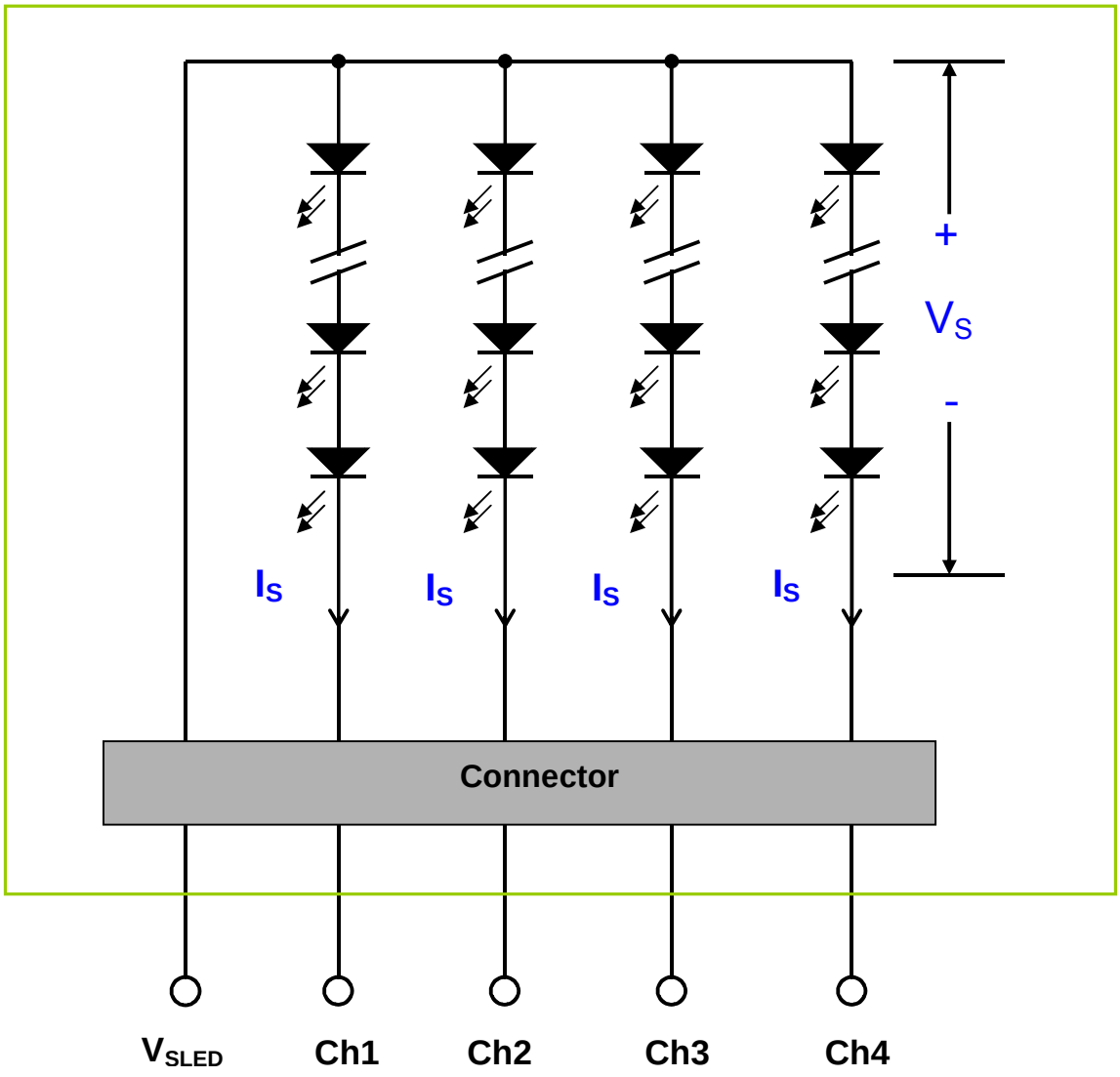
Note 3-7 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note 3-8 : During T5 period , please keep the level of input LVDS signals with Hi-Z state.

4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 23.8 inch Backlight Unit. And it includes 64pcs LED in the LED light bar. (4 strings and 16 pcs LED of one string).



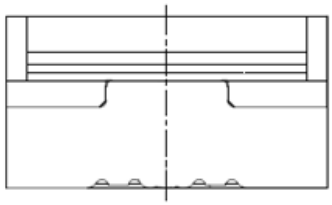
4.2 Interface Connection

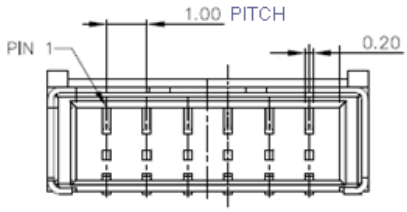
4.2.1 Connector Type

Backlight Connector	Manufacturer	CviLux
	Part Number	CI1406M1VLD-NH
Mating Connector	Manufacturer	CviLux
	Part Number	CI1406SL000-NH(Lock)

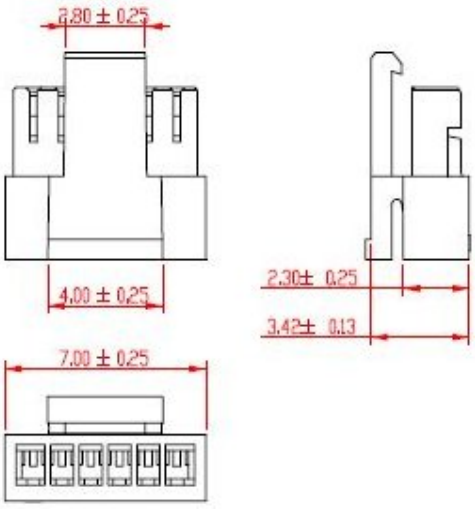
Backlight Connector dimension:

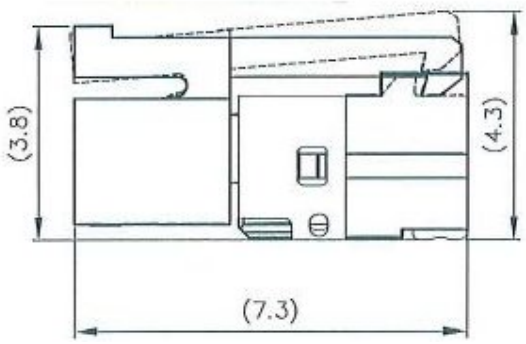
$H \times V \times D = 13.9 \times 3.00 \times 4.25, Pitch = 1.0(unit = mm)$





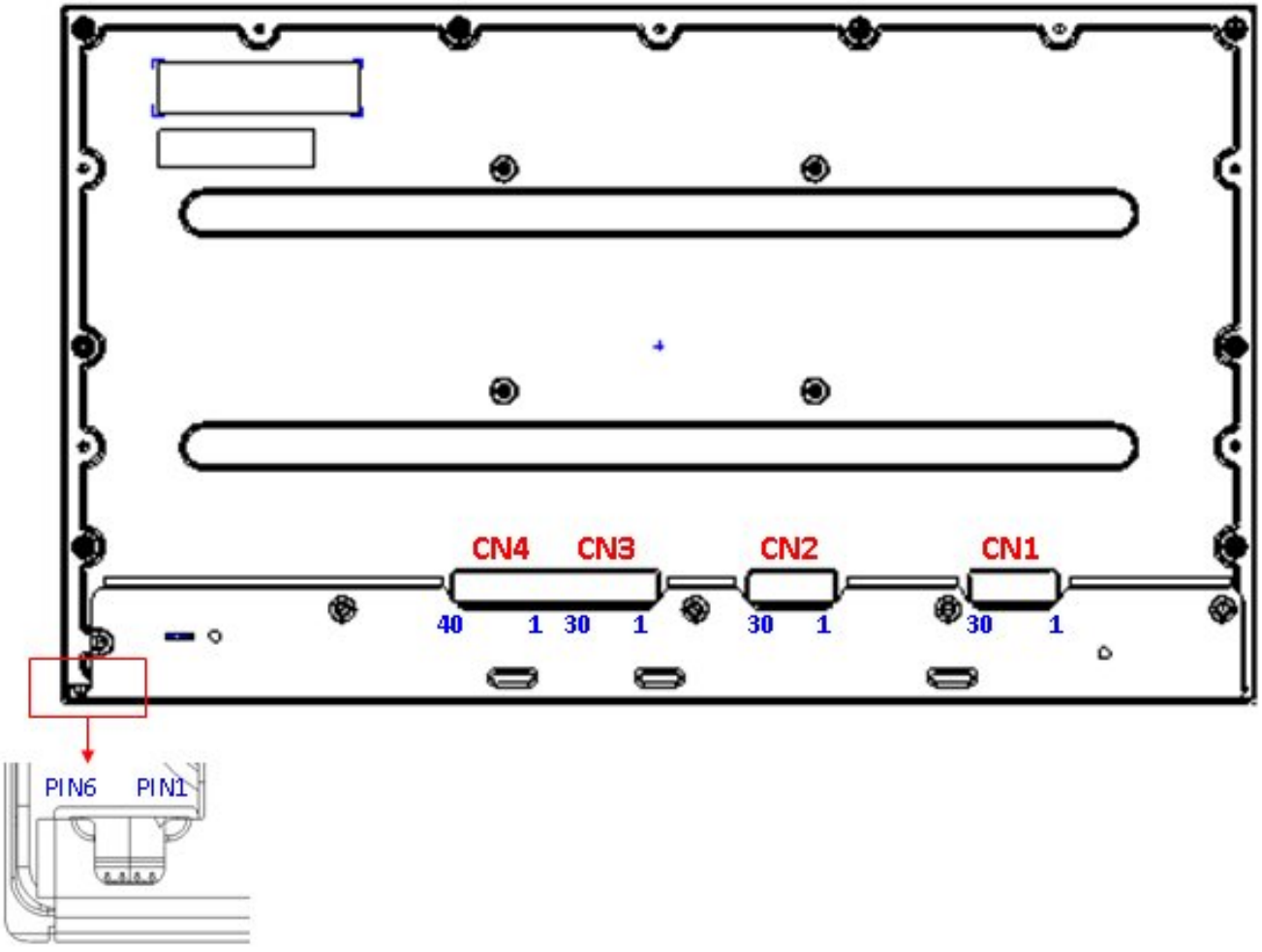
Mating Connector dimension:





4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	



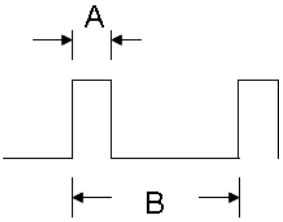
4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25□)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	150	[mA]	100% duty ratio
			210	[mA]	*Duty ratio□ 10%* *Pulse time=10 ms*



Duty ratio= (A / B) X 100% ; (A: Pulse time, B: Period)

4.3.2 Recommended Operating Condition

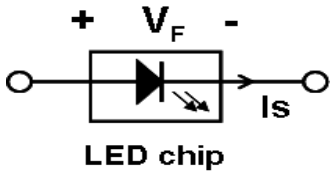
(Ta=25°C)

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
Is	LED String Current	-	80	88	[mA]	100% duty ratio of LED chip
Vs	LED String Voltage	46.4	49.6	52.8	[Volt]	Is=80mA @ 100% duty ratio; ***Note 4-1, Note 4-5***
ΔVs	Maximum Vs Voltage Deviation of light bar	-	-	3	[Volt]	Is=80mA @ 100% duty ratio; ***Note 4-2***
P_{BLU}	LED Light Bar Power Consumption	-	15.9	16.9	[Watt]	***Note 4-3***
LT_{LED}	LED Life Time	30,000	-	-	[Hour]	***Note 4-4***
OVP	Over Voltage Protection in system board	110% Vs max	-	-	[Volt]	***Note 4-5***

Note 4-1: Vs (Typ.) = V_F (Typ.) X LED No. (one string);

a. V_F: LED chip forward voltage, V_F (Min.)= 2.9V, V_F(Typ.)=3.1V, V_F(Max.)=3.3V

b. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F(Max.);



Note 4-2: ΔVs (Max.) = ΔV_F X LED No. (one string);

a. ΔV_F: LED chip forward voltage deviation; (0.2 V , each Bin of LED V_F)

Note 4-3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 4 ; (4 is total String No. of LED Light bar)

P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 4 ;

Note 4-4: Definition of life time:

a. Brightness of LED becomes to 50% of its original value

b. Test condition: Is = 80mA and 25□ (Room Temperature)

Note 4-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

Note 4-6: AUO strongly recommend “Analog Dimming” method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency.

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

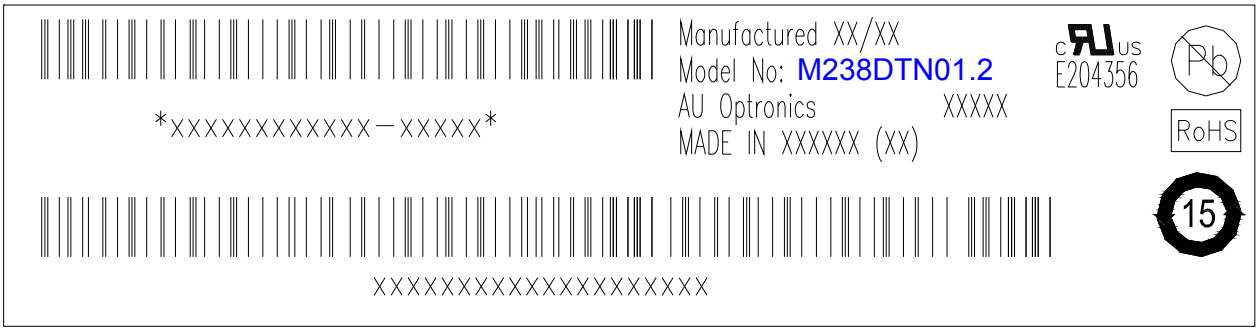
Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50□, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50□, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0□, 300hours	
High Temperature Storage (HTS)	Ta= 60□, 300hours	
Low Temperature Storage (LTS)	Ta= -20□, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20□/30min, 60□/30min, 100 cycles	***Note 5-1***
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	***Note 5-2***
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20□ to 60□, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed
No data lost
Self-recoverable
No hardware failures.

6 Shipping Label

The label is on the panel as shown below:



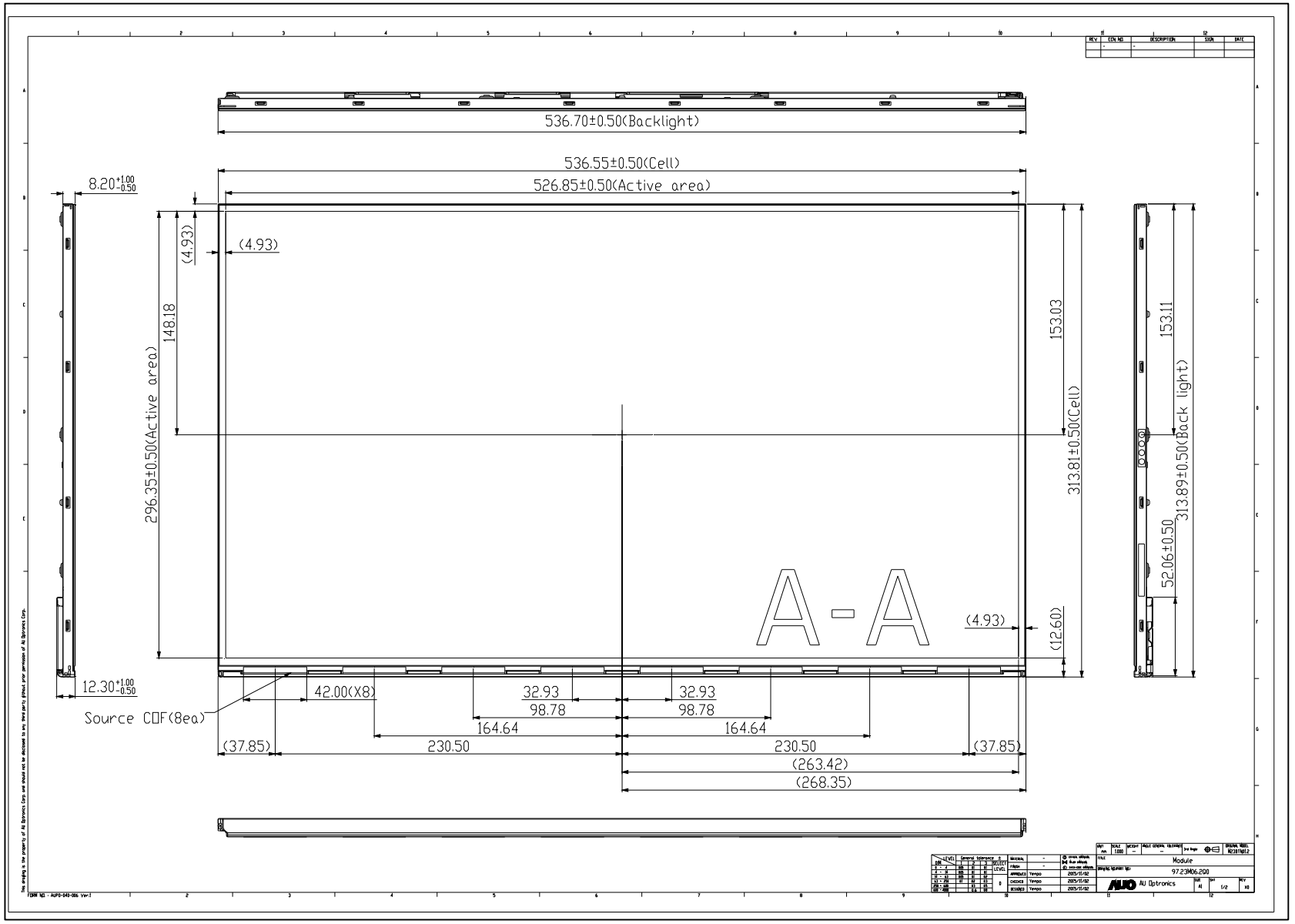
Note 6-1: For Pb Free products, AUO will add for identification.

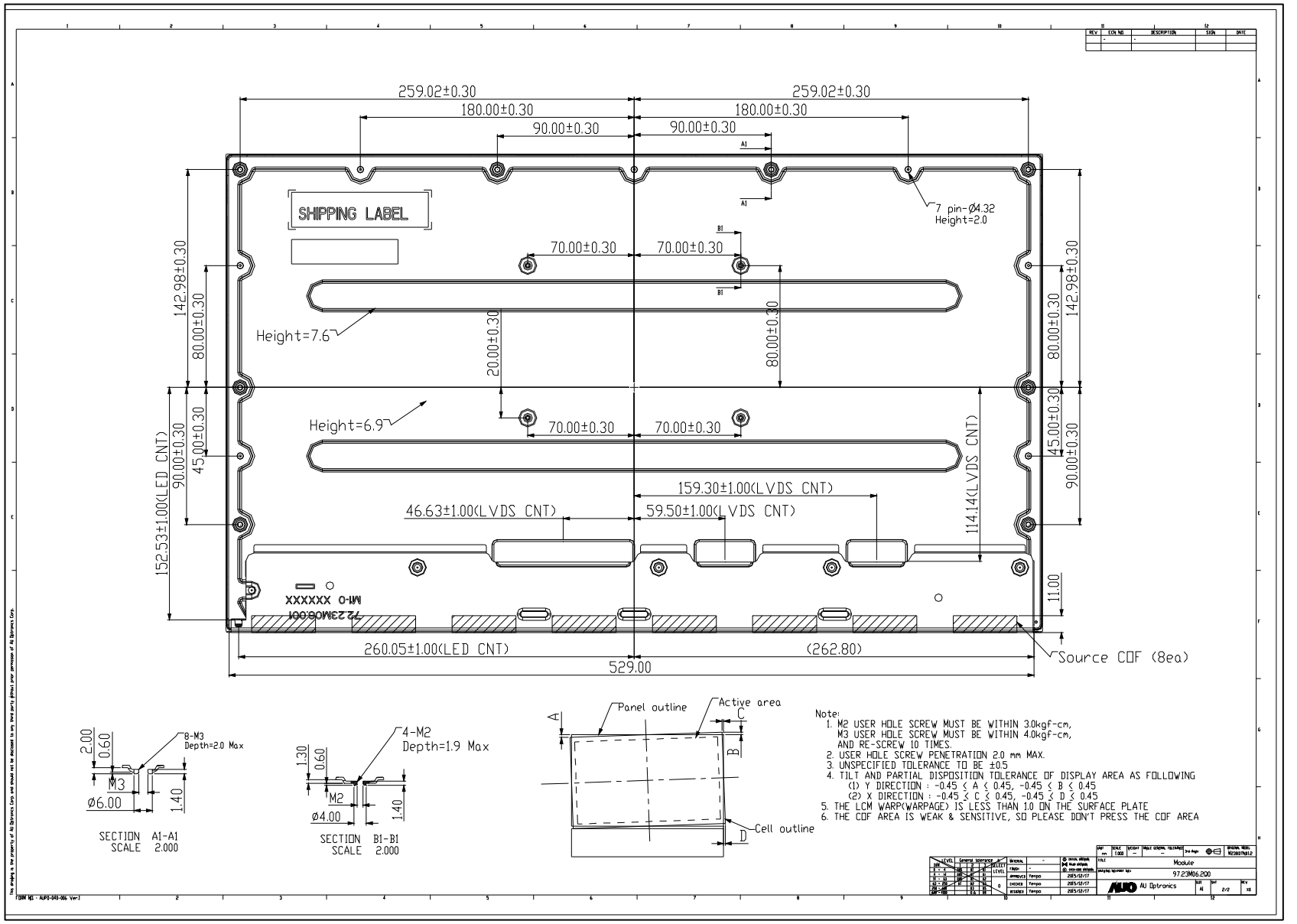
Note 6-2: For RoHS compatible products, AUO will add for identification.

Note 6-3: For China RoHS compatible products, AUO will add for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

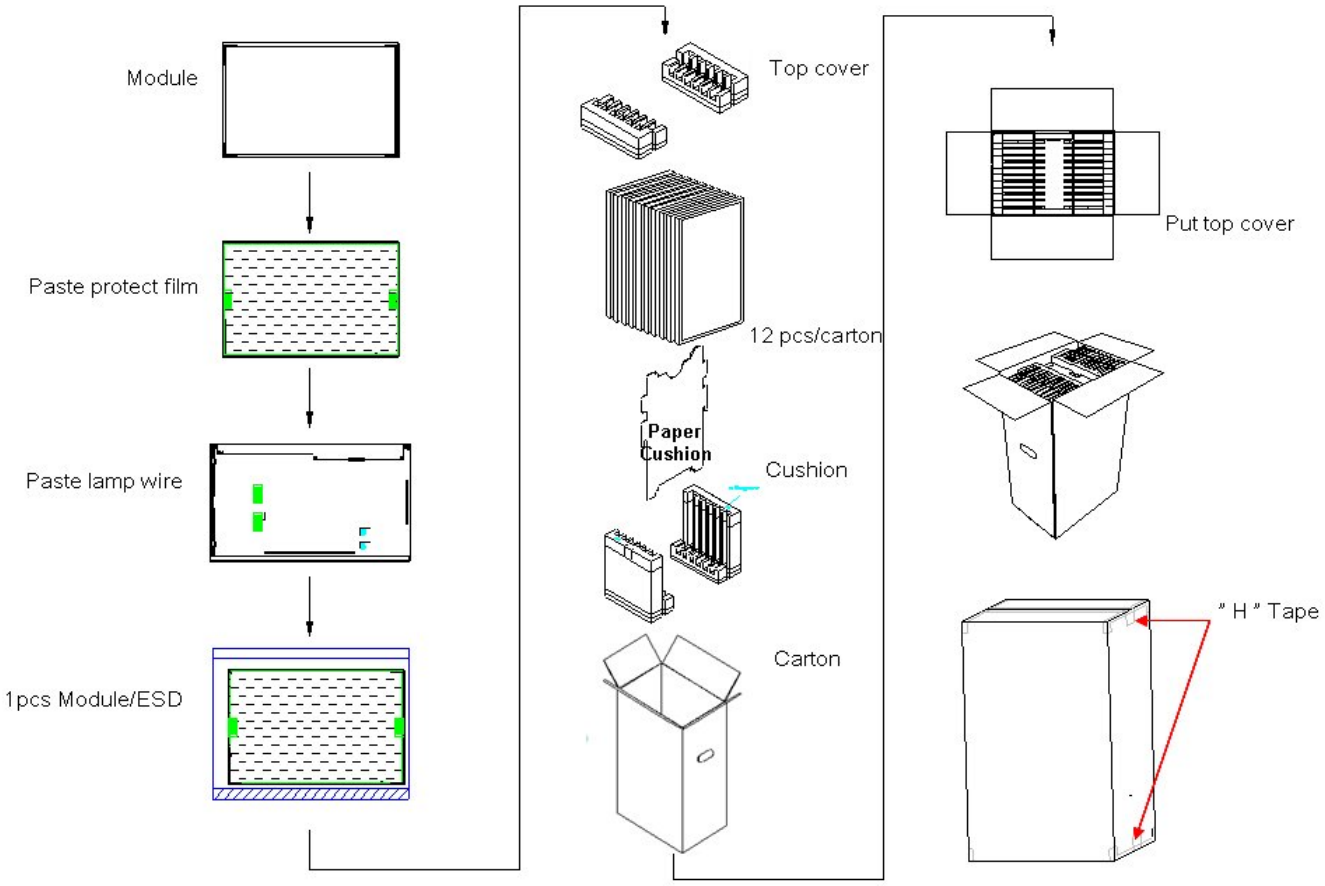
7 Mechanical Characteristics

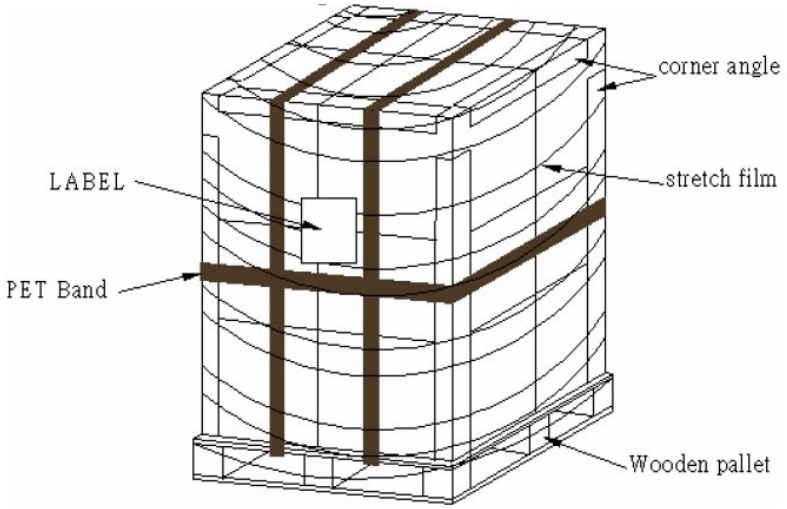



259.02±0.30
180.00±0.30
90.00±0.30
SHIPPING LABEL
7 pin-Ø4.32
Height=2.0
70.00±0.30
142.98±0.30
80.00±0.30
Height=7.6
20.00±0.30
Height=6.9
45.00±0.30
90.00±0.30
152.53±1.00(LED CNT)
159.30±1.00(LVDS CNT)
46.63±1.00(LVDS CNT)
59.50±1.00(LVDS CNT)
114.14(LVDS CNT)
11.00
260.05±1.00(LED CNT)
(262.80)
529.00
Source COF (8ea)
8-M3
Depth=2.0 Max
4-M2
Depth=1.9 Max
SECTION A1-A1
SCALE 2.000
SECTION B1-B1
SCALE 2.000
Panel outline
Active area
Cell outline
Note:
1. M2 USER HOLE SCREW MUST BE WITHIN 3.0kgf-cm,
M3 USER HOLE SCREW MUST BE WITHIN 4.0kgf-cm,
AND RE-SCREW 10 TIMES.
2. USER HOLE SCREW PENETRATION 2.0 mm MAX.
3. UNSPECIFIED TOLERANCE TO BE ±0.5
4. TILT AND PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA AS FOLLOWING
(1) Y DIRECTION : -0.45 ≤ A ≤ 0.45, -0.45 ≤ B ≤ 0.45
(2) X DIRECTION : -0.45 ≤ C ≤ 0.45, -0.45 ≤ D ≤ 0.45
5. THE LCM WARP(WARPAGE) IS LESS THAN 1.0 ON THE SURFACE PLATE
6. THE COF AREA IS WEAK & SENSITIVE, SO PLEASE DON'T PRESS THE COF AREA
Module
97.23M06.200
AU Optronics

8 Packing Specification

8.1 Packing Flow





8.2 Pallet and shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight (kg)	
Panel	1	536.7(H) x 313.89(V) x 12.3 (D)	2.32(TBD)	
Cushion	1	-	0.435	
Box	1	395(L)mm x 284(W)mm x652(H)mm	1.56	without Panel & cushion
Packing Box	12 pcs/Box	395(L)mm x 284(W)mm x652(H)mm	29.8(TBD)	with panel & cushion
Pallet	1	1150(L)mm x840(W)mm x 132(H)mm	12	
Pallet after Packing	16 boxes/pallet	1150(L)mm x 840(W)mm x1436(H)mm	488.8(TBD)	