( ) Preliminary Specification
(V) Final Specification

Module	27” Color TFT-LCD
Model Name	M270DAN02.6
Suffix Name	Q0
Document version	D05

Document		
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CUSTOMER APPROVED AND FEEDBACK		
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APPROVED BY		Date :

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Document Version	Date (Y/M/D)	Page	Description
D01	2015/05/26		First Version
D02	2015/07/17	6	Modify Viewing Angle Spec.
D03	2015/07/27	5	Panel Weight
D04	2015/09/01	6	Optical Characteristics
		5	Power Consumption(LED line)
		14	Backlight Unit
D05	2015/10/05	31	Add Reliability Test

1. Handling Precautions

1. Since front polarizer is easily damaged, pay attention not to scratch it.
2. Be sure to turn off power supply when inserting or disconnecting from input connector.
3. Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4. When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5. Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6. Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7. Do not open or modify the Module Assembly.
8. Do not press the reflector sheet at the back of the module to any directions.
9. In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be da
10. At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11. After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12. Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13. Please avoid touching COF Position while you are doing mechanical design.
14. When storing modules as spares for a long time, the following precaution is necessary:
    a. Store them in a dark place. Do not expose the module to sunlight or fluorescent light.
    b. Keep the temperature between 5℃ and 35℃ at normal humidity.

2. General Description

This specification applies to the 27 inch wide Color a-Si TFT-LCD Module M270DAN02.6. The display supports the QHD - 2560(H) x 1440(V) screen format and 1.07B colors (8bits RGB data input). The input interface is 8 channel LVDS.

Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	mm	684.7(27.0")
Active Area	mm	596.74 (H) x 335.66 (V)
Pixels H x V		2560(x3) x 1440
Pixel Pitch	um	233.1 (per one triad) ×233.1
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally Black
White Luminance (Center)	cd/m^2	350 cd/m^2 (Typ.)
Contrast Ratio		1000 (Typ.)
Optical Response Time	msec	12ms (Typ., Gray to Gray)
Power Consumption (VDD line + LED line)	Watt	Total=32.2W (Typ.) LCD module: PDD(Typ.)=5.3W @ white pattern, Fv=144Hz Backlight unit: P_{BLU}(Typ.)=26.9 W @ I_{RLED}=95 mA
Color Gamut		sRGB
Weight	Grams	3400 (Typ.)
Outline Dimension	mm	606.44(H)x355.81(V)x13.03(D) Typ.
Electrical Interface		8 channel LVDS (8bits RGB data input)
Support Color		16.7M colors
Surface Treatment		Anti-Glare, 3H
Temperature Range Operating Storage (Shipping)	°C °C	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance
TCO Compliance		TCO 6.0 Compliance

Optical Characteristics

The optical characteristics are measured on the following test condition.

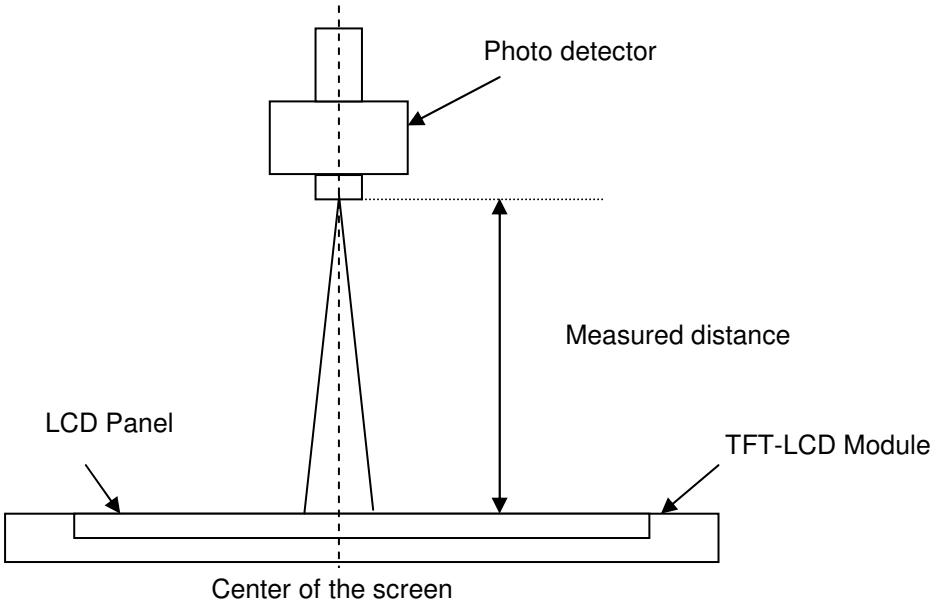
Test Condition：

1. Equiment setup: Please refer to Note 1
2. Panel Lighting: 30 minutes
3. VDD=5.0V, Fv=144Hz, Is=110 mA, Ta=25℃

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	degree	Horizontal (Right) CR = 10 (Left)	75 75	89 89	- -	*2*
		Vertical (Up) CR = 10 (Down)	75 75	89 89	- -	
Contrast ratio (Center of Screen)		Normal Direction	600	1000	-	*3*
Response Time	msec	Gray to Gray	-	12		*4*
Color / Chromaticity Coordinates (CIE)		Red x	0.638	0.668	0.698	*5*
		Red y	0.303	0.332	0.363	
		Green x	0.270	0.300	0.330	
		Green y	0.595	0.625	0.655	
		Blue x	0.113	0.143	0.173	
		Blue y	0.025	0.052	0.082	
Color Coordinates (CIE) White		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
Central Luminance	cd/m^2		280	350	-	*6*
Luminance Uniformity	%		75	80	-	*7*
Crosstalk	%				1.5	*8*
Flicker (Center od Screen)	dB				-20	*9*

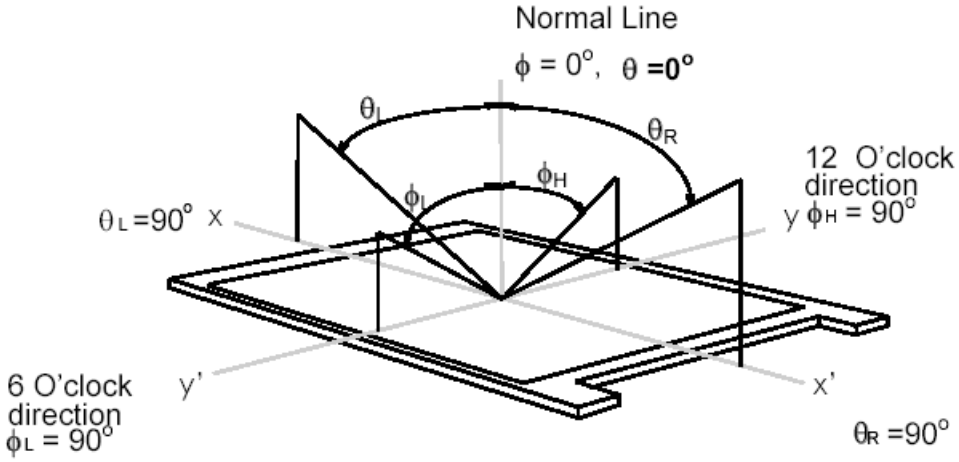
Note 1: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring (at surface 35℃). In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 2: Definition of viewing angle measured by ELDIM (EZContrast 88)

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 3: Contrast ratio is measured by TOPCON SR-3

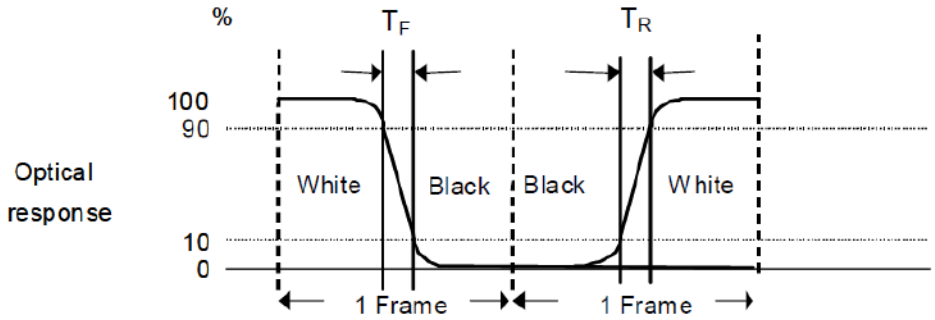
Definition:

$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

Measured position: Center of screen (P5) & perpendicular to the screen ($\theta = \phi = 0°$)

Note 4: Definition of Response time measured by Westar TRD-100A

The output signals of photo detector are measured when the input signals are changed from "Black" to "White" (rising time, T_R), and from "White" to "Black" (falling time, T_F), respectively. The response time is interval between the 10% and 90% of optical response.



The gray to gray response time is defined as the following table. The algorithm is $|\text{Gray Level A} - 8a\ \text{Gray level B}| \geqq 256$.

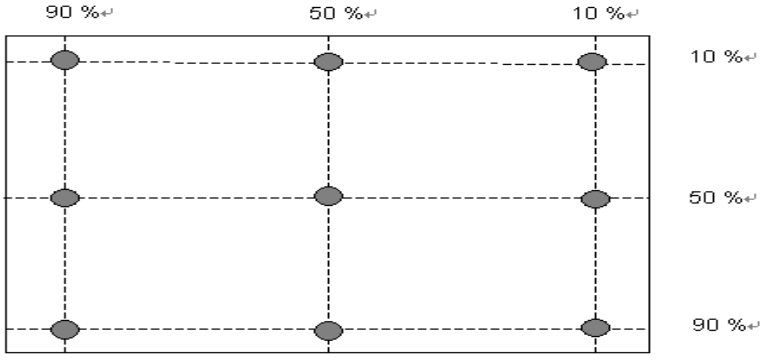
Gray Level to Gray Level		Falling Time				
		G0	G255	G511	G767	G1023
Rising Time	G0					
	G255					
	G511					
	G767					
	G1023					

- T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.
- T_{GTG_max} is the maximum time at rising time or falling time of gray to gray.

Note 5: Color chromaticity and coordinates (CIE) is measured by TOPCON SR-3

Note 6: Central luminance is measured by TOPCON SR-3

Note 7: Luminance uniformity of these 9 points is defined as below and measured by TOPCON SR-3



$$\text{Uniformity} = \frac{\text{Minimum Luminance in 9 points (1-9)}}{\text{Maximum Luminance in 9 Points (1-9)}}$$

Note 8: Crosstalk is defined as below and measured by TOPCON SR-3

Definition:

$CT = \text{Max.}\ (CT_H, CT_V)$;

Where

a.Maximum Horizontal Crosstalk :

$CT_H = \text{Max.}\ (|\ Y_{BL} - Y_{AL}\ |\ /\ Y_{AL} \times 100\ \%,\ |\ Y_{BR} - Y_{AR}\ |\ /\ Y_{AR} \times 100\ \%)$;

Maximum Vertical Crosstalk:

$CT_V = \text{Max.}\ (|\ Y_{BU} - Y_{AU}\ |\ /\ Y_{AU} \times 100\ \%,\ |\ Y_{BD} - Y_{AD}\ |\ /\ Y_{AD} \times 100\ \%)$;

b. Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR} = Luminance of measured location without Black pattern

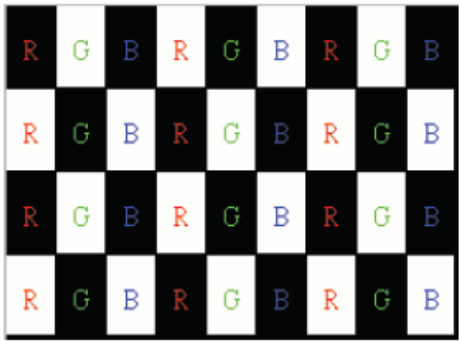
Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR} = Luminance of measured location with Black pattern

Black pattern

Note 9: Flicker is measured by TOPCON SR-3

Flicker measurement

a. Test pattern: It is listed as following.



Gray level = L0

Gray level = L127

R: Red, G: Green, B:Blue

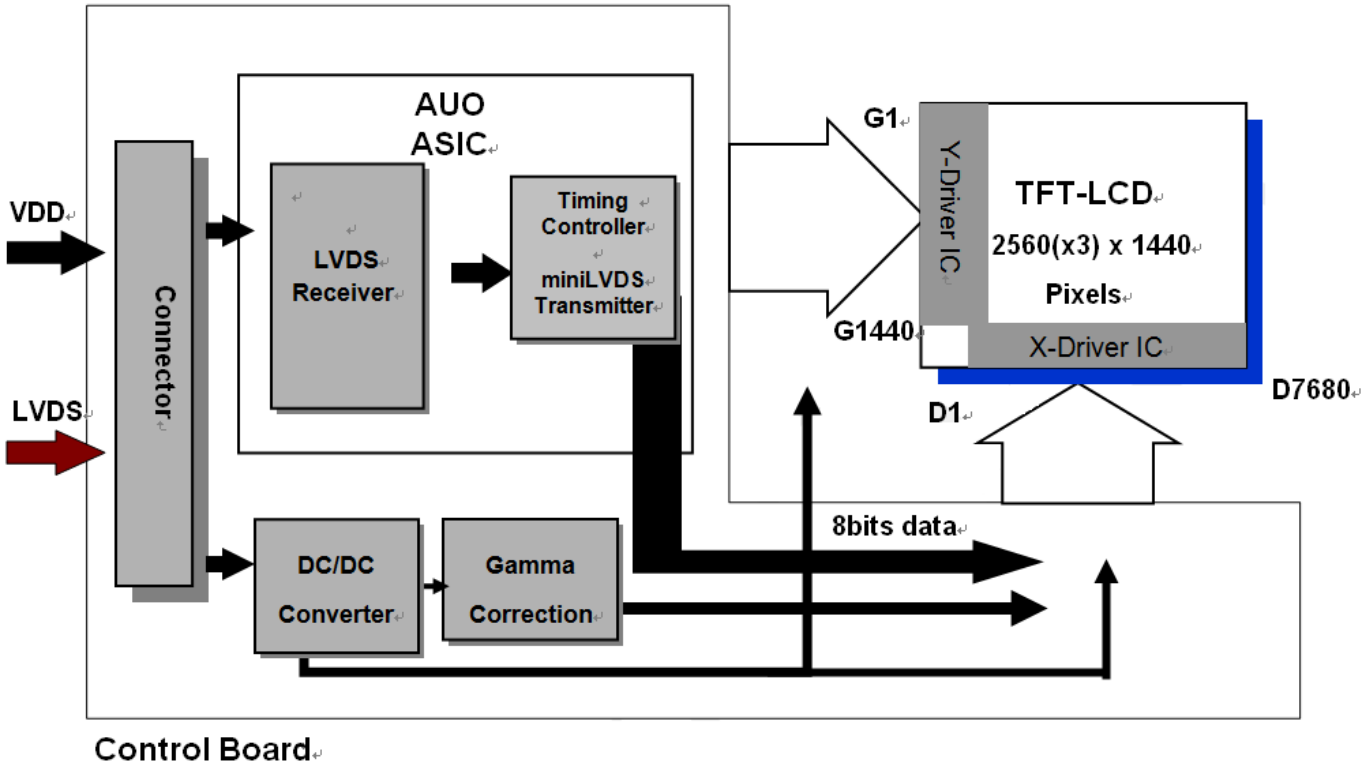
b. Measured position: Center of screen & perpendicular to the screen

b. Measure position: Center of screen (P5) & perpendicular to the screen ($\theta = \phi$ =0 deg)

3. Functional Block Diagram

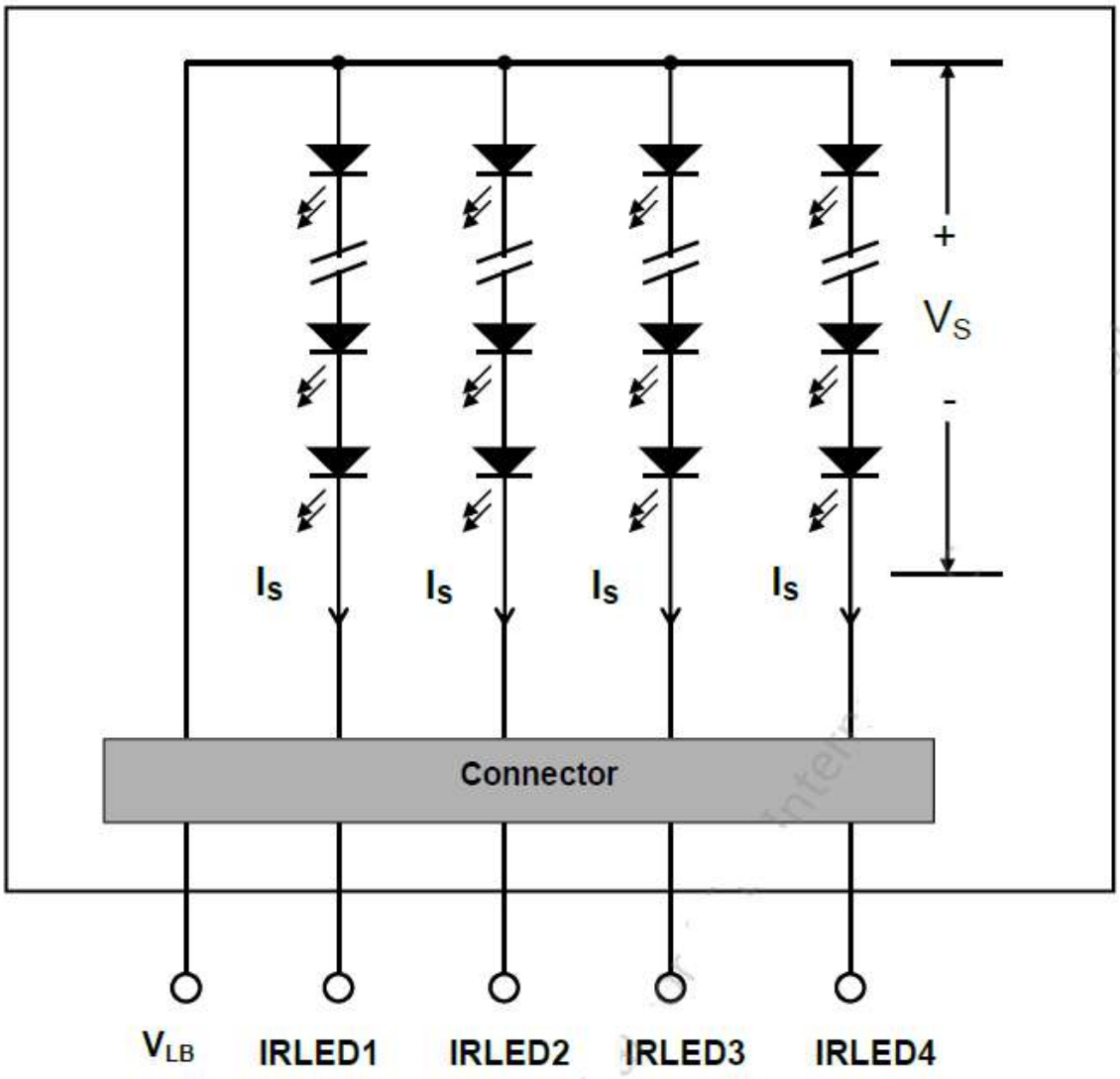
TFT LCD Module

The following shows the block diagram of the 27.0 inch Color TFT-LCD Module.



Backlight Unit

The following shows the block diagram of 27 inch Backlight Unit. And it includes 68 ea LEDs in the LED light bar . (4 strings and 17 pcs LED of one string).



4. Absolute Maximum Ratings

Permanent damage may occur if exceeding the following maximum rating:

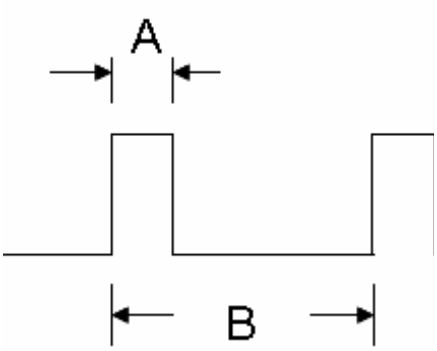
TFT-LCD Module

Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25℃

Backlight Unit

(Ta=25℃)

Symbol	Description	Min.	Max.	Unit	Remark
Is	LED String Current	0	150	[mA]	*100% duty ratio*
			300	[mA]	*Duty ratio 10%* *Pulse time=10ms*



Duty ratio= (A / B) X 100% ; (A: Pulse time, B: Period)

5. Electrical characteristics-TFT LCD Module

Input power specifications are as following:

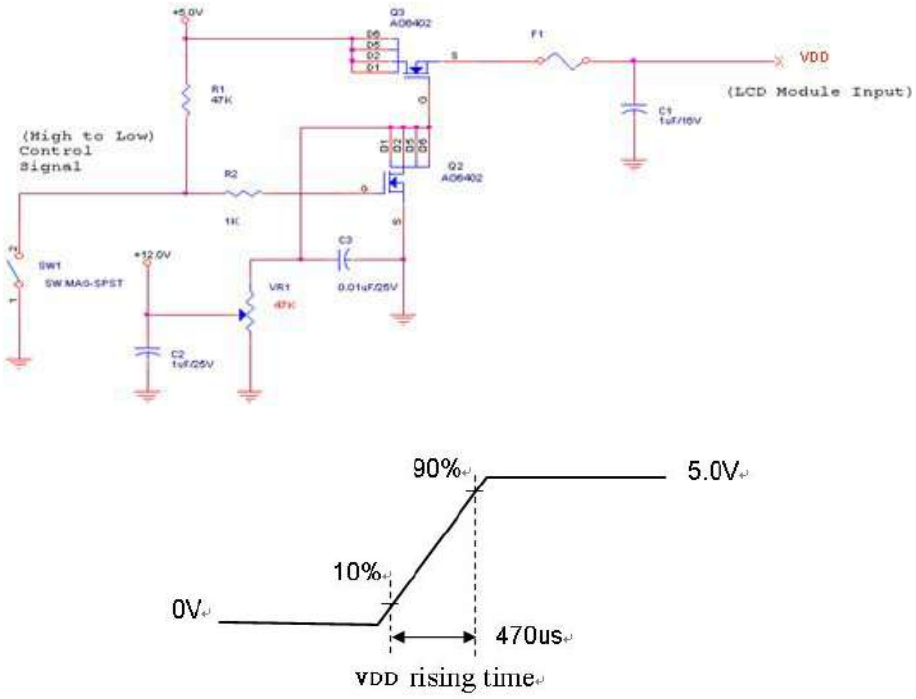
Recommended Operating Condition

TFT-LCD Module

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power Supply Input Voltage	10.8	12.0	13.2	[Volt]	
IDD	Power Supply Input Current (RMS)	-	0.44	0.94	[A]	VDD= 12.0V, All Black Pattern At 144Hz,
PDD	VDD Power Consumption	-	5.3	11.28	[Watt]	VDD= 12.0V, All Black Pattern At 144Hz
IRush	Inrush Current	-	-	3.0	[A]	*Note 1*
VDDrp	Allowable VDD Ripple Voltage	-	-	VDD*10%	[mV]	VDD= 12.0V, All Black Pattern At 144Hz

Note 1: Inrush Current measurement:

Test circuit:



The duration of VDD rising time: 470us.

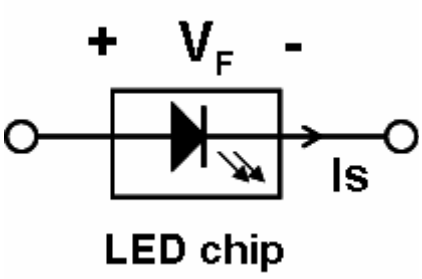
Backlight Unit

Symbol	Description	Min	Typ.	Max	Unit	Remark
Is	LED String Current	-	95	105	[mA]	100% duty ratio of LED chip
Vs	LED String Voltage	47.6	56.1	61.2	[Volt]	Is=95mA @ 100% duty ratio; ***Note 1, Note 5***
ΔVs	Maximum Vs Voltage Deviation of light bar	-	-	3.6	[Volt]	Is=95mA @ 100% duty ratio; ***Note 2***
P_{BLU}	LED Light Bar Power Consumption	-	21.4	25.1	[Watt]	***Note 3***
LT_{LED}	LED Life Time	30,000	-	-	[Hour]	***Note 4***
OVP	Over Voltage Protection insystem board	110% Vs_{max}	-	-	[Volt]	***Note 5***

Note 1: Vs (Typ.) = VF (Typ.) X LED No. (one string);

a. V_F: LED chip forward voltage, V_F (Min.)=2.8V, V_F(Typ.)=3.3V, V (Max.)=3.6V

b. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F(Max.);



Note 2: ΔVs (Max.) = ΔVF X LED No. (one string);

a. ΔVF: LED chip forward voltage deviation; (0.2 V , each Bin of LED VF)

Note 3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 4 ; (4 is total String No. of LED Light bar)

P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 4 ;

Note 4: Definition of life time:

a. Brightness of LED becomes to 50% of its original value

b. Test condition: Is = 120mA and 25℃ (Room Temperature)

Note 5: Recommendation for LED driver power design:

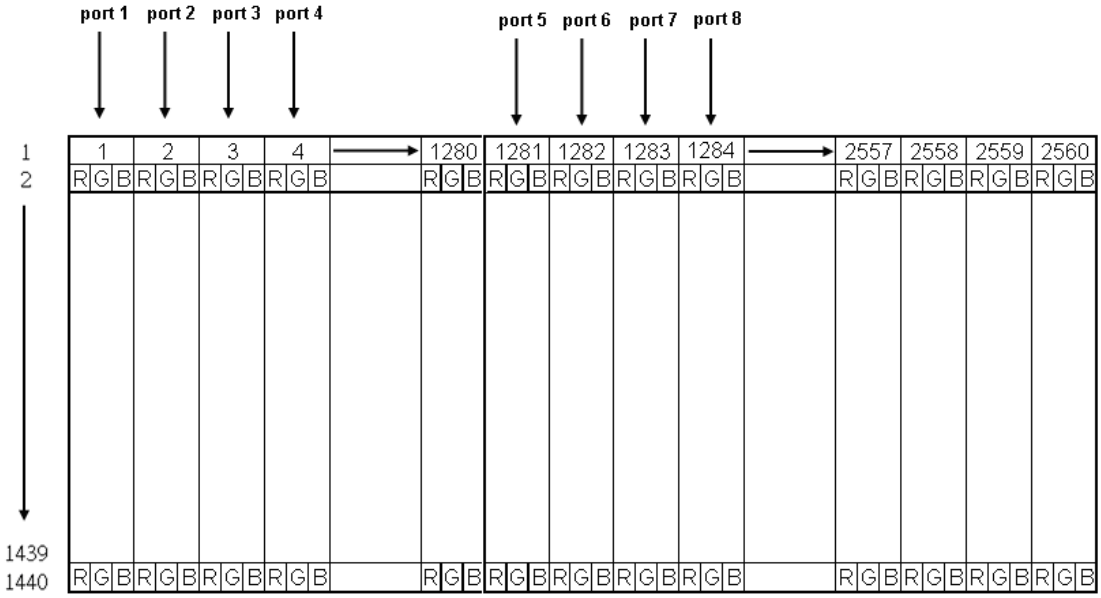
Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

Note 6: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency.

6. Signal Characteristic

LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.



Note 1: The module use 8port-LVDS interface.

Port 1：4N+1 N=0,~ 319 (1,5.. 1277pixel)

Port 2：4N+2 N=0,~ 319 (2,6.. 1278pixel)

Port 3：4N+3 N=0,~ 319 (3,7.. 1279pixel)

Port 4：4N+4 N=0,~ 319 (4,8.. 1280pixel)

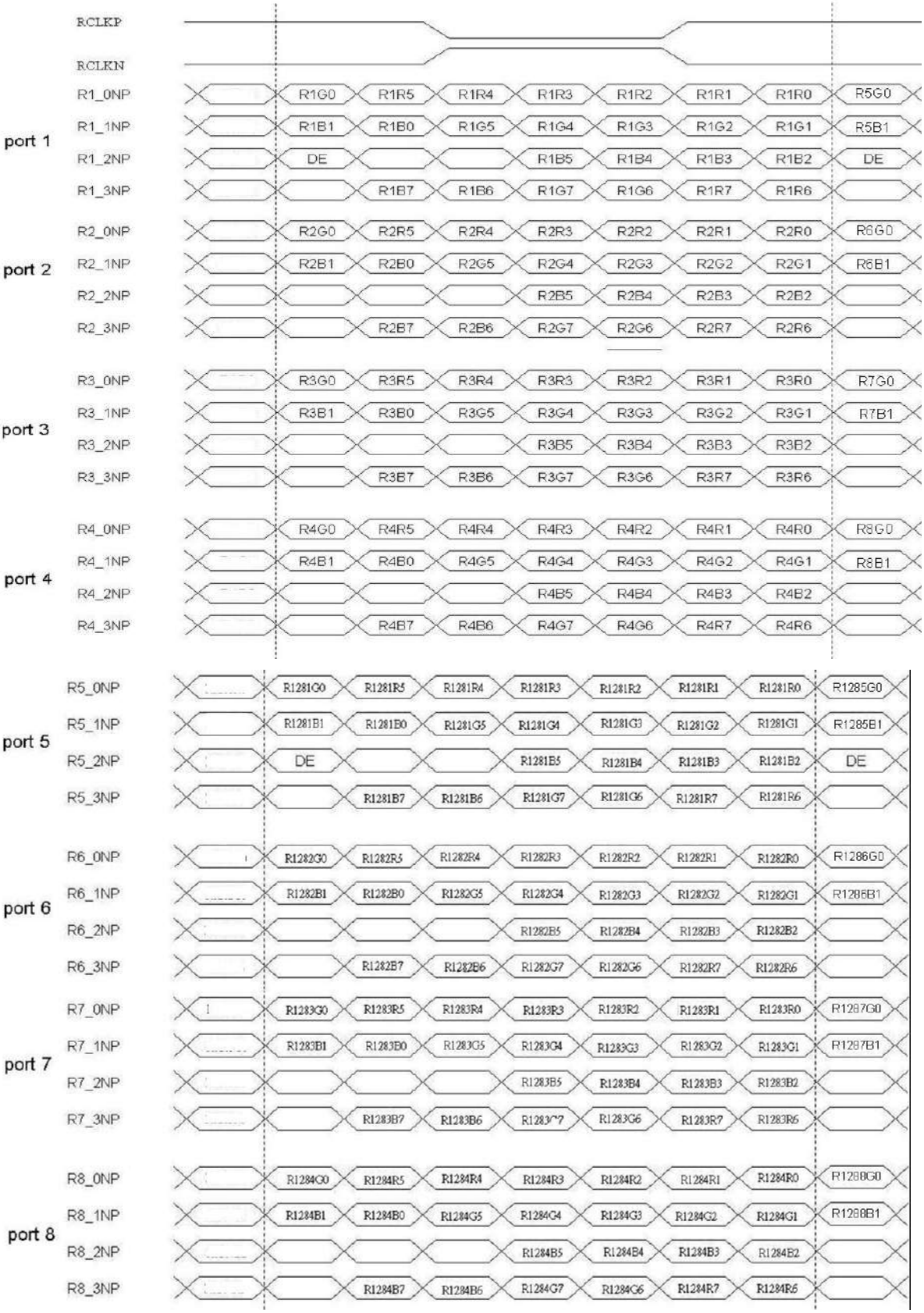
Port 5：4N+1281 N=0,~ 319 (1281,1285.. 2557pixel)

Port 6：4N+1282 N=0,~ 319 (1282,1286.. 2558pixel)

Port 7：4N+1283 N=0,~ 319 (1283,1287.. 2559pixel)

Port 8：4N+1284 N=0,~ 319 (1284,1288.. 2560pixel)

LVDS Data Format



Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

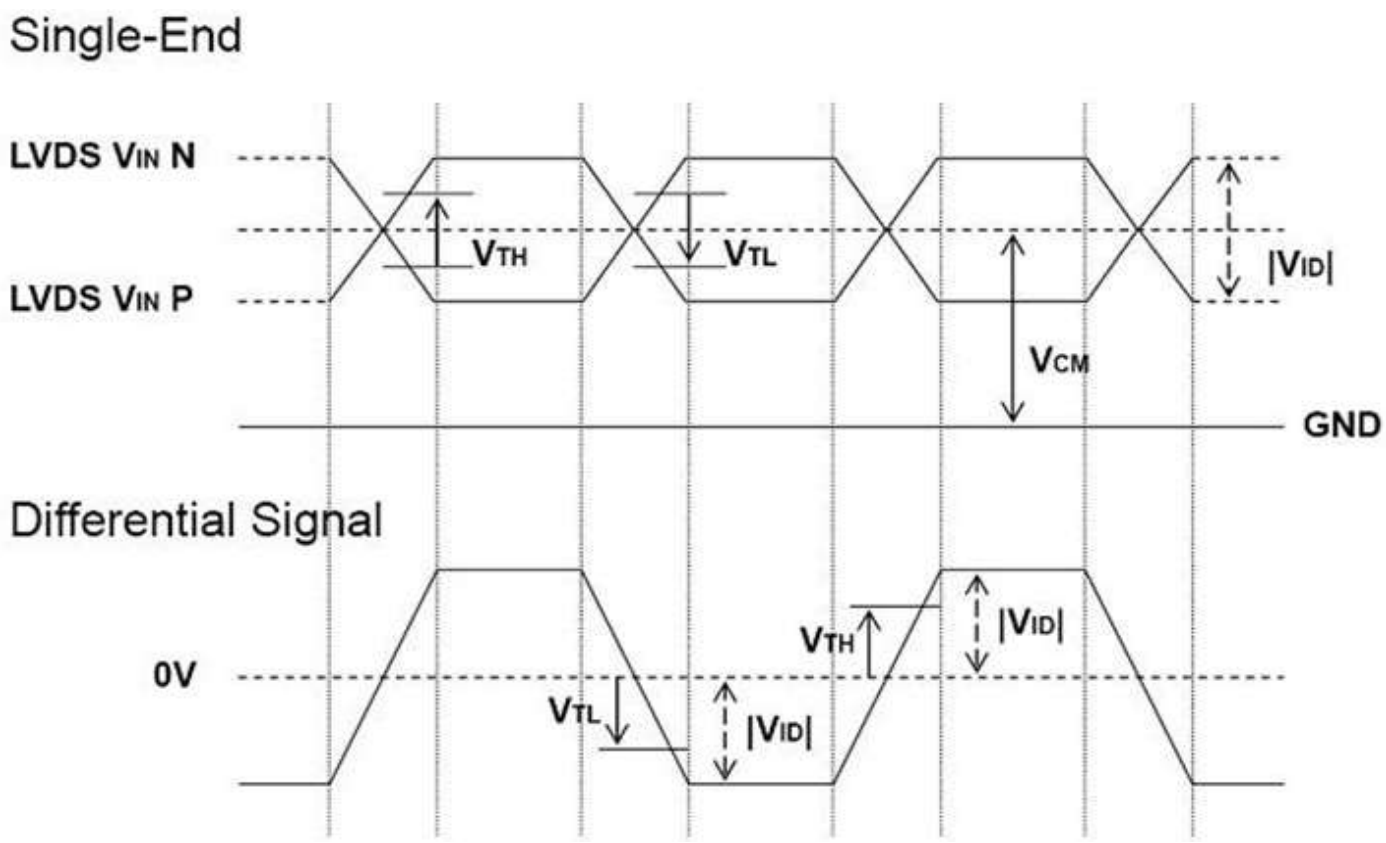
Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

LVDS Specification

a. DC Characteristics:

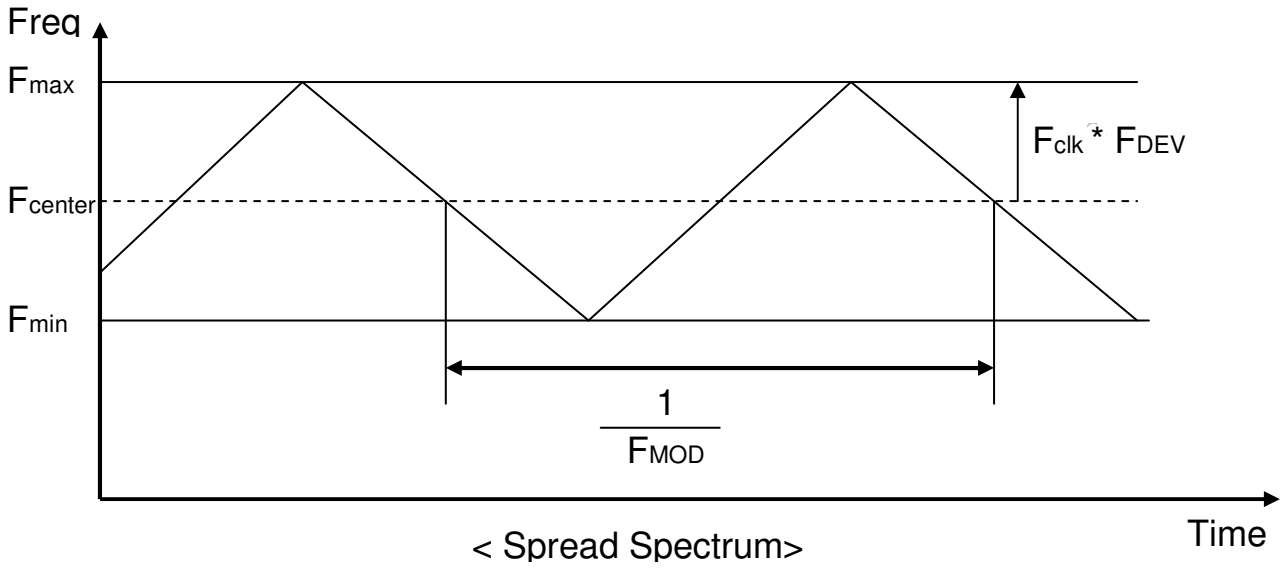
Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{TH}	LVDS Differential Input High Threshold	-	-	+100	[mV]	V_{CM} = 1.2V
V_{TL}	LVDS Differential Input Low Threshold	-100	-	-	[mV]	V_{CM} = 1.2V
$\lvert V_{ID} \rvert$	LVDS Differential Input Low Threshold	100	-	600	[mV]	
V_{CM}	LVDS Common Mode Voltage	+1.0	+1.2	+1.5	[V]	V_{TH}-V_{TL} = 200mV

LVDS Signal Waveform:



b. AC Characteristics

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation ofinput clock frequencyduring Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulationfrequency of input clockduring Spread Spectrum	-	200	KHz	



< Spread Spectrum>

Fclk: LVDS Clock Frequenc

Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min	Typ	Max	Unit	Remark
Tv	Vertical Section	Period	1452	1481	8192	Th	
Tdisp(v)		Active	1440	1440	1440	Th	
Tblk(v)		Blanking	12	41	6752	Th	
Fv		Frequency	119	120	144	Hz	
Th	Horizontal Section	Period	345	360	1023	Tclk	
Tdisp(h)		Active	320	320	320	Tclk	
Tblk(h)		Blanking	25	40	703	Tclk	
Fh		Frequency	173	177.8	254.2	KHz	***Note 1***
Tclk	LVDS Clock	Period	11.5	15.6	16.7	ns	1/Fclk
Fclk		Frequency	59.6	64	87.7	MHz	***Note 2***

Note 1: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th ((Min.);

Fh (Typ.)= Fclk (Typ.) / Th (Typ.);

Fh (Max.)= Fclk (Max.) / Th (Min.);

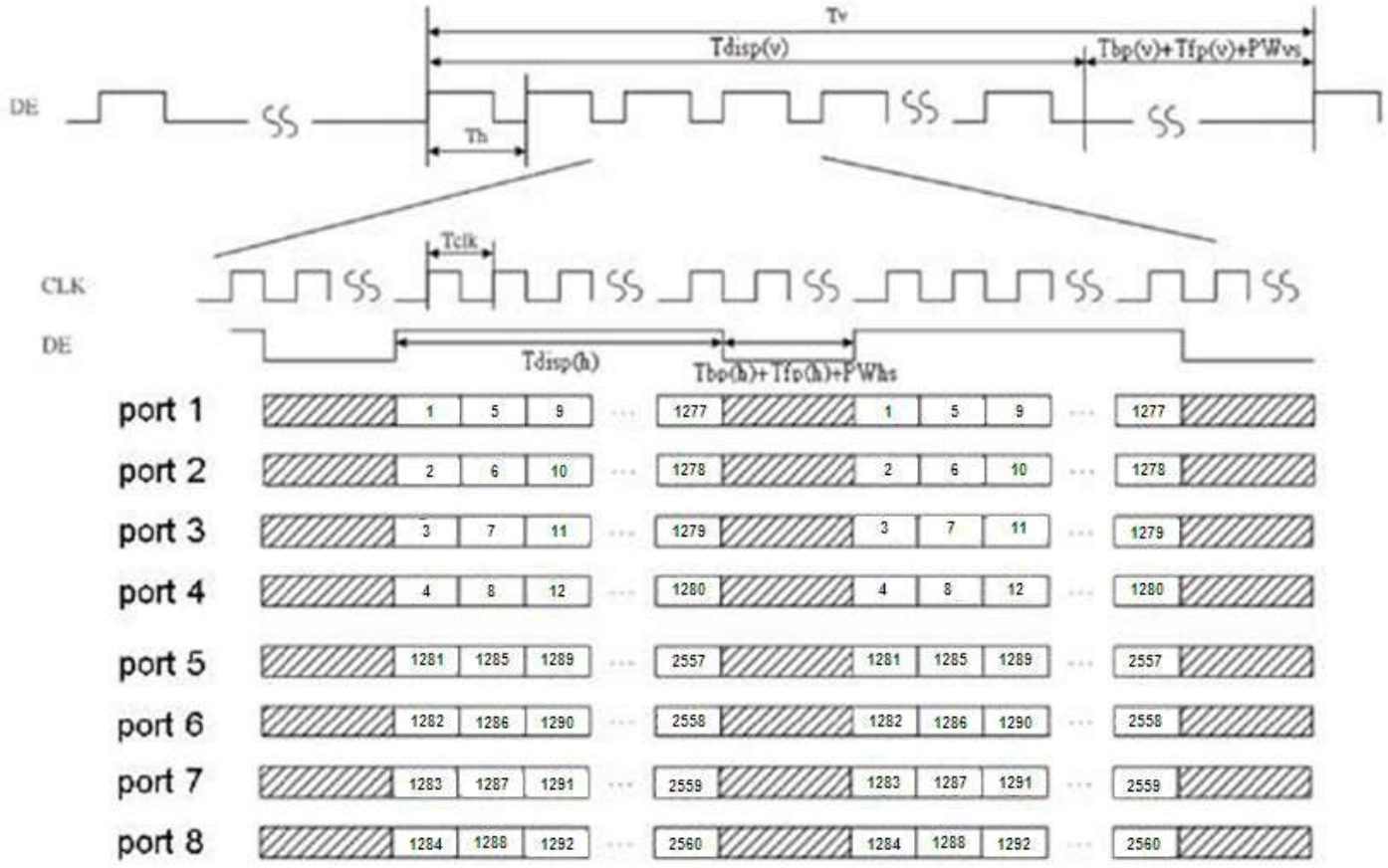
Note 2: The equation is listed as following. Please don't exceed the above recommended value.

Fclk (Min.) = Fv (Min.) x Th ((Min.) x Tv (Min.);

Fclk (Typ.) = Fv (Typ.) x Th ((Typ.) x Tv (Typ.);

Fv x Th x Tv < Fclk (Max.)

Input Timing Diagram



3D Control

3D control I/O Characteristics

Pin#	Symbol	I/O	Buffer	Description	Remark
CN2_pin 30	Polarity_SYNC	O	4mA	Frame Inversion polarity Index 3D_EN=L :1-frame inversion 3D_EN=H :2-frame inversion	***Note 1***
CN2_pin 30	3D_EN	I	IPL*	3D enable control signal	

* IPL : internal pull low

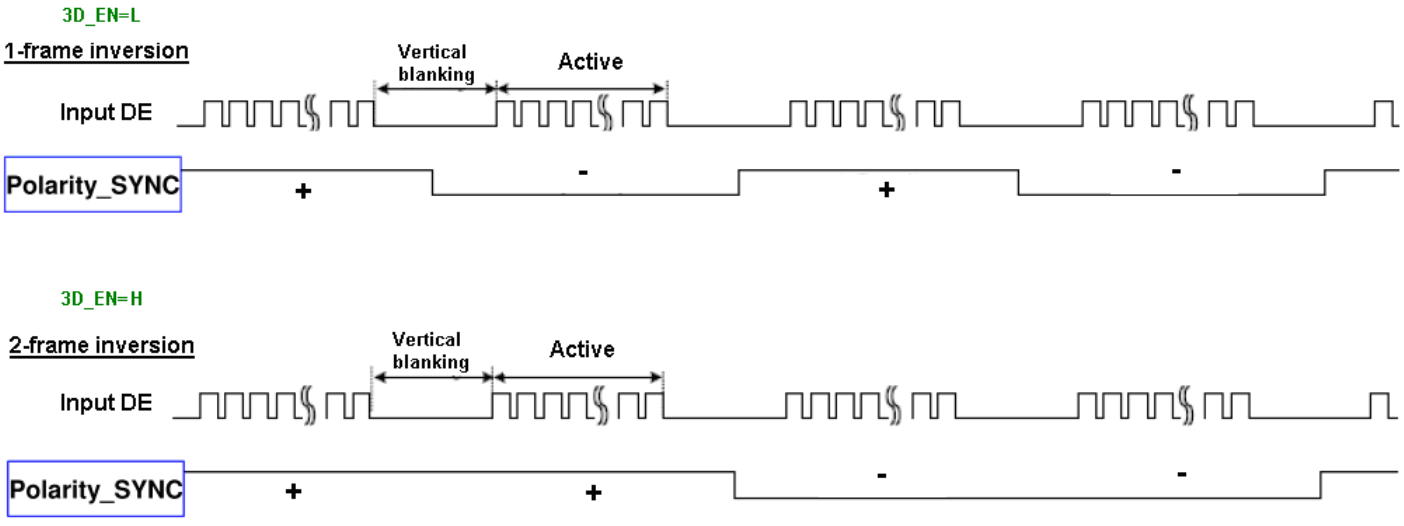
Absolute Maximum Rating

Symbol	Descripition	Min	Max	Unit	Remark
3D_EN	3D enable control signal	GND-0.3	5.0	[Volt]	Ta=25℃

Recommended Operating Condition

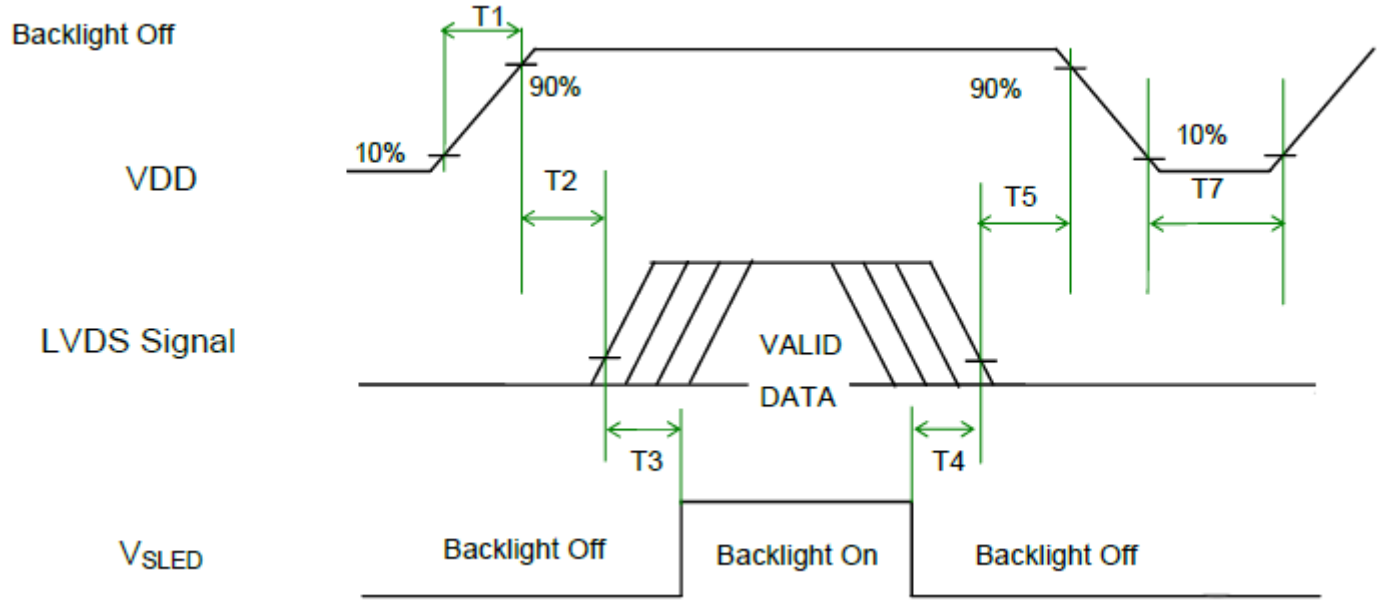
Symbol	Descripition	Condition	Rating			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage		2.0	-	3.6	[Volt]
V_{IL}	Input Low Voltage		0	-	0.8	[Volt]
V_{OH}	Output High Voltage	I =4mA	2.4	-	3.4	[Volt]
V_{OL}	Output Low Voltage	I_{OL}=4mA	0	-	0.4	[Volt]

Note 1:



Power ON/OFF Sequence

VDD power,LVDS signal and backlight on/off sequence are as following. LVDS signals from any system sha
Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	500	-	-	[ms]	
T4	100	-	-	[ms]	
T5	0	-	-	[ms]	
T6	0	-	50	[ms]	*Note 1* *Note 2*
T7	1000	-	150	[ms]	

Note 1: *Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.*
Note 2: *During T6 and T7 period , please keep the level of input eDP signals with Hi-Zstate.*

7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

TFT LCD Module

Connector Type

TFT-LCD Connector	Manufacturer	STM	Starconn
	Part Number	MSCKT2407P30HB (CN1 / CN2 /CN3)	115F40-R000RA-M3 (CN4)
Mating Connector	Manufacturer	STM or compatible	JAE or compatible
	Part Number	PK2407P30V	FI-NX40HL

Connector Pin Assignment

CN1

PIN #	Symbol	DESCRIPTION
1	R1_0N	Negative LVDS differential data input (Port1 data)
2	R1_0P	Positive LVDS differential data input (Port1 data)
3	R1_1N	Negative LVDS differential data input (Port1 data)
4	R1_1P	Positive LVDS differential data input (Port1 data)
5	R1 2N	Negative LVDS differential data input (Port1 data)
6	R1 2P	Positive LVDS differential data input (Port1 data)
7	GND	Ground
8	R1_CLKN	Negative LVDS differential clock input (Port1 clock)
9	R1_CLKP	Positive LVDS differential clock input (Port1 clock)
10	GND	Ground
11	R1 3N	Negative LVDS differential data input (Port1 data)
12	R1 3P	Positive LVDS differential data input (Port1 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R2_0N	Negative LVDS differential data input (Port2 data)
17	R2_0P	Positive LVDS differential data input (Port2 data)
18	R2_1N	Negative LVDS differential data input (Port2 data)
19	R2_1P	Positive LVDS differential data input (Port2 data)
20	R2 2N	Negative LVDS differential data input (Port2 data)

21	R2 2P	Positive LVDS differential data input (Port2 data)
22	GND	Ground
23	R2 CLKP	Negative LVDS differential clock input (Port2 clock)
24	R2 CLKP	Positive LVDS differential clock input (Port2 clock)
25	GND	Ground
26	R2_3N	Negative LVDS differential data input (Port2 data)
27	R2_3P	Positive LVDS differential data input (Port2 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	NC	No connection (for AUO test only. Do not connect)

CN2

PIN #	Symbol	DESCRIPTION
1	R3_0N	Negative LVDS differential data input (Port3 data)
2	R3_0P	Positive LVDS differential data input (Port3 data)
3	R3_1N	Negative LVDS differential data input (Port3 data)
4	R3_1P	Positive LVDS differential data input (Port3 data)
5	R3_2N	Negative LVDS differential data input (Port3 data)
6	R3_2P	Positive LVDS differential data input (Port3 data)
7	GND	Ground
8	R3_CLKN	Negative LVDS differential clock input (Port3 clock)
9	R3_CLKP	Positive LVDS differential clock input (Port3 clock)
10	GND	Ground
11	R3_3N	Negative LVDS differential data input (Port3 data)
12	R3_3P	Positive LVDS differential data input (Port3 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R4_0N	Negative LVDS differential data input (Port4 data)
17	R4_0P	Positive LVDS differential data input (Port4 data)
18	R4_1N	Negative LVDS differential data input (Port4 data)
19	R4_1P	Positive LVDS differential data input (Port4 data)
20		Negative LVDS differential data input (Port4 data)
21		Positive LVDS differential data input (Port4 data)
22		Ground
23	R4 CLKP	Negative LVDS differential clock input (Port4 clock)
24	R4 CLKP	Positive LVDS differential clock input (Port4 clock)
25	GND	Ground
26	R4 3N	Negative LVDS differential data input (Port4 data)

27	R4_3P	Positive LVDS differential data input (Port4 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	Polarity_SYNC	Polarity SYNC (O)

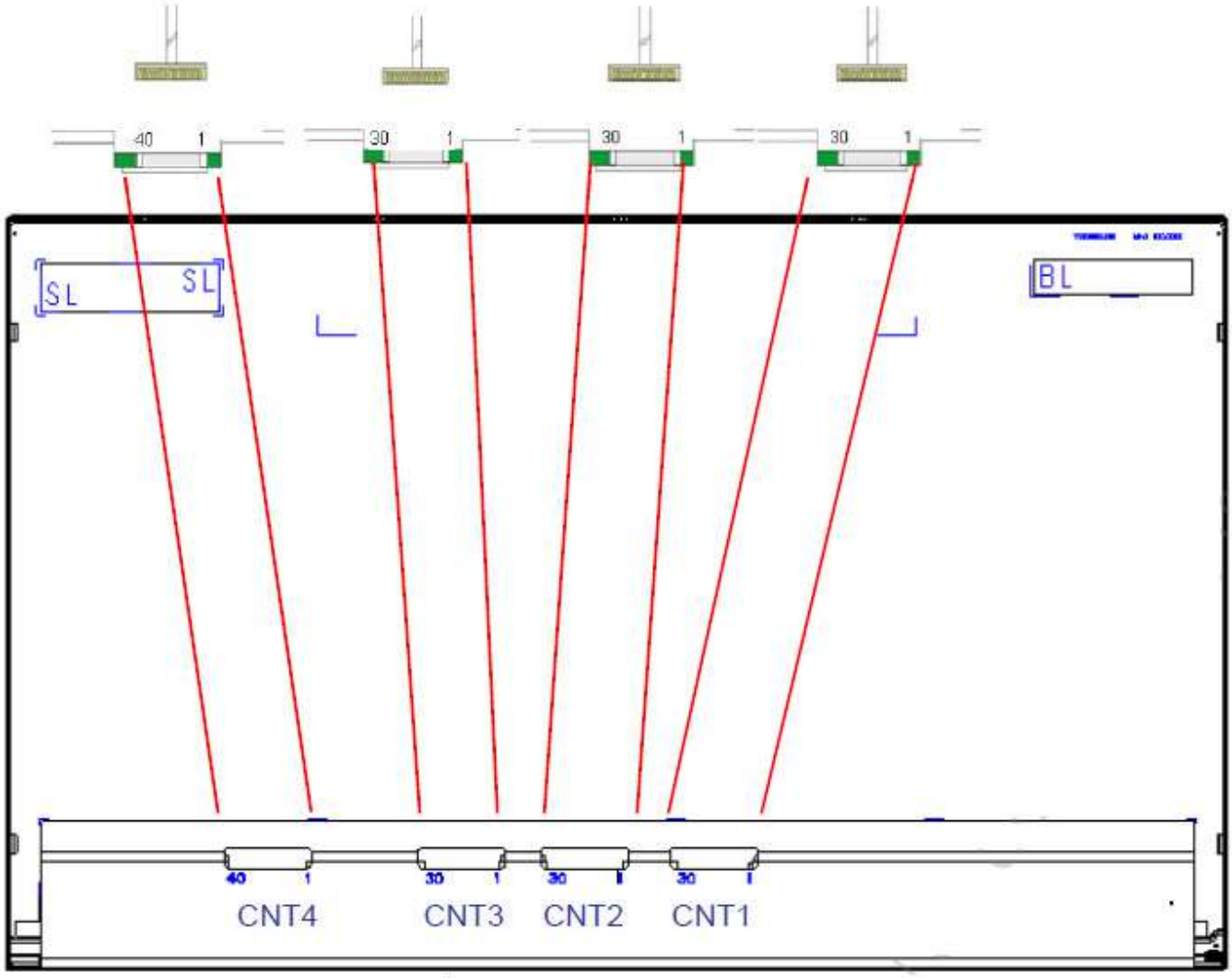
CN3

PIN #	Symbol	DESCRIPTION
1	R5_0N	Negative LVDS differential data input (Port5 data)
2	R5_0P	Positive LVDS differential data input (Port5 data)
3	R5 1N	Negative LVDS differential data input (Port5 data)
4	R5 1P	Positive LVDS differential data input (Port5 data)
5	R5 2N	Negative LVDS differential data input (Port5 data)
6	R5 2P	Positive LVDS differential data input (Port5 data)
7	GND	Ground
8	R5_CLKN	Negative LVDS differential clock input (Port5 clock
9	R5_CLKP	Positive LVDS differential clock input (Port5 clock)
10	GND	Ground
11	R5 3N	Negative LVDS differential data input (Port5 data)
12	R5 3P	Positive LVDS differential data input (Port5 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R6_0N	Negative LVDS differential data input (Port6 data)
17	R6_0P	Positive LVDS differential data input (Port6 data)
18	R6_1N	Negative LVDS differential data input (Port6 data)
19	R6_1P	Positive LVDS differential data input (Port6 data)
20	R6 2N	Negative LVDS differential data input (Port6 data)
21	R6 2P	Positive LVDS differential data input (Port6 data)
22	GND	
23	R6 CLKP	Negative LVDS differential clock input (Port6 clock)
24	R6 CLKP	Positive LVDS differential clock input (Port6 clock)
25	GND	Ground
26	R6_3N	Negative LVDS differential data input (Port6 data)
27	R6_3P	Positive LVDS differential data input (Port6 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	3D EN	3D EN (I)

CN4

PIN #	Symbol	DESCRIPTION
1	R7_0N	Negative LVDS differential data input (Port7 data)
2	R7_0P	Positive LVDS differential data input (Port7 data)
3	R7_1N	Negative LVDS differential data input (Port7 data)
4	R7_1P	Positive LVDS differential data input (Port7 data)
5	R7_2N	Negative LVDS differential data input (Port7 data)
6	R7_2P	Positive LVDS differential data input (Port7 data)
7	GND	Ground
8	R7_CLKN	Negative LVDS differential clock input (Port7 clock)
9	R7_CLKP	Positive LVDS differential clock input (Port7 clock
10	GND	Ground
11	R7_3N	Negative LVDS differential data input (Port7 data)
12	R7_3P	Positive LVDS differential data input (Port7 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R8_0N	Negative LVDS differential data input (Port8 data)
17	R8_0P	Positive LVDS differential data input (Port8 data)
18	R8_1N	Negative LVDS differential data input (Port8 data)
19	R8_1P	Positive LVDS differential data input (Port8 data)
20	R8_2N	Negative LVDS differential data input (Port8 data)
21	R8_2P	Positive LVDS differential data input (Port8 data)
22	GND	Ground
23	R8_CLKP	Negative LVDS differential clock input (Port8 clock)
24	R8_CLKP	Positive LVDS differential clock input (Port8 clock)
25	GND	Ground
26	R8_3N	Negative LVDS differential data input (Port8 data)
27	R8_3P	Positive LVDS differential data input (Port8 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	NC	No connection (for AUO test only. Do not connect)
31	NC	No connection (for AUO test only. Do not connect)
32	NC	No connection (for AUO test only. Do not connect)
33	NC	No connection (for AUO test only. Do not connect)
34	GND	Ground
35	GND	Ground
36	NC	No connection (for AUO test only. Do not connect)
37	VDD	Power Supply Input Voltage

38	VDD	Power Supply Input Voltage
39	VDD	Power Supply Input Voltage
40	VDD	Power Supply Input Voltage



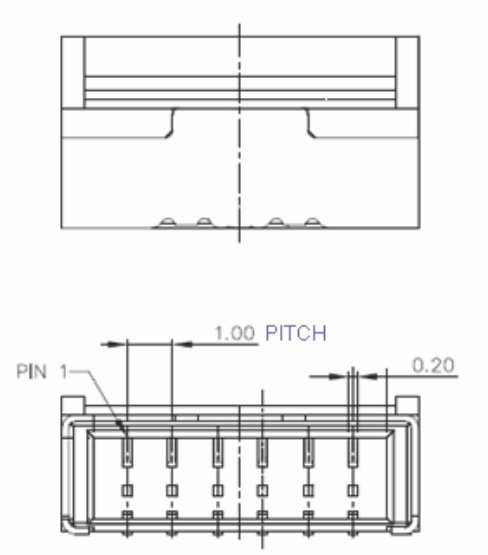
Backlight Unit

Connector Type

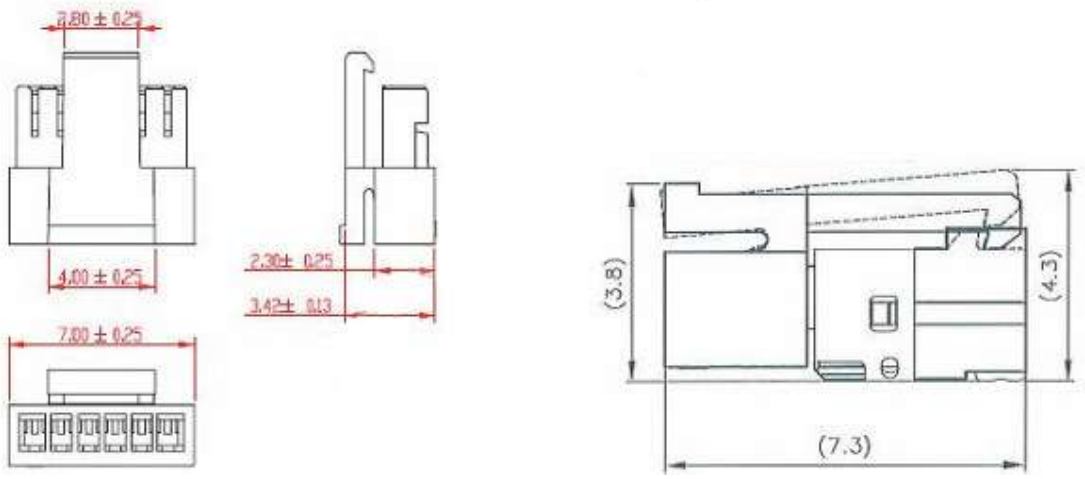
Backlight Connector	Manufacturer	ENTERY
	Part Number	3707K-S06N-21R
Mating Connector	Manufacturer	ENTERY
	Part Number	H112K-P06N-00B (Non-Locking type) H112K-P06N-03B (Locking type)

Backlight Connector dimension:

$$H \times V \times D = 13.9 \times 3.00 \times 4.25, Pitch = 1.0(unit = mm)$$

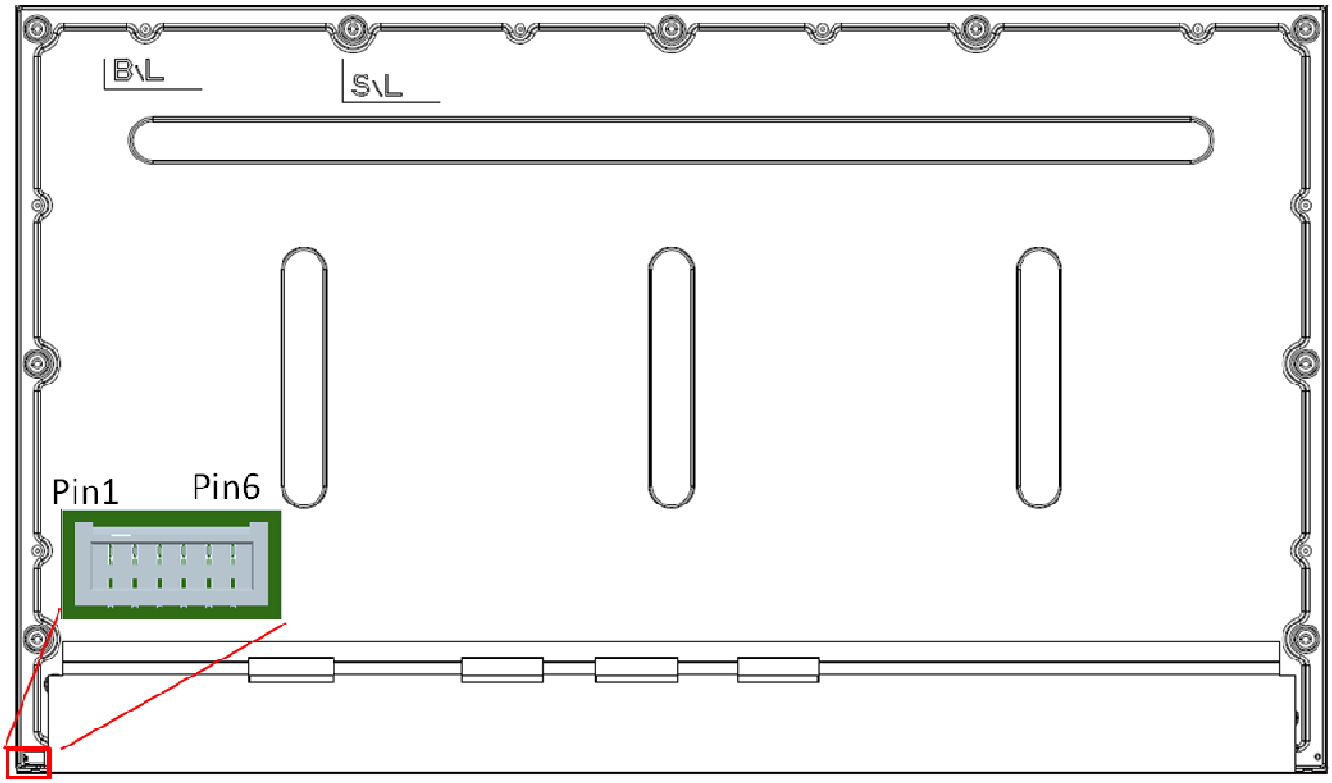


Mating Connector dimension



Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	



8. Reliability Test

Environment test conditions are listed as following Monitor test condition.

	Test Item
1	TST (Thermal Shock Test) -20℃/0.5h ~ 60℃/0.5h, 100 cycles
2	THB (Temperature Humidity Bias) 50℃/ 80%RH, 300hrs
3	LTO (Low Temperature Operation) 0℃/dry, 300hrs
4	LTS (Low Temperature Storage -20℃, 300hrs
5	Optical
6	Vibration (X、Y、Z 軸各半小時)

Note 1: a. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃,and back again.Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at
c. least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Certain performance degradation allowed:

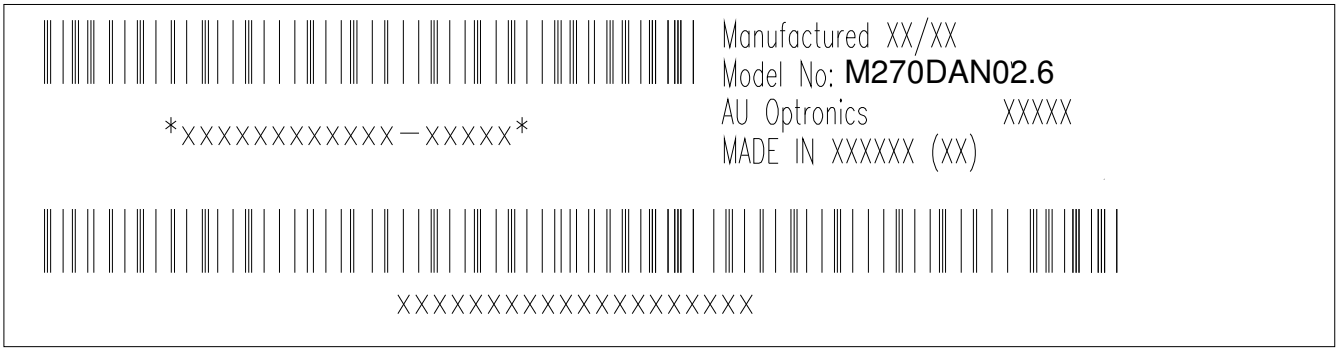
No data lost.

Self-recoverable.

No hardware failures.

9. Shipping label

The label is on the panel as shown below:



Note 6-1: For Pb Free products, AUO will add for identification.

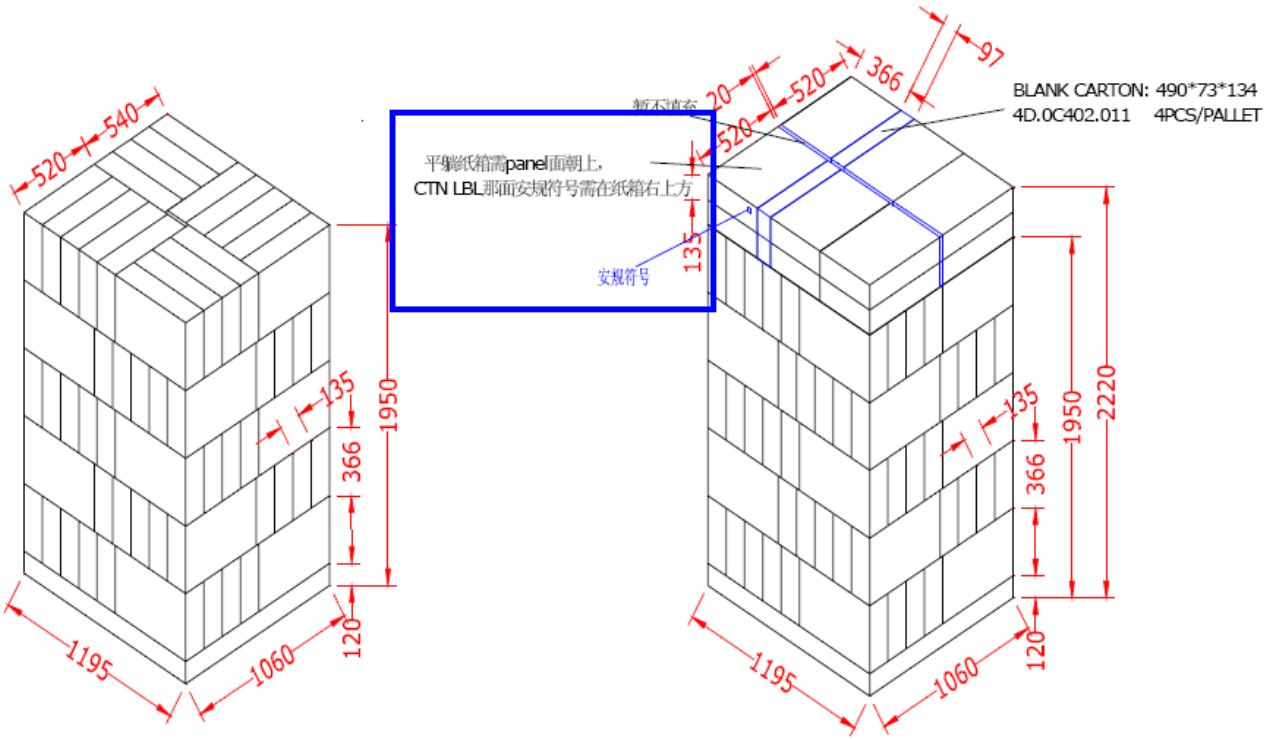
Note 6-2: For RoHS compatible products, AUO will add for identification.

Note 6-3: For China RoHS compatible products, AUO will add for identification.

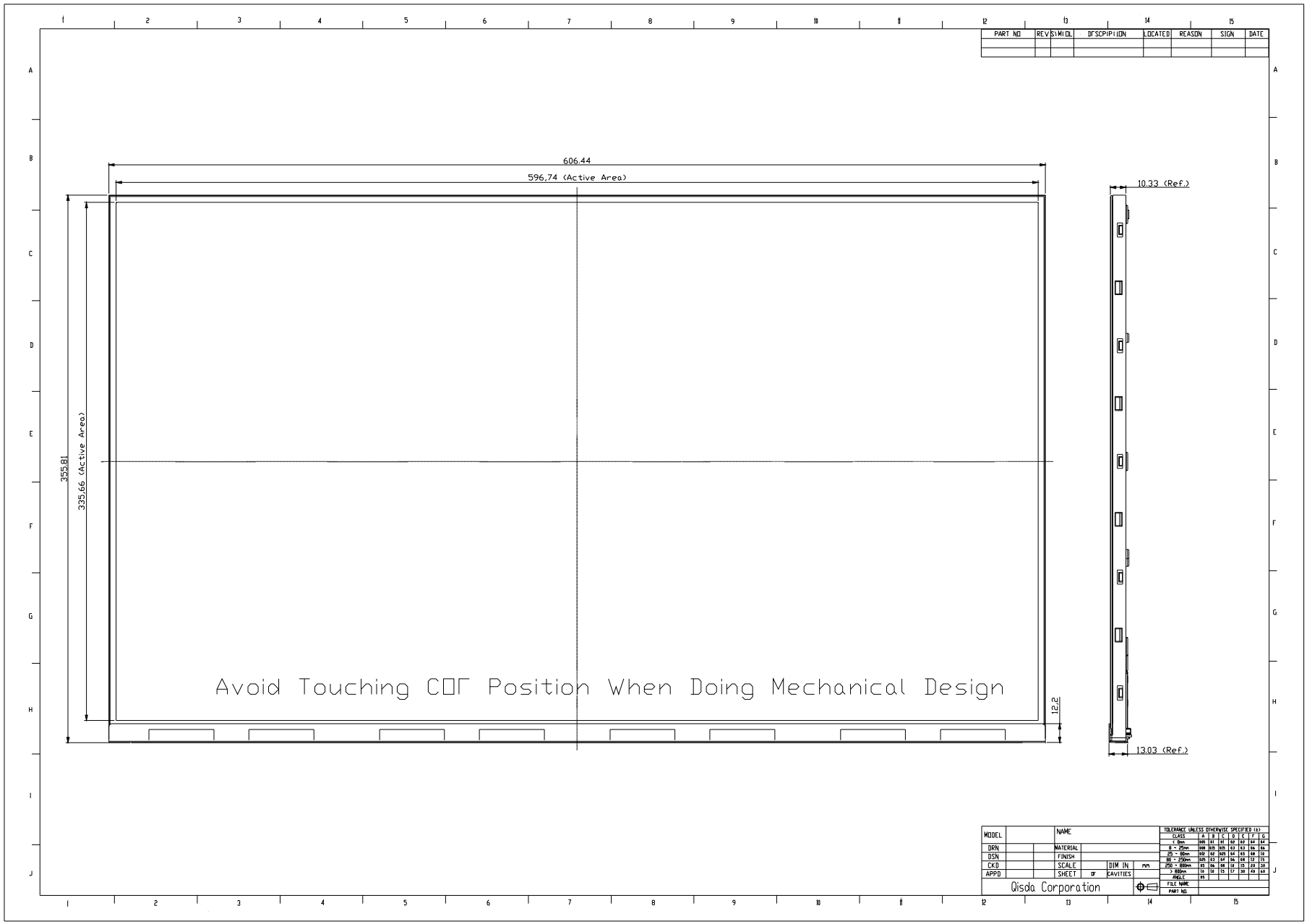
Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

10. Packing Precautions

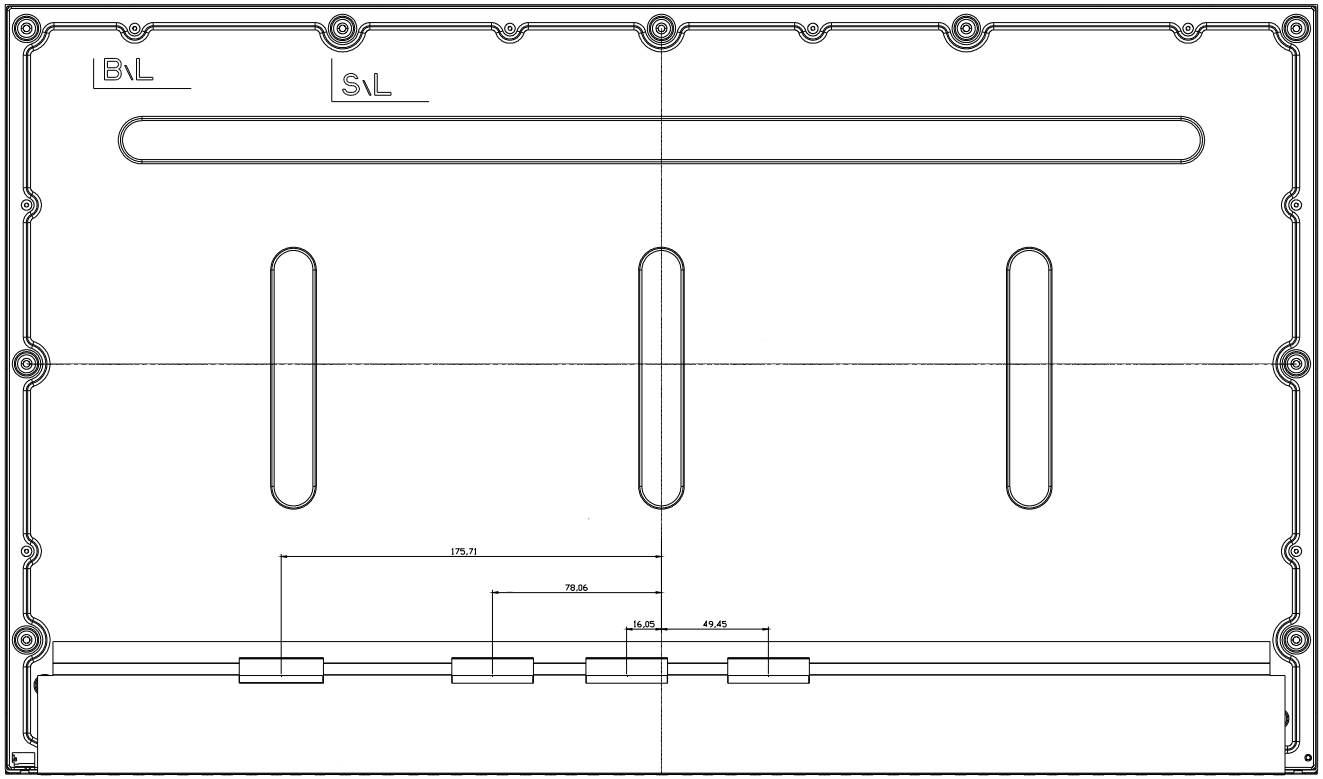
TFT-LCD Module (or monitor) should be stand or be placed face up in traffic or storage conditions; please do not keep TFT-LCD Module face down (polarizer side down).
Monitor maker should add the notice above in packing description; See the configuration example as bel



栈板尺寸参照： 1199*1061*120
18*5+12=102 PCS


606.44
596,74 (Active Area)
355.81
335.66 (Active Area)
Avoid Touching COF Position When Doing Mechanical Design
12.2
10.33 (Ref.)
13.03 (Ref.)
PART NO
REV
SYMBOL
DESCRIPTION
LOCATED
REASON
SIGN
DATE
MODEL
NAME
DRN
MATERIAL
DSN
FINISH
CKD
SCALE
DIM IN
mm
APPD
SHEET
OF
CAVITIES
Qisda Corporation
TOLERANCE UNLESS OTHERWISE SPECIFIED (±)
CLASS
FILE NAME
PART NO.

PART NO.	REV SYMBOL	DESCRIPTION	LOCATED	REASON	SIGN	DATE
	A	FIRST RELEASE				



MODEL			NAME			
DRN		06/13/2015	MATERIAL			
DSN			FINISH			
CKD			SCALE	1:1	DIM IN	mm
APPD			SHEET	1 OF 1	CAVITIES	
Qisda Corporation						

TOLERANCE UNLESS OTHERWISE SPECIFIED (±)						
CLASS	A	B	C	D	E	F	G
< 8mm	0.05	0.1	0.1	0.2	0.2	0.4	0.4
8 ~ 25mm	0.08	0.15	0.15	0.3	0.3	0.6	0.6
25 ~ 80mm	0.12	0.2	0.25	0.4	0.5	0.8	1.0
80 ~ 250mm	0.25	0.3	0.4	0.6	0.8	1.2	1.5
250 ~ 800mm	0.5	0.6	0.8	1.0	1.5	2.0	3.0
> 800mm	1.0	1.0	1.5	1.7	3.0	4.0	6.0
ANGLE	0.5						
FILE NAME							
PART NO.	0						