( ) Preliminary Specification
(V) Final Specification

Module	27” Color TFT-LCD
Model Name	M270DTN01.3Q0
Suffix Name	Q0
Document version	D03

Document		
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CUSTOMER APPROVED AND FEEDBACK		
CUSTOMER		Date:
APPROVED BY		Date :

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Document Version	Date (Y/M/D)	Page	Description
D01	2014/09/28		First Version
D02	2014/12/10	12	Modify the Input Timing Specification
D02	2014/12/10	27	Add TFT-LCD Connector Type
D03	2015/090/03	38	ADD Panel PCB Connector Position 2D Drawing

1. Handling Precautions

1. Since front polarizer is easily damaged, pay attention not to scratch it.
2. Be sure to turn off power supply when inserting or disconnecting from input connector.
3. Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4. When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5. Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6. Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7. Do not open or modify the Module Assembly.
8. Do not press the reflector sheet at the back of the module to any directions.
9. In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10. At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11. After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12. Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13. Please avoid touching COF Position while you are doing mechanical design.
14. When storing modules as spares for a long time, the following precaution is necessary:
    a. Store them in a dark place. Do not expose the module to sunlight or fluorescent light.
    b. Keep the temperature between 5℃ and 35℃ at normal humidity.

2. General Description

This specification applies to the 27 inch-FHD Color a-Si TFT-LCD Module M270DTN01.3.The display supports the QHD - 2560(H) x 1440(V) screen format and 16.7M colors (RGB 8-bits data). The input interface is 8 port LVDS and this module doesn't contain a driver board for backlight.

Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	mm	684.67(27.0")
Active Area	mm	596.74 (H) x 335.66 (V)
Pixels H x V		2560(x3) x 1440
Pixel Pitch	um	233.1 (per one triad) ×233.1
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		TN Mode, Normally White
White Luminance (Center)	cd/m^2	350 cd/m^2 (Typ.)
Contrast Ratio		1000(Typ.)
Optical Response Time	msec	5ms (Typ., on/off)
Power Consumption (VDD line + LED line)	Watt	34.3 W (Typ 60Hz) LCD module:PDD(Typ)=7.0 @Black pattern Fv=144 Hz Backlight unit:P_{BLu}(Typ)=27.3 @Is=120mA
Color gamut	%	72
Weight	Grams	2388 (Typ.)
Outline Dimension	mm	608.8(H)x354.71(V)x14.85(D)
Electrical Interface		8 port LVDS
Support Color		16.7M colors (RGB 8-bit)
Surface Treatment		Anti-Glare, 3H
Temperature Range Operating Storage (Shipping)	 °C °C	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance
TCO Compliance		TCO 6.0 Compliance

Optical Characteristics

The optical characteristics are measured on the following test condition.

Test Condition：

1.Equiment setuo:Please refer to Note 2-1

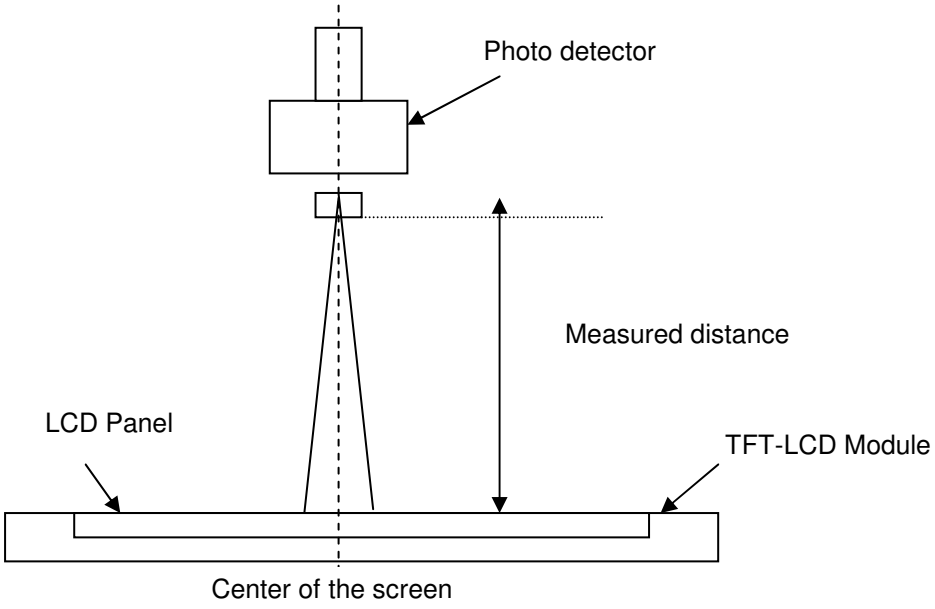
2.Panel Lighting:30 Minutes

3.VDD=12.0V, Fv=144Hz, Is=120mA, Ta=2.5℃

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_w	White Luminance (Center of screen)		300	350	-	[cd/m^2]	*Note 2-1*
L_{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	*Note 2-1*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	*Note 2-1*
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	85	-	[degree]	*Note 2-2* *By SR-3*
θ_L		Left	75	85	-		
Φ_R	Vertical Viewing Angle (CR=10)	Up	70	80	-		
Φ_L		Down	70	80	-		
θ_R	Horizontal Viewing Angle (CR=5)	Right	75	88	-		
θ_L		Left	75	88	-		
Φ_R	Vertical Viewing Angle (CR=5)	Up	70	85	-		
Φ_L		Down	70	85	-		
T_R	Response Time	Rising Time	-	3.5	5.5	[msec]	*Note 2-4* *By TRD-1000*
T_L		Falling Time	-	1.5	2.5		
		Rising + Falling	-	5	8		
R_x	Color Coordinates (CIE 1931)	Red x	0.616	0.646	0.676	-	*By SR-3*
R_y		Red y	0.314	0.344	0.374		
G_x		Green x	0.285	0.315	0.345		
G_y		Green y	0.595	0.625	0.655		
B_x		Blue x	0.110	0.140	0.170		
B_y		Blue y	0.015	0.045	0.075		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
CT	Crosstalk		-	-	1.5	[%]	*Note 2-8*
F_{dB}	Flicker (Center of screen)		-	-	-20	[dB]	*Note 2-9*

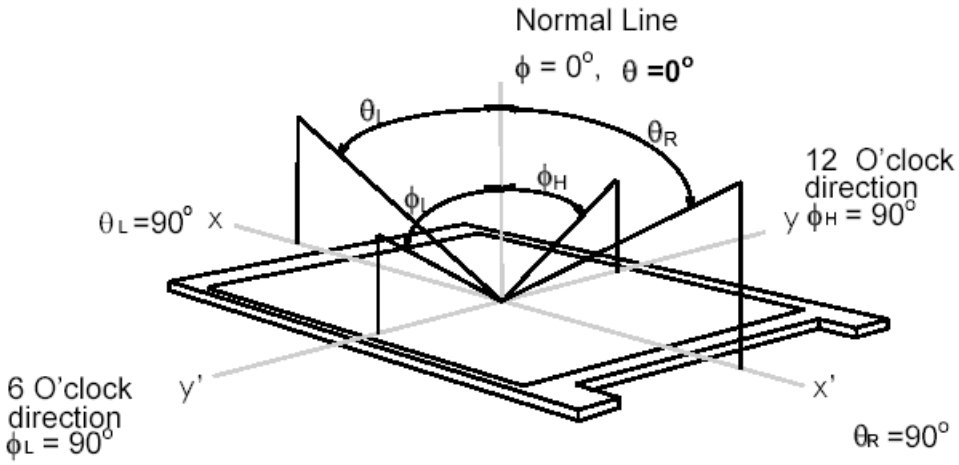
Note 2-1: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring (at surface 35℃). In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 2-2: Definition of viewing angle measured by ELDIM (EZContrast 88)

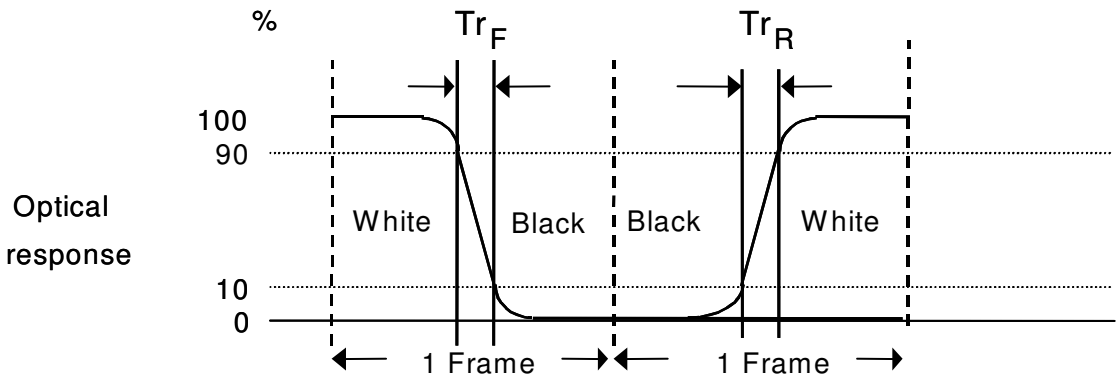
Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2-3: Contrast ratio is measured by TOPCON SR-3

Note 2-4: Definition of Response time measured by Westar TRD-100A

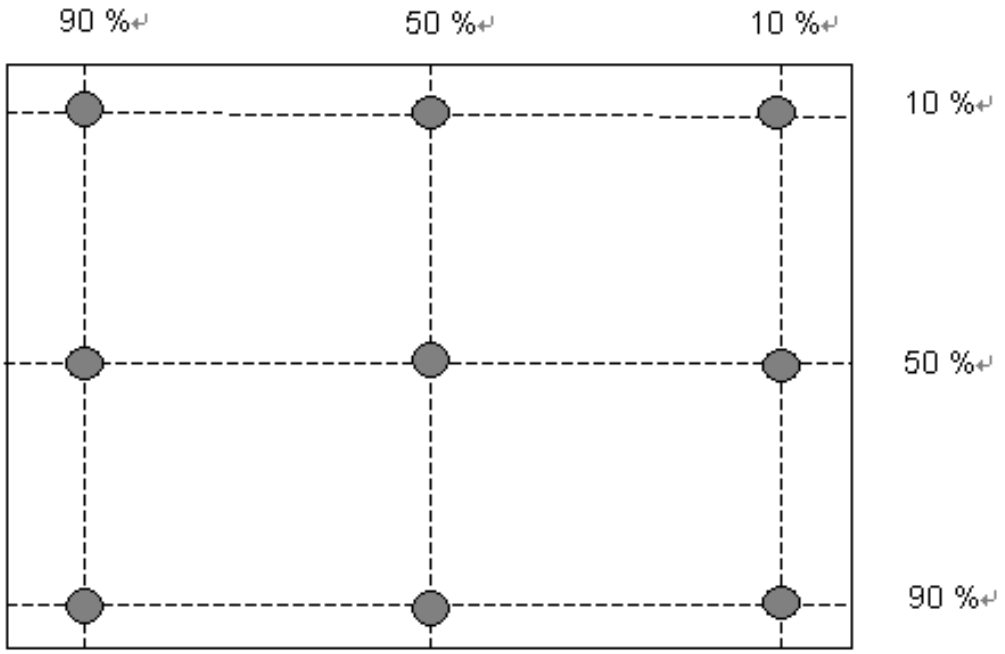
The output signals of photo detector are measured when the input signals are changed from "Black" to "White" (rising time, T_R), and from "White" to "Black" (falling time, T_F), respectively. The response time is interval between the 10% and 90% of optical response.(*Black & White color definition: Please refer section 3.4.3*)



Note 2-5: Color chromaticity and coordinates (CIE) is measured by TOPCON SR-3

Note 2-6: Central luminance is measured by TOPCON SR-3

Note 2-7: Luminance uniformity of these 9 points is defined as below and measured by TOPCON SR-3



$$\text{Uniformity} = \frac{\text{Minimum Luminance in 9 points (1-9)}}{\text{Maximum Luminance in 9 Points (1-9)}}$$

Note 2-8: Crosstalk is defined as below and measured by TOPCON SR-3

Crosstalk measurement

Definition:

$CT = Max. (CT_H, CT_V)$;

Where

a.Maximum Horizontal Crosstalk :

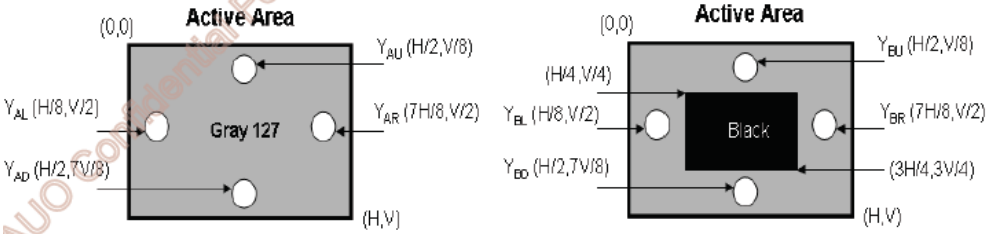
$CT_H = Max. (| Y_{BL} - Y_{AL} | / Y_{AL} \times 100\ \%, | Y_{BR} - Y_{AR} | / Y_{AR} \times 100\ \%)$;

Maximum Vertical Crosstalk:

$CT_V = Max. (| Y_{BU} - Y_{AU} | / Y_{AU} \times 100\ \%, | Y_{BD} - Y_{AD} | / Y_{AD} \times 100\ \%)$;

b. Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR} = Luminance of measured location without Black pattern

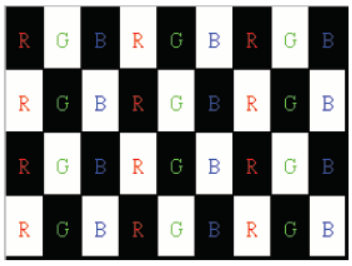
Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR} = Luminance of measured location with Black pattern



Note 2-9: Test Patern: Subchecker Pattern measured by TOPCON SR-3

Flicker measurement

a. Test pattern: It is listed as following.



Gray level = L0

Gray level = L127

R: Red, G: Green, B:Blue

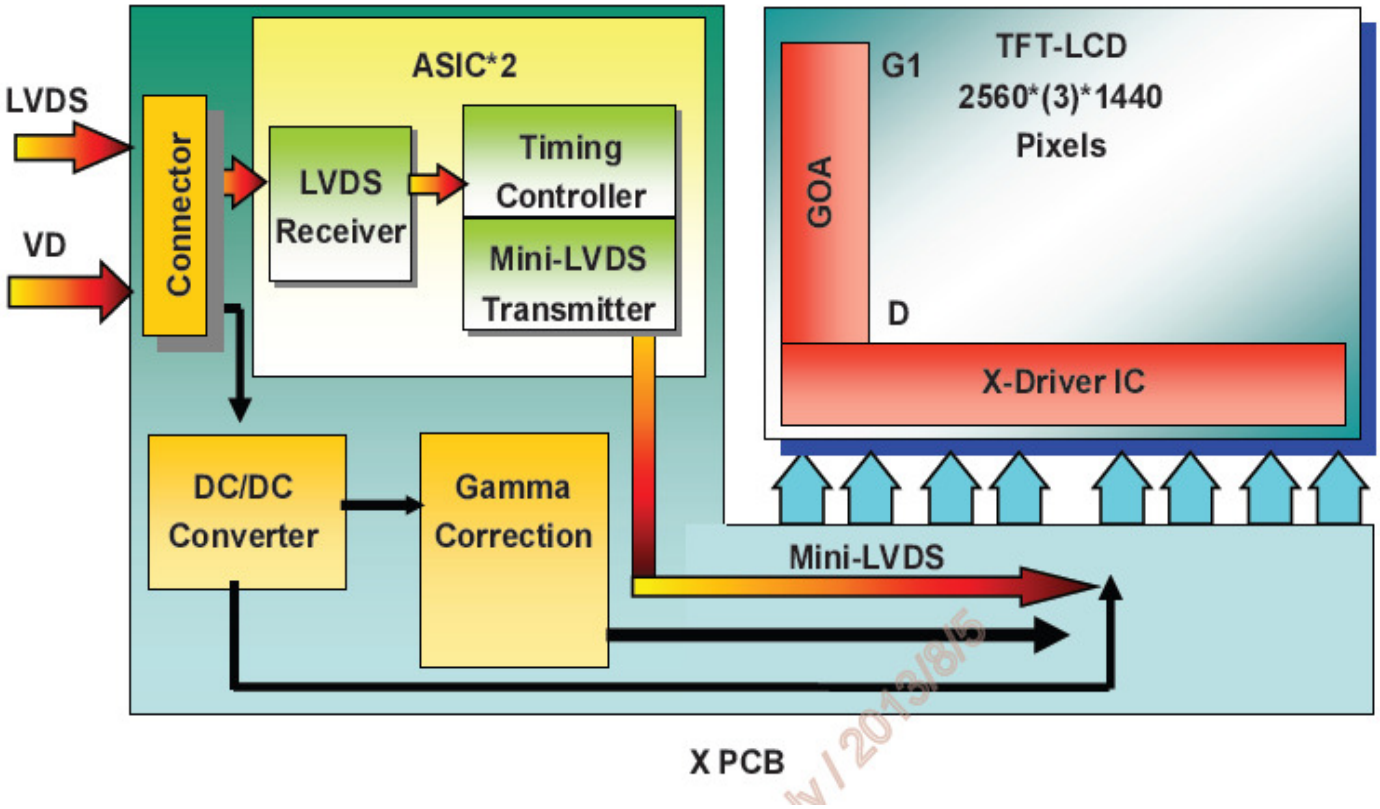
b. Measured position: Center of screen & perpendicular to the screen

3. Functional Block Diagram

3.TFT-LCD

3-1. Block Diagram

The following shows the block diagram of the 27 inch Color TFT-LCD Module



3.2. Signal Description

CN1

PIN #	Symbol	DESCRIPTION
1	R1_0N	Negative LVDS differential data input (Port1 data)
2	R1_0P	Positive LVDS differential data input (Port1 data)
3	R1_1N	Negative LVDS differential data input (Port1 data)
4	R1_1P	Positive LVDS differential data input (Port1 data)
5	R1 2N	Negative LVDS differential data input (Port1 data)
6	R1 2P	Positive LVDS differential data input (Port1 data)
7	GND	Ground
8	R1_CLKN	Negative LVDS differential clock input (Port1 clock)
9	R1_CLKP	Positive LVDS differential clock input (Port1 clock)
10	GND	Ground
11	R2 3N	Negative LVDS differential data input (Port1 data)
12	R2 3P	Positive LVDS differential data input (Port1 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R2_0N	Negative LVDS differential data input (Port2 data)
17	R2_0P	Positive LVDS differential data input (Port2 data)
18	R2_1N	Negative LVDS differential data input (Port2 data)
19	R2_1P	Positive LVDS differential data input (Port2 data)
20	R2 2N	Negative LVDS differential data input (Port2 data)
21	R2 2P	Positive LVDS differential data input (Port2 data)
22	GND	Ground
23	R2 CLKP	Negative LVDS differential clock input (Port2 clock)
24	R2 CLKP	Positive LVDS differential clock input (Port2 clock)
25	GND	Ground
26	R2_3N	Negative LVDS differential data input (Port2 data)
27	R2_3P	Positive LVDS differential data input (Port2 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	NC	No connection (for AUO test only. Do not connect)

CN2

PIN #	Symbol	DESCRIPTION
1	R3_0N	Negative LVDS differential data input (Port3 data)
2	R3_0P	Positive LVDS differential data input (Port3 data)
3	R3_1N	Negative LVDS differential data input (Port3 data)
4	R3_1P	Positive LVDS differential data input (Port3 data)
5	R3_2N	Negative LVDS differential data input (Port3 data)
6	R3_2P	Positive LVDS differential data input (Port3 data)
7	GND	Ground
8	R3_CLKN	Negative LVDS differential clock input (Port3 clock)
9	R3_CLKP	Positive LVDS differential clock input (Port3 clock)
10	GND	Ground
11	R3_3N	Negative LVDS differential data input (Port3 data)
12	R3_3P	Positive LVDS differential data input (Port3 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R4_0N	Negative LVDS differential data input (Port4 data)
17	R4_0P	Positive LVDS differential data input (Port4 data)
18	R4_1N	Negative LVDS differential data input (Port4 data)
19	R4_1P	Positive LVDS differential data input (Port4 data)
20	R4_2N	Negative LVDS differential data input (Port4 data)
21	R4_2P	Positive LVDS differential data input (Port4 data)
22	GND	Ground
23	R4_CLKP	Negative LVDS differential clock input (Port4 clock)
24	R4_CLKP	Positive LVDS differential clock input (Port4 clock)
25	GND	Ground
26	R4_3N	Negative LVDS differential data input (Port4 data)
27	R4_3P	Positive LVDS differential data input (Port4 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	Polarity_SYNC	Polarity SYNC (O)

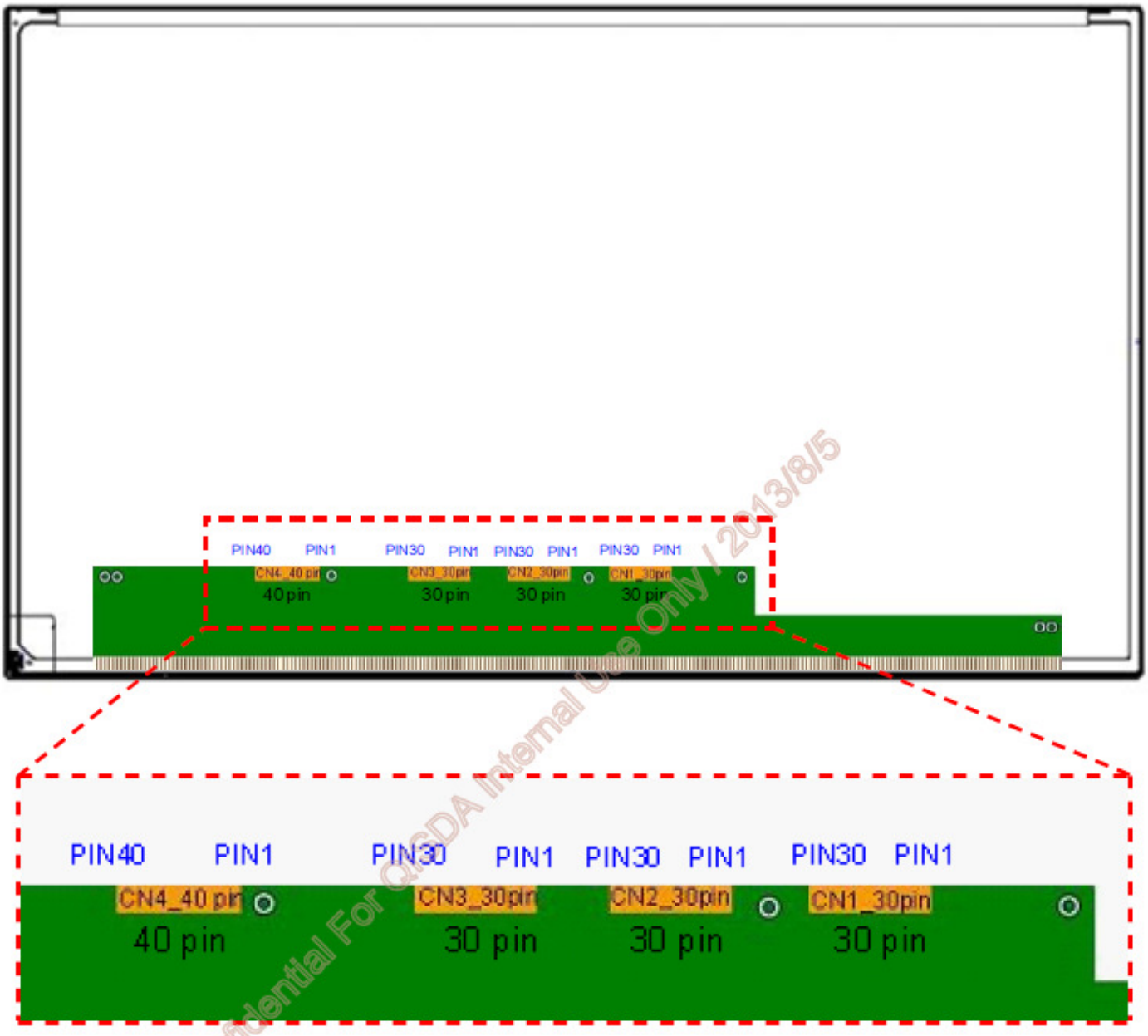
CN3

PIN #	Symbol	DESCRIPTION
1	R5_0N	Negative LVDS differential data input (Port5 data)
2	R5_0P	Positive LVDS differential data input (Port5 data)
3	R5 1N	Negative LVDS differential data input (Port5 data)
4	R5 1P	Positive LVDS differential data input (Port5 data)
5	R5 2N	Negative LVDS differential data input (Port5 data)
6	R5 2P	Positive LVDS differential data input (Port5 data)
7	GND	Ground
8	R5_CLKN	Negative LVDS differential clock input (Port5 clock)
9	R5_CLKP	Positive LVDS differential clock input (Port5 clock)
10	GND	Ground
11	R5 3N	Negative LVDS differential data input (Port5 data)
12	R5 3P	Positive LVDS differential data input (Port5 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R6_0N	Negative LVDS differential data input (Port6 data)
17	R6_0P	Positive LVDS differential data input (Port6 data)
18	R6_1N	Negative LVDS differential data input (Port6 data)
19	R6_1P	Positive LVDS differential data input (Port6 data)
20	R6 2N	Negative LVDS differential data input (Port6 data)
21	R6 2P	Positive LVDS differential data input (Port6 data)
22	GND	Ground
23	R6 CLKP	Negative LVDS differential clock input (Port6 clock)
24	R6 CLKP	Positive LVDS differential clock input (Port6 clock)
25	GND	Ground
26	R6_3N	Negative LVDS differential data input (Port6 data)
27	R6_3P	Positive LVDS differential data input (Port6 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	3D_EN (I)	3D_EN (I)

CN4

PIN #	Symbol	DESCRIPTION
1	R7_0N	Negative LVDS differential data input (Port7 data)
2	R7_0P	Positive LVDS differential data input (Port7 data)
3	R7_1N	Negative LVDS differential data input (Port7 data)
4	R7_1P	Positive LVDS differential data input (Port7 data)
5	R7_2N	Negative LVDS differential data input (Port7 data)
6	R7_2P	Positive LVDS differential data input (Port7 data)
7	GND	Ground
8	R7_CLKN	Negative LVDS differential clock input (Port7 clock)
9	R7_CLKP	Positive LVDS differential clock input (Port7 clock)
10	GND	Ground
11	R7_3N	Negative LVDS differential data input (Port7 data)
12	R7_3P	Positive LVDS differential data input (Port7 data)
13	NC	No connection (for AUO test only. Do not connect)
14	NC	No connection (for AUO test only. Do not connect)
15	GND	Ground
16	R8_0N	Negative LVDS differential data input (Port8 data)
17	R8_0P	Positive LVDS differential data input (Port8 data)
18	R8_1N	Negative LVDS differential data input (Port8 data)
19	R8_1P	Positive LVDS differential data input (Port8 data)
20	R8_2N	Negative LVDS differential data input (Port8 data)
21	R8_2P	Positive LVDS differential data input (Port8 data)
22	GND	Ground
23	R8_CLKP	Negative LVDS differential clock input (Port8 clock)
24	R8_CLKP	Positive LVDS differential clock input (Port8 clock)
25	GND	Ground
26	R8_3N	Negative LVDS differential data input (Port8 data)
27	R8_3P	Positive LVDS differential data input (Port8 data)
28	NC	No connection (for AUO test only. Do not connect)
29	NC	No connection (for AUO test only. Do not connect)
30	NC	No connection (for AUO test only. Do not connect)
31	NC	No connection (for AUO test only. Do not connect)
32	NC	No connection (for AUO test only. Do not connect)
33	NC	No connection (for AUO test only. Do not connect)
34	GND	Ground
35	GND	Ground
36	NC	No connection (for AUO test only. Do not connect)

37	VDD	Power Supply Input Voltage
38	VDD	Power Supply Input Voltage
39	VDD	Power Supply Input Voltage
40	VDD	Power Supply Input Voltage



4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

Backlight Unit

	Symbol	Min	Typ	Max	Unit	Conditions
LED Current	ILED	-	120	132	[mA]	*Note 4-1,4-2*

Absolute Ratings of Environment

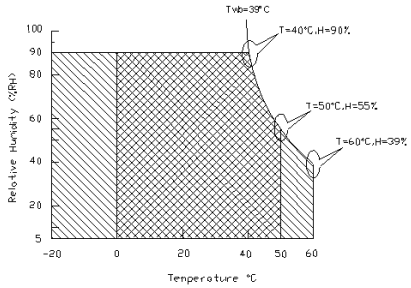
Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	***Note 4-3***
Center Glass Surface temperature (Operation)	TGS	0	+65	[°C]	***Note 4-3*** ***Function judged only***
Operation Humidity	HOP	5	90	[%RH]	***Note 4-3***
Storage Temperature	TST	-20	+60	[°C]	
Storage Humidity	HST	5	90	[%RH]	

Note 4-1: With in Ta (25℃)

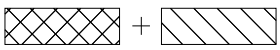
Note 4-2: Permanent damage to the device may occur if exceeding maximum values

Note 4-3: For quality perfermance, please refer to AUO IIS(Incoming Inspection Standard).

1. 90% RH Max (Ta ≦39℃)
2. Max wet-bulb temperature at 39℃ or less. (Ta ≦39℃)
3. No condensation



Operating Range 

Storage Range 

5. Electrical characteristics-TFT LCD Module

Power Specification

Input power specifications are as following:

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25℃

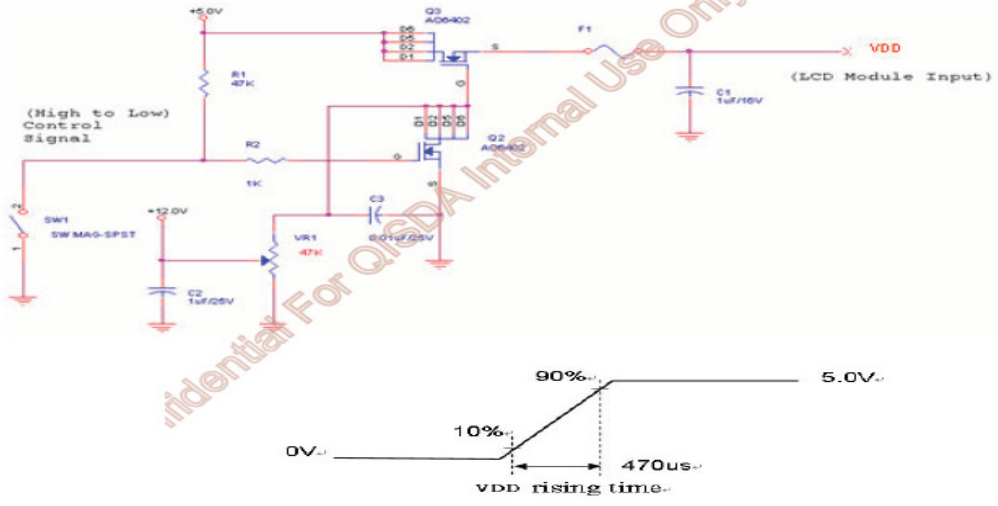
Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power Supply Input Voltage	10.8	12	13.2	[Volt]	
IDD	Power Supply Input Current (RMS)	-	0.5	1.3	[A]	VDD= 12.0V, All Black Pattern At 144Hz,
PDD	VDD Power Consumption	-	6.5	15.6	[Watt]	VDD= 12.0V, All Black Pattern At 144Hz
IRush	Inrush Current	-	-	3.0	[A]	**Note 5-1**
VDDrp	Allowable LCD Ripple Voltage	-	-	500	[mV]	VDD= 12.0V, All Black Pattern At 144Hz

Note 5-1: Measurement conditions:

Inrush Current measurement:

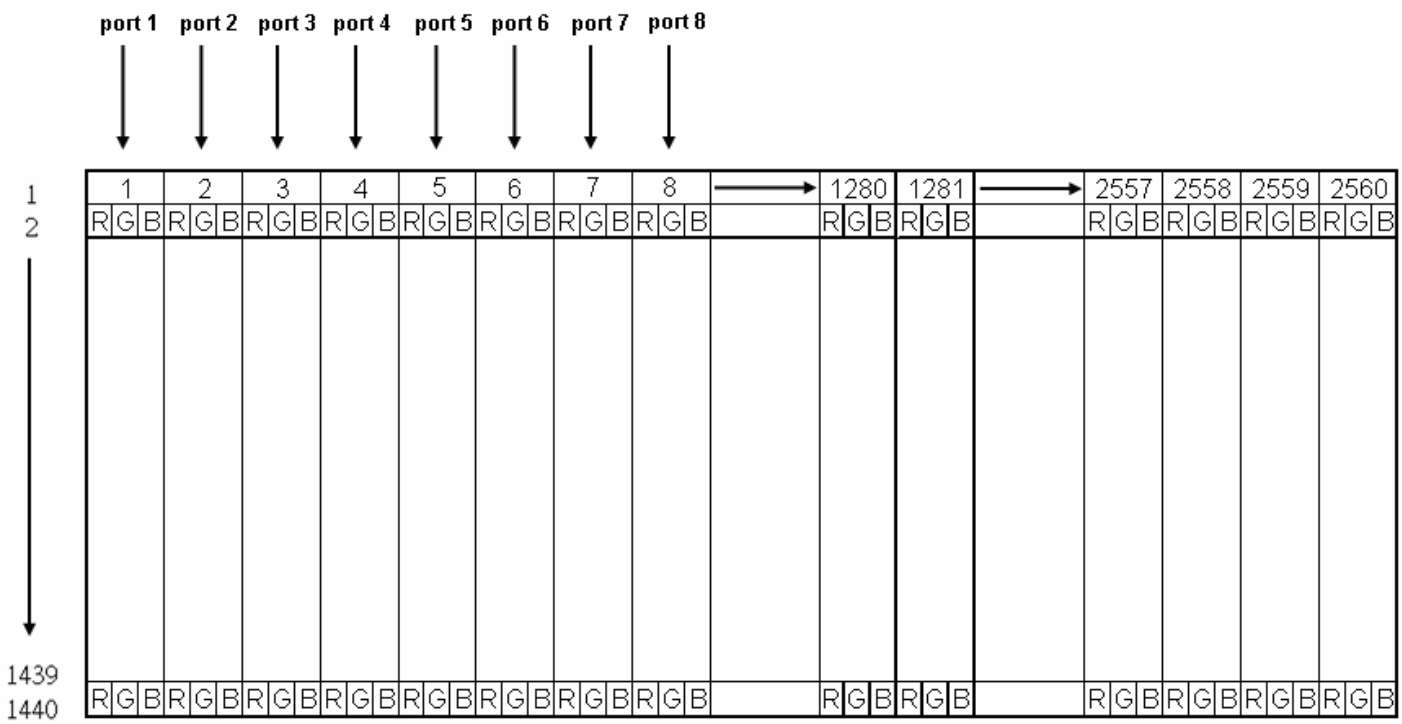
Test circuit:



The duration of VDD rising time: 470us.

6. Signal Characteristic

LCD Pixel Format



Note 6-1: The module use 8 port-LVDS interface.

Port 1 : 1, 9…..…….. →2557pixel _ 8N+1 N=0,~ 319 (1,9.. 2553pixe)

Port 2 : 2, 10…….. →2558pixel _ 8N+2 N=0,~ 319 (2,10.. 2554pixe)

Port 3 : 3, 11..…….. →2559 pixel _ 8N+3 N=0,~ 319 (3,11.. 2555pixe)

Port 4 : 4, 12…….. →2560 pixel _ 8N+4 N=0,~ 319 (4,12.. 2556pixe)

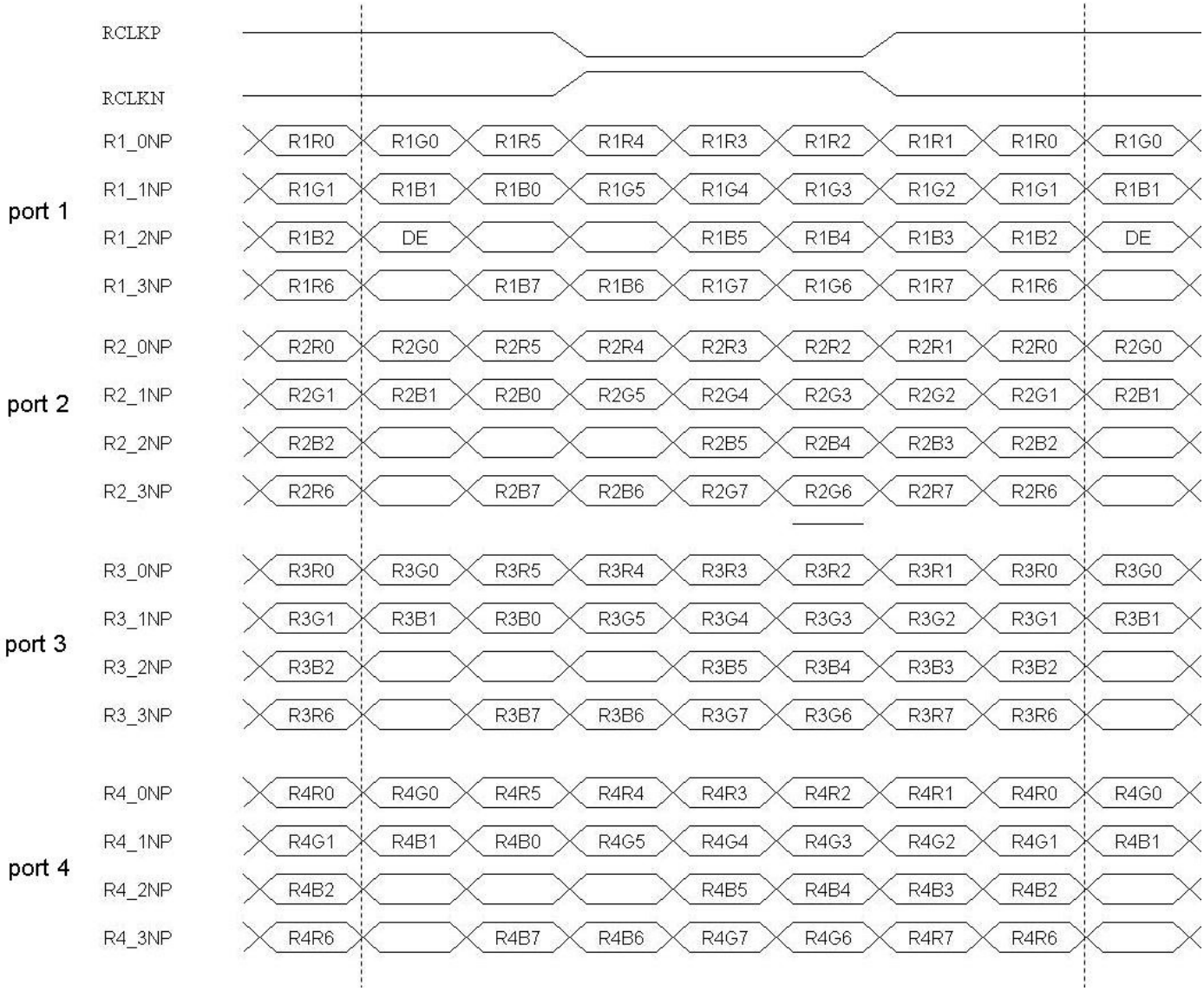
Port 5 : 5, 13…….. →2557pixel _ 8N+5 N=0,~ 319 (5,13.. 2557pixe)

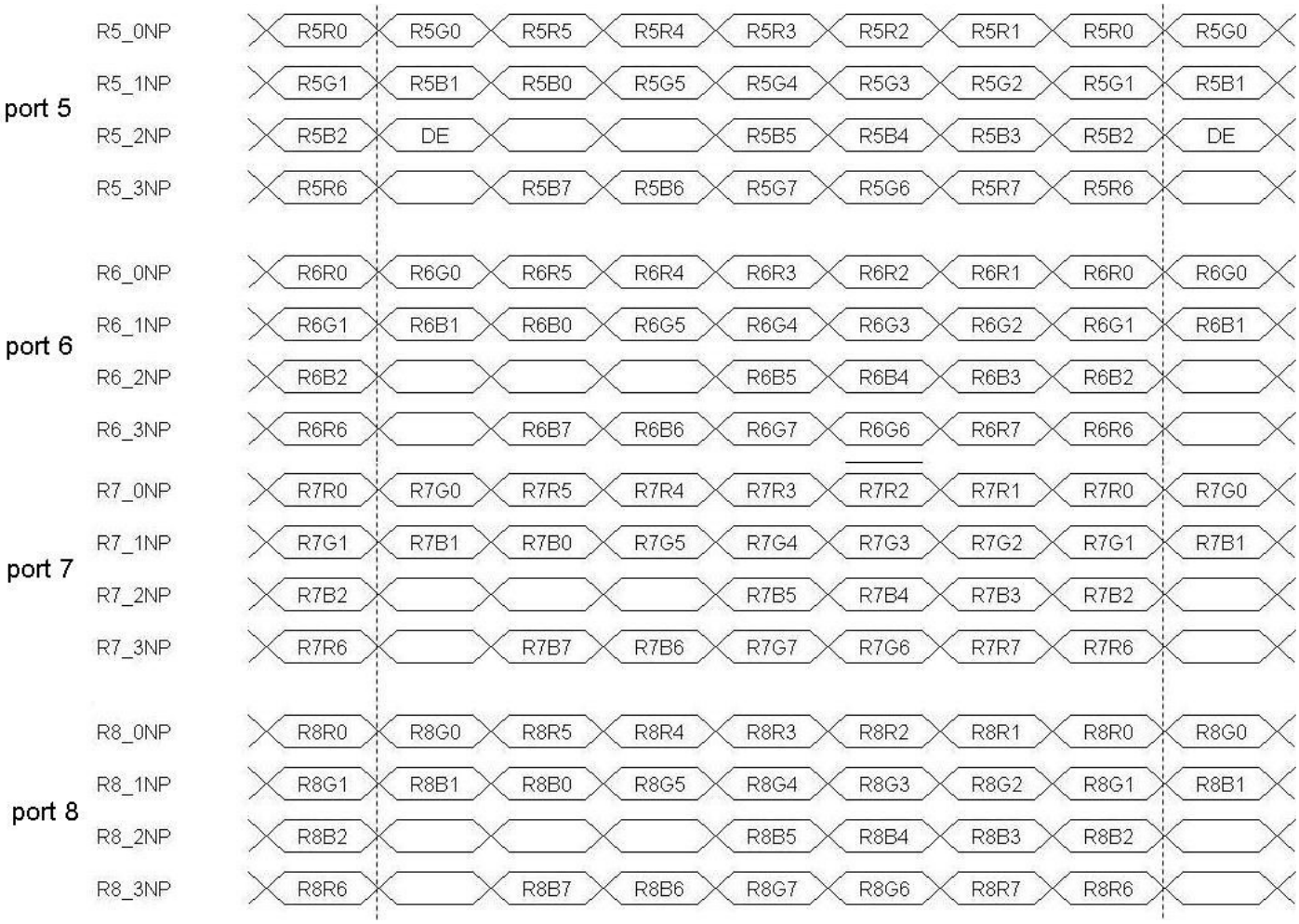
Port 6 : 6, 14…….. →2558pixel _ 8N+6 N=0,~ 319 (6,14.. 2558pixe)

Port 7 : 7, 15…….. →2559 pixel _ 8N+7 N=0,~ 319 (7,15.. 2559pixe)

Port 8 : 8, 16…….. →2560 pixel _ 8N+8 N=0,~ 319 (8,16.. 2560pixe)

LVDS Data Format




port 5
R5_0NP R5R0 R5G0 R5R5 R5R4 R5R3 R5R2 R5R1 R5R0 R5G0
R5_1NP R5G1 R5B1 R5B0 R5G5 R5G4 R5G3 R5G2 R5G1 R5B1
R5_2NP R5B2 DE R5B5 R5B4 R5B3 R5B2 DE
R5_3NP R5R6 R5B7 R5B6 R5G7 R5G6 R5R7 R5R6
port 6
R6_0NP R6R0 R6G0 R6R5 R6R4 R6R3 R6R2 R6R1 R6R0 R6G0
R6_1NP R6G1 R6B1 R6B0 R6G5 R6G4 R6G3 R6G2 R6G1 R6B1
R6_2NP R6B2 R6B5 R6B4 R6B3 R6B2
R6_3NP R6R6 R6B7 R6B6 R6G7 R6G6 R6R7 R6R6
port 7
R7_0NP R7R0 R7G0 R7R5 R7R4 R7R3 R7R2 R7R1 R7R0 R7G0
R7_1NP R7G1 R7B1 R7B0 R7G5 R7G4 R7G3 R7G2 R7G1 R7B1
R7_2NP R7B2 R7B5 R7B4 R7B3 R7B2
R7_3NP R7R6 R7B7 R7B6 R7G7 R7G6 R7R7 R7R6
port 8
R8_0NP R8R0 R8G0 R8R5 R8R4 R8R3 R8R2 R8R1 R8R0 R8G0
R8_1NP R8G1 R8B1 R8B0 R8G5 R8G4 R8G3 R8G2 R8G1 R8B1
R8_2NP R8B2 R8B5 R8B4 R8B3 R8B2
R8_3NP R8R6 R8B7 R8B6 R8G7 R8G6 R8R7 R8R6

Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter. the color.

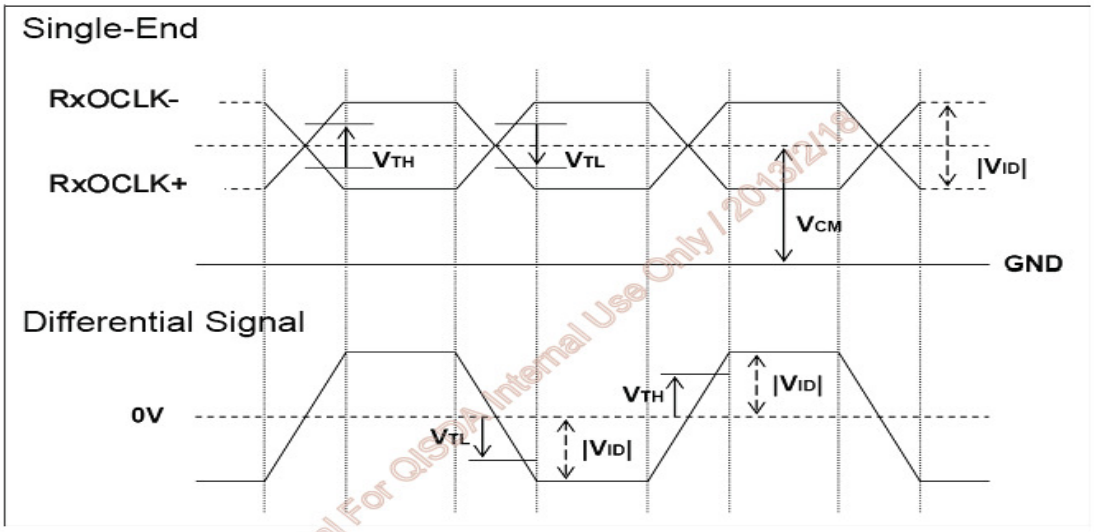
Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

LVDS Specification

DC Characteristics of each signal are as following:

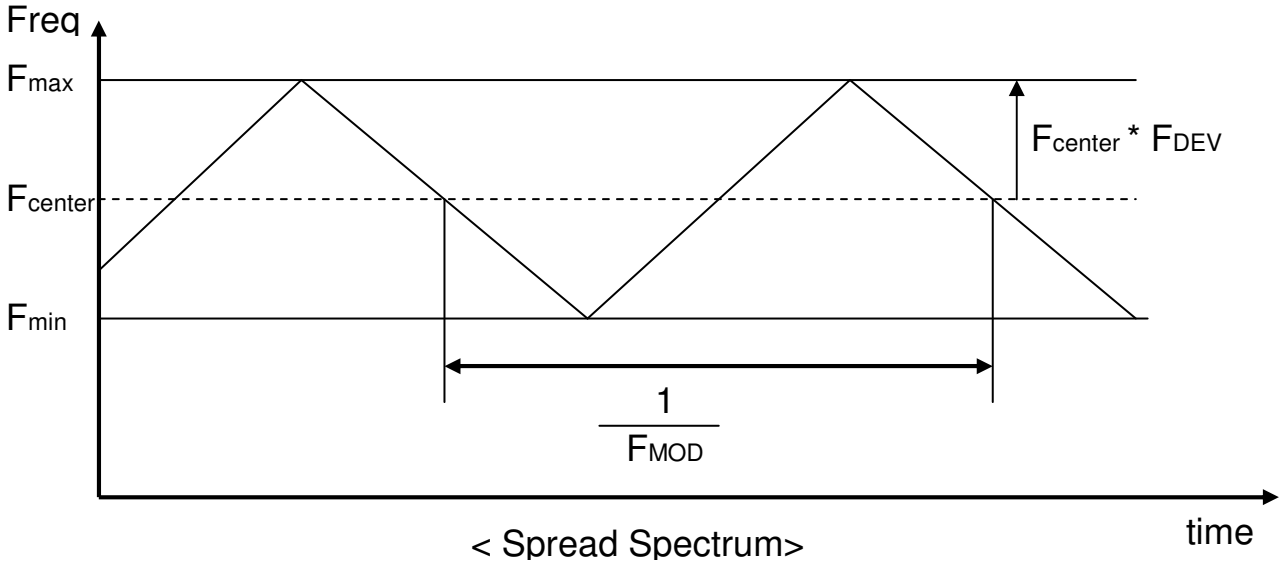
Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{TH}	Differential Input High Threshold	-	-	+100	mV	VICM = 1.2V *Note 1*
V_{TL}	Differential Input Low Threshold	-100	-	-	mV	VICM = 1.2V *Note 1*
$\lvert V_{ID} \rvert$	Input Differential Voltage	100	-	600	mV	*Note 6-2*
V_{CM}	Differential Input Common Mode Voltage	+1.0	+1.2	+1.5	V	VTH-VTL = 200MV (max) *Note 1*

Note 6-2: LVDS Signal Waveform



AC Characteristics

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	200	KHz	



Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min	Typ	Max	Unit	Remark
Tv	Vertical Section	Period	1452	1481	8192	Th	
Tdisp(v)		Active	1440	1440	1440	Th	
Tblk(v)		Blanking	12	41	6752	Th	
Fv		Frequency	30	120	145	Hz	***Note 6-3***
Th	Horizontal Section	Period	359	360	1023	Tclk	
Tdisp(h)		Active	320	320	320	Tclk	
Tblk(h)		Blanking	39	40	703	Tclk	
Fh		Frequency	69.7	177.7	250.6	KHz	***Note 6-4***
Tclk	LVDS Clock	Period	11.1	15.6	39.9	ns	1/Fclk
Fclk		Frequency	25	64	90	MHz	***Note 6-5***

Note 6-3: The optimized setting is 119~145 Hz to driving for good picture quality.

Note 6-4: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th ((Min.);

Fh (Typ.)= Fclk (Typ.) / Th (Typ.);

Fh (Max.)= Fclk (Max.) / Th (Min.);

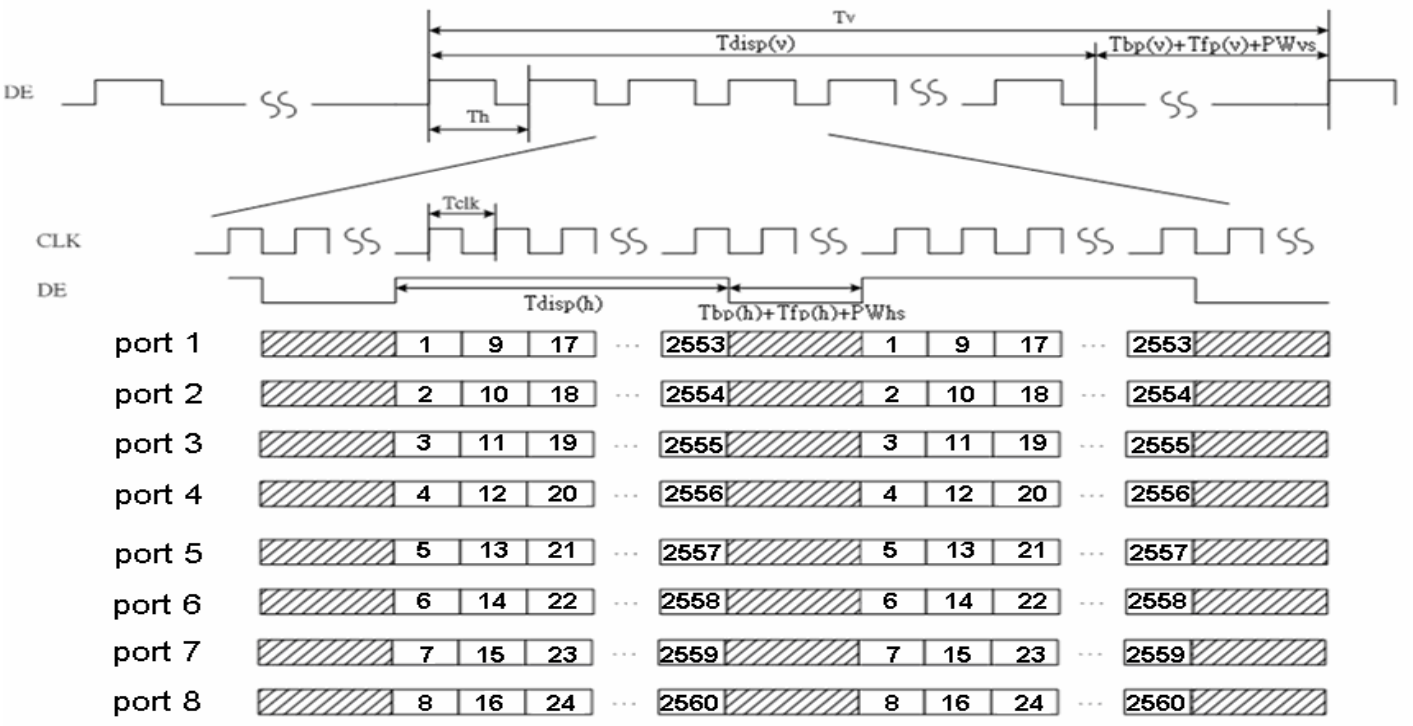
Note 6-5: The equation is listed as following. Please don't exceed the above recommended value.

Fclk (Min.) = Fv (Min.) x Th ((Min.) x Tv (Min.);

Fclk (Typ.) = Fv (Typ.) x Th ((Typ.) x Tv (Typ.);

Fv x Th x Tv < Fclk (Max.)

Input Timing Diagram



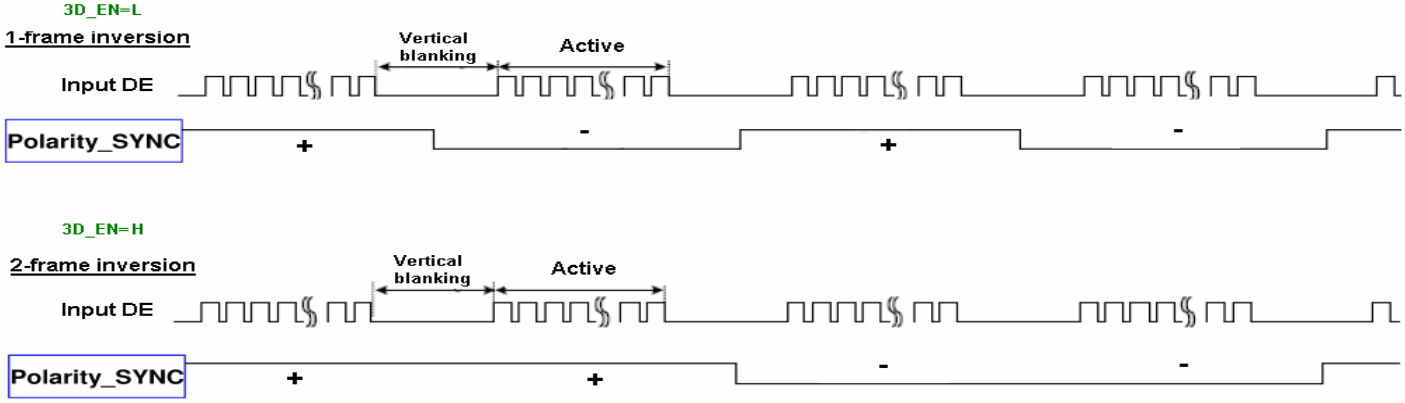
3D Control

3D Control I/O Characteristics

Pin#	Symbol	I/O	Buffer	Description	Remark
CN2_pin30	Polarity_SYNC	O	4mA	Frame Inversion polarity Index 3D_EN=L :1-frame inversion 3D_EN=H :2-frame inversion	***Note 6-6***
CN3_pin30	3D_EN	I	IPL*	3D enable control signal	

IPL:internal pull low

Note 6-6



Absolute Maximum Rating

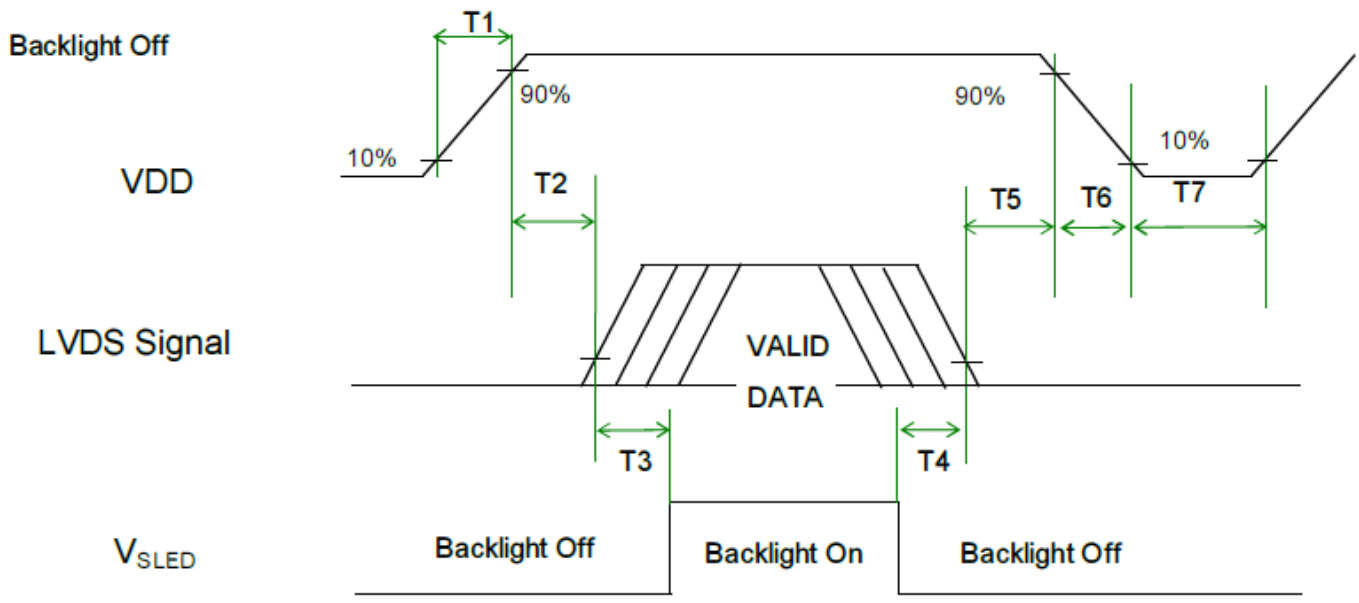
Symbol	Description	Min	Max	Unit	Remark
3D_EN	3D enable control singnal	GND-0.3	5.0	[Volt]	Ta=25

Recommended Operating Condition

Symbol	Parameter	Condition	Rating			Unit
			Min	Typ	Max	
V_{TH}	Input High Voltage	-	2.0	-	3.6	[V]
V_{TL}	Input Low Voltage	-	0	-	0.8	[V]
V_{OH}	Output High Voltage	I_{OH}=4mA	2.4	-	3.4	[V]
V_{OL}	Output Low Voltage	I_{OL}=-4mA	0	-	0.4	[V]

Power ON/OFF Sequence

VDD power, LVDS signal and backlight on/off sequence are as follows. LVDS signals from any system shall be Hi-Z state when VDD is off.



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	50	[ms]	
T3	500	-	-	[ms]	

T4	100	-	-	[ms]	
T5	0		50	[ms]	*Note 6-7* *Note 6-8*
T6	0	-	150	[ms]	*Note 6-8*
T7	1000	-	-	[ms]	

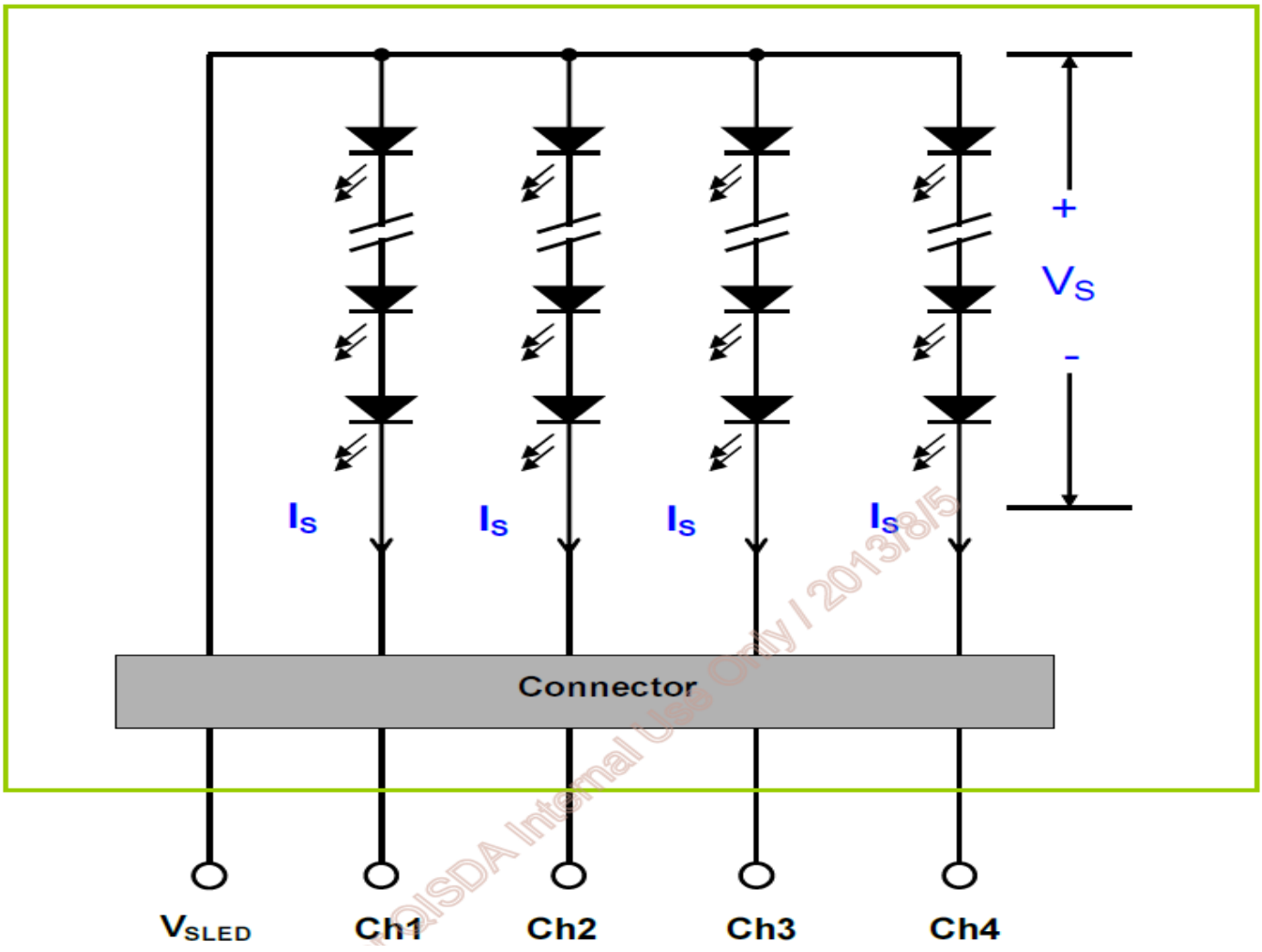
Note 6-7 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note 6-8 : During T5 and T6 period, please keep the level of input LVDS signals with Hi-Z state.

Backlight Unit

Block Diagram

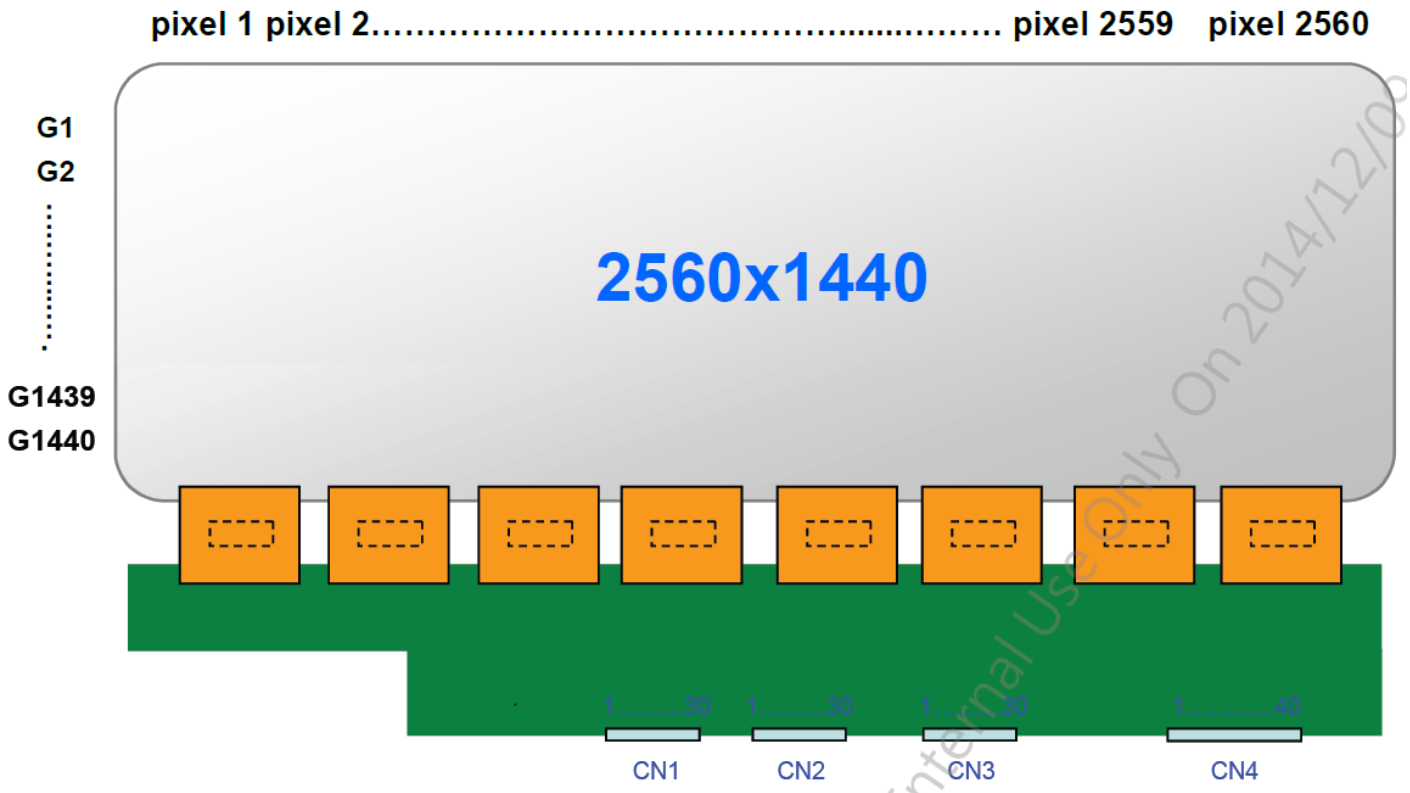
The following shows the block diagram of the 27 inch Backlight Unit. And it includes 72 pcs LED in the LED light bar. (4 strings and 18 pcs LED of one string).



7. Connector & Pin Assignment

TFT LCD Module

TFT-LCD Connector	**Manufacturer**	STM	Starconn
	Part Number	MSCKT2407P30HB (CN1 / CN2 / CN3)	115F40-R000RA-M3 (CN4)
Mating Connector	**Manufacturer**	STM or compatible	JAE or compatible
	Part Number	PK2407P30V	FI-NX40HL



Connector on Backlight Unit.

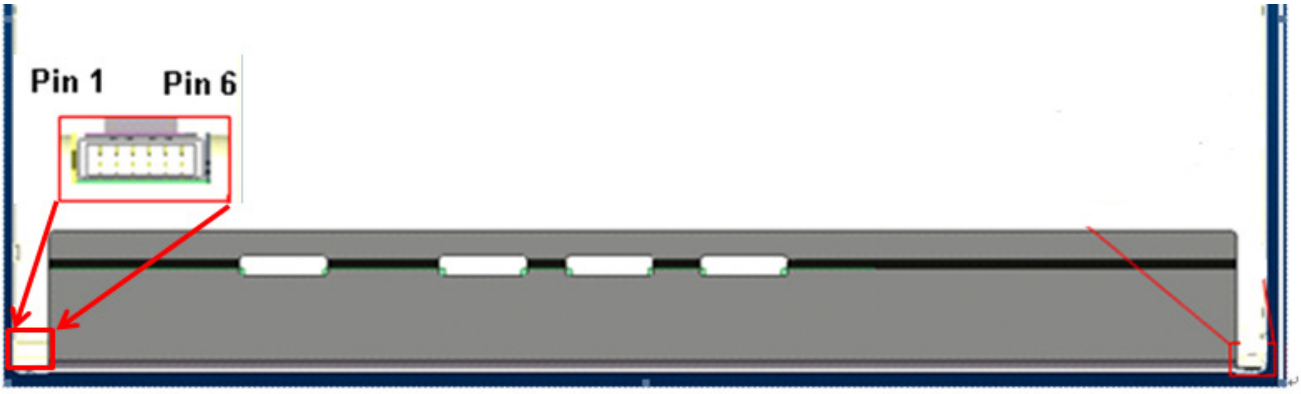
This connector is mounted on LED light-bar.

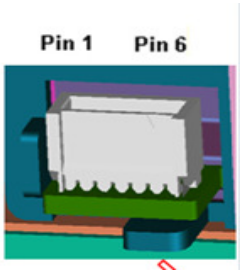
Backlight Connector	**Manufacturer**	CVILUX
	Part Number	CI1406M1VL0-NH
Mating Connector	**Manufacturer**	ENTERY
	Part Number	H112K-P06N-00B (Non-Locking type) H112K-P06N-11B(White) (Lockingtype) H112K-P06N-13B(Black) (Lockingtype)

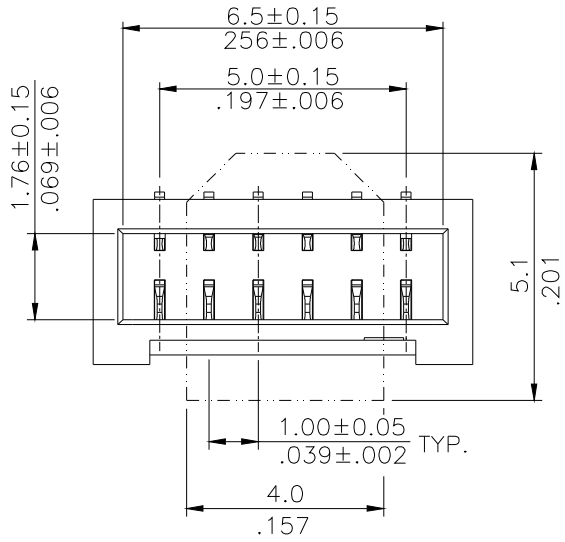
Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

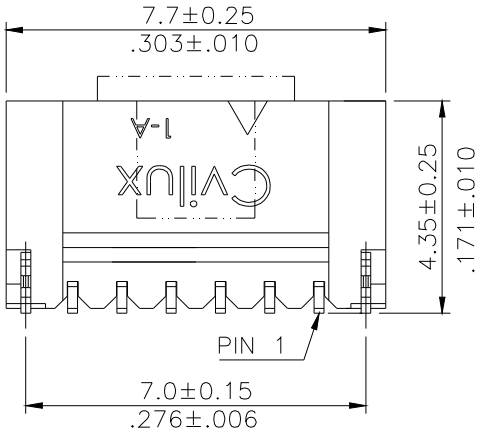
LED connector Pin assignment

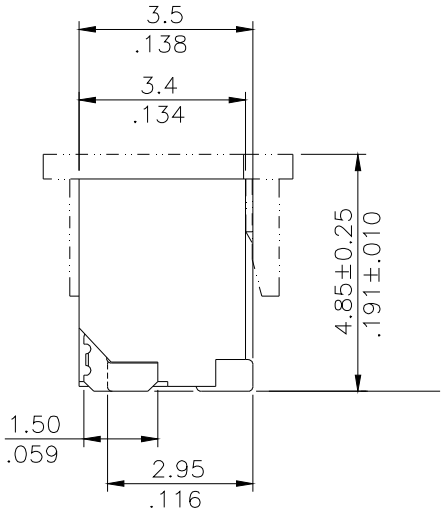
Pin no.	Signal name
1	IRLED (current out)
2	IRLED (current out)
3	VLED (voltage in)
4	VLED (voltage in)
5	IRLED (current out)
6	IRLED (current out)











Connector Pin Assignment

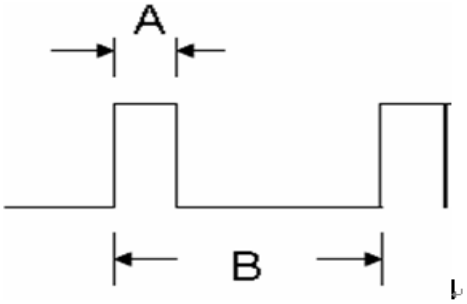
Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	

Electrical Characteristics

Absolute Maximum Rating

Parameter damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
Is	LED String Current	0	150	[mA]	*100% duty ratio*
			210	[mA]	*Duty ratio 10%* *Pulse time=10ms*



Duty ratio= (A / B) X 100% ; (A: Pulse time, B: Period)

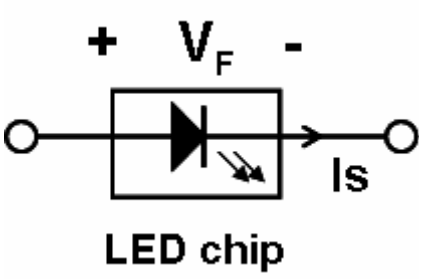
Parameter guideline for LED driving is under stable conditions at 25℃ (Room Temperature):

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
IR_{LED}	LED Operation Current	-	120	132	[mA]	Operating with fixed driving current
V_{LB}	Light Bar Operation Voltage (for reference)	53.1	56.7	60.3	[Volt] Note 7-1 Note 7-5	
ΔVs	Maximum Vs Voltage Deviation of light bar	-	-	3.6	[Volt] Note 7-2	
P_{BLU}	BLU Power consumption (for reference)		27.3	29.0	[Watt] Note 7-3	
LT_{LED}	LED life Time (Typical)	30,000		-	[Hour] Note 7-4	

Note 7-1: Vs (Typ.) = VF (Typ.) X LED No. (one string);

a. V_F: LED chip forward voltage, V_F (Min.)=2.95V, V_F(Typ.)=3.15V, V_F(Max.)=3.35V

b. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F(Max.);



Note 7-2: ΔVs (Max.) = ΔVF X LED No. (one string);

a. ΔVF: LED chip forward voltage deviation; (0.2 V , each Bin of LED VF)

Note 7-3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 4 ; (4 is total String No. of LED Light bar)

P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 4 ;

Note 7-4: Definition of life time:

a. Brightness of LED becomes to 50% of its original value

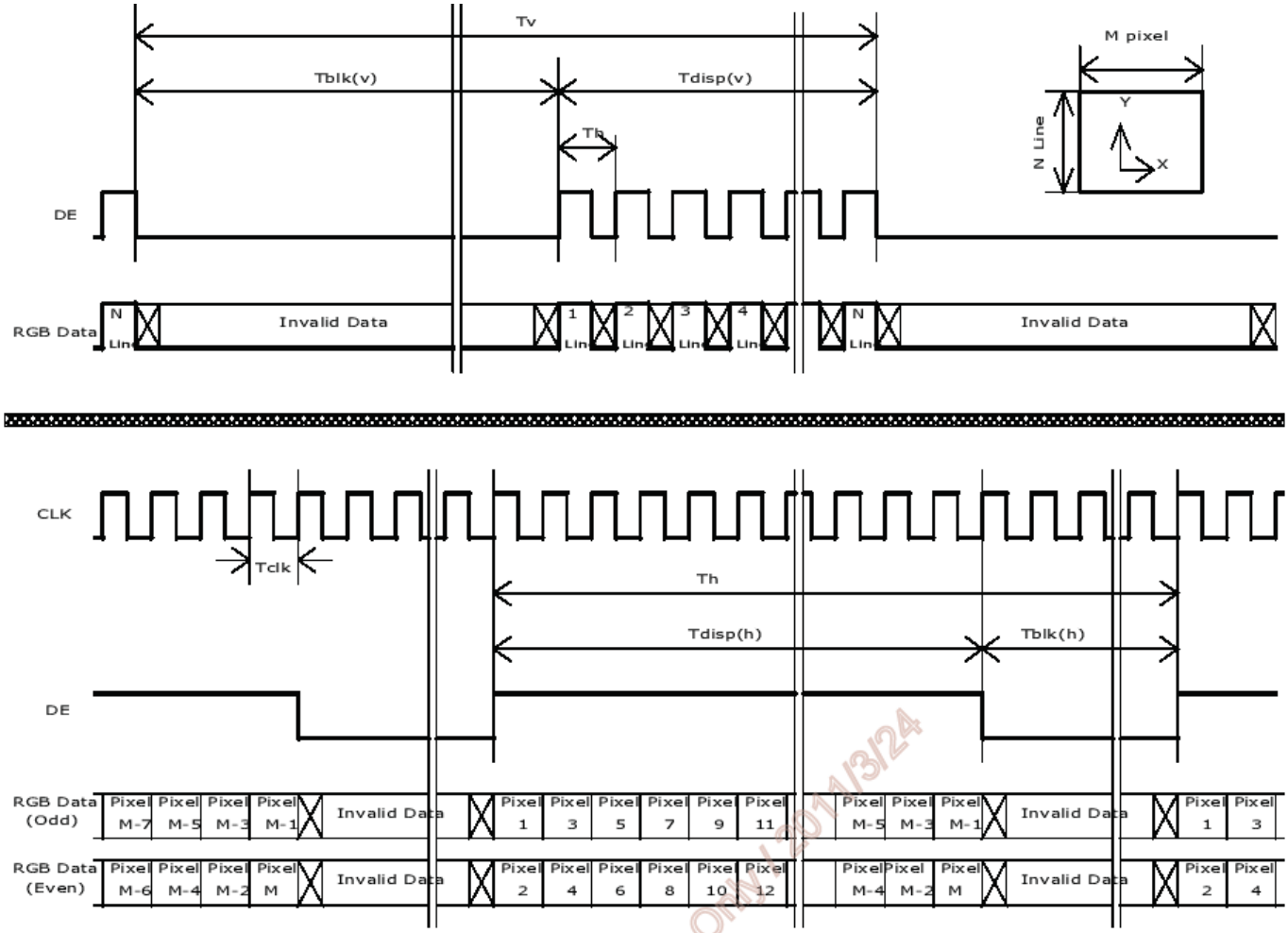
b. Test condition: Is = 120mA and 25℃(Room Temperature)

Note 7-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

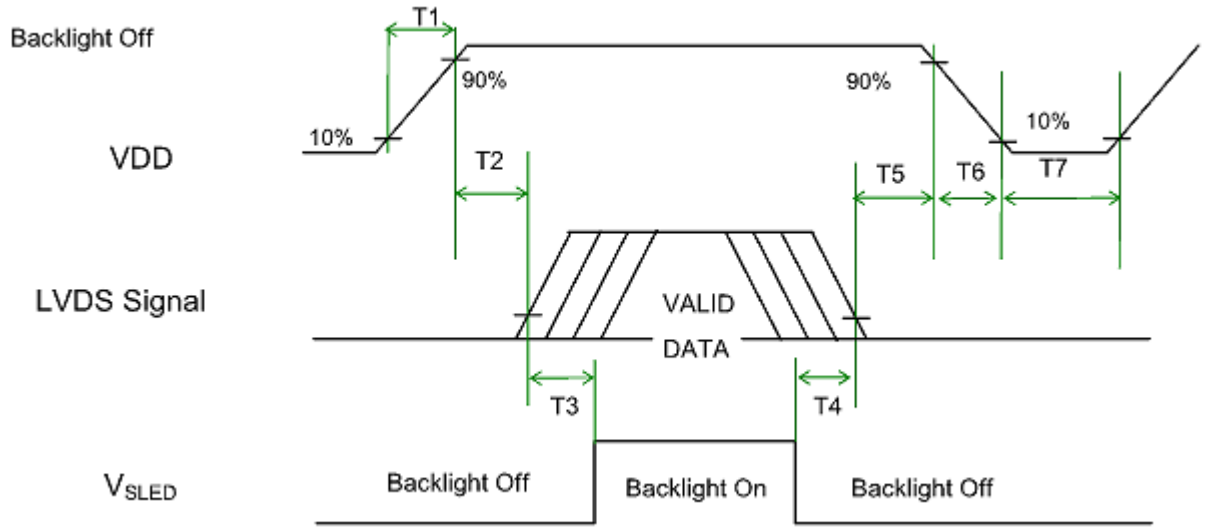
Note 7-6: AUO strongly recommend “Analog Dimming” method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency.

Timing diagram



Power ON/OFF Sequence

VDD power, LVDS signal and backlight on/off sequence are as follows. LVDS signals from any system shall be Hi-Z state when VDD is off.



Parameter	Value		Unit
	Min.	Max.	
T1	0.5	10	[ms]
T2	0	50	[ms]
T3	500	-	[ms]
T4	100	-	[ms]
T5	0	50	[ms]
T6	0	150	[ms]
T7	1000	-	[ms]

Note1 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note2 : During T5 and T6 period , please keep the level of input LVDS signals with Hi-Z state.

8. Reliability Test

Environment test conditions are listed as following Monitor test condition.

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	***Note 8-1***
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	***Note 8-2***
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

Note 8-1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note8- 2: According to EN61000-4-2 , ESD class B: Certain performance degradation allowed:

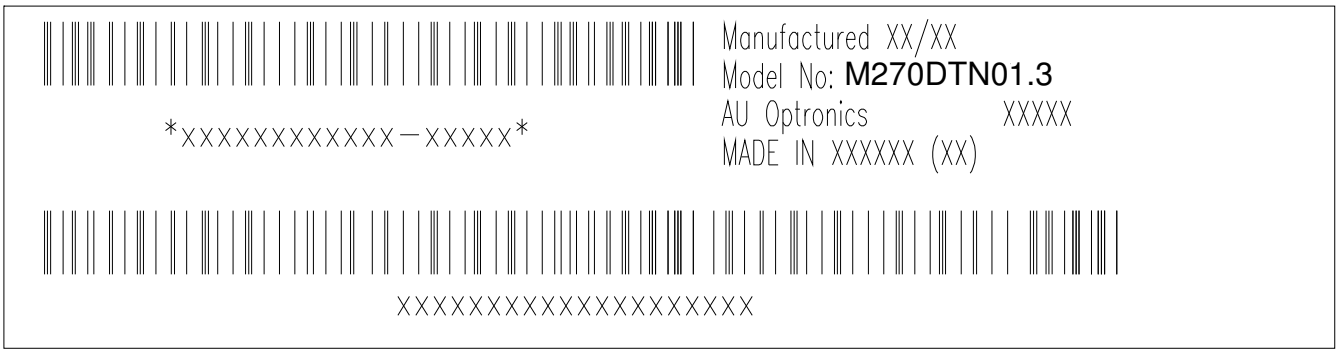
No data lost.

Self-recoverable.

No hardware failures.\

9. Shipping label

The label is on the panel as shown below:



Note 6-1: For Pb Free products, AUO will add for identification.

Note 6-2: For RoHS compatible products, AUO will add for identification.

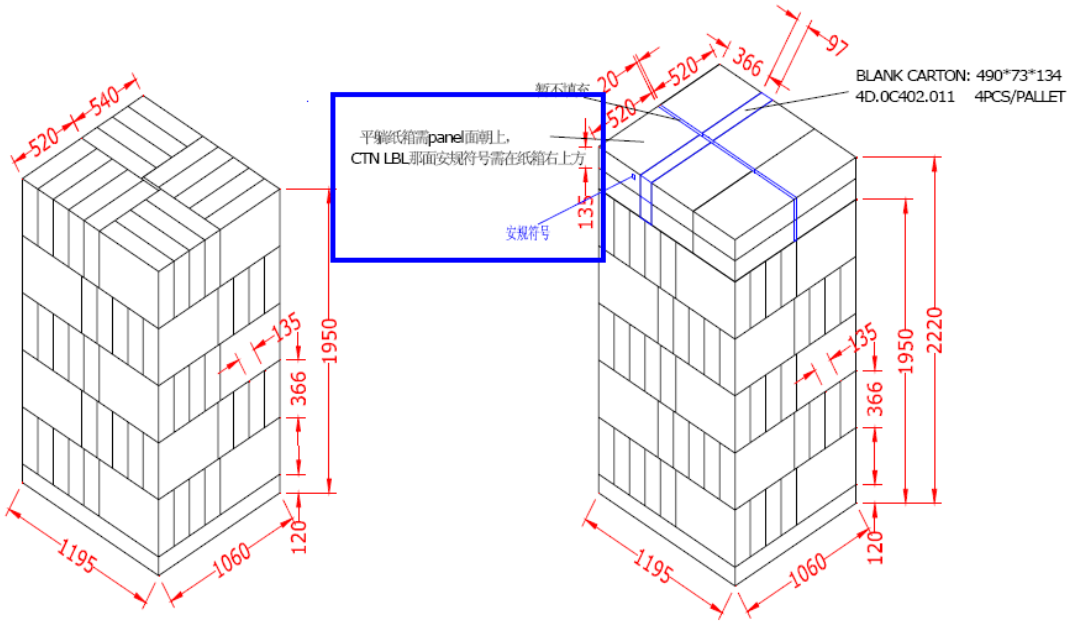
Note 6-3: For China RoHS compatible products, AUO will add for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

10. Packing Precautions

TFT-LCD Module (or monitor) should be stand or be placed face up in traffic or storage conditions; please do not keep TFT-LCD Module face down (polarizer side down).

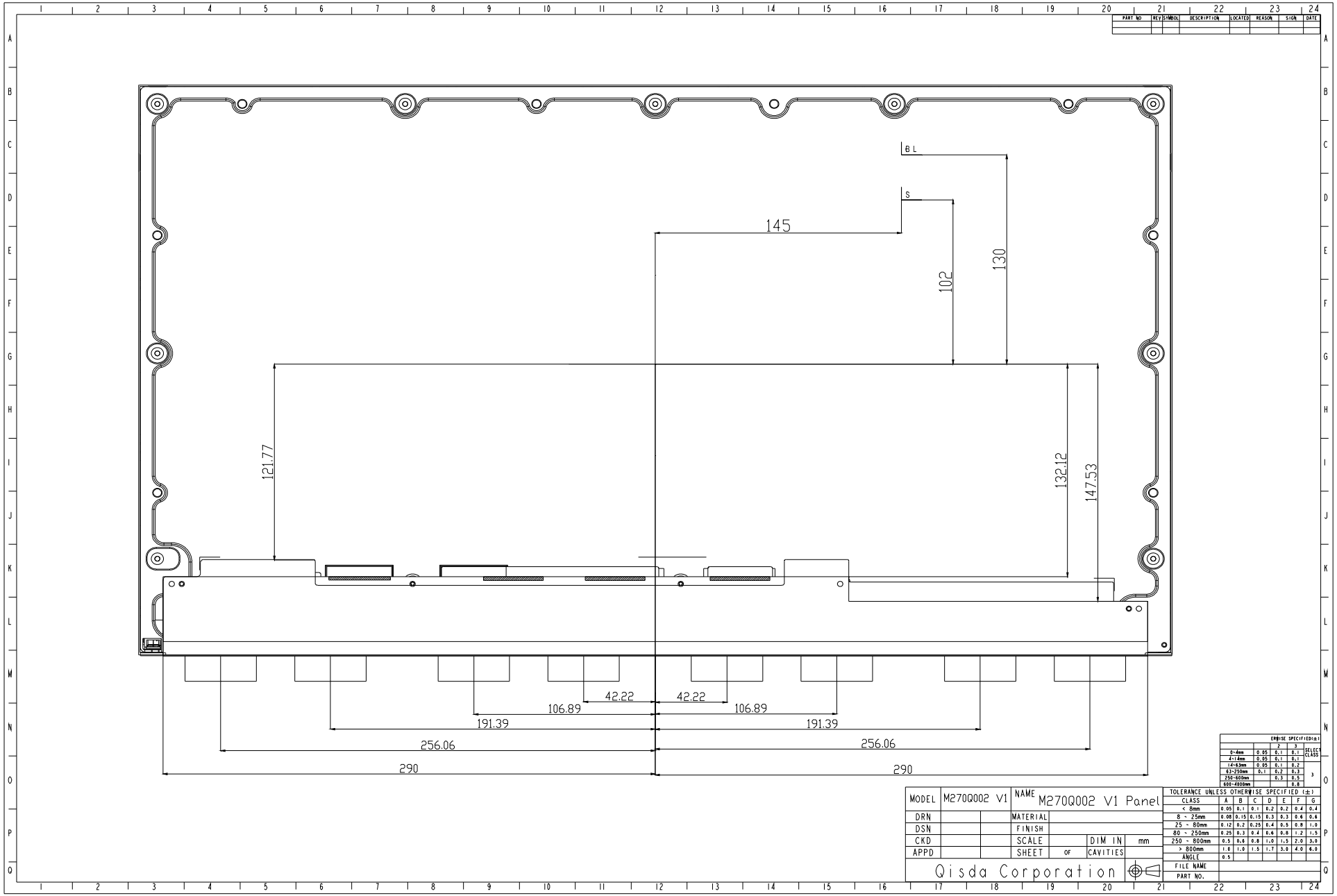
Monitor maker should add the notice above in packing description; See the configuration example as below:



栈板尺寸参照： 1199*1061*120

18*5+12=102 PCS


608.8±0.5 (OUTLINE)
596.74±0.5(ACTIVE AREA)
304.4
298.37
354.81±0.5 (OUTLINE)
335.66±0.5 (ACTIVE AREA)
173.33
167.83
9.99±0.5
11.45
14.58
MODEL M270Q002 V1
NAME M270Q002 V1 Panel
DRN
DSN
CKD
APPD
MATERIAL
FINISH
SCALE
SHEET OF
DIM IN mm
CAVITIES
Qisda Corporation
TOLERANCE UNLESS OTHERWISE SPECIFIED (±)
FILE NAME
PART NO.



PART NO	REV	SYMBOL	DESCRIPTION	LOCATED	REASON	SIGN	DATE

MODEL	M270Q002 V1	NAME	M270Q002 V1 Panel
DRN		MATERIAL	
DSN		FINISH	
CKD		SCALE	DIM IN mm
APPD		SHEET	OF CAVITIES
Qisda Corporation			

TOLERANCE UNLESS OTHERWISE SPECIFIED (±)							
CLASS	A	B	C	D	E	F	G
< 8mm	0.05	0.1	0.1	0.2	0.2	0.4	0.4
8 ~ 25mm	0.08	0.15	0.15	0.3	0.3	0.6	0.6
25 ~ 80mm	0.12	0.2	0.25	0.4	0.5	0.8	1.0
80 ~ 250mm	0.25	0.3	0.4	0.6	0.8	1.2	1.5
250 ~ 800mm	0.5	0.6	0.8	1.0	1.5	2.0	3.0
> 800mm	1.0	1.0	1.5	1.7	3.0	4.0	6.0
ANGLE	0.5						
FILE NAME							
PART NO.							

EMPISE SPECIFIED(±)				
		2	3	
0~4mm	0.05	0.1	0.1	SELECT CLASS
4~14mm	0.05	0.1	0.1	
14~63mm	0.05	0.1	0.2	
63~250mm	0.1	0.2	0.3	3
250~600mm		0.3	0.5	
600~4000mm			0.8	