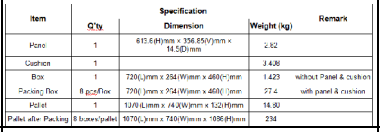
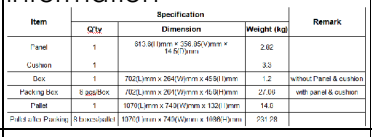
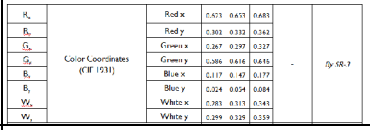
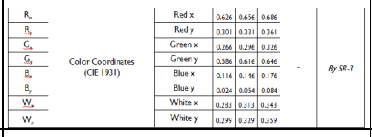
( ) Preliminary Specification
(V) Final Specification

Module	**27.0" Color TFT-LCD**
Model Name	**M270QAN02.0**

Customer	Date	Approved by	Date
		Howard Lee	Feb 16, 2017
Approved by		**Prepared by**	**Date**
		ShinYu Lin	Feb 14, 2017
Note: This Specification is subject to change without notice.		AU Optronics corporation	

Contents

Record of Revision

Version	Date	Page	Old description	New Description	Remark
0.1	2016/4/21	All			
0.2	2016/9/13	21	Follow as VESA DisplayPort Standard Version 1.2	Follow as VESA DisplayPort Standard Version 1.1	
	2016/9/13	35	-	Add bezel open specfication	
0.3	2016/9/13	22	-	Add item d for intra-pair skew Add item e for inter-pair skew	
		39	Old pallet and shipment information 	New pallet and shipment information 	
		40	-	Add system design guide	
0.4	2016/10/21	33	-	Add note5-3 evaluation criteria	
0.5	2017/1/17	7	Original color coordinates 	New color coordinates 	
		14	-	Add starconn connector	
1.0	2017/2/14	7	-	Delete minimum of sRGB coverage ratio	

1 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
12) Please avoid touching COF position while you are doing mechanical design.
13) When storing modules as spares for a long time, the following precaution is necessary:
Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

2 General Description

This specification applies to the 27.0 inch wide Color a-Si TFT-LCD Module M270QAN02.0. The display supports the UHD - 3840(H) x 2160(V) screen format and 1.07B colors (RGB 8bits + Hi-FRC). The input interface is 8-lanes eDP and this module doesn't contain an driver board for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	684 (26.93")
Active Area	[mm]	596.16 (H) x 335.34 (V)
Pixels H x V	-	3840x3(RGB) x 2160
Pixel Pitch	[um]	155.25 (per one triad) × 155.25
Pixel Arrangement	-	R.G.B. Vertical Stripe
Display Mode	-	AHVA Mode (Advanced Hyper-Viewing Angle), Normally Black
White Luminance (Center)	[cd/m^2]	300 (Typ.)
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	12 (Typ., Gray to Gray)
Power Consumption (LCD Module + Backligh unit)	[Watt]	Total = 30.2 W(Typ.) LCD module : PDD (Typ.)=10.8W @ white pattern, 60Hz, 12 V Backlight unit : PBLU (Typ.) =19.4 W @ Is=90mA
Weight	[Grams]	2820 (Typ.)
Outline Dimension	[mm]	613.6 (H) x 356.85 (V) × 14.5 (D) (Typ.)
Electrical Interface	-	8-lanes eDP , 10bits RGB data input (RGB 8bits + Hi-FRC)
Support Color	-	1.07B colors (8bit+Hi-FRC)
Surface Treatment	-	Anti-Glare, 3H
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance
TCO Compliance	-	TCO 7.0 Compliance

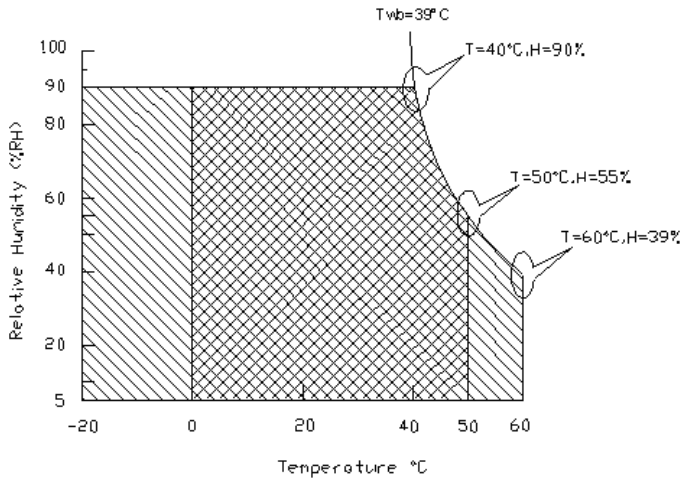
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	***Note 2-1***
TGS	Glass surface temperature (operation)	0	+65	[°C]	***Note 2-1*** *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	***Note 2-1***
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta ≦39℃)
2. Max wet-bulb temperature at 39℃ or less. (Ta ≦39℃)
3. No condensation



Operating Range Storage Range +

2.3 Optical Characteristics

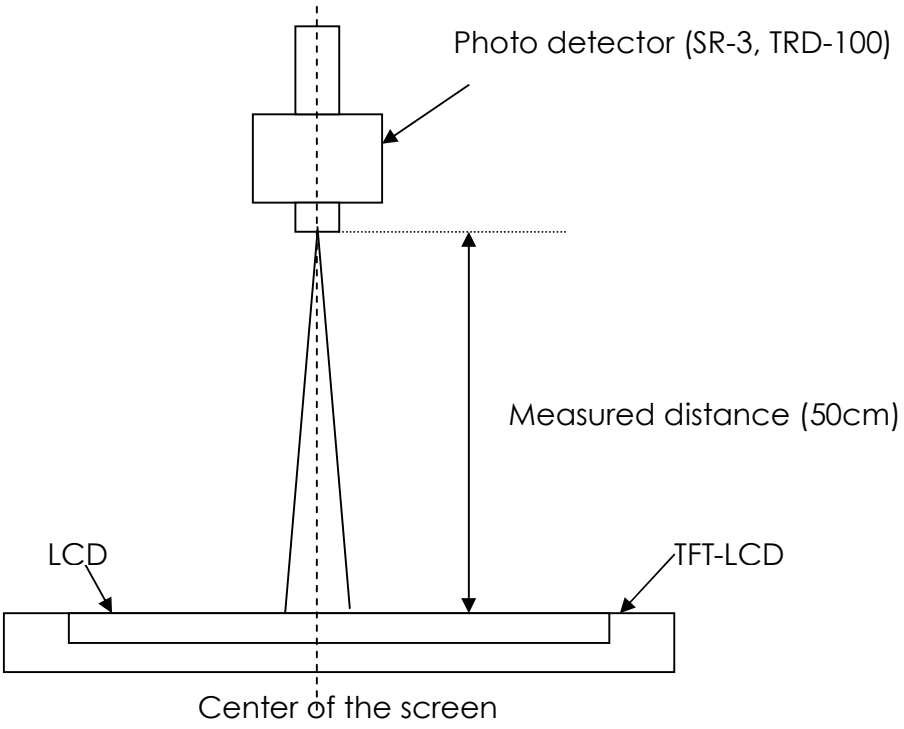
The optical characteristics are measured on the following test condition.

Test Condition:

1. Equipment setup: Please refer to ***Note 2-2***.
2. Panel Lighting time: 30 minutes
3. VDD=12.0V, Fv=60Hz, Is=90mA, Ta=25℃

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_w	White Luminance (Center of screen)		240	300	-	[cd/m2]	***Note 2-2*** *By SR-3*
L_{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	***Note 2-3*** *By SR-3*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	***Note 2-4*** *By SR-3*
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	***Note 2-5*** *By SR-3*
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	75	89	-		
Φ_L		Down	75	89	-		
T_{GTG}	Response Time	Gray to Gray	-	12	-	[msec]	***Note 2-6*** *By TRD-100*
R_x	Color Coordinates (CIE 1931)	Red x	0.626	0.656	0.686	-	*By SR-3*
R_y		Red y	0.301	0.331	0.361		
G_x		Green x	0.266	0.296	0.326		
G_y		Green y	0.586	0.616	0.646		
B_x		Blue x	0.116	0.146	0.176		
B_y		Blue y	0.024	0.054	0.084		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
sRGB coverage ratio			-	100		[%]	*By SR-3*
CT	Crosstalk		-	-	1.5	[%]	***Note 2-7*** *By SR-3*
F_{dB}	Flicker (Center of screen)		-	-	-20	[dB]	***Note 2-8*** *By SR-3*

Note 2-2: Equipment setup:

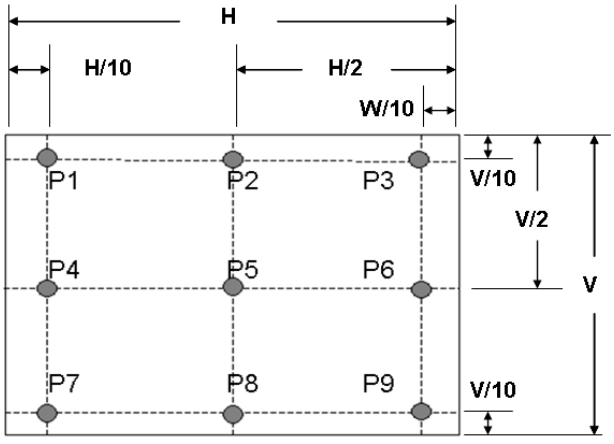


Note 2-3: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformity} = \frac{\text{Minimum Luminance of 9 Points (P1} \sim \text{P9)}}{\text{Maximum Luminance of 9 Points (P1} \sim \text{P9)}}$$

a. Test pattern: White Pattern



Note 2-4: Contrast Ratio Measurement

Definition:

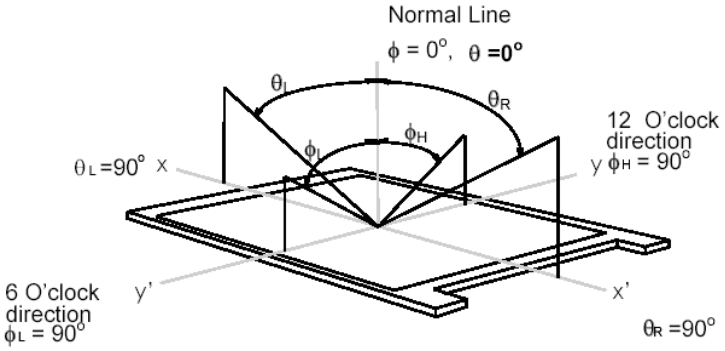
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen (Θ=Φ=0°)

Note 2-5: Viewing angle measurement

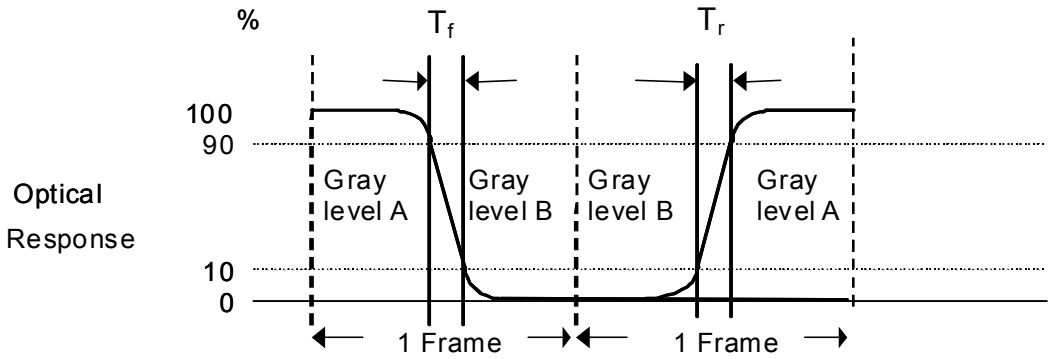
Definition: The angle at which the contrast ratio is greater than 10 & 5 .

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)



Note 2-6: Response time measurement

The output signals of photo detector are measured when the input signals are changed from "Gray level A" to "Gray level B" (falling time, T_f), and from "Gray level B" to "Gray level A" (rising time, T_r), respectively. The response time is interval between the 10% and 90% of optical response.



The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L255	L511	L767	L1023
Start gray level	L0					
	L255					
	L511					
	L767					
	L1023					

- T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

Note 2-7: Crosstalk measurement

Definition:

CT = Max. (CT_H,CT_V);

Where

a. Maximum Horizontal Crosstalk:

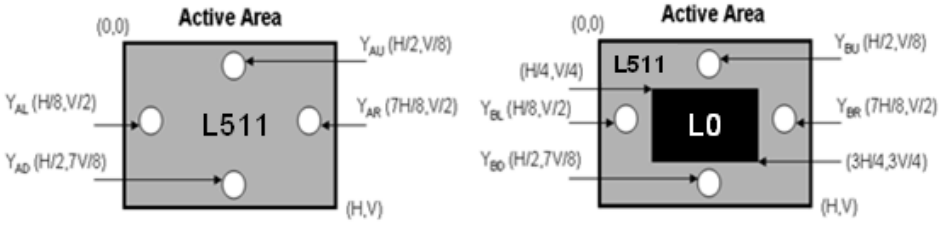
CT_H = Max. (| $Y_{BL} - Y_{AL}$ | / Y_{AL} × 100 %, | $Y_{BR} - Y_{AR}$ | / Y_{AR} × 100 %);

Maximum Vertical Crosstalk:

CT_V = Max. (| $Y_{BU} - Y_{AU}$ | / Y_{AU} × 100 %, | $Y_{BD} - Y_{AD}$ | / Y_{AD} × 100 %);

b. Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR} = Luminance of measured location without Black pattern

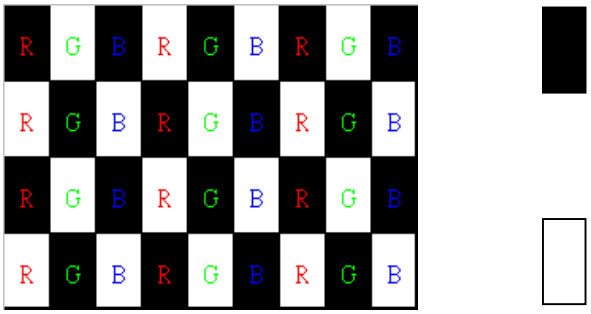
Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR} = Luminance of measured location with Black pattern



Note 2-8: Flicker measurement

a. Test pattern: It is listed as following.

Gray level = L0



R: Red, G: Green, B:Blue

b. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

2.4 Mechanical Characteristics

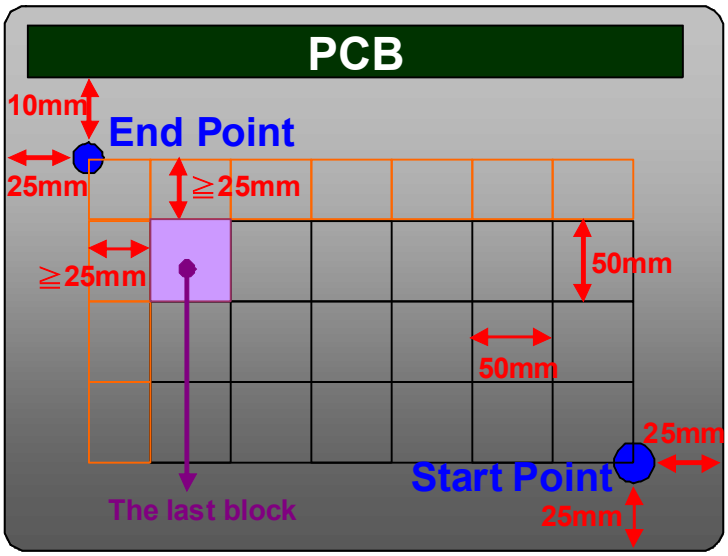
Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	***Note 2-9***

Note 2-9: Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

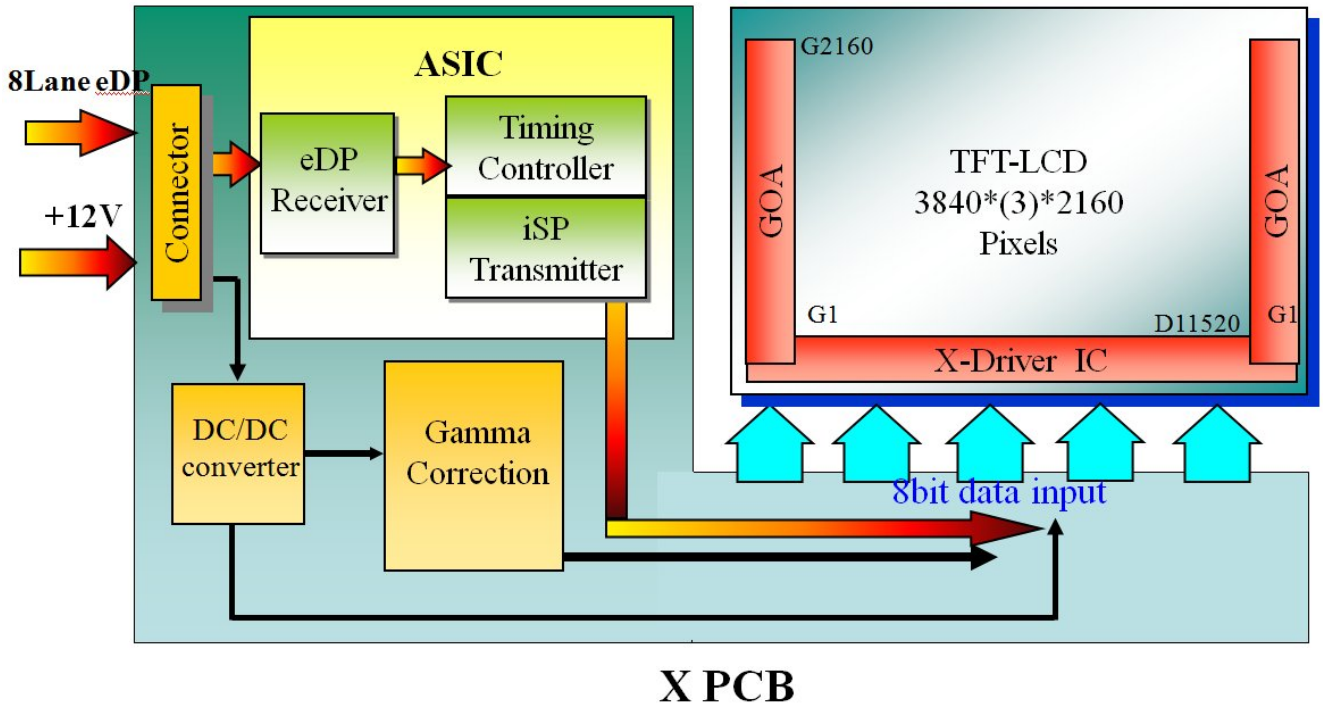
If the distance from the last block to each side of the End Point ≧ 25mm, add other blocks to make sure that most area of Bezel Back can be measured.



3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 27.0 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

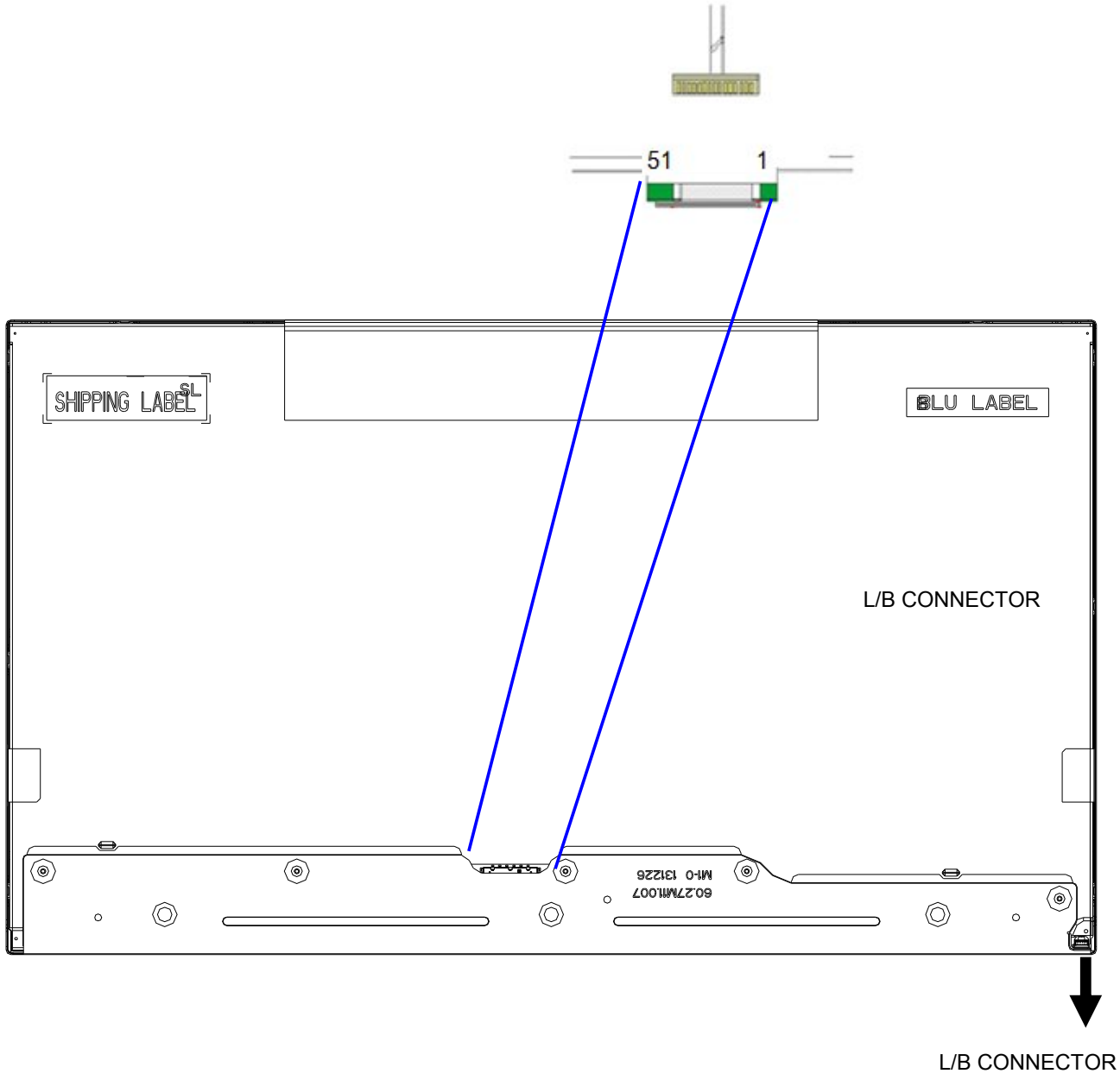
TFT-LCD Connector	Manufacturer	P-TWO	JAE	STARCONN
	Part Number	187059-5122	FI-RTE51SZ-HF	115E51-0000RA-M3-R
Mating Connector	Manufacturer	JAE		
	Part Number	FI-RE51CL		

3.2.2 Connector Pin Assignment

PIN #	Symbol	Description	Remark
1	VDD	Power +12V	
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	NC	No connection (for AUO test only. Do not connect)	
10	NC	No connection (for AUO test only. Do not connect)	
11	NC	No connection (for AUO test only. Do not connect)	
12	NC	No connection (for AUO test only. Do not connect)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	NC	No connection (for AUO test only. Do not connect)	
16	NC	No connection (for AUO test only. Do not connect)	
17	GND	Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	

20	GND	Ground	
21	1st Lane2_N	Negative eDP differential data input	
22	1st Lane2_P	Positive eDP differential data input	
23	GND	Ground	
24	1st Lane1_N	Negative eDP differential data input	
25	1st Lane1_P	Positive eDP differential data input	
26	GND	Ground	
27	1st Lane0_N	Negative eDP differential data input	
28	1st Lane0_P	Positive eDP differential data input	
29	GND	Ground	
30	1st AUX_CH_P	Positive AUX Channel differential data input	
31	1st AUX_CH_N	Negative AUX Channel differential data input	
32	GND	Ground	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	2nd Lane3_N	Negative eDP differential data input	
36	2nd Lane3_P	Positive eDP differential data input	
37	GND	Ground	
38	2nd Lane2_N	Negative eDP differential data input	
39	2nd Lane2_P	Positive eDP differential data input	
40	GND	Ground	
41	2nd Lane1_N	Negative eDP differential data input	
42	2nd Lane1_P	Positive eDP differential data input	
43	GND	Ground	
44	2nd Lane0_N	Negative eDP differential data input	
45	2nd Lane0_P	Positive eDP differential data input	
46	GND	Ground	
47	2nd AUX_CH_P	Positive AUX Channel differential data input	
48	2nd AUX_CH_N	Negative AUX Channel differential data input	

49	GND	Ground	
50	HPD	Hot plug detection	
51	GND	Ground	



Note 3-1: Input signals of port 1 to port 4 clocks shall be the same timing.

3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

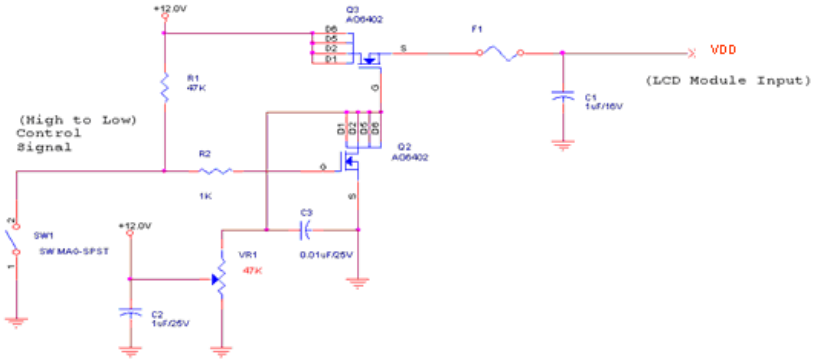
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25℃

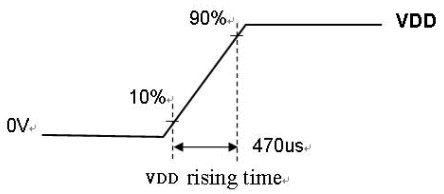
3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.9	1.08	[A]	VDD= 12.0V, White pattern, Fv=60Hz
PDD	VDD Power Consumption	-	10.8	12.96	[Watt]	VDD= 12.0V , White pattern, Fv=60Hz
IRush	Inrush Current	-	-	3.0	[A]	***Note 3-2***
VDDrp	Allowable VDD Ripple Voltage	-	-	VDD*5%	[mV]	VDD= 12.0V, White pattern, Fv=60Hz

Note 3-2: Inrush Current measurement:

Test circuit:



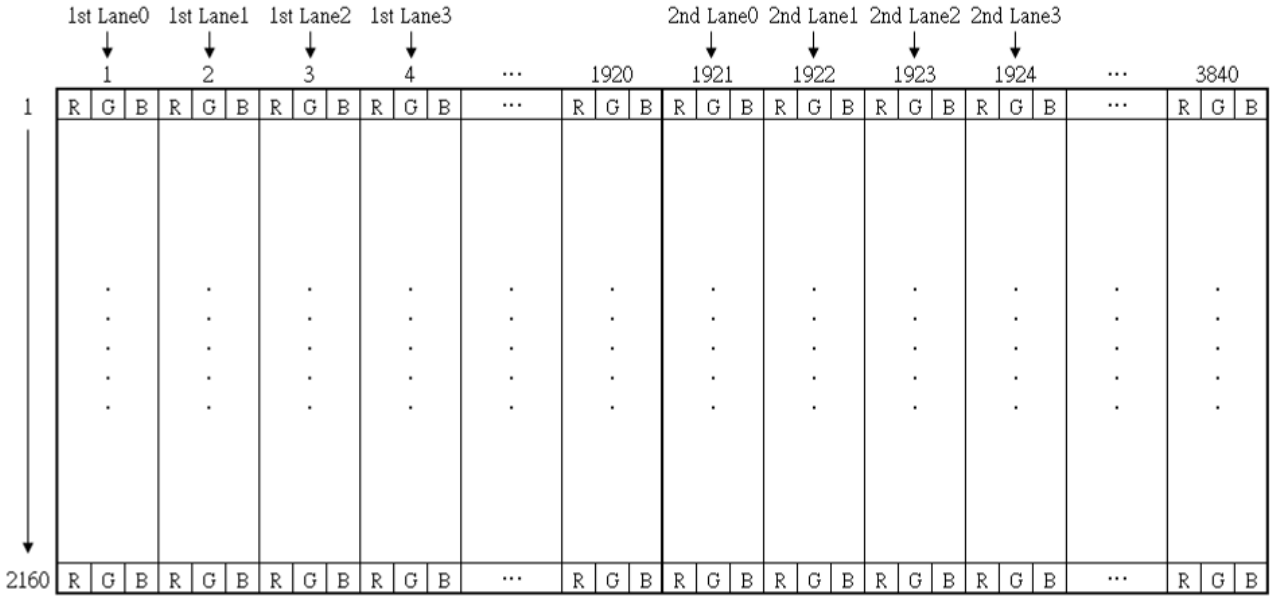


The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.



Note 3-3: The module use 8-Lanes eDP interface.

1st port:

1st Lane0：1+4n pixel

1st Lane1：2+4n pixel

1st Lane2：3+4n pixel

1st Lane3：4+4n pixel

2nd port:

2nd Lane0：1921+4n pixel

2nd Lane1：1922+4n pixel

2nd Lane2：1923+4n pixel

2nd Lane3：1924+4n pixel

n=0~479

3.4.2 eDP Data Format

1st Lane0	1st Lane1	1st Lane2	1st Lane3
R1-9:2	R2-9:2	R3-9:2	R4-9:2
R1-1:0IG1-9:4	R2-1:0IG2-9:4	R3-1:0IG3-9:4	R4-1:0IG4-9:4
G1-3:0IB1-9:6	G2-3:0IB2-9:6	G3-3:0IB3-9:6	G4-3:0IB4-9:6
B1-5:0IR5-9:8	B2-5:0IR6-9:8	B3-5:0IR7-9:8	B4-5:0IR8-9:8
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-9:2	G6-9:2	G7-9:2	G8-9:2
G5-1:0IB5-9:4	G6-1:0IB6-9:4	G7-1:0IB7-9:4	G8-1:0IB8-9:4
B5-3:0IR9-9:6	B6-3:0IR10-9:6	B7-3:0IR11-9:6	B8-3:0IR12-9:6
R9-5:0IG9-9:8	R10-5:0IG10-9:8	R11-5:0IG11-9:8	R12-5:0IG12-9:8
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-9:2	B10-9:2	B11-9:2	B12-9:2
B9-1:0IR13-9:4	B10-1:0IR14-9:4	B11-1:0IR15-9:4	B12-1:0IR16-9:4
R13-3:0IG13-9:6	R14-3:0IG14-9:6	R15-3:0IG15-9:6	R16-3:0IG16-9:6
G13-5:0IB13-9:8	G14-5:0IB14-9:8	G15-5:0IB15-9:8	G16-5:0IB16-9:8
B13-7:0	B14-7:0	B15-7:0	B16-7:0
.	.	.	.
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.	.	.	.

2nd Lane0	2nd Lane1	2nd Lane2	2nd Lane3
R1921-9:2	R1922-9:2	R1923-9:2	R1924-9:2
R1921-1:0IG1921-9:4	R1922-1:0IG1922-9:4	R1923-1:0IG1923-9:4	R1924-1:0IG1924-9:4
G1921-3:0IB1921-9:6	G1922-3:0IB1922-9:6	G1923-3:0IB1923-9:6	G1924-3:0IB1924-9:6
B1921-5:0IR1925-9:8	B1922-5:0IR1926-9:8	B1923-5:0IR1927-9:8	B1924-5:0IR1928-9:8
R1925-7:0	R1926-7:0	R1927-7:0	R1928-7:0
G1925-9:2	G1926-9:2	G1927-9:2	G1928-9:2
G1925-1:0IB1925-9:4	G1926-1:0IB1926-9:4	G1927-1:0IB1927-9:4	G1928-1:0IB1928-9:4
B1925-3:0IR1929-9:6	B1926-3:0IR1930-9:6	B1927-3:0IR1931-9:6	B1928-3:0IR1932-9:6
R1929-5:0IG1929-9:8	R1930-5:0IG1930-9:8	R1931-5:0IG1931-9:8	R1932-5:0IG1932-9:8
G1929-7:0	G1930-7:0	G1931-7:0	G1932-7:0
B1929-9:2	B1930-9:2	B1931-9:2	B1932-9:2
B1929-1:0IR1933-9:4	B1930-1:0IR1934-9:4	B1931-1:0IR1935-9:4	B1932-1:0IR1936-9:4
R1933-3:0IG1933-9:6	R1934-3:0IG1934-9:6	R1935-3:0IG1935-9:6	R1936-3:0IG1936-9:6
G1933-5:0IB1933-9:8	G1934-5:0IB1934-9:8	G1935-5:0IB1935-9:8	G1936-5:0IB1936-9:8
B1933-7:0	B1934-7:0	B1935-7:0	B1936-7:0
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.

3.4.3 Color versus Input Data

The following table is for color versus input data (10bit). The higher the gray level, the brighter the color.

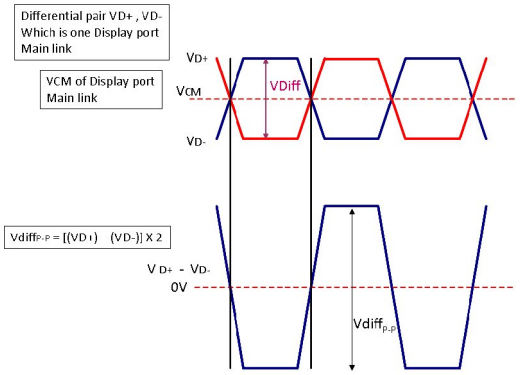
.

Color	Gary Level	Color Input Data																													Remark
		RED data (MSB:R9,LSB:R0)										GREEN data (MSB:G9,LSB:G0)										BLUE data (MSB:B9,LSB:B0)									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
L511	-	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	

3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.1)

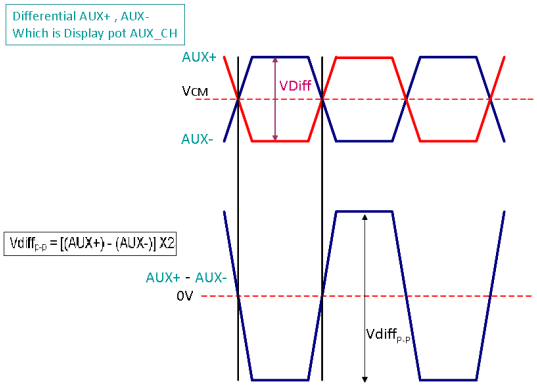
a. DisplayPort main link signal:

DisplayPort main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage	-	0	-	V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	150			mV



b. DisplayPort AUX_CH signal:

DisplayPort AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	2.0	V
$VDiff_{P-P}$	AUX Peak-to-peak voltage at a receiving device	0.27	-	1.36	V



c. DisplayPort VHPD signal:

DisplayPort VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	V

d. Intra-Pair skew

LRX-SKEW-INTRA_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTRA_PAIR	Lane Intra-pair Skew Tolerance	-	-	60	ps

e. Inter-Pair Skew

LRX-SKEW-INTER_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTER_PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	ps

3.4.5 Input Timing Specification

The input timing is shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	2180	2200	4500	Th	
Tdisp (v)		Active	2160	2160	2160	Th	
Tblk (v)		Blanking	20	40	2340	Th	
Fv		Frequency	29	60	65	Hz	***Note 3-6*** ***Note 3-7***
Th	Horizontal Section	Period	2000	2100	3520	Tclk	
Tdisp (h)		Active	1920	1920	1920	Tclk	
Tblk (h)		Blanking	80	180	1600	Tclk	
Fh		Frequency	40	132	151	kHz	***Note 3-4***
Tclk	Pixel Clock	Period	3.330	3.608	12.500	ns	1/Fclk
Fclk		Frequency	80	277	300.3	MHz	***Note 3-5***
Link Rate per Lane				2.7		Gbps	

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.)
Fh (Typ.) = Fclk (Typ.) / Th (Typ.)
Fh (Max.)= Fclk (Max.) / Th (Min.)

Note 3-5: The equation is listed as following. Please don't exceed the above recommended

value.

1st Lane N & 2nd Lane N skew < 200ns

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)

Fclk (Min.) ≦ Fv x Th x Tv ≦ Fclk (Max.)

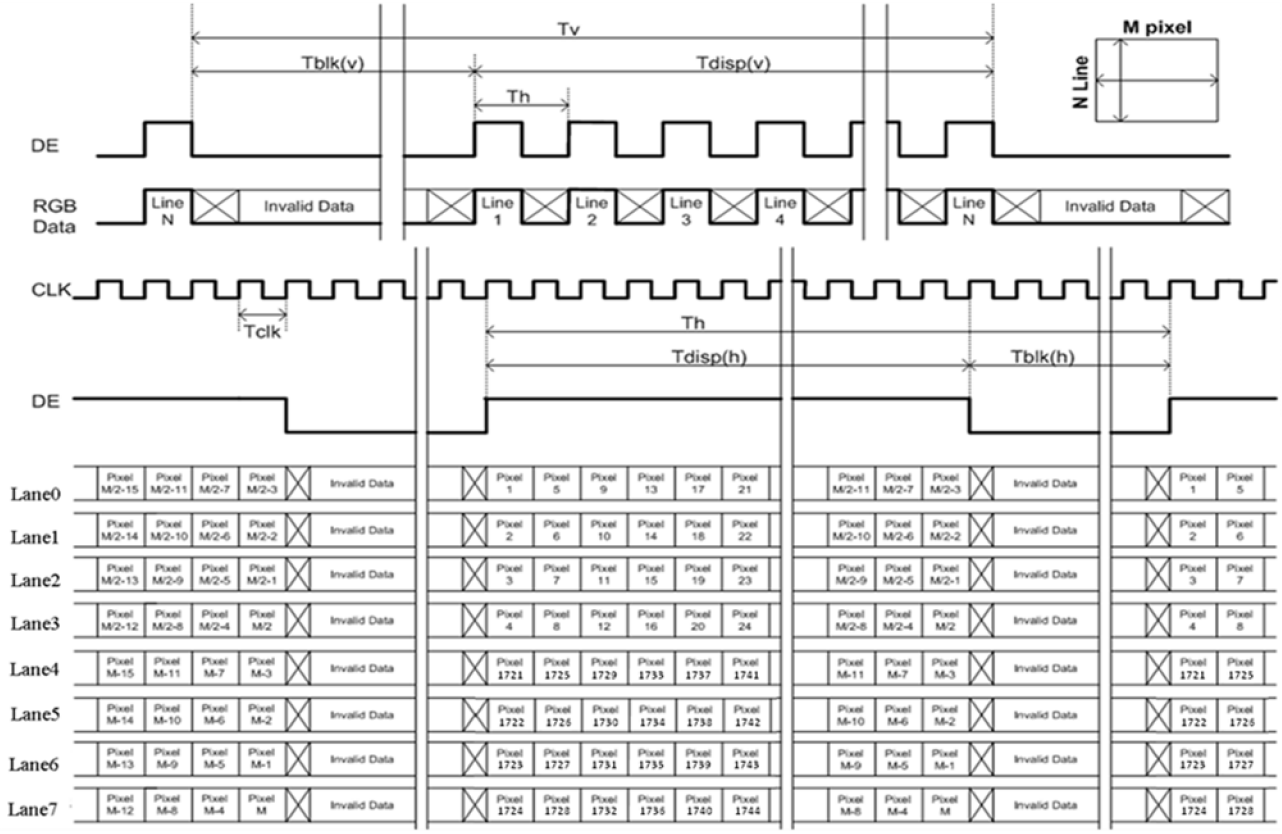
Note 3-6: The equation is listed as following. Please don't exceed the above recommended value.

Fv =Fclk(Typ.) / (Tv x Th)

Note 3-7: The optimal Vertical Frequency is 50~65 Hz for best picture quality.

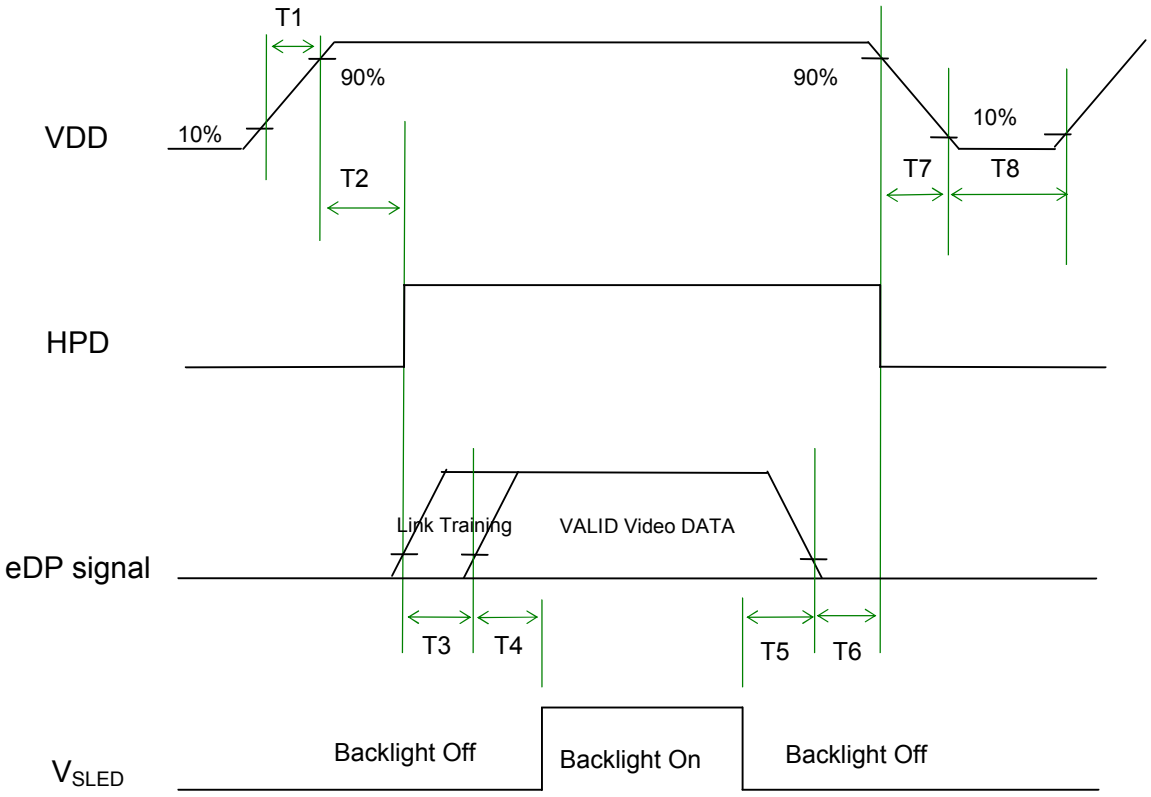
3.4.6 Input Timing Diagram

(Lane0~7 eDP data:1, 2, 3, 4, 1921, 1922, 1923, 1924)



3.5 Power ON/OFF Sequence

VDD power,eDP signal and backlight on/off sequence are as following. eDP signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

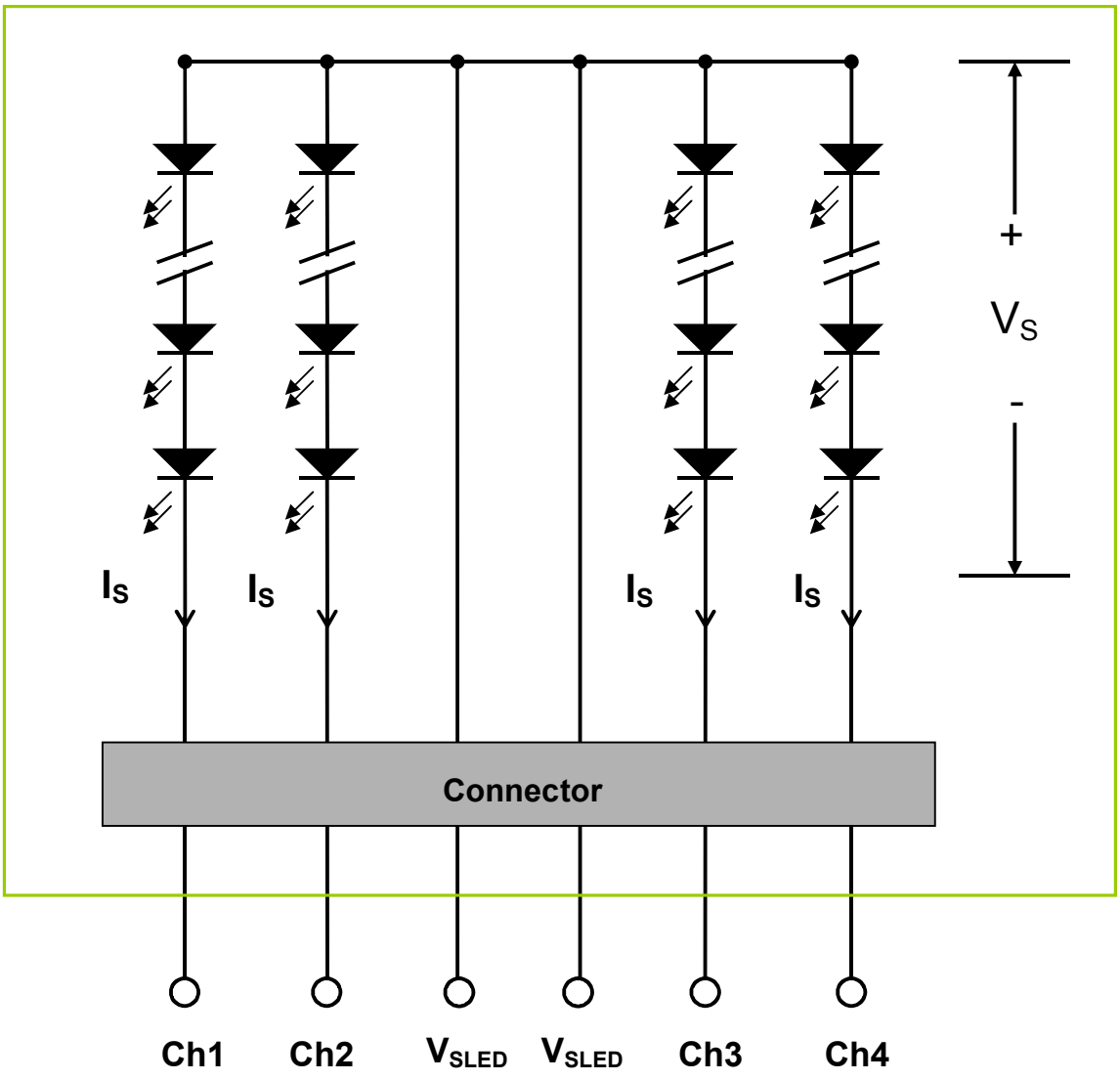
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	***Note 3-8***
T4	500	-	-	[ms]	
T5	100	-	-	[ms]	
T6	0		50	[ms]	***Note 3-9*** ***Note 3-10***
T7	0	-	200	[ms]	***Note 3-10*** ***Note 3-11***
T8	1000	-	-	[ms]	

Note 3-8: During T3 period , eDP link training time by customer's system.
Note 3-9: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.
Note 3-10: During T6 and T7 period , please keep the level of input eDP signals with Hi-Z state.
Note 3-11: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 27.0 inch Backlight Unit. Each LED light bar includes 72 pcs LED package. (4 strings and 18 pcs LED of one string).



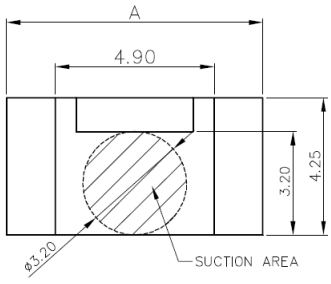
4.2 Interface Connection

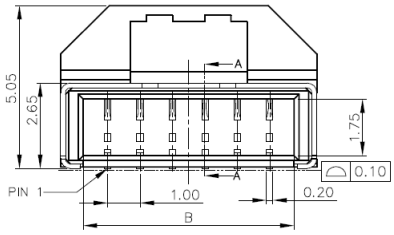
4.2.1 Connector Type

Backlight Connector	Manufacturer	ENTERY
	Part Number	3707K-S06N-07R
Mating Connector	Manufacturer	ENTERY
	Part Number	H112K-P06N-13B (Locked type)

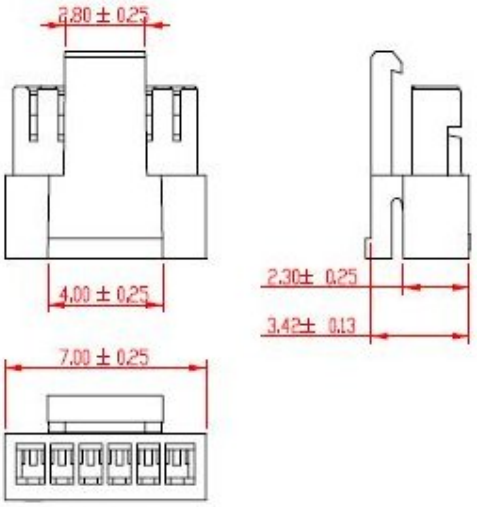
Backlight Connector dimension:

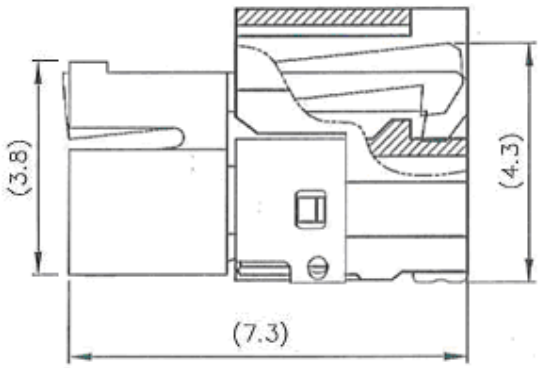
$H \times V \times D = 7.9 \times 5.05 \times 4.25, Pitch = 1.0(unit = mm)$





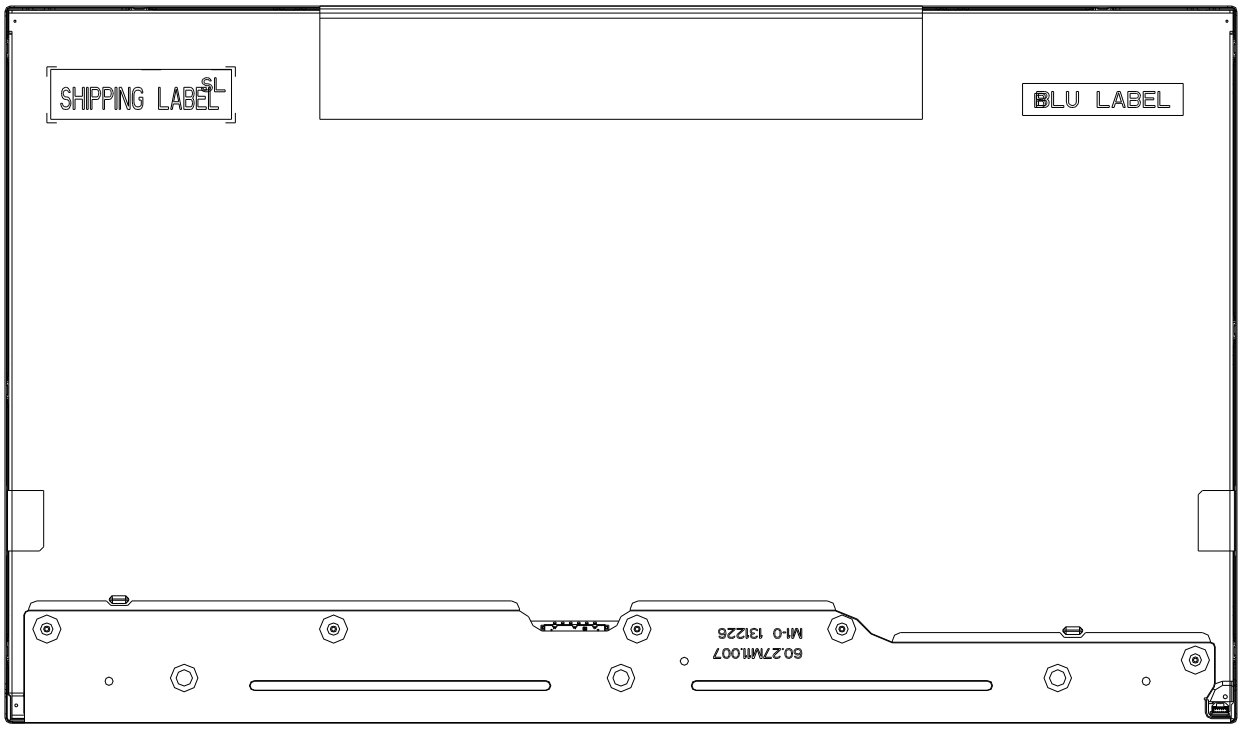
Mating Connector dimension:

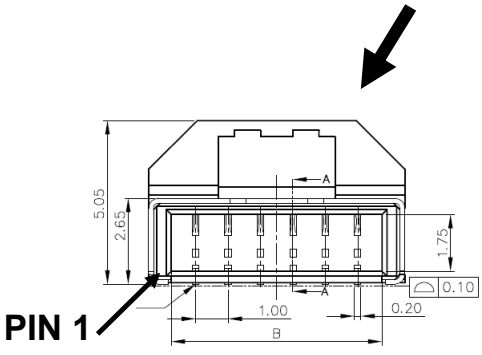




4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	





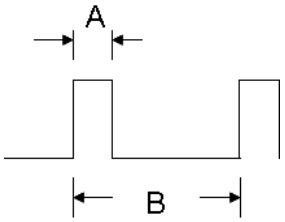
4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25℃)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	150	[mA]	100% duty ratio
			300	[mA]	Duty ratio≦ 10% Pulse time=10 ms



Duty ratio= (A / B) X 100% ; (A: Pulse time, B: Period)

4.3.2 Recommended Operating Condition

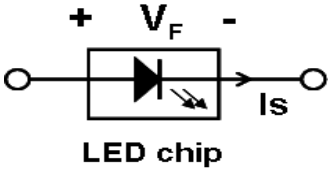
(Ta=25℃)

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
Is	LED String Current		90	99	[mA]	100% duty ratio of LED chip ***Note 4-7***
Vs	LED String Voltage	48.6	54	59.4	[Volt]	Is=90mA @ 100% duty ratio; ***Note 4-1&Note 4-5***
ΔVs	Maximum Vs Voltage Deviation of light bar			3.6	[Volt]	Is=90mA @ 100% duty ratio; ***Note 4-2***
P_{BLU}	LED Light Bar Power Consumption		19.4	21.4	[Watt]	***Note 4-3***
LT_{LED}	LED Life Time	30000			[Hour]	***Note 4-4***
OVP	Over Voltage Protection in system board	110% Vs(Max.)			[Volt]	***Note 4-5***

Note 4-1: Vs (Typ.) = V_F (Typ.) X LED No. (one string);

a. V_F: LED chip forward voltage, V_F (Min.)=2.7V, V_F(Typ.)=3.0V, V_F(Max.)=3.3V

b. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F(Max.);



Note 4-2: ΔVs (Max.) = ΔV_F X LED No. (one string);

a. ΔV_F: LED chip forward voltage deviation (0.2V , each Bin of LED V_F)

Note 4-3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 4 (4 is total String No. of BLU)

P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 4

Note 4-4: Definition of life time:

a. Brightness of LED becomes to 50% of its original value

b. Test condition: Is = 90mA and 25℃ (Room Temperature)

Note 4-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

Note 4-6: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency

Note 4-7 Ensure that the LED light bar is not subjected either forward or reverse voltage while monitor set is on standby mode or not in use.

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	***Note 5-1***
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	***Note 5-2***
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

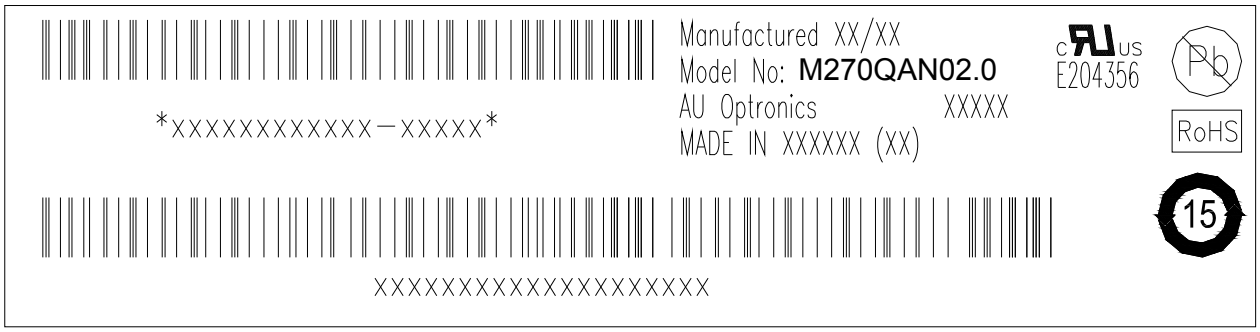
Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed
No data lost
Self-recoverable
No hardware failures.

Note5-3: Result Evaluation Criteria: TFT-LCD panels test should take place after gradually cooling enough at room temperature. In the normal application, there should be no particular problems that may affect the display function.

6 Shipping Label

The label is on the panel as shown below:



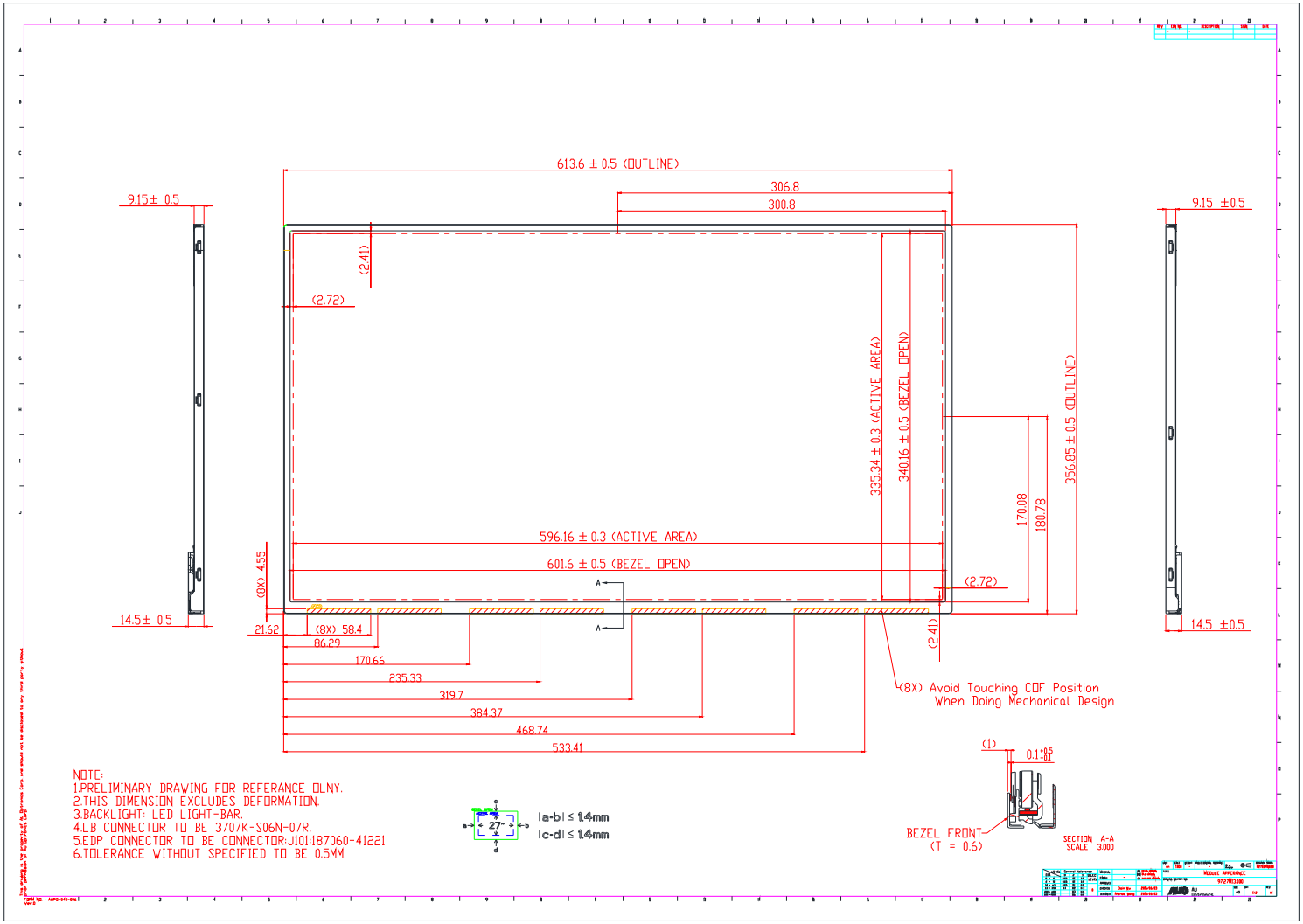
Note 6-1: For Pb Free products, AUO will add Pb for identification.

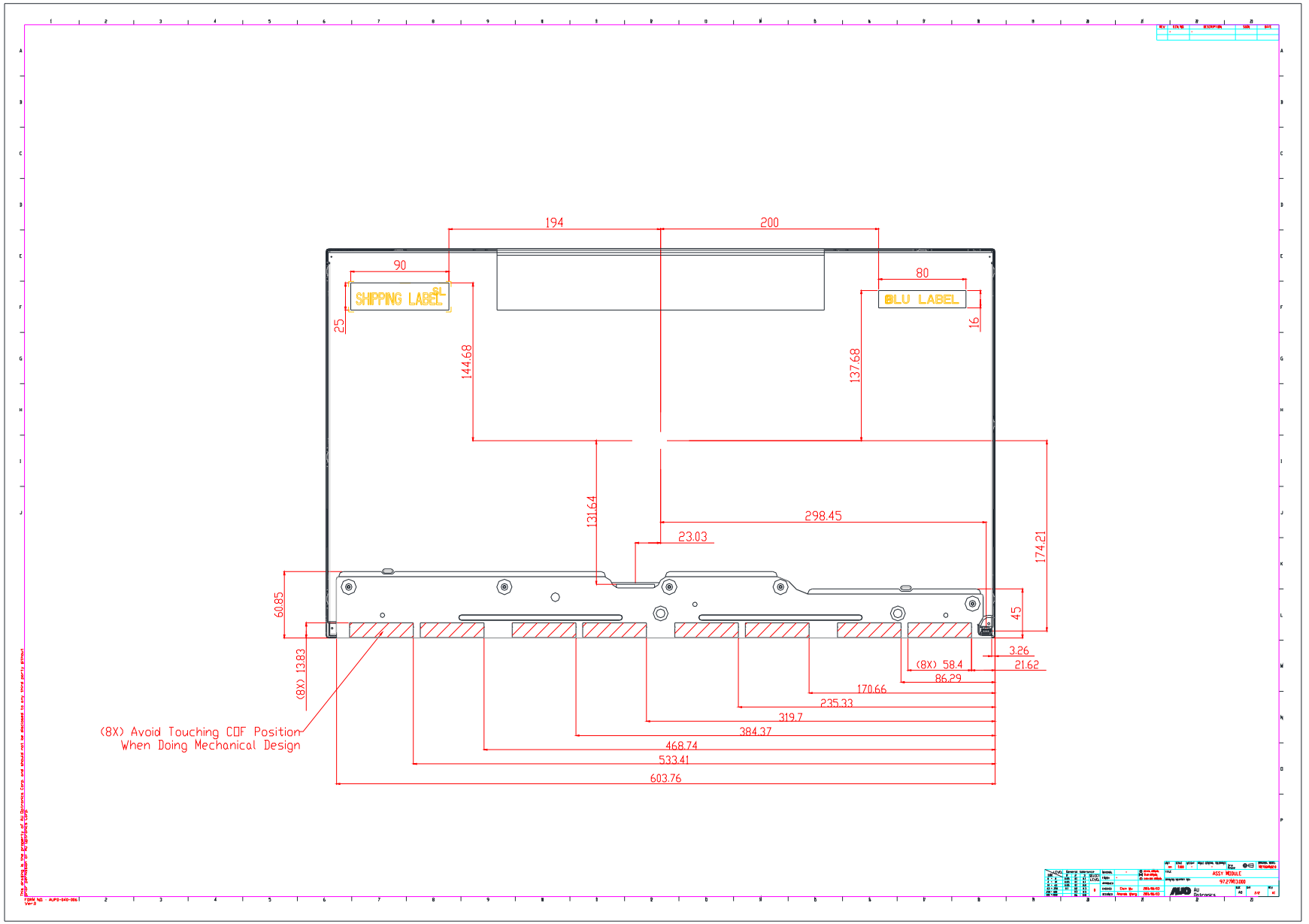
Note 6-2: For RoHS compatible products, AUO will add RoHS for identification.

Note 6-3: For China RoHS compatible products, AUO will add 15 for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

7 Mechanical Characteristics

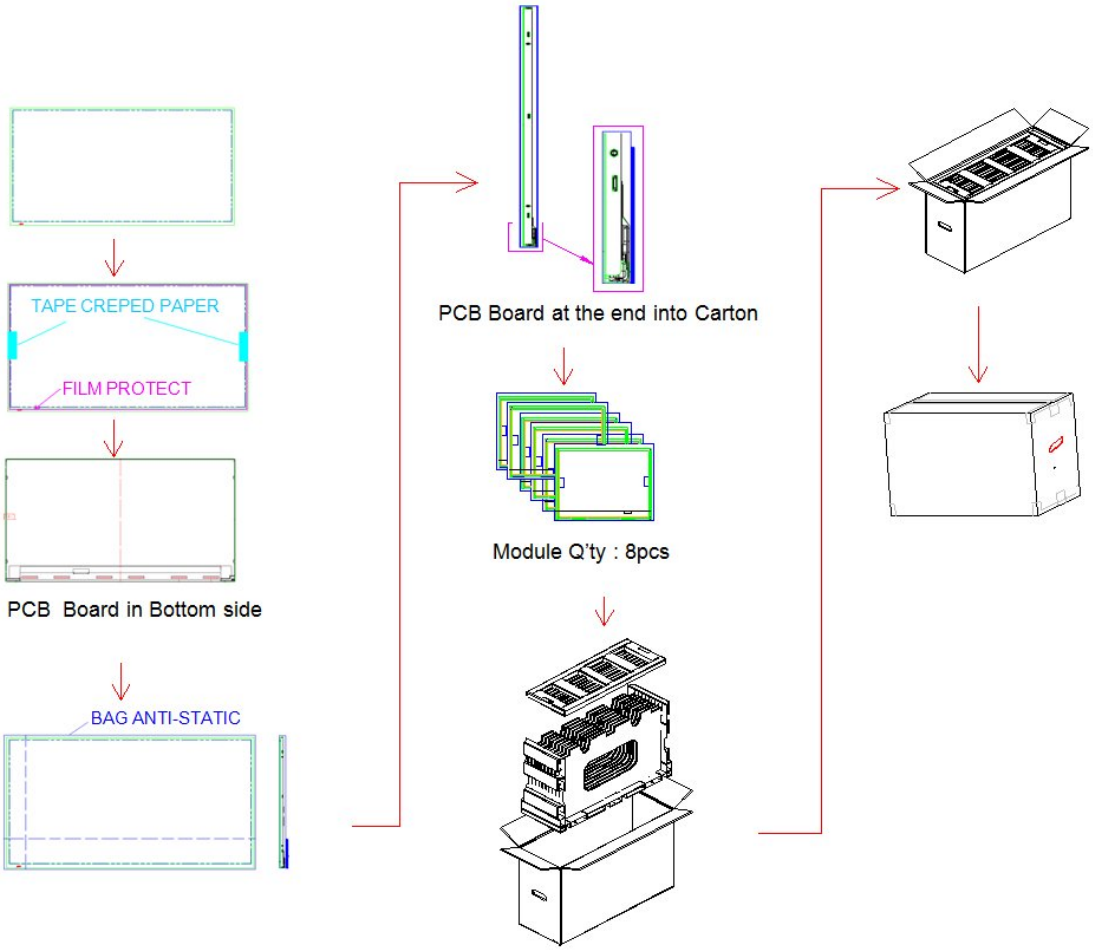


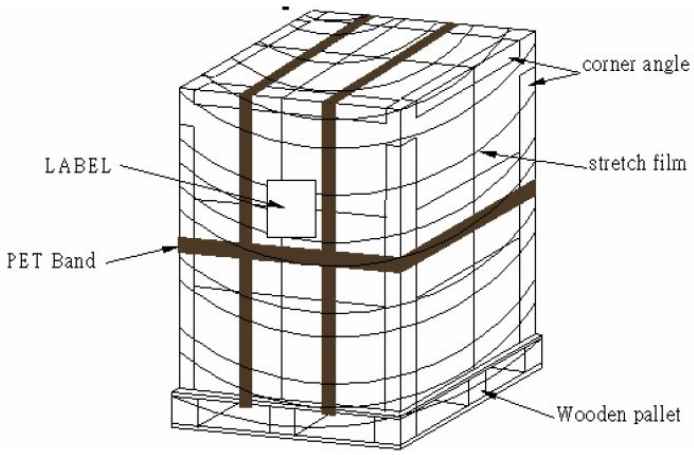

194
200
90
80
SHIPPING LABEL
BLU LABEL
25
16
144.68
137.68
131.64
298.45
23.03
174.21
60.85
45
3.26
21.62
(8X) 58.4
86.29
170.66
235.33
319.7
384.37
468.74
533.41
603.76
(8X) 13.83
(8X) Avoid Touching COF Position
When Doing Mechanical Design

Ver 0.3

8 Packing Specification

8.1 Packing Flow





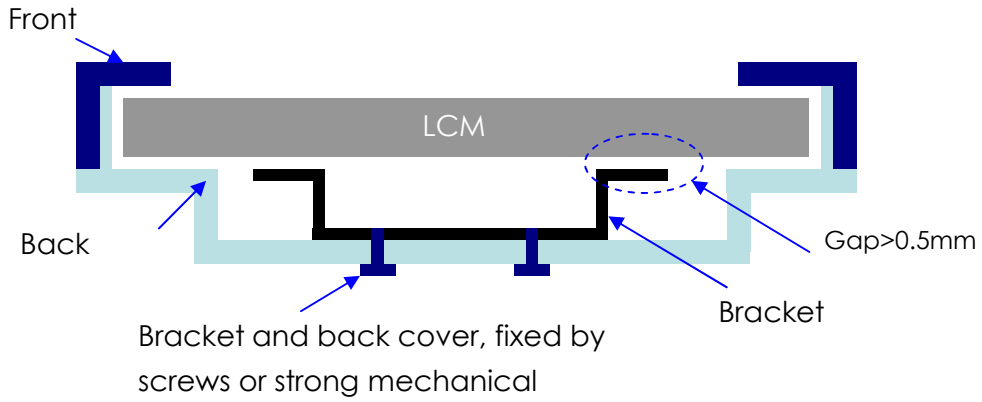
8.2 Pallet and Shipment Information

Item	Specification			Remark
	Q'ty	Dimension	Weight (kg)	
Panel	1	613.6(H)mm × 356.85(V)mm × 14.5(D)mm	2.82	
Cushion	1	-	3.3	
Box	1	702(L)mm x 264(W)mm x 456(H)mm	1.2	without Panel & cushion
Packing Box	8 pcs/Box	702(L)mm x 264(W)mm x 456(H)mm	27.06	with panel & cushion
Pallet	1	1070(L)mm x 740(W)mm x 132(H)mm	14.8	
Pallet after Packing	8 boxes/pallet	1070(L)mm x 740(W)mm x 1086(H)mm	231.28	

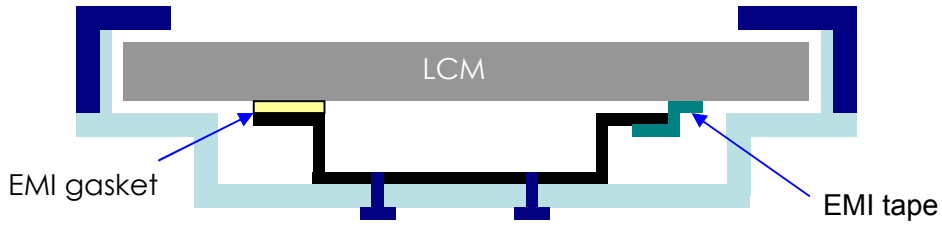
9 Design Guide for System

9.1 The gap between LCM and system rear bracket should be bigger than 0.5mm.

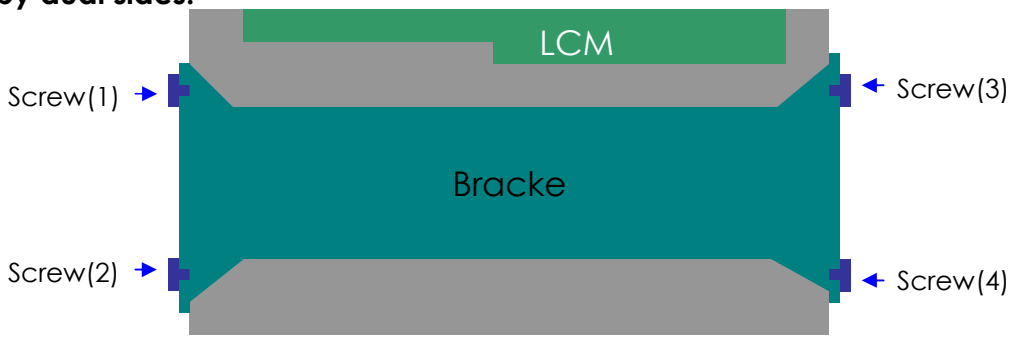
9.2 The system bracket should be fixed on back cover firmly.



9.3 The EMI gasket should be uniform and not push panel strongly.

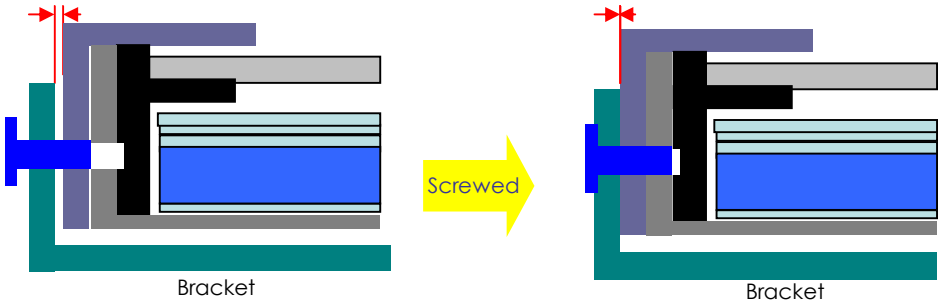


9.4 For stable assembly, the system bracket should use 4 screws to fix system and panel by dual sides.



9.5 The system bracket and panel should be in parallel with having no gap after inserting screws.

Proper and Parallel	0 gap and no mechanical damage



9.6 Avoid scratching LCM, the rib on system front-cover should not exceed the bottom edge of LCM's front-bezel.