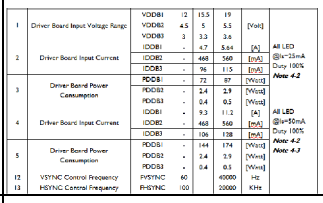
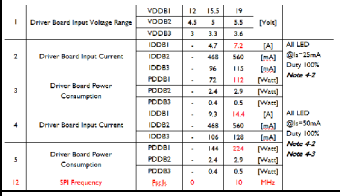
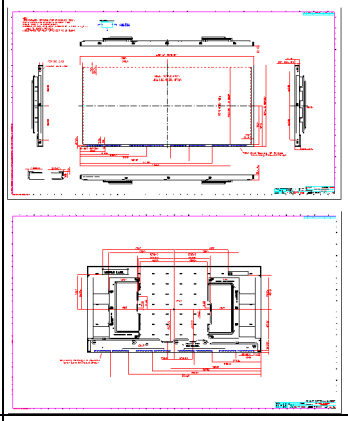
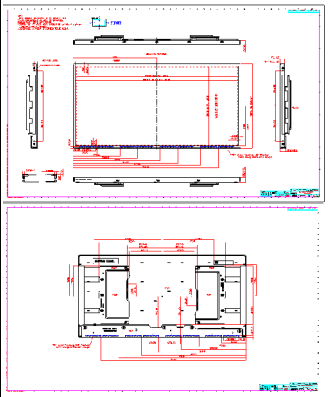
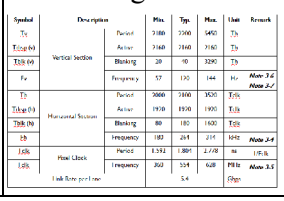
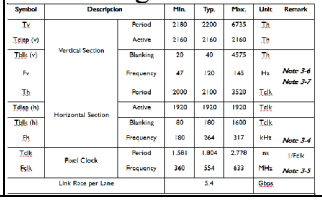
( ) Preliminary Specification
(V) Final Specification

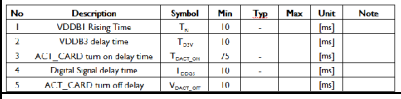
Module	**27.0” Color TFT-LCD**
Model Name	**M270QAN02.2**

Customer	**Date**	**Approved by**	**Date**
		Howard Lee	Feb 1, 2018
Approved by		**Prepared by**	**Date**
		ShinYu Lin	Feb 1, 2018
Note: This Specification is subject to change without notice.		AU Optronics corporation	

Contents

Record of Revision

Version	Date	Page	Old description	New Description	Remark
0.1	2017/2/13	All			
0.2	2017/4/10	34	Old LED driver board operating condition 	New LED driver board operating condition 	
		35	-	Add Note4-6 for SPI command at one frame interval	
		41~42	Old mechanical characteristics 	New mechanical characteristics 	
		29	Old LED driver board connector Item / CNT2 Driver Connector: Manufacturer: JST; Part Number: PHAR14 Mating Connector: Manufacturer: JST; Part Number: S14B-PHA-SM-K-TB(D)(HF)	New LED driver board connector Item / CNT2 Driver Connector: Manufacturer: JST; Part Number: S14B-PHA-SM3-TB(HF) Mating Connector: Manufacturer: JST; Part Number: PHAR14	
0.3	2017/4/28	9	-	Add RGB color coordinates	
		24	Old timing table 	New timing table 	

<table>
<tr><td rowspan="6">0.4</td><td rowspan="6">2017/10/31</td><td>6</td><td>The tolerance of weight is 80g</td><td>The tolerance of weight is 190g</td><td></td></tr>
<tr><td>7, 9, 10</td><td>-</td><td>Add luminance at HDR off</td><td></td></tr>
<tr><td>14</td><td>-</td><td>Update backside compression</td><td></td></tr>
<tr><td>14,15, 25, 36</td><td>-</td><td>Add note 2-12, 2-13, 3-4, 4-2</td><td></td></tr>
<tr><td>33</td><td>-</td><td>Add LED Recommended Operating Condition</td><td></td></tr>
<tr><td>34</td><td>-</td><td>Add LED diver board Recommended Operating Condition</td><td></td></tr>
<tr><td rowspan="3">0.5</td><td rowspan="3">2017/12/6</td><td>33~36</td><td>1. The range of VDDB1 is 12~19V
2. The absoluting max of VDDB3 is 3V.
3. The min of FAILED_1&2 is 1.8V
4. The max of BST_EN and ACT_CARD is 2~3.3V at OFF.
5. The max of BL_CARD is 2~3.3V at ON.
6. Modify H/L level range for SPI / I2C / SYNC signal.
7. Modify 4.3.4->
T_{R1} 10ms(min)
$T_{D3V,}$ 10ms(min)
T_{DACT_OFF}10ms(min)
8. Modify 3.4.4 eDP Specification</td><td>1. The range of VDDB1 is 11.4~19.95V
2. The absoluting max of VDDB3 is 4V.
3. The min of FAILED_1&2 is 1.71V
4. The max of BST_EN is 2.5~3.45V at OFF.
5. The max of BL_CARD is 2.5~19.95V at ON.
6. Modify H/L level range for SPI /I2C / SYNCsignal.
7. Modify 4.3.4->
T_{R1} 1ms(min)
T_{D3V}0ms(min)
T_{DACT_OFF} -50ms(min); 10ms(typ)
8. Modify 3.4.4 eDP Specification
9. Add SPI_SDO and I^2C signal</td><td></td></tr>
<tr><td>37</td><td>The original of backlight power sequence.
 
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<tr><th>No</th><th>Description</th><th>Symbol</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th><th>Note</th></tr>
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<tr><td>2</td><td>VDDB3 delay time</td><td>T_{D3V}</td><td>10</td><td></td><td></td><td>[ms]</td><td></td></tr>
<tr><td>3</td><td>ACT_CARD turn on delay time</td><td>T_{DACT_ON}</td><td>75</td><td>-</td><td></td><td>[ms]</td><td></td></tr>
<tr><td>4</td><td>Digital Signal delay time</td><td>T_{DDB1}</td><td>10</td><td>-</td><td></td><td>[ms]</td><td></td></tr>
<tr><td>5</td><td>ACT_CARD turn off delay</td><td>V_{DACT_OFF}</td><td>10</td><td></td><td></td><td>[ms]</td><td></td></tr>
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 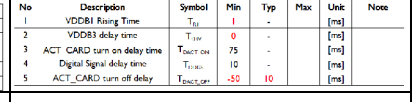
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</table></td><td></td></tr>
<tr><td>9</td><td>-</td><td>Remove crosstalk and flicker</td><td></td></tr>
<tr><td>1.0</td><td>2018/2/1</td><td>-</td><td>-</td><td>Final version</td><td></td></tr>
</table>

1 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container.
10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
12) Please avoid touching COF position while you are doing mechanical design.
13) When storing modules as spares for a long time, the following precaution is necessary:
    Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

2 General Description

This specification applies to the 27.0 inch wide Color a-Si TFT-LCD Module M270QAN02.2. The display supports the UHD - 3840(H) x 2160(V) screen format and 16.7M colors (8 bits RGB data input). The input interface is 8-lanes eDP HBR2 and this module contain 2 driver boards for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	684 (26.93")
Active Area	[mm]	596.16 (H) x 335.34 (V)
Pixels H x V	-	3840x3(RGB) x 2160
Pixel Pitch	[um]	155.25 (per one triad) × 155.25
Pixel Arrangement	-	R.G.B. Vertical Stripe
Display Mode	-	Normally Black (AHVA)
HDR off White Luminance (Center)	[cd/m^2]	300 (Typ.) @HDR off
HDR on White Luminance (Center)	[cd/m^2]	600 (Typ.) @HDR on
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	12 (Typ., Gray to Gray)
Power Consumption (LCD Module + Backligh unit)	[Watt]	Total = 83.37 W(Typ.) LCD module : PDD (Typ.) =8.57W @ white pattern, 144Hz, 12 V Backlight unit@HDR on White Luminunce(Typ.) with LED driver board & all LED Is=25mA(Typ.) PDDB1 (Typ.) = 72W PDDB2(Typ.) = 2.4W PDDB3(Typ.) = 0.4W
Weight	[Grams]	3850 +/- 190
Outline Dimension	[mm]	620.0(H) x 359.3 (V) × 40.0(D) (Typ.)
Electrical Interface	-	8-lanes eDP HBR2, 8bits RGB data input
Support Color	-	16.7M colors
Surface Treatment	-	Anti-Glare, 3H, 25%
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance

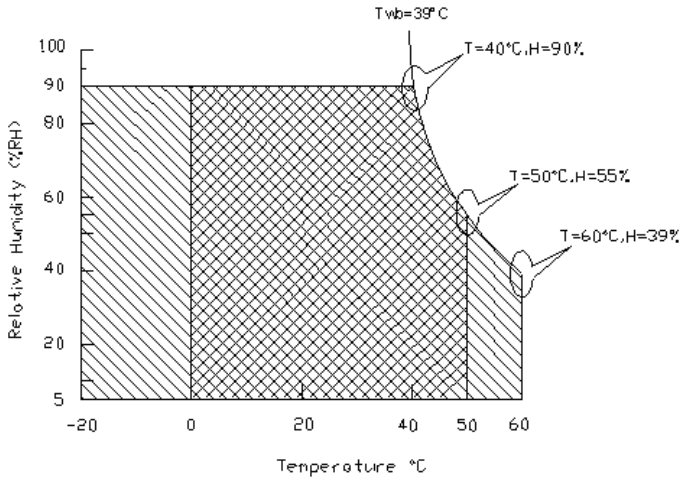
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	***Note 2-1***
TGS	Glass surface temperature (operation)	0	+65	[°C]	***Note 2-1*** *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	***Note 2-1***
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta ≦39℃)
2. Max wet-bulb temperature at 39℃ or less. (Ta ≦39℃)
3. No condensation



Operating Range Storage Range +

2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

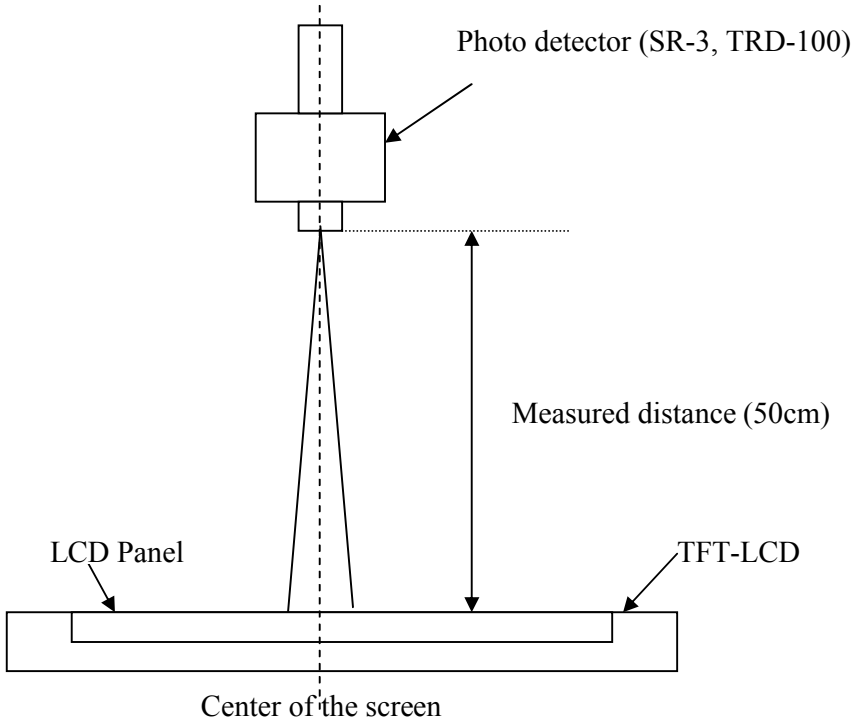
Test Condition:

1. Equipment setup: Please refer to ***Note 2-2***.
2. Panel lighting time: 30 minutes
3. VDD=12.0V, Fv=120Hz,Ta=25℃

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_w	White Luminance (Center of screen)		240	300	-	[cd/m^2]	***@ HDR off*** ***Note 2-2*** ***Note 2-3*** *By SR-3*
L_{w1}	White Luminance (Center of screen)		480	600	-	[cd/m^2]	***@ HDR on*** ***Note 2-2*** ***Not 2-4*** *By SR-3*
L_{w2}	White Luminance (10% of screen)		800	1000	-	[cd/m2]	***@ HDR on*** ***Note 2-5*** *By SR-3*
L_{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	***Note 2-6*** *By SR-3*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	***Note 2-7*** *By SR-3*
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	***Note 2-8*** *By SR-3*
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	75	89	-		
Φ_L		Down	75	89	-		
T_{GTG}	Response Time	Gray to Gray	-	12	-	[msec]	***Note 2-9*** *By TRD-100*
R_x	Color Coordinates (CIE 1931)	Red x	0.652	0.682	0.712	-	*By SR-3*
R_y		Red y	0.274	0.304	0.334		
G_x		Green x	0.177	0.207	0.237		
G_y		Green y	0.677	0.707	0.737		

B_x		Blue x	0.122	0.152	0.182		
B_y		Blue y	0.017	0.047	0.077		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
Adobe RGB coverage ratio			-	99	-	[%]	*By SR-3*

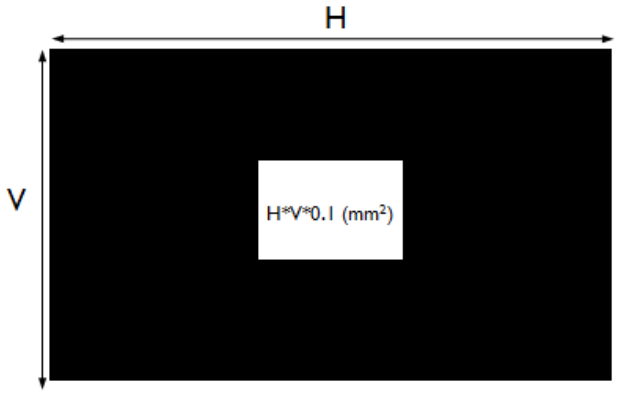
Note 2-2: Equipment setup:



Note 2-3: LED current condition @HDR off Is=12.5mA.

Note 2-4: LED current condition @HDR on Is=25mA.

Note 2-5: Measurement Pattern: 10% active area with L255 at center.
LED light on condition: 8(H) x 6(V)=48pcs , Is= 50mA

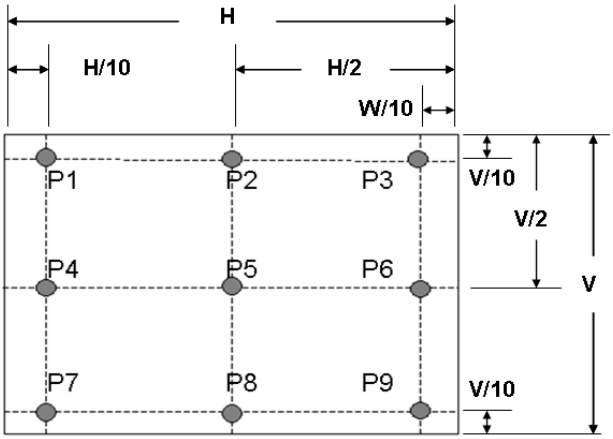


Note 2-6: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformity} = \frac{\text{Minimum Luminance of 9 Points (P1 ~ P9)}}{\text{Maximum Luminance of 9 Points (P1 ~ P9)}}$$

a. Test pattern: White Pattern



Note 2-7: Contrast Ratio Measurement

Definition:

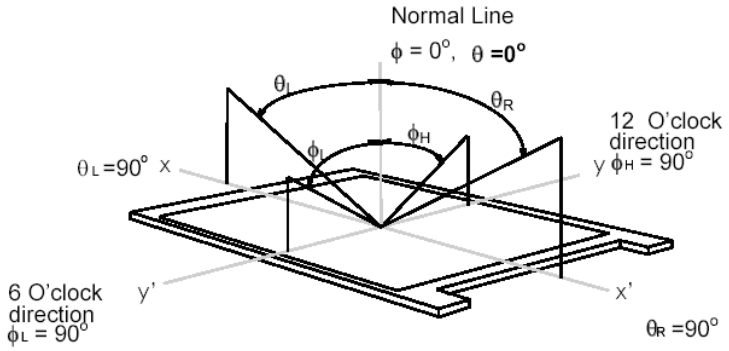
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen ($\theta=\Phi=0°$)

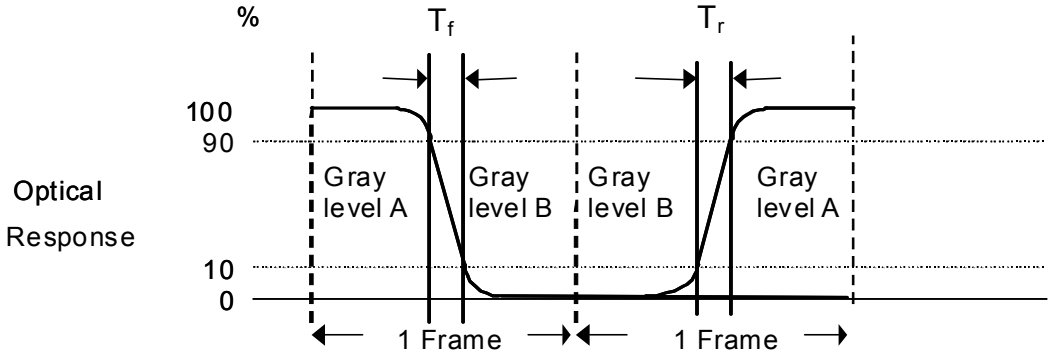
Note 2-8: Viewing angle measurement

Definition: The angle at which the contrast ratio is greater than 10 & 5 .

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)



Note 2-9: Response time measurement
The output signals of photo detector are measured when the input signals are changed from "Gray level A" to "Gray level B" (falling time, T_f), and from "Gray level B" to "Gray level A" (rising time, T_r), respectively. The response time is interval between the 10% and 90% of optical response.



The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

- T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

Note 2-11: Evaluation test and mass production inspection shall be applied with LED current Is @ HDR off condition if there is not specified condition.

2.4 Mechanical Characteristics

Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	***Note 2-13***

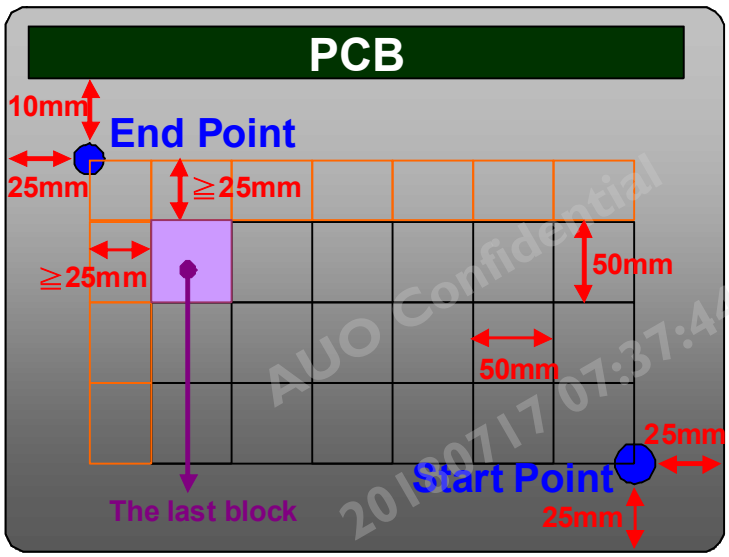
Note 2-13: Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

Test pattern: L128 gray pattern

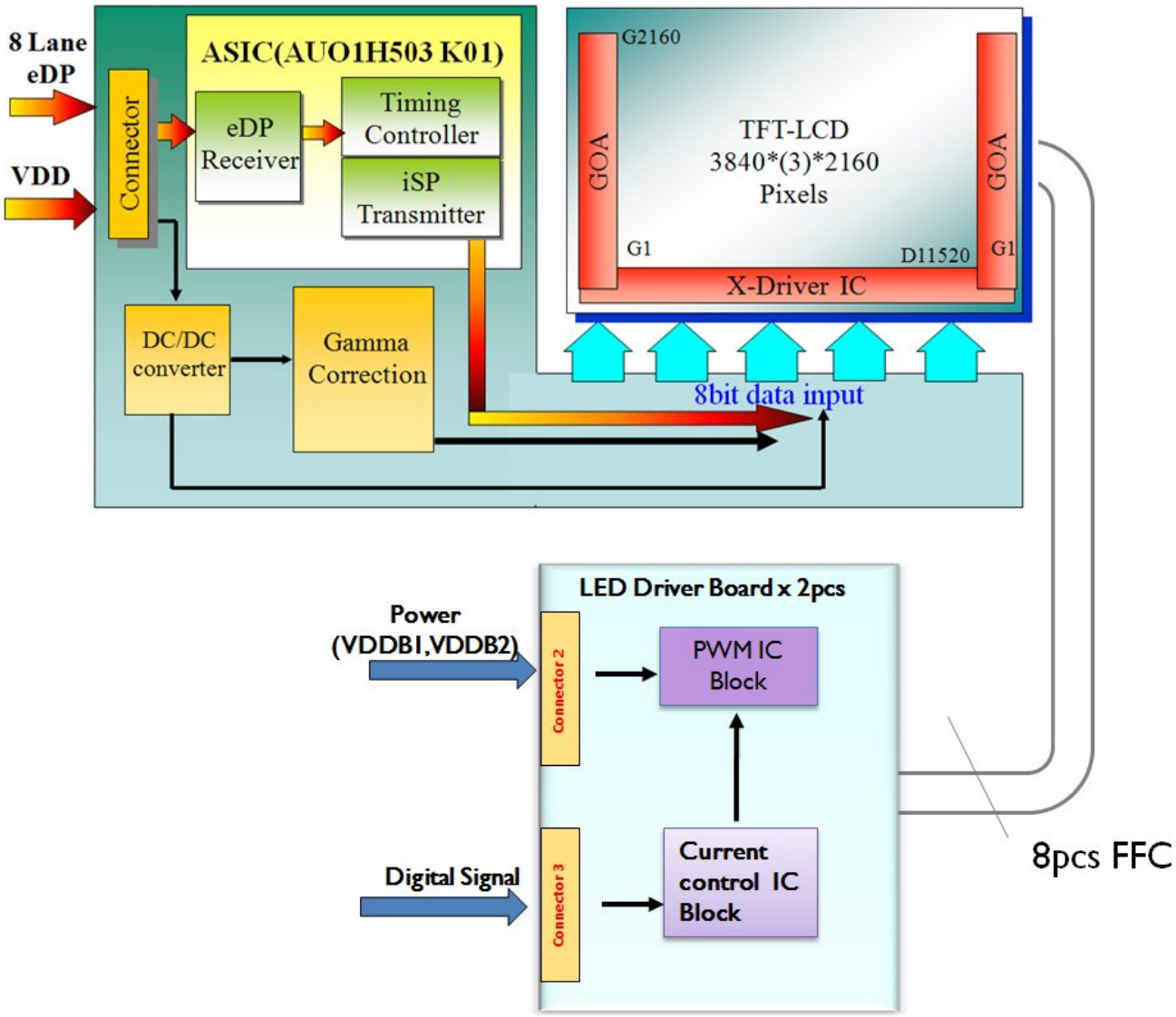
If the distance from the last block to each side of the End Point ≧ 25mm, add other blocks to make sure that most area of Bezel Back can be measured.



3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 27.0 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD Connector	Manufacturer	P-TWO	JAE	STARCONN
	Part Number	187059-5122	FI-RTE51SZ-HF	115E51-0000RA-M3-R
Mating Connector	Manufacturer	JAE		
	Part Number	FI-RE51CL		

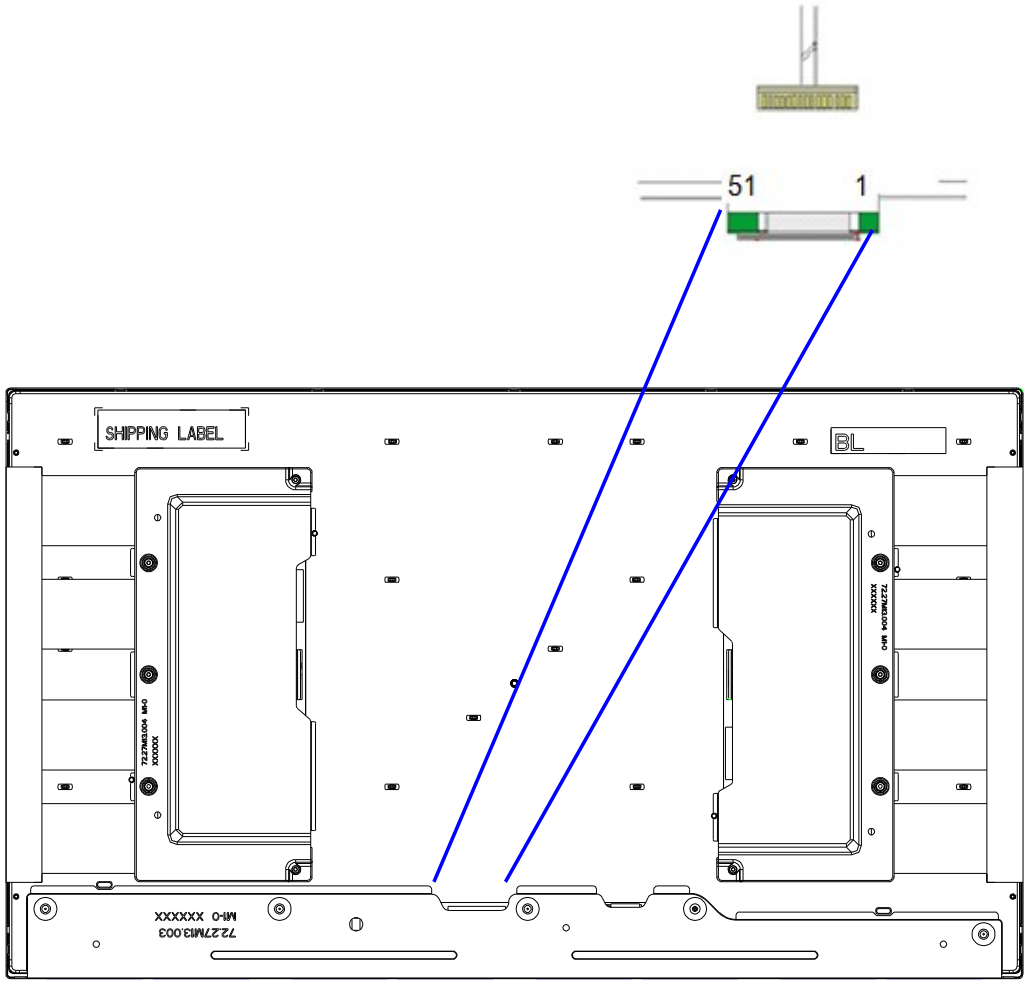
3.2.2 Connector Pin Assignment

PIN #	Symbol	Description	Remark
1	VDD	Power +12V	
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	NC	No connection (for AUO test only. Do not connect)	
10	NC	No connection (for AUO test only. Do not connect)	
11	NC	No connection (for AUO test only. Do not connect)	
12	NC	No connection (for AUO test only. Do not connect)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	IMS	Interlace Mode Selection (I)	
16	IMS_POL	Interlace Mode Selection Polarity (O)	
17	GND	Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	

20	GND	Ground	
21	1st Lane2_N	Negative eDP differential data input	
22	1st Lane2_P	Positive eDP differential data input	
23	GND	Ground	
24	1st Lane1_N	Negative eDP differential data input	
25	1st Lane1_P	Positive eDP differential data input	
26	GND	Ground	
27	1st Lane0_N	Negative eDP differential data input	
28	1st Lane0_P	Positive eDP differential data input	
29	GND	Ground	
30	1st AUX_CH_P	Positive AUX Channel differential data input	
31	1st AUX_CH_N	Negative AUX Channel differential data input	
32	GND	Ground	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	2nd Lane3_N	Negative eDP differential data input	
36	2nd Lane3_P	Positive eDP differential data input	
37	GND	Ground	
38	2nd Lane2_N	Negative eDP differential data input	
39	2nd Lane2_P	Positive eDP differential data input	
40	GND	Ground	
41	2nd Lane1_N	Negative eDP differential data input	
42	2nd Lane1_P	Positive eDP differential data input	
43	GND	Ground	
44	2nd Lane0_N	Negative eDP differential data input	
45	2nd Lane0_P	Positive eDP differential data input	
46	GND	Ground	
47	2nd AUX_CH_P	Positive AUX Channel differential data input	
48	2nd AUX_CH_N	Negative AUX Channel differential data input	

49	GND	Ground	
50	HPD	Hot plug detection	
51	GND	Ground	

1



Note 3-1: Input signals of port 1 to port 4 clocks shall be the same timing.

3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

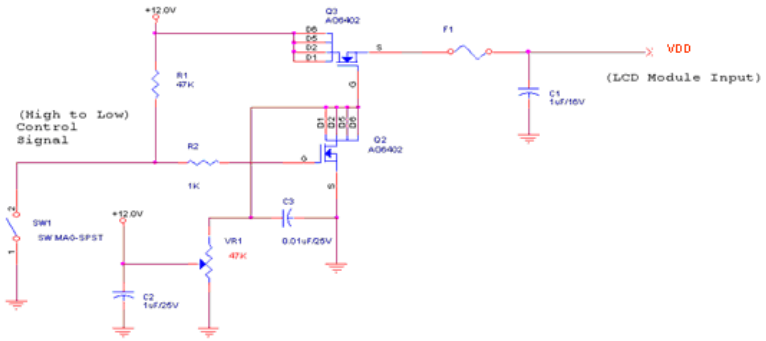
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25℃

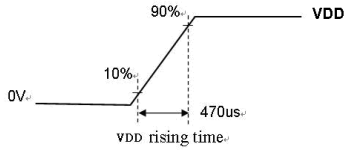
3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.71	1.75	[A]	VDD= 12.0V, White pattern, Fv=144Hz
			0.65	1.53		VDD= 12.0V, White pattern, Fv=120Hz
PDD	VDD Power Consumption	-	8.57	21.68	[Watt]	VDD= 12.0V , White pattern, Fv=144Hz
			7.80	18.36		VDD= 12.0V, White pattern, Fv=120Hz
IRush	Inrush Current	-	-	3	[A]	***Note 3-2***
VDDrp	Allowable VDD Ripple Voltage	-	-	VDD*5 %	[mVolt]	VDD= 12.0V, White pattern, Fv=144Hz

Note 3-2: Inrush Current measurement:

Test circuit:



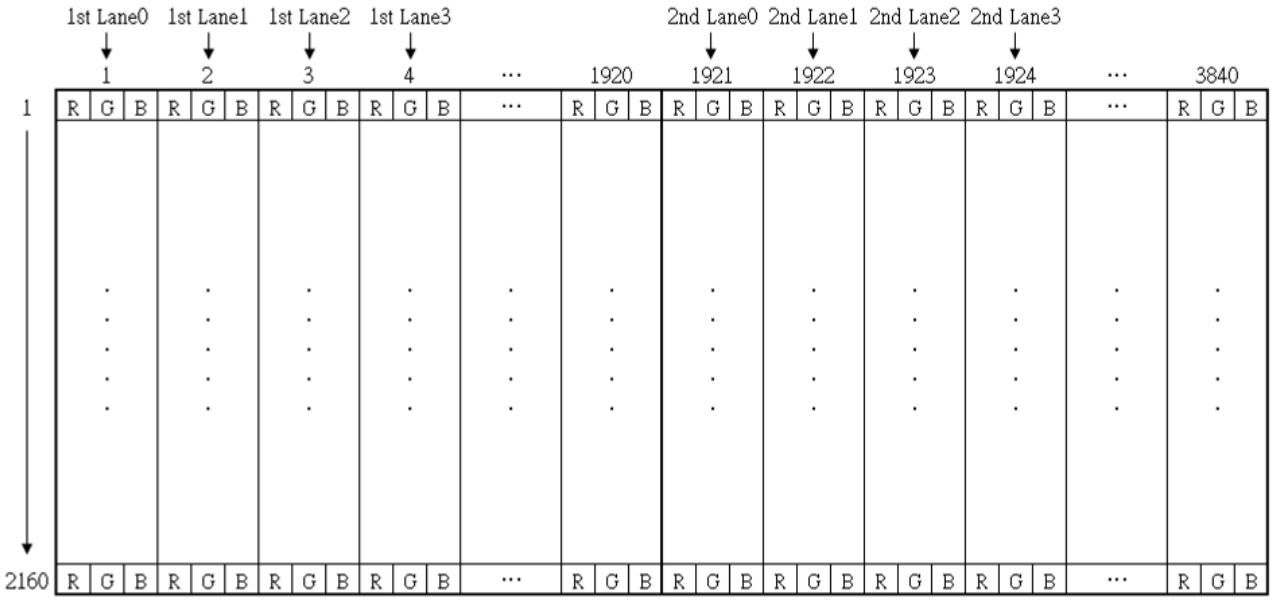


The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.



Note 3-3: The module use 8-Lanes eDP interface.

1st port:

1st Lane0：1+4n pixel

1st Lane1：2+4n pixel

1st Lane2：3+4n pixel

1st Lane3：4+4n pixel

2nd port:

2nd Lane0：1921+4n pixel

2nd Lane1：1922+4n pixel

2nd Lane2：1923+4n pixel

2nd Lane3：1924+4n pixel

n=0~479

3.4.2 eDP Data Format

1st Lane0	1st Lane1	1st Lane2	1st Lane3
R1-7:0	R2-7:0	R3-7:0	R4-7:0
G1-7:0	G2-7:0	G3-7:0	G4-7:0
B1-7:0	B2-7:0	B3-7:0	B4-7:0
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-7:0	G6-7:0	G7-7:0	G8-7:0
B5-7:0	B6-7:0	B7-7:0	B8-7:0
R9-7:0	R10-7:0	R11-7:0	R12-7:0
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-7:0	B10-7:0	B11-7:0	B12-7:0
. . .	. . .	. . .	. . .

2nd Lane0	2nd Lane1	2nd Lane2	2nd Lane3
R1921-7:0	R1922-7:0	R1923-7:0	R1924-7:0
G1921-7:0	G1922-7:0	G1923-7:0	G1924-7:0
B1921-7:0	B1922-7:0	B1923-7:0	B1924-7:0
R1925-7:0	R1926-7:0	R1927-7:0	R1928-7:0
G1925-7:0	G1926-7:0	G1927-7:0	G1928-7:0
B1925-7:0	B1926-7:0	B1927-7:0	B1928-7:0
R1929-7:0	R1930-7:0	R1931-7:0	R1932-7:0
G1929-7:0	G1930-7:0	G1931-7:0	G1932-7:0
B1929-7:0	B1930-7:0	B1931-7:0	B1932-7:0
. . .	. . .	. . .	. . .

3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

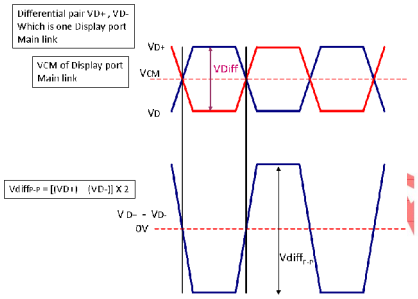
3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.1 and support 5.4Gbps)

a. DisplayPort main link signal:

DisplayPort main link					
		Min	Typ	Max	unit
Frequency	Main link Frequency	-	5.4	-	Gbps
UI	Unit Interval	-	185	-	ps
VCM	RX input DC Common Mode Voltage	-	0	-	[Volt]
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	70	-	-	[mVolt]
Down_Spread_Freq	Link clock down spread frequency	30	-	33	KHz
Down_Spread_Amplitude	Link clock down spread amplitude	-	-	0.5	%

Point	Time (UI)	Voltage (V)
1	0.310	0
2	0.375~0.625	35mV
3	0.690	0
4	0.375~0.625	-35mV

Figure 5.55.2 Downstream Device EYE Mask at Receiver Connector for HBR2



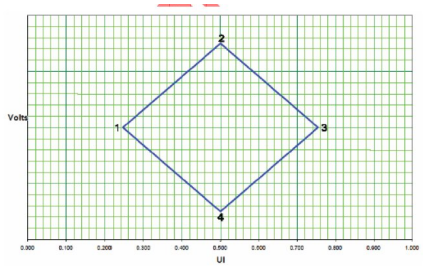
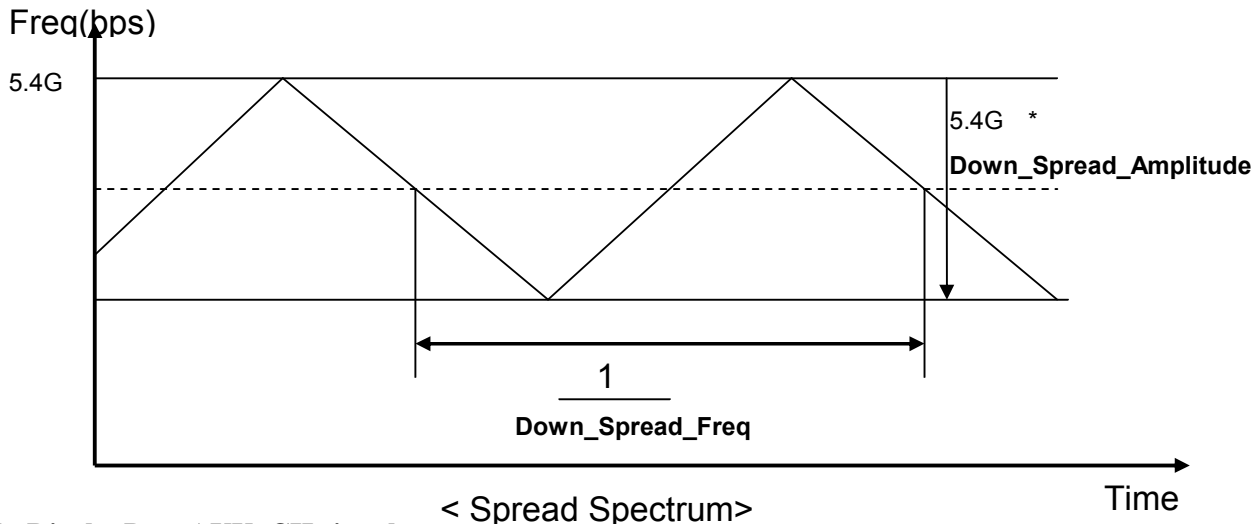


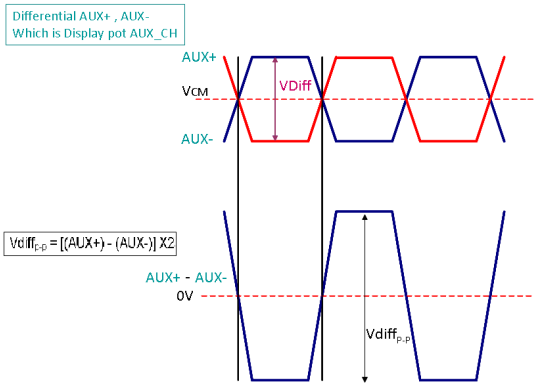
Figure 5.55.1 Downstream Device EYE Mask at Receiver Connector Pins



< Spread Spectrum>

b. DisplayPort AUX_CH signal:

DisplayPort AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	2.0	[Volt]
$VDiff_{P-P}$	AUX Peak-to-peak voltage at a receiving device	0.27	-	1.36	[Volt]



c. DisplayPort VHPD signal:

Display Port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	[Volt]

d. Intra-Pair skew

LRX-SKEW-INTRA_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTRA	Lane Intra-pair Skew Tolerance	-	-	50	[ps]

_PAIR					

e. Inter-Pair Skew

LRX-SKEW-INTER_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTER PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	[ps]

3.4.5 Input Timing Specification

The input timing is shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	2180	2200	6735	Th	
Tdisp (v)		Active	2160	2160	2160	Th	
Tblk (v)			20	40	4575	Th	
Fv		Frequency	47	120	145	Hz	***Note 3-4*** ***Note 3-7***
Th	Horizontal Section	Period	2000	2100	3520	Tclk	
Tdisp (h)		Active	1920	1920	1920	Tclk	
Tblk (h)		Blanking	80	180	1600	Tclk	
Fh		Frequency	180	264	317	kHz	***Note 3-5***
Tclk	Pixel Clock	Period	1.581	1.804	2.778	ns	1/Fclk
Fclk		Frequency	360	554	633	MHz	***Note 3-6***
Link Rate per Lane			5.4			Gbps	

Note 3-4: The optimal Vertical Frequency is 119~145 Hz for best picture quality.

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.)
Fh (Typ.) = Fclk (Typ.) / Th (Typ.)
Fh (Max.)= Fclk (Max.) / Th (Min.)

Note 3-6: The equation is listed as following. Please don't exceed the above recommended value.

1st Lane N & 2nd Lane N skew < 200ns

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)

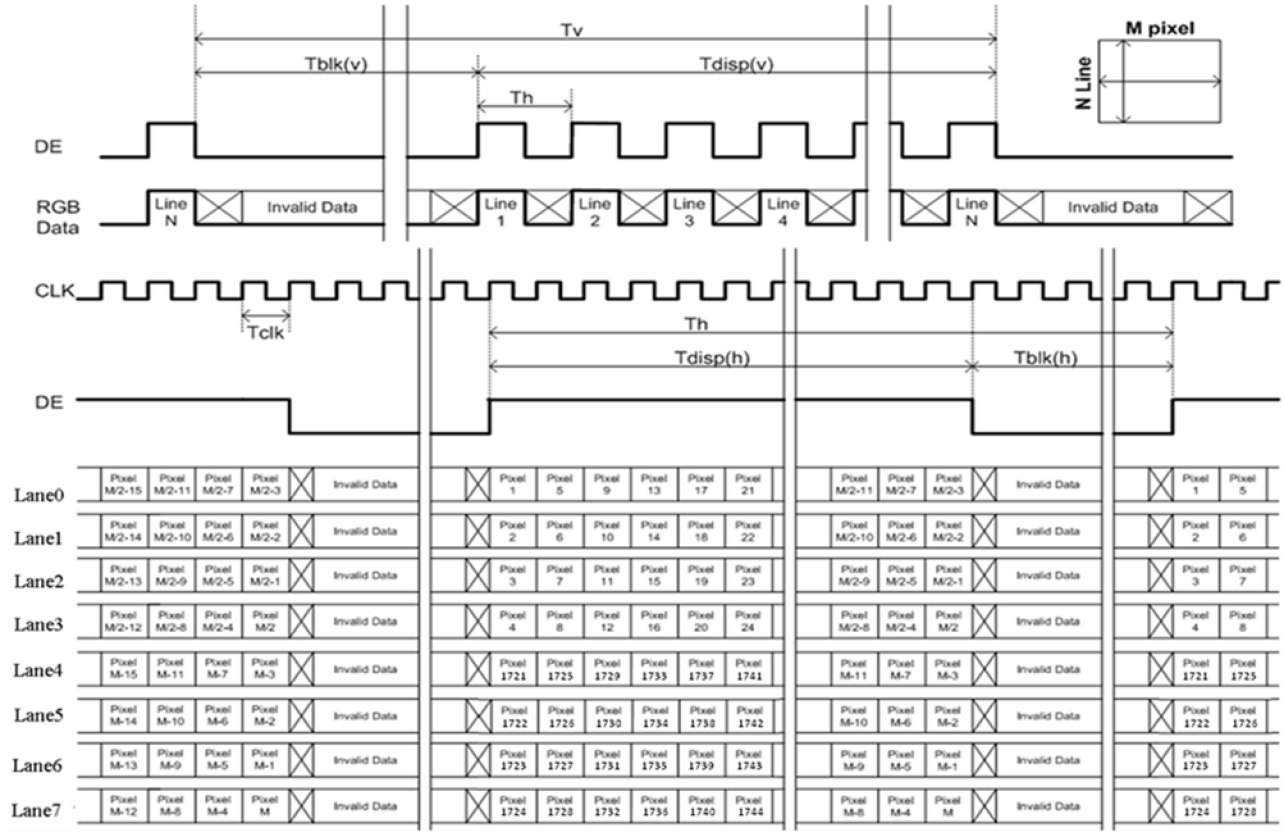
Fclk (Min.)≦Fv x Th x Tv ≦ Fclk (Max.)

Note 3-7: The equation is listed as following. Please don't exceed the above recommended value.

Fv =Fclk(Typ.) / (Tv x Th)

3.4.6 Input Timing Diagram

(Lane0~7 eDP data:1, 2, 3, 4, 1721, 1722, 1723, 1724)



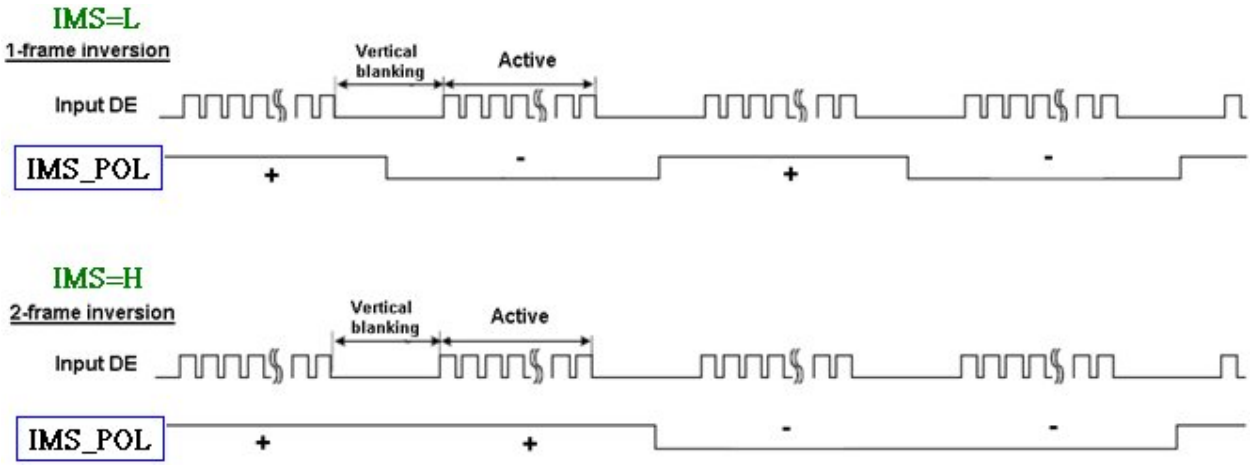
3.4.7 3D Control

3.4.7.1. 3D control I/O Characteristics

Pin #	Symbol	I/O	Buffer	Description	Remark
pin 16	IMS_POL	O	4mA	Frame Inversion polarity Index IMS=L :1-frame inversion IMS=H :2-frame inversion	***Note 3-8***
pin 15	IMS	I	IPL*	3D enable control signal	

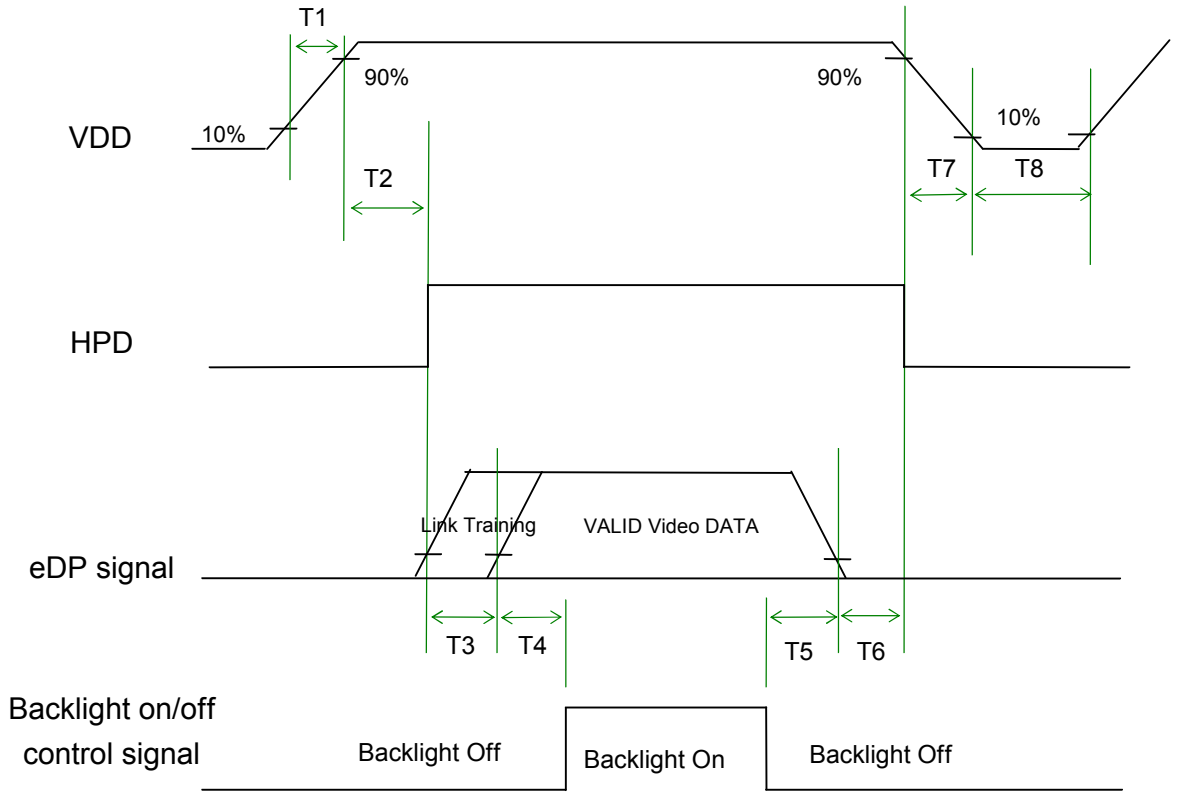
* IPL : internal pull low

Note 3-8



3.5 Power ON/OFF Sequence

VDD power,eDP signal and backlight on/off sequence are as following. eDP signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	***Note 3-8***
T4	500	-	-	[ms]	
T5	100	-	-	[ms]	
T6	0		50	[ms]	***Note 3-9*** ***Note 3-10***
T7	0	-	200	[ms]	***Note 3-10*** ***Note 3-11***
T8	1000	-	-	[ms]	

Note 3-8: During T3 period , eDP link training time by customer's system.
Note 3-9: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.
Note 3-10: During T6 and T7 period , please keep the level of input eDP signals with Hi-Z state.
Note 3-11: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

4 Backlight Unit

4.1 Interface Connection

4.1.1 Connector Type

Item		CNT2	CNT3
Driver Connector	Manufacturer	JST	PTWO
	Part Number	S14B-PHA-SM3-TB(HF)	187060-4122
Mating Connector	Manufacturer	JST	JAE
	Part Number	PHAR14	FI-RE41CL

4.1.2 Connector Pin Assignment

CNT2:

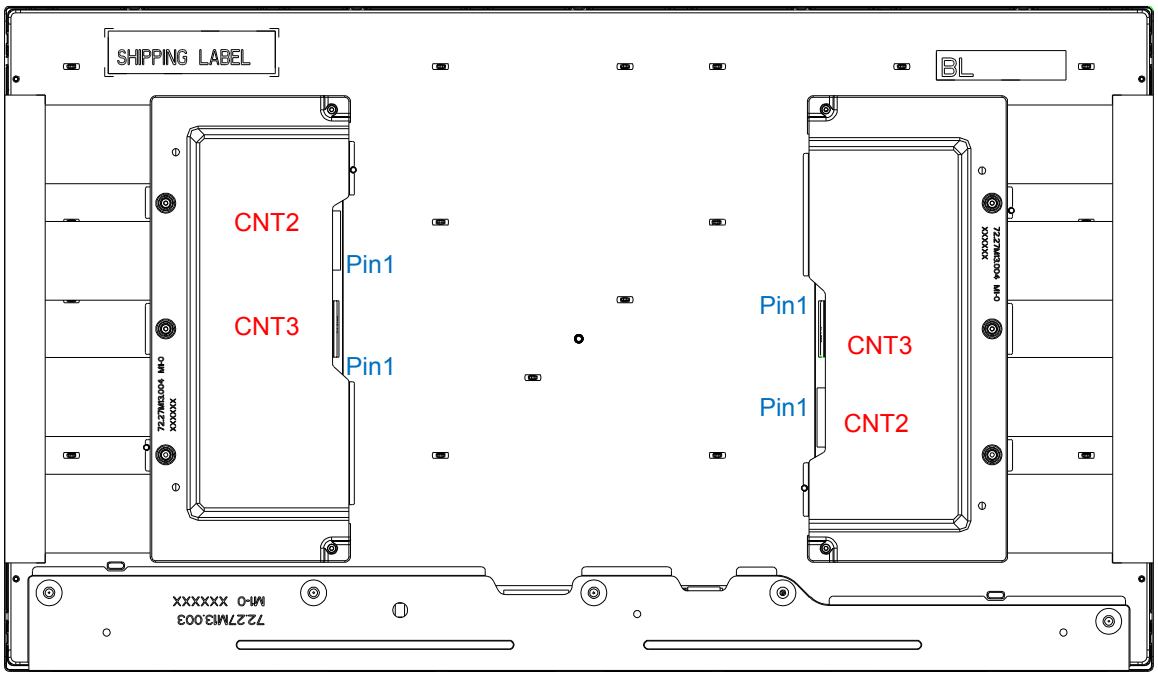
PIN #	Symbol	Description	Remark
1	VDDB1	Main Operation voltage supply (12~19V)	
2	VDDB1	Main Operation voltage supply (12~19V)	
3	VDDB1	Main Operation voltage supply (12~19V)	
4	VDDB1	Main Operation voltage supply (12~19V)	
5	VDDB1	Main Operation voltage supply (12~19V)	
6	VDDB1	Main Operation voltage supply (12~19V)	
7	VDDB2	Operation voltage supply (5V)	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	

CNT3:

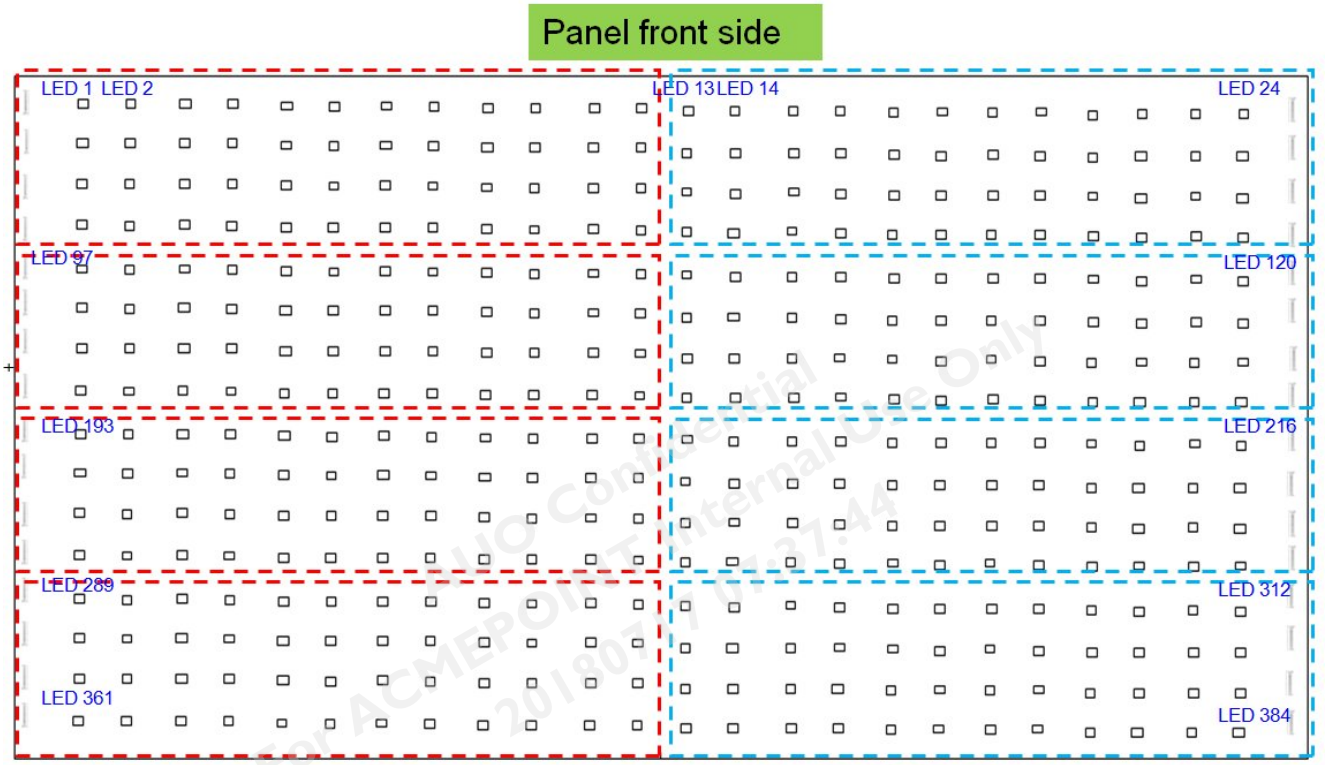
PIN #	Symbol	Description	Remark
1	GND	Ground	
2	GND	Ground	
3	GND	Ground	

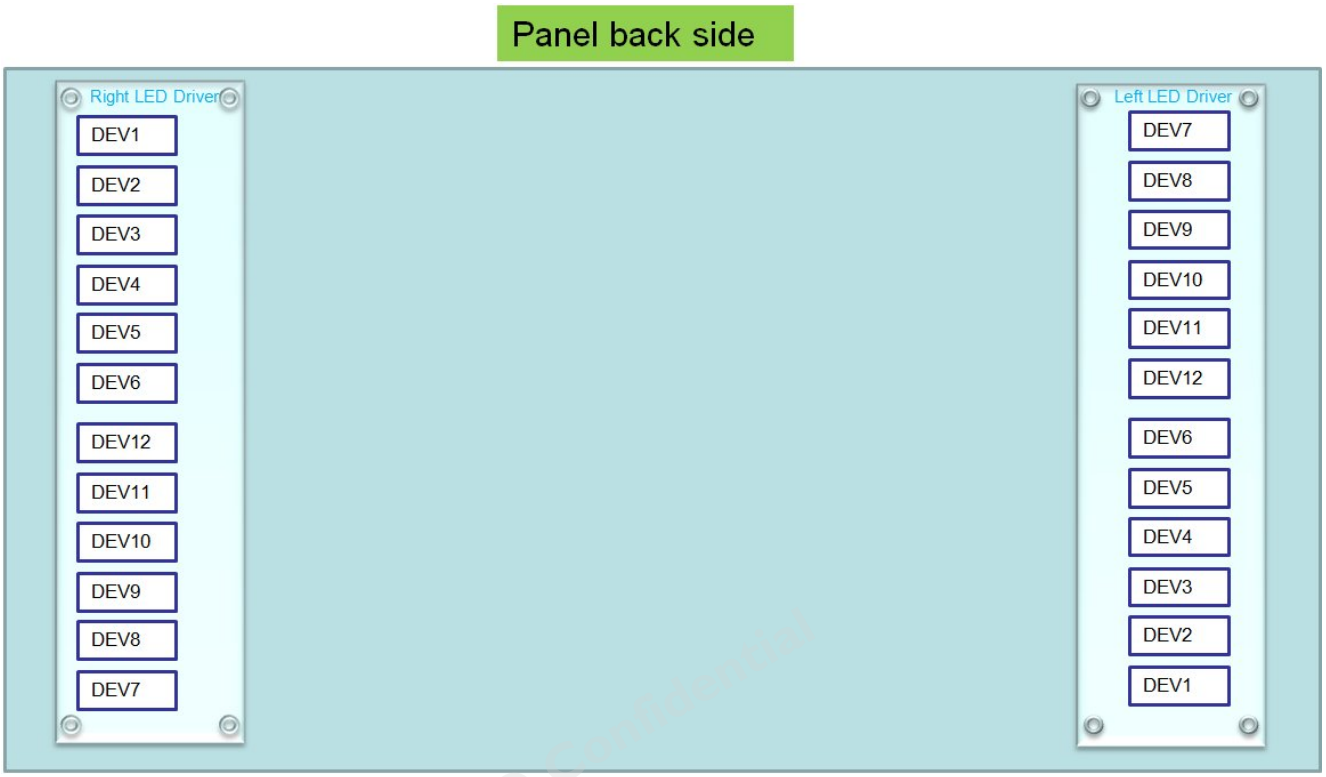
4	GND	Ground	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	NC	NC	
9	NC	NC	
10	I^2C_SDA	Serial data input for TMP100	
11	SPI2_SCL	SPI interface clock input for AS8324E	
12	GND	Ground and current return	
13	SPI2_SDI	SPI interface data input for AS8324E	
14	VSYNC2	Vertical sync frequency	
15	HSYNC2	Clock input for PWM generators	
16	GND	Ground and current return	
17	SPI2_CS	SPI interface chip select for AS8324E	
18	SPI1_CS	SPI interface chip select for AS8324E	
19	ACT_CARD	Active LED driver board	
20	BL_CARD	BL Bleed card on	
21	BST_EN	Output double current	
22	FAILED_2	Error signal output (DEV7/8/9/10/11/12) (Open drain output. Pull H (3.3 or 1.8V) by system with 10K ohm)	
23	FAILED_1	Error signal output (DEV1/2/3/4/5/6) (Open drain output. Pull H (3.3 or 1.8V) by system with 10K ohm)	
24	VDDB3	Digital Operation voltage supply(3.3V)	
25	SPI2_SDO1	SPI interface data output. Tristate output	
26	SPI1_SDO7	SPI interface data output. Tristate output	
27	GND	Ground and current return	
28	VSYNC1	Vertical sync frequency	
29	HSYNC1	Clock input for PWM generators	
30	SPI1_SDI	SPI interface data input for AS8324E	
31	GND	Ground and current return	

32	SPI1_SCL	SPI interface clock input for AS8324E	
33	I^2C_SCL	Serial clock input for TMP100	
34	NC	NC	
35	NC	NC	
36	GND	GND	
37	GND	GND	
38	GND	GND	
39	GND	GND	
40	GND	GND	
41	GND	GND	



4.2 LED Control mapping





Below is the LED& driver mapping.

Panel front side

(Left LED Driver)												(Right LED Driver)											
(7,12)	(7,11)	(7,10)	(7,9)	(7,8)	(7,7)	(7,6)	(7,5)	(7,4)	(7,3)	(7,2)	(7,1)	(1,5)	(1,6)	(1,7)	(1,8)	(1,9)	(1,10)	(1,11)	(1,12)	(1,13)	(1,14)	(1,15)	(1,16)
(8,8)	(8,7)	(8,6)	(8,5)	(8,4)	(8,3)	(8,2)	(8,1)	(7,16)	(7,15)	(7,14)	(7,13)	(2,9)	(2,10)	(2,11)	(2,12)	(2,13)	(2,14)	(2,15)	(2,16)	(1,1)	(1,2)	(1,3)	(1,4)
(9,4)	(9,3)	(9,2)	(9,1)	(8,16)	(8,15)	(8,14)	(8,13)	(8,12)	(8,11)	(8,10)	(8,9)	(3,13)	(3,14)	(3,15)	(3,16)	(2,1)	(2,2)	(2,3)	(2,4)	(2,5)	(2,6)	(2,7)	(2,8)
(9,16)	(9,15)	(9,14)	(9,13)	(9,12)	(9,11)	(9,10)	(9,9)	(9,8)	(9,7)	(9,6)	(9,5)	(3,1)	(3,2)	(3,3)	(3,3)	(3,5)	(3,6)	(3,7)	(3,8)	(3,9)	(3,10)	(3,11)	(3,12)
(10,12)	(10,11)	(10,10)	(10,9)	(10,8)	(10,7)	(10,6)	(10,5)	(10,4)	(10,3)	(10,2)	(10,1)	(4,5)	(4,6)	(4,7)	(4,8)	(4,9)	(4,10)	(4,11)	(4,12)	(4,13)	(4,14)	(4,15)	(4,16)
(11,8)	(11,7)	(11,6)	(11,5)	(11,4)	(11,3)	(11,2)	(11,1)	(10,16)	(10,15)	(10,14)	(10,13)	(5,9)	(5,10)	(5,11)	(5,12)	(5,13)	(5,14)	(5,15)	(5,16)	(4,1)	(4,2)	(4,3)	(4,4)
(12,4)	(12,3)	(12,2)	(12,1)	(11,16)	(11,15)	(11,14)	(11,13)	(11,12)	(11,11)	(11,10)	(11,9)	(6,13)	(6,14)	(6,15)	(6,16)	(5,1)	(5,2)	(5,3)	(5,4)	(5,5)	(5,6)	(5,7)	(5,8)
(12,16)	(12,15)	(12,14)	(12,13)	(12,12)	(12,11)	(12,10)	(12,9)	(12,8)	(12,7)	(12,6)	(12,5)	(6,1)	(6,2)	(6,3)	(6,4)	(6,5)	(6,6)	(6,7)	(6,8)	(6,9)	(6,10)	(6,11)	(6,12)
(6,12)	(6,11)	(6,10)	(6,9)	(6,8)	(6,7)	(6,6)	(6,5)	(6,4)	(6,3)	(6,2)	(6,1)	(12,5)	(12,6)	(12,7)	(12,8)	(12,9)	(12,10)	(12,11)	(12,12)	(12,13)	(12,14)	(12,15)	(12,16)
(5,8)	(5,7)	(5,6)	(5,5)	(5,4)	(5,3)	(5,2)	(5,1)	(6,16)	(6,15)	(6,14)	(6,13)	(11,9)	(11,10)	(11,11)	(11,12)	(11,13)	(11,14)	(11,15)	(11,16)	(12,1)	(12,2)	(12,3)	(12,4)
(4,4)	(4,3)	(4,2)	(4,1)	(5,16)	(5,15)	(5,14)	(5,13)	(5,12)	(5,11)	(5,10)	(5,9)	(10,13)	(10,14)	(10,15)	(10,16)	(11,1)	(11,2)	(11,3)	(11,4)	(11,5)	(11,6)	(11,7)	(11,8)
(4,16)	(4,15)	(4,14)	(4,13)	(4,12)	(4,11)	(4,10)	(4,9)	(4,8)	(4,7)	(4,6)	(4,5)	(10,1)	(10,2)	(10,3)	(10,4)	(10,5)	(10,6)	(10,7)	(10,8)	(10,9)	(10,10)	(10,11)	(10,12)
(3,12)	(3,11)	(3,10)	(3,9)	(3,8)	(3,7)	(3,6)	(3,5)	(3,4)	(3,3)	(3,2)	(3,1)	(9,5)	(9,6)	(9,7)	(9,8)	(9,9)	(9,10)	(9,11)	(9,12)	(9,13)	(9,14)	(9,15)	(9,16)
(2,8)	(2,7)	(2,6)	(2,5)	(2,4)	(2,3)	(2,2)	(2,1)	(3,16)	(3,15)	(3,14)	(3,13)	(8,9)	(8,10)	(8,11)	(8,12)	(8,13)	(8,14)	(8,15)	(8,16)	(9,1)	(9,2)	(9,3)	(9,4)
(1,4)	(1,3)	(1,2)	(1,1)	(2,16)	(2,15)	(2,14)	(2,13)	(2,12)	(2,11)	(2,10)	(2,9)	(7,13)	(7,14)	(7,15)	(7,16)	(8,1)	(8,2)	(8,3)	(8,4)	(8,5)	(8,6)	(8,7)	(8,8)
(1,16)	(1,15)	(1,14)	(1,13)	(1,12)	(1,11)	(1,10)	(1,9)	(1,8)	(1,7)	(1,6)	(1,5)	(7,1)	(7,2)	(7,3)	(7,4)	(7,5)	(7,6)	(7,7)	(7,8)	(7,9)	(7,10)	(7,11)	(7,12)

The mapping format is (device, channel)

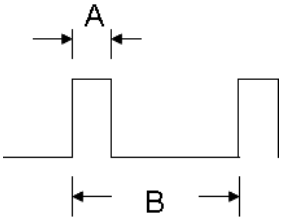
4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25℃)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current (VDD)	0	66	[mA]	100% duty ratio
			132	[mA]	Duty ratio≦ 10% Pulse time=10 ms
VDDB1	Main Operation voltage supply	10	20	[Volt]	
VDDB2	Operation voltage supply	4.5	7	[Volt]	
VDDB3	Digital Operation voltage supply	3	4	[Volt]	
Vsignal/ Vset	Signal and Setting pin voltage supply	0	5	[Volt]	SPIx_SDI, SPIx_SCL,SPIx_CS, I^2C_SCL,I^2C_SDA, , FAILED_x, BST_EN, HSYNCx, VSYNCx, ACT_CARD, BL_CARD



Duty ratio= (A / B) X 100% ; (A: Pulse time, B: Period)

Note: *The current sensing resistor of LED driver IC is 12ohm.*

4.3.2 LED Recommended Operating Condition

(Ta=25℃)

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
Is	LED String Current		12.5	13.1	[mA]	@HDR off 100% duty ratio of LED chip
Is	LED String Current		25	26.3	[mA]	@HDR on 100% duty ratio of LED chip
LT_{LED}	LED Life Time	30000			[Hour]	***Note 4-1***

4.3.3 LED Driver Board Recommended Operating Condition

No	Description		Symbol	Min	Typ	Max	Unit	Remark
1	Driver Board Input Voltage Range		VDDB1	11.4	15.5	19.95	[Volt]	
			VDDB2	4.5	5	5.5		
			VDDB3	3	3.3	3.6		
2	Driver Board Input Current		IDDB1	-	2.4	2.9	[A]	@HDR off All LED @Is=12.5mA Duty 100% ***Note 4-2***
			IDDB2	-	468	560	[mA]	
			IDDB3	-	96	115	[mA]	
3	Driver Board Power Consumption		PDDB1	-	36	43.2	[Watt]	
			PDDB2	-	2.4	2.9	[Watt]	
			PDDB3	-	0.4	0.5	[Watt]	
4	Driver Board Input Current		IDDB1	-	4.7	7.2	[A]	@HDR on All LED @Is=25mA Duty 100% ***Note 4-2***
			IDDB2	-	468	560	[mA]	
			IDDB3	-	96	115	[mA]	
5	Driver Board Power Consumption		PDDB1	-	72	112	[Watt]	
			PDDB2	-	2.4	2.9	[Watt]	
			PDDB3	-	0.4	0.5	[Watt]	
6	Driver Board Input Current		IDDB1	-	9.3	14.4	[A]	@HDR on All LED @Is=50mA Duty 100% ***Note 4-3*** ***Note 4-4***
			IDDB2	-	468	560	[mA]	
			IDDB3	-	106	128	[mA]	
7	Driver Board Power Consumption		PDDB1	-	144	224	[Watt]	
			PDDB2	-	2.4	2.9	[Watt]	
			PDDB3	-	0.4	0.5	[Watt]	
8	Output double current	ON	BST_EN	0	-	0.8	[Volt]	Is double on/off:

		OFF		2.5	-	3.45		Low for on, High for off.
9	Active LED driver board	ON	ACT_CARD	0	-	0.8	[Volt]	BL on/off: Low for on, High for off.
		OFF		2.5	-	3.45		
10	BL Bleed card on	ON	BL_CARD	2.5	10	19.95	[Volt]	BL_discharge on/off: High for on. Low for off,
		OFF		0	-	0.8		
11	SPI_SDI, SPI_SCL, SPI_CS, VSYNC, HSYNC	V_{IH}	SPIx_SDI, SPIx_SCL,SPIx_CS, HSYNCx, VSYNCx	2.5	-	3.6	[Volt]	VDDB3=3.0~3.6 V
		V_{IL}		0	-	0.8		
12	SPI_SDO	V_{OH}	SPI1_SDO7, SPI2_SDO1	2.7	-	3.3	[Volt]	
		V_{OL}		0	-	0.3		
13	I^2C signal	V_{IH}	I^2C_SDA, I^2C_SCL	2.6		3.6	[Volt]	VDDB3=3.0~3.6 V
		V_{IL}		0		0.8		
		V_{oL}	I^2C_SDA	0		0.4		
14	Error Signal output	H	FAILED_1&2	1.71	-	3.6	[Volt]	LED DB status High by system pull high with 10K ohm for normal work ; Low for some LED channel open
		L		0		1		
15	SPI Input impedance		RIN	300	-	-	KΩ	
16	SPI Frequency		Fsclk	0		10	MHz	12
17	VSYNC Control Frequency		FVSYNC	60		40000	Hz	
18	HSYNC Control Frequency		FHSYNC	100		20000	KHz	

Note 4-1: Definition of life time:

a. Brightness of LED becomes to 50% of its original value

b. Test condition: Is = 25mA and 25℃ (Room Temperature)

Note 4-2: Evaluation test and mass production inspection shall be applied with LED current Is @ HDR off condition if there is not specified condition and all power define at Typ. VDDBx .

Note 4-3: It can't use over 0.5 second when all LED are working at 50mA with 100% duty.

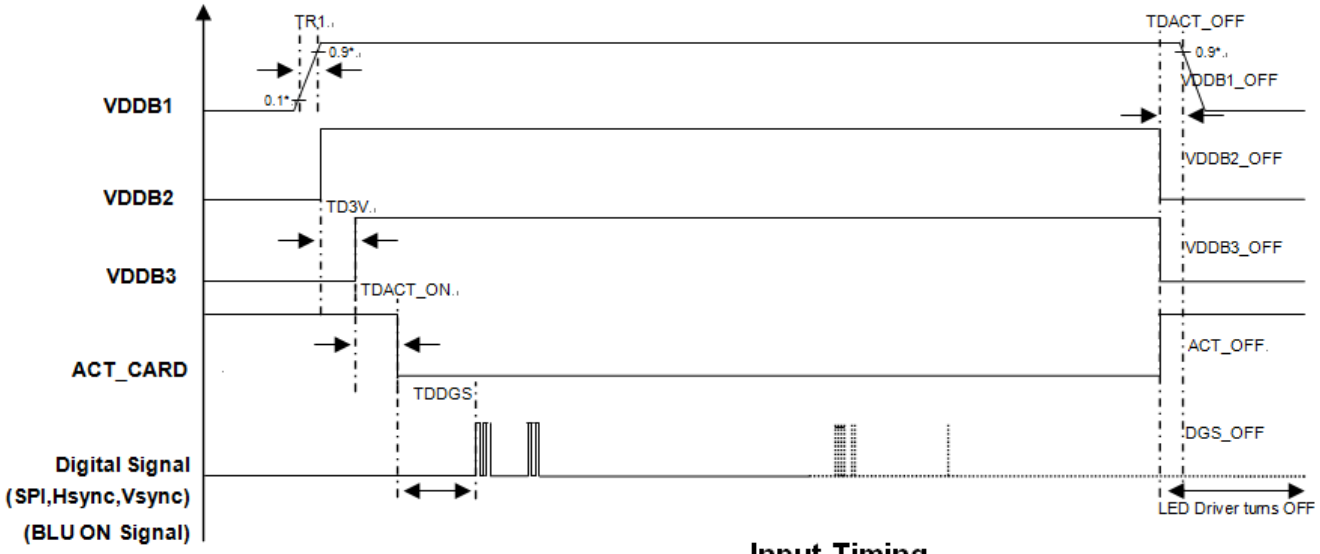
Note 4-4: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency

Note 4-5: Ensure that the LED light bar is not subjected either forward or reverse voltage while monitor set is on standby mode or not in use.

Note 4-6: Please resend the SPI command at one frame interval.

4.3.4 Power Sequence for Backlight

Digital signal is the BLU ON signal.



Input Timing

No	Description	Symbol	Min	Typ	Max	Unit	Note
1	VDDB1 Rising Time	T_{R1}	1	-		[ms]	
2	VDDB3 delay time	T_{D3V}	0	-		[ms]	
3	ACT_CARD turn on delay time	T_{DACT_ON}	75	-		[ms]	
4	Digital Signal delay time	T_{DDGS}	10	-		[ms]	
5	ACT_CARD turn off delay	T_{DACT_OFF}	-50	10		[ms]	

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	***Note 5-1***
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	***Note 5-2***
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

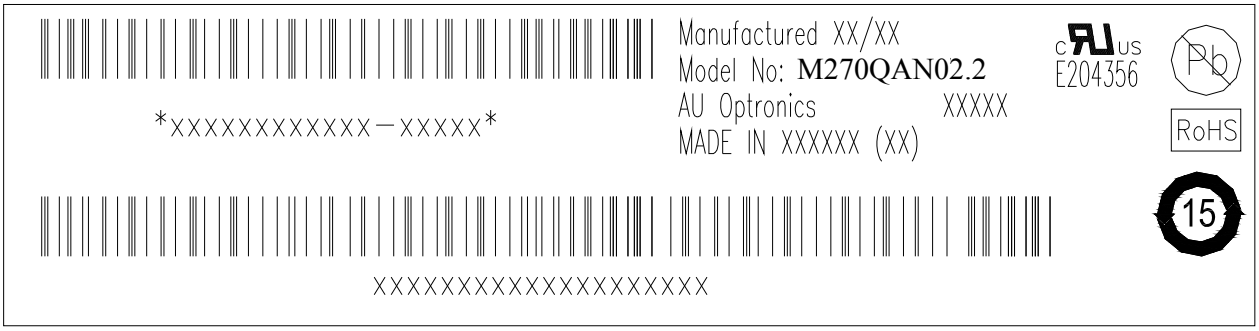
Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed No data lost
Self-recoverable
No hardware failures.

Note5-3: Result Evaluation Criteria: TFT-LCD panels test should take place after gradually cooling enough at room temperature. In the normal application, there should be no particular problems that may affect the display function.

6 Shipping Label

The label is on the panel as shown below:



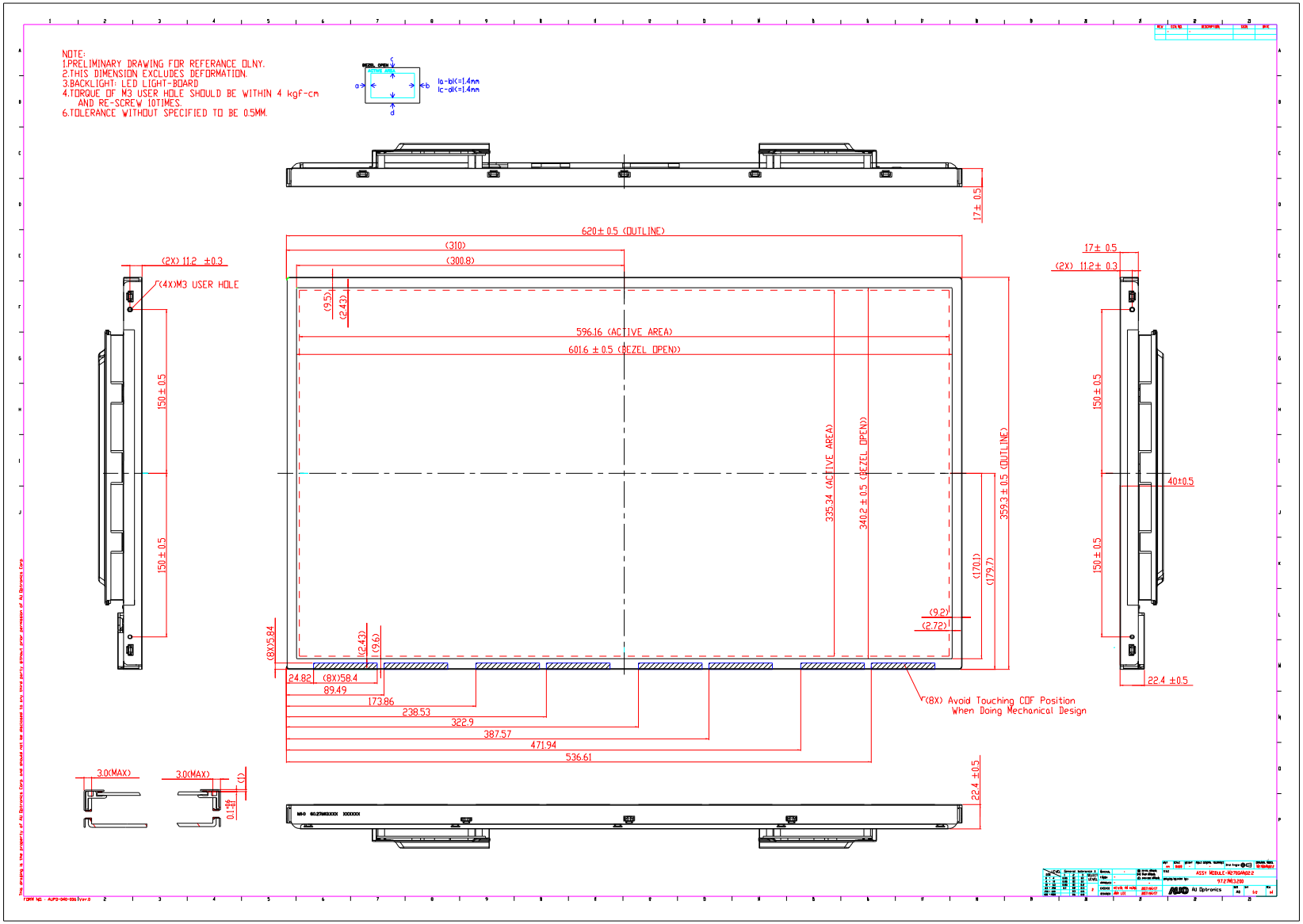
Note 6-1: For Pb Free products, AUO will add for identification.

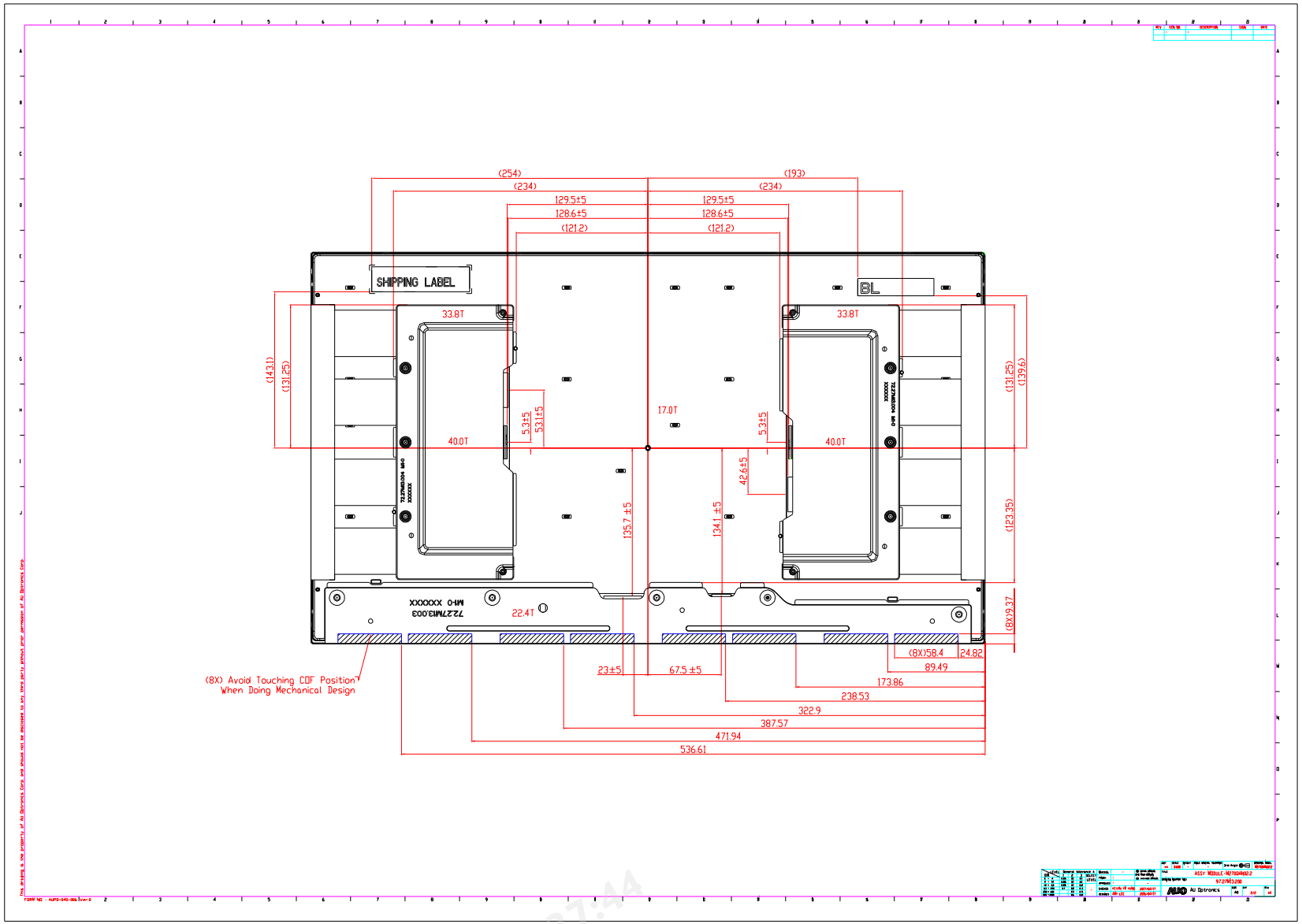
Note 6-2: For RoHS compatible products, AUO will add for identification.

Note 6-3: For China RoHS compatible products, AUO will add for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

7 Mechanical Characteristics

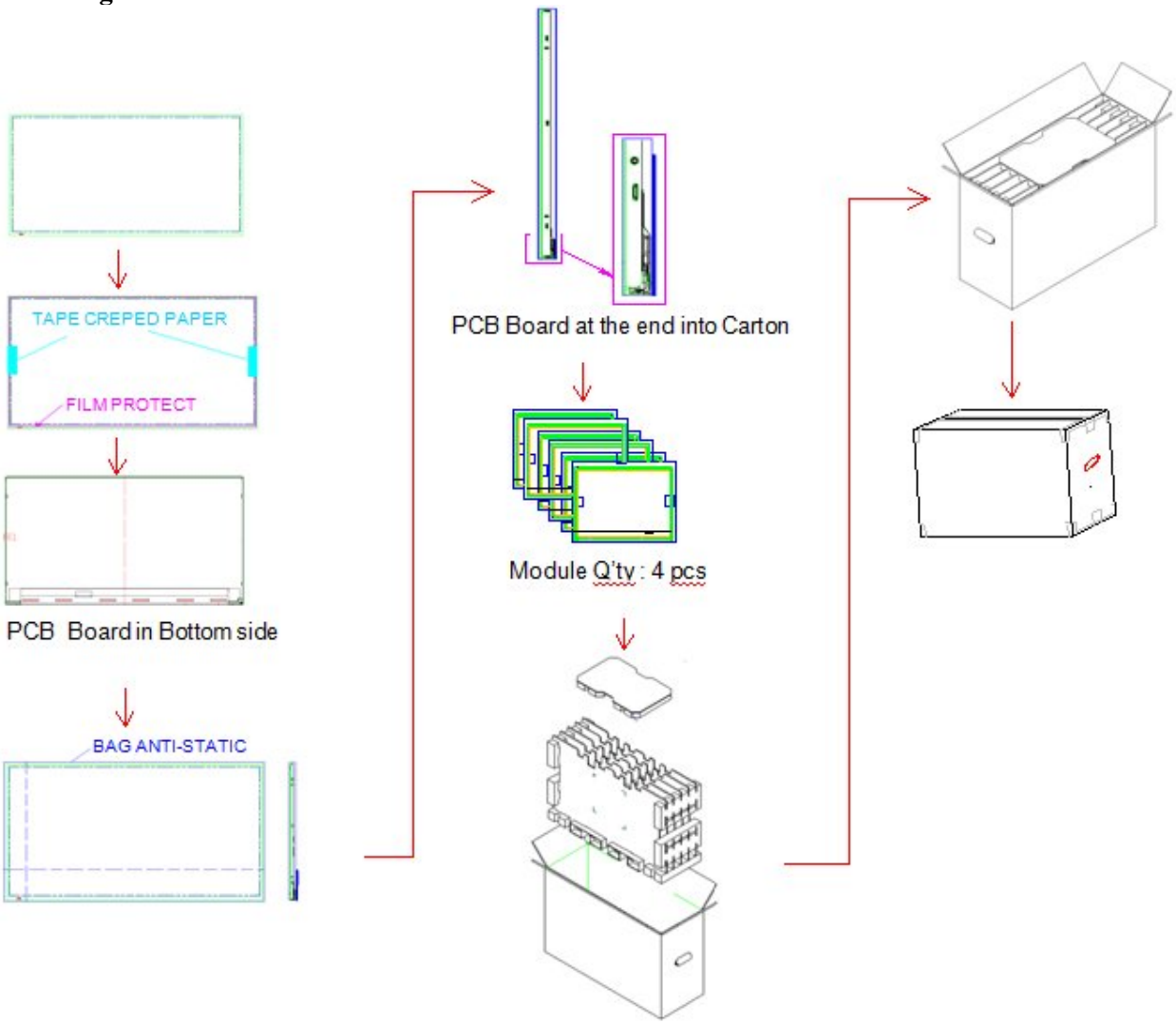


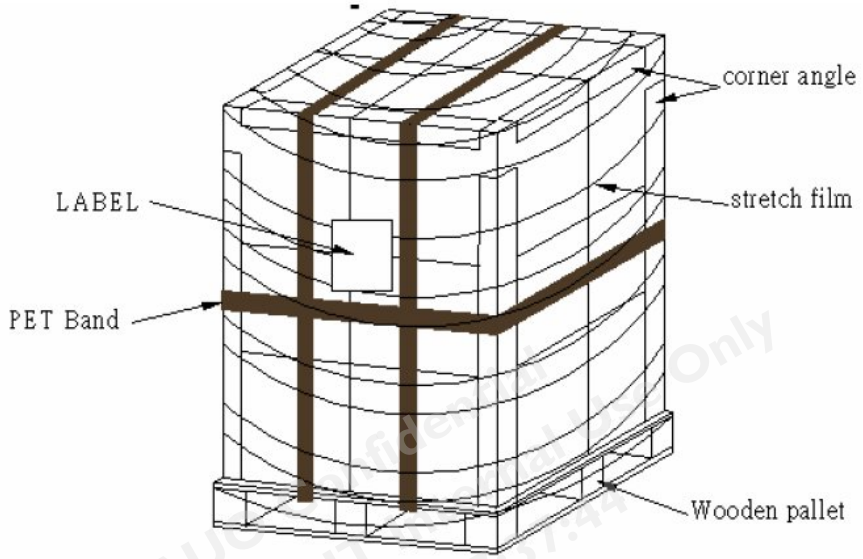

(254)
(234)
129.5±5
128.6±5
(121.2)
(193)
(234)
129.5±5
128.6±5
(121.2)
SHIPPING LABEL
BL
33.8T
33.8T
(143.1)
(131.25)
(131.25)
(139.6)
17.0T
40.0T
40.0T
5.3±5
53.1±5
5.3±5
42.6±5
135.7 ±5
134.1 ±5
(123.35)
22.4T
(8X)9.37
(8X)58.4
24.82
89.49
173.86
238.53
322.9
387.57
471.94
536.61
23±5
67.5 ±5
(8X) Avoid Touching COF Position
When Doing Mechanical Design

Ver 0.1

8 Packing Specification

8.1 Packing Flow





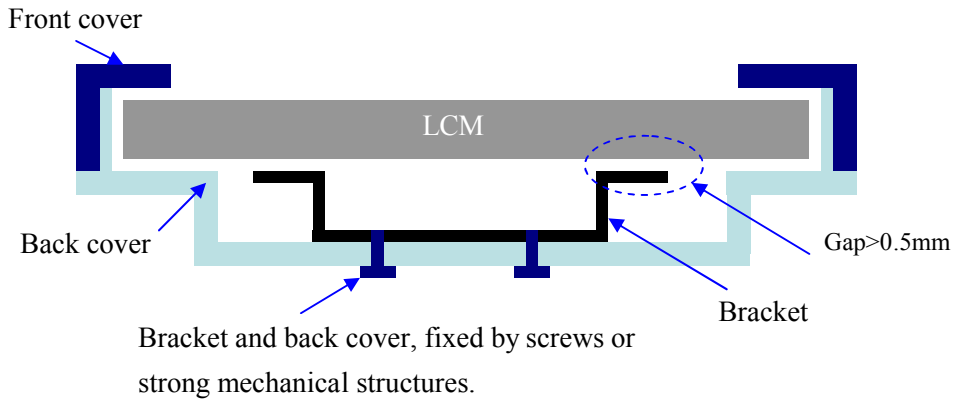
8.2 Pallet and shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight (kg)	
Panel	1	620.0(H)mm × 359.3(V)mm × 40.0(D)mm	3.85	
Cushion	1	-	0.85	
Box	1	723(L)mm x 265(W)mm x 463(H)mm	1.3	without Panel & cushion
Packing Box	4 pcs/Box	723(L)mm x 265(W)mm x 463(H)mm	17.55	with panel & cushion
Pallet	1	1070(L)mm x 740(W)mm x 132(H)mm	14.8	
Pallet after Packing	8 boxes/pallet	1070(L)mm x 740(W)mm x 1086(H)mm	155.2	

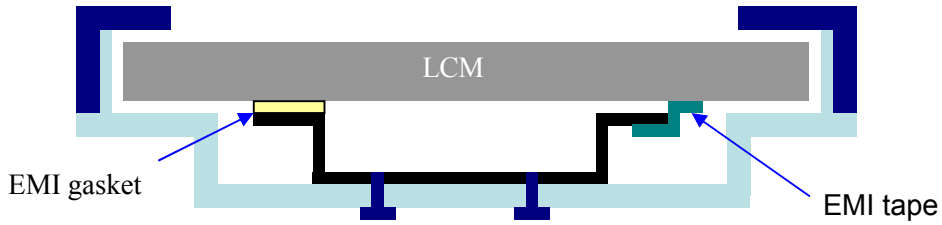
9 Design Guide for System

9.1 The gap between LCM and system rear bracket should be bigger than 0.5mm.

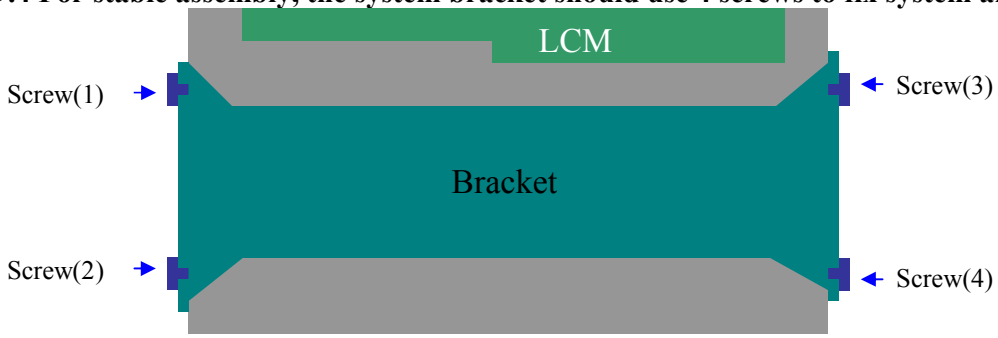
9.2 The system bracket should be fixed on back cover firmly.



9.3 The EMI gasket should be uniform and not push panel strongly.

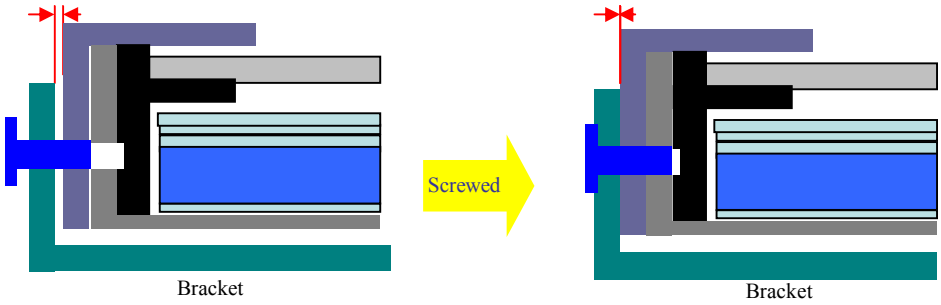


9.4 For stable assembly, the system bracket should use 4 screws to fix system and panel by dual sides.



9.5 The system bracket and panel should be in parallel with having no gap after inserting screws.

Proper and Parallel gap	0 gap and no mechanical damage



9.6 Avoid scratching LCM, the rib on system front-cover should not exceed the bottom edge of LCM's front-bezel.