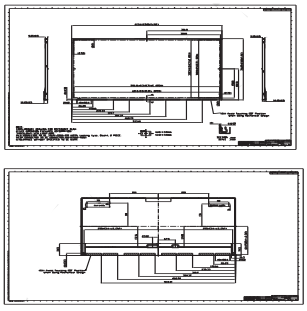
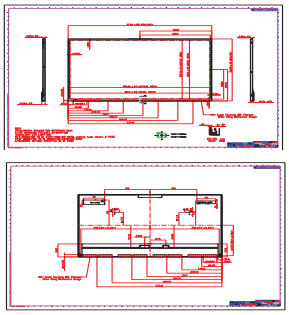
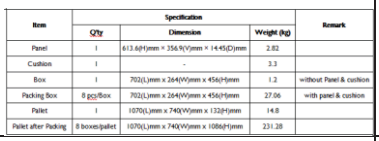
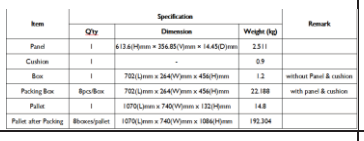
( ) Preliminary Specification
(V) Final Specification

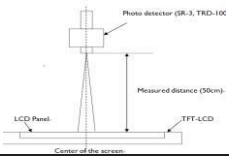
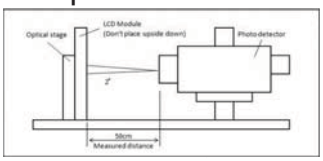
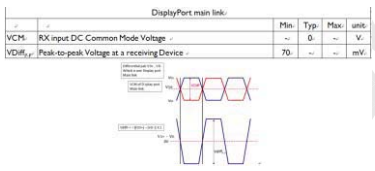
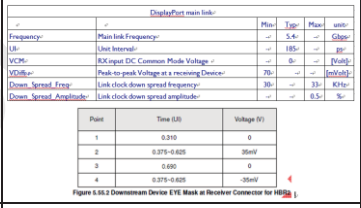
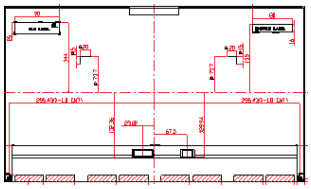
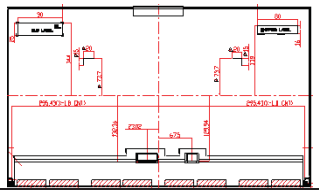
Module	**27.0" Color TFT-LCD**
Model Name	**M270QAN02.3**

Customer	**Date**	**Approved by**	**Date**
			August 7, 2018
Approved by		**Prepared by**	**Date**
			August 7, 2018
Note: This Specification is subject to change without notice.		AU Optronics corporation	

Contents

Record of Revision

Version	Date	Page	Old description	New Description	Remark
0.1	2018/2/8	All			
0.2	2018/4/30	5	The module weight is 2820 +/- 80g	The module weight is 2511 +/- 125g	
		8	-	Add color coordinates	
		29/30		Update backlight diagram and LED connector pin defin	
		37/38	Mechanical Characteristics 	Mechanical Characteristics 	
		39	Packing information 	Packing information 	
0.3	2018/5/22	9	-	Add Note2-1 condition	
		32	-	Add Note4-8	
		34	-	Update Note4-4 test condition	

0.4	2018/8/7	9	Red x 0.650 0.680 0.710 Red y 0.278 0.308 0.338 Green x 0.229 0.259 0.289 Green y 0.645 0.675 0.705 Blue x 0.122 0.152 0.182 Blue y 0.013 0.043 0.073 -	Red x 0.650 0.680 0.710 Red y 0.278 0.308 0.338 Green x 0.234 0.264 0.294 Green y 0.636 0.666 0.696 Blue x 0.121 0.151 0.181 Blue y 0.014 0.044 0.074 Add CIE 1976 Color Coordinates	
		9	Update Note 2-2 	Update Note 2-2 	
		41	-	Add Design Guide for System	
		21	3.4.4 eDP Specification 	3.4.4 eDP Specification 	
		-	Packing 	Packing 	
		-	Shielding Mylar 	Shielding Mylar 	
		5	-	Add Handling Precautions 14	
1.0	2018/8/10			Final Version	

1 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
12) Please avoid touching COF position while you are doing mechanical design.
13) When storing modules as spares for a long time, the following precaution is necessary:
    Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.
14) When this reverse-type model(PCBA on bottom side) is used as forward-type model(PCBA on top side),AUO can not guarantee any defects of LCM

2 General Description

This specification applies to the 27.0 inch wide Color a-Si TFT-LCD Module M270QAN02.3. The display supports the UHD - 3840(H) x 2160(V) screen format and 16.7M colors (8 bits RGB data input). The input interface is 8-lanes eDP and this module doesn't contain an driver board for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25°C condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	684 (26.93")
Active Area	[mm]	596.16 (H) x 335.34 (V)
Pixels H x V	-	3840x3(RGB) x 2160
Pixel Pitch	[um]	155.25 (per one triad) × 155.25
Pixel Arrangement	-	R.G.B. Vertical Stripe
Display Mode	-	AHVA Mode (Advanced Hyper-Viewing Angle), Normally Black
HDR off White Luminance (Center)	[cd/m^2]	350 (Typ.) @HDR off
HDR on White Luminance (Center)	[cd/m^2]	400 (Typ.) @HDR on
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	12 (Typ., Gray to Gray)
Power Consumption (LCD Module + Backligh unit)	[Watt]	Total = 40.87 W(Typ.) LCD module : PDD (Typ.) =8.57W @ white pattern, 144Hz, 12 V Backlight unit : PBLU (Typ.) =32.3W @ Is=90mA and HDR off mode
Weight	[Grams]	2511 +/-125
Outline Dimension	[mm]	613.6 (H) x 356.9 (V) × 14.45(D)
Electrical Interface	-	8-lanes eDP , 8bits RGB data input
Support Color	-	16.7M colors
Surface Treatment	-	Anti-Glare, 3H, Haze 25%
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance

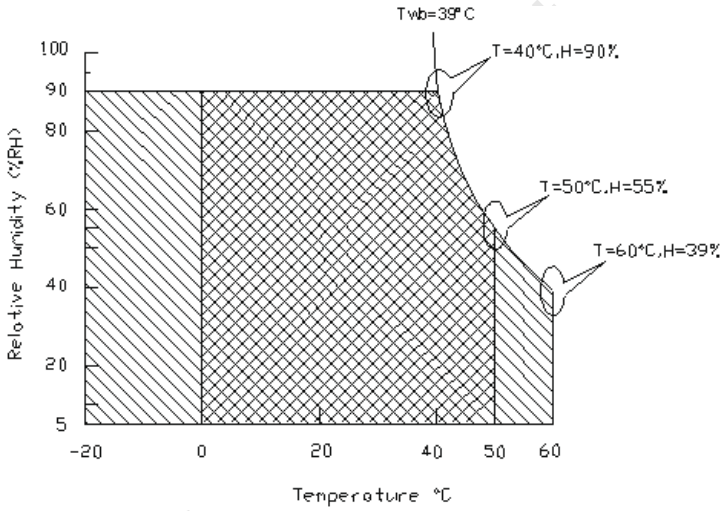
2.2 Absolute Maximum Rating of Environment

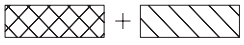
Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	***Note 2-1***
TGS	Glass surface temperature (operation)	0	+65	[°C]	***Note 2-1*** *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	***Note 2-1***
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta ≦39℃)
2. Max wet-bulb temperature at 39℃ or less. (Ta ≦39℃)
3. No condensation
4. LED string current is typical value



Operating Range  Storage Range 

2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

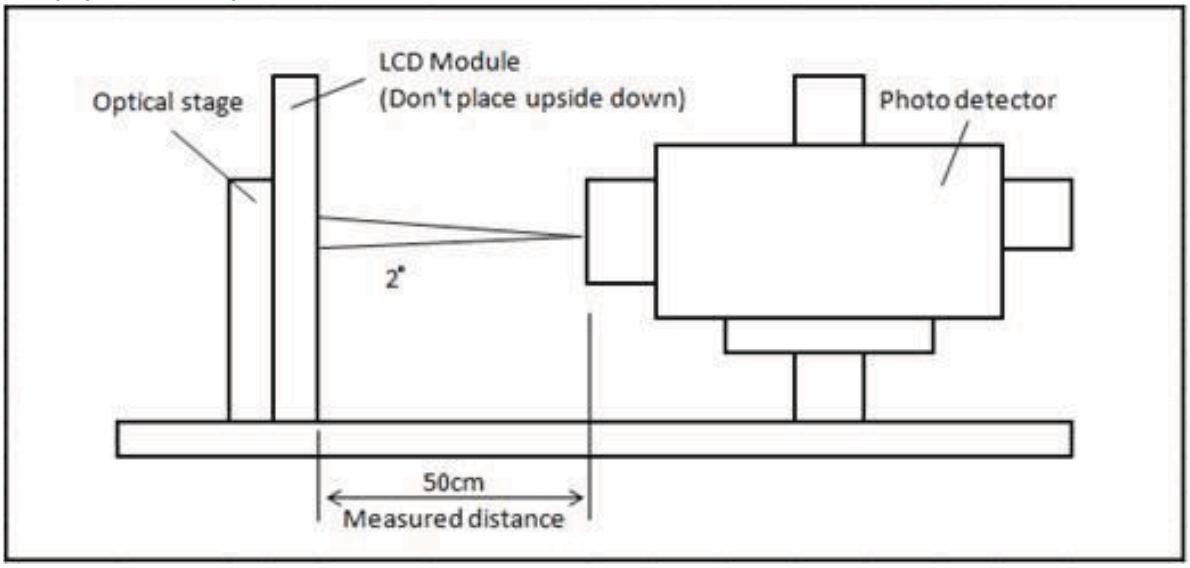
Test Condition:

1. Equipment setup: Please refer to ***Note 2-2***.
2. Panel Lighting time: 30 minutes
3. VDD=12.0V, Fv=60Hz, Ta=25°C

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_w	White Luminance (Center of screen)		280	350	-	[cd/m2]	***@ HDR off*** ***Note 2-2*** ***Note 2-3*** *By SR-3*
L_{wI}	White Luminance (Center of screen)		320	400	-	[cd/m^2]	***@ HDR on*** ***Note 2-2*** ***Not 2-4*** *By SR-3*
L_{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	***Note 2-5*** *By SR-3*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	***Note 2-6*** *By SR-3*
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	***Note 2-7*** *By SR-3*
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	75	89	-		
Φ_L		Down	75	89	-		
T_{GTG}	Response Time	Gray to Gray	-	12	-	[msec]	***Note 2-8*** *By TRD-100*
R_x	Color Coordinates (CIE 1931)	Red x	0.650	0.680	0.710	-	*By SR-3*
R_y		Red y	0.278	0.308	0.338		
G_x		Green x	0.234	0.264	0.294		
G_y		Green y	0.636	0.666	0.696		
B_x		Blue x	0.121	0.151	0.181		
B_y		Blue y	0.014	0.044	0.074		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
Ru'	Color Coordinates (CIE 1976)	Red u'	-	0.510	-		By SR-3
Rv'		Red v'	-	0.519	-		

Gu'		Green u'	-	0.101	-		
Gv'		Green v'	-	0.573	-		
Bu'		Blue u'	-	0.187	-		
Bv'		Blue v'	-	0.123	-		
Wu'		White u'	-	0.191	-		
Wv'		White v'	-	0.485	-		
DCIP3			-	90	-	[%]	*By SR-3*

Note 2-2: Equipment setup:



Note 2-3: LED current condition @HDR off Is=90mA.

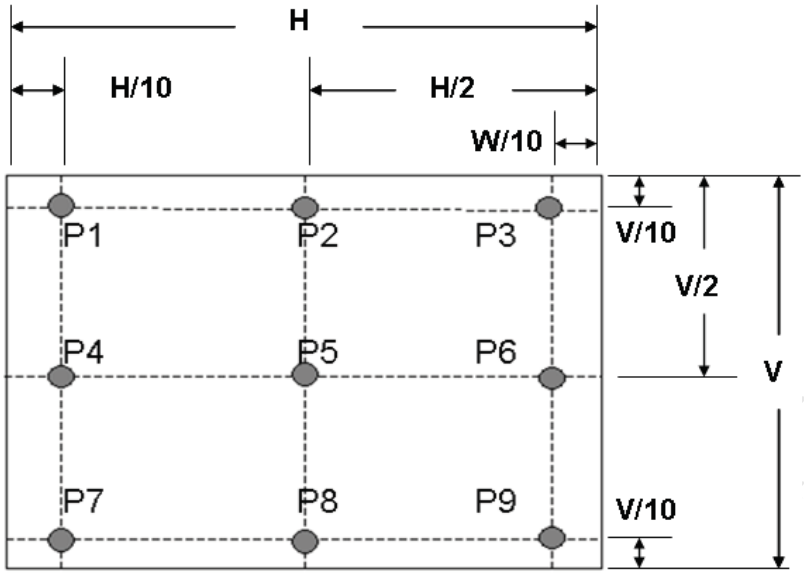
Note 2-4: LED current condition @HDR on Is=100mA.

Note 2-5: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformit y} = \frac{\text{Minimum Luminance of 9 Points (P1} \sim \text{P9)}}{\text{Maximum Luminance of 9 Points (P1} \sim \text{P9)}}$$

a. Test pattern: White Pattern



Note 2-6: Contrast Ratio Measurement

Definition:

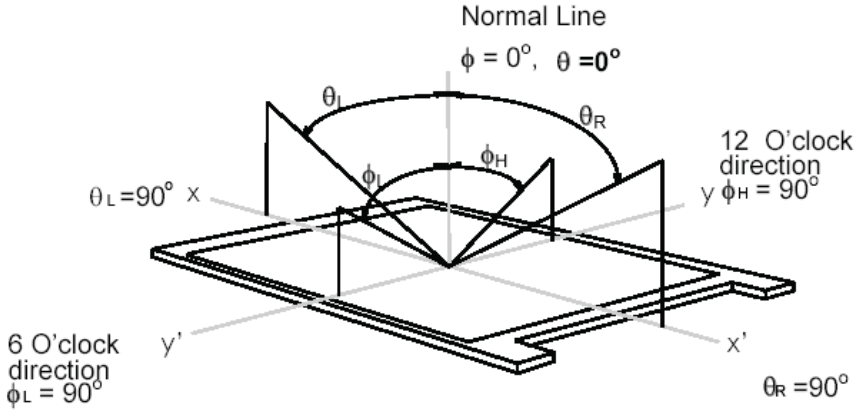
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

Note 2-7: Viewing angle measurement

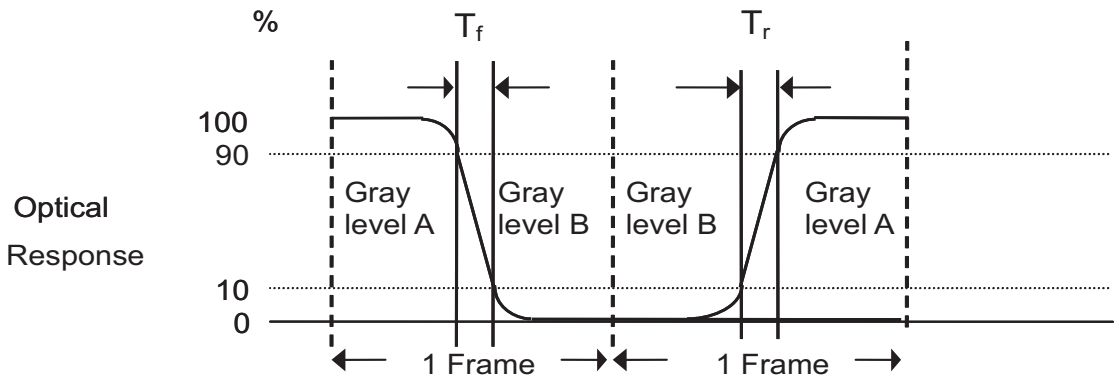
Definition: The angle at which the contrast ratio is greater than 10 & 5 .

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)



Note 2-8: Response time measurement

The output signals of photo detector are measured when the input signals are changed from "Gray level A" to "Gray level B" (falling time, T_f), and from "Gray level B" to "Gray level A" (rising time, T_r), respectively. The response time is interval between the 10% and 90% of optical response.



The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

- T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

Note 2-9: Evaluation test and mass production inspection shall be applied with LED current Is @ HDR off condition if there is not specified condition.

2.4 Mechanical Characteristics

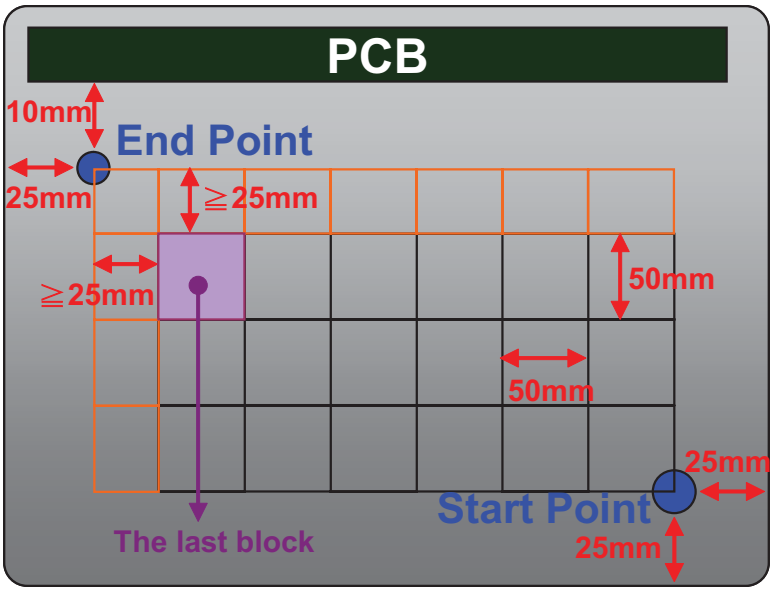
Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	***Note 2-10***

Note 2-10: Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

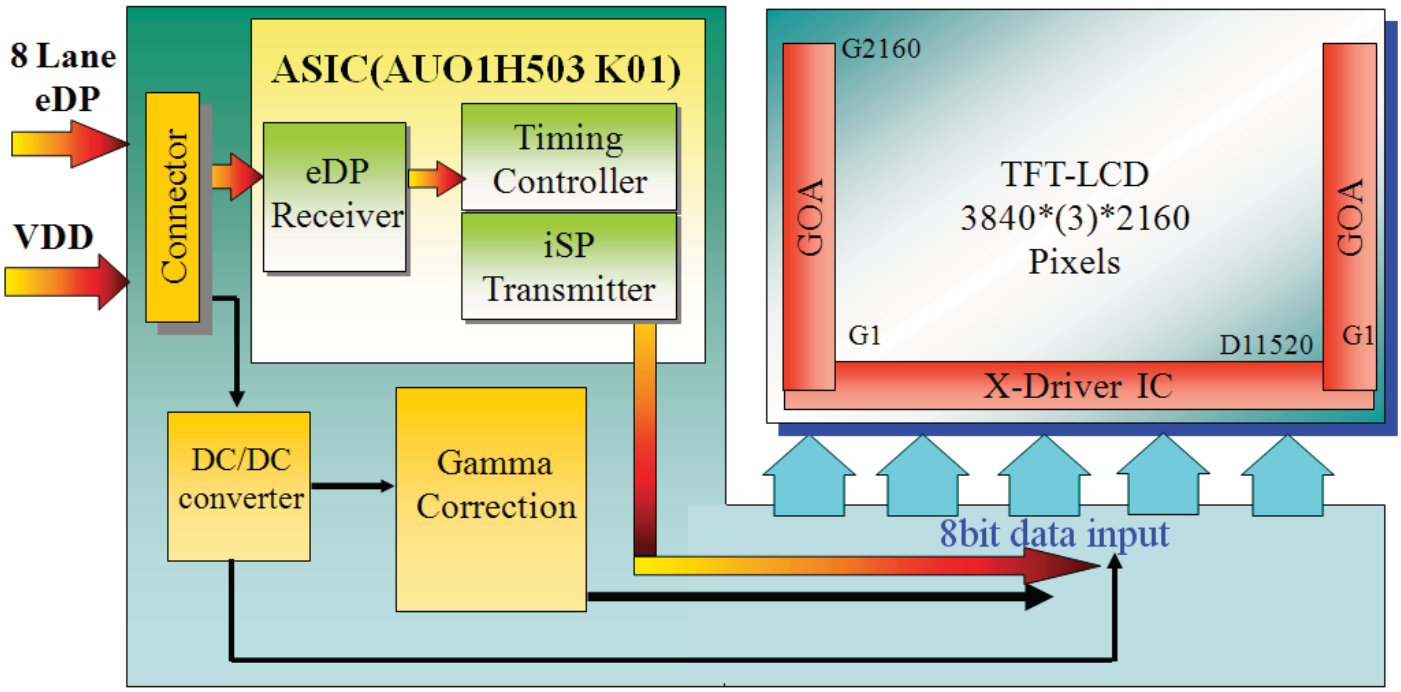
If the distance from the last block to each side of the End Point ≧ 25mm, add other blocks to make sure that most area of Bezel Back can be measured.



3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 27.0 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

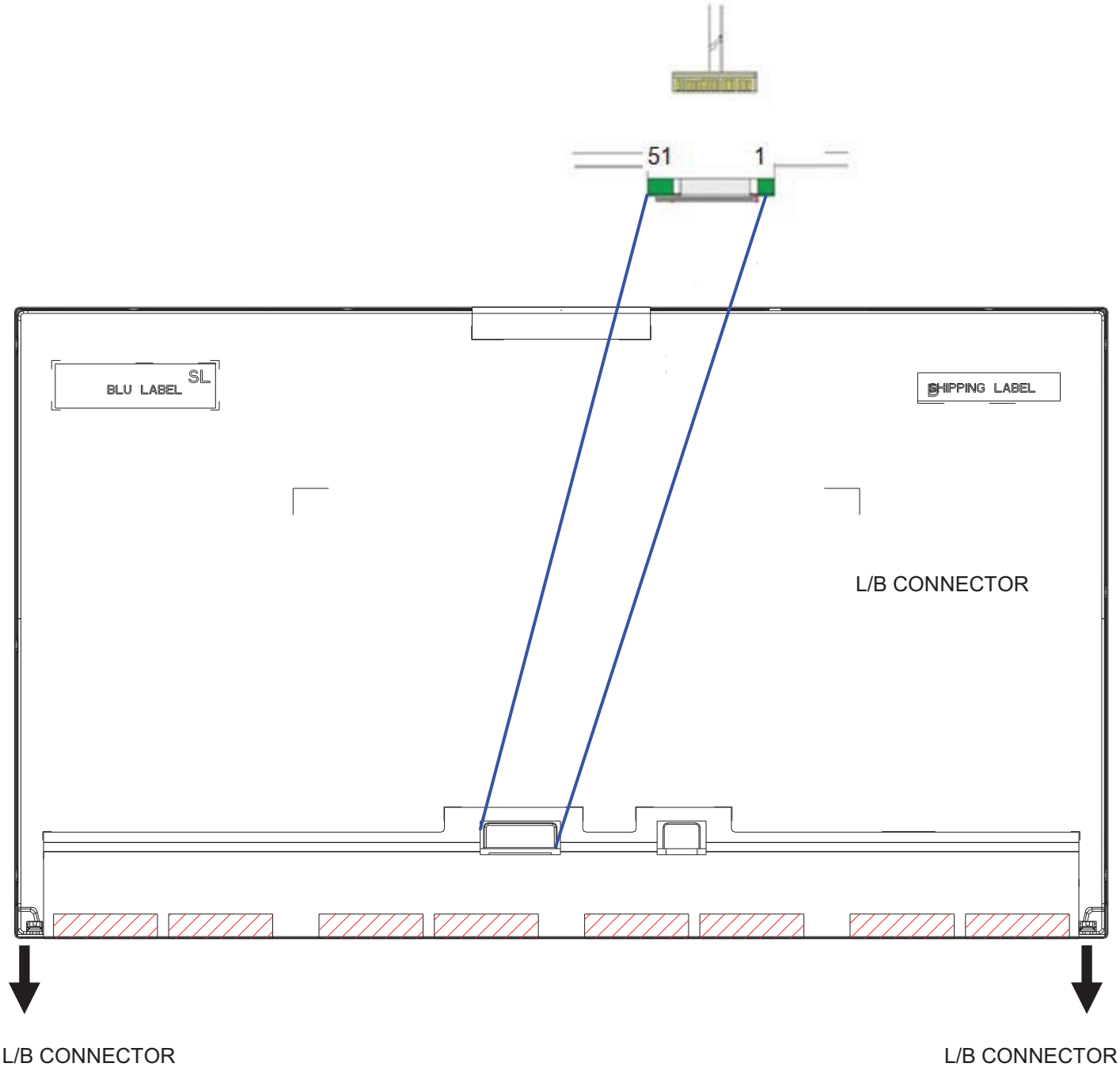
TFT-LCD Connector	Manufacturer	P-TWO	JAE	STARCONN
	Part Number	187059-5122	FI-RTE51SZ-HF	115E51-0000RA-M3-R
Mating Connector	Manufacturer	JAE		
	Part Number	FI-RE51CL		

3.2.2 Connector Pin Assignment

PIN #	Symbol	Description	Remark
1	VDD	Power +12V	
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	NC	No connection (for AUO test only. Do not connect)	
10	NC	No connection (for AUO test only. Do not connect)	
11	NC	No connection (for AUO test only. Do not connect)	
12	NC	No connection (for AUO test only. Do not connect)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	NC	No connection (for AUO test only. Do not connect)	
16	NC	No connection (for AUO test only. Do not connect)	
17	GND	Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	
20	GND	Ground	

21	1st Lane2_N	Negative eDP differential data input	
22	1st Lane2_P	Positive eDP differential data input	
23	GND	Ground	
24	1st Lane1_N	Negative eDP differential data input	
25	1st Lane1_P	Positive eDP differential data input	
26	GND	Ground	
27	1st Lane0_N	Negative eDP differential data input	
28	1st Lane0_P	Positive eDP differential data input	
29	GND	Ground	
30	1st AUX_CH_P	Positive AUX Channel differential data input	
31	1st AUX_CH_N	Negative AUX Channel differential data input	
32	GND	Ground	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	2nd Lane3_N	Negative eDP differential data input	
36	2nd Lane3_P	Positive eDP differential data input	
37	GND	Ground	
38	2nd Lane2_N	Negative eDP differential data input	
39	2nd Lane2_P	Positive eDP differential data input	
40	GND	Ground	
41	2nd Lane1_N	Negative eDP differential data input	
42	2nd Lane1_P	Positive eDP differential data input	
43	GND	Ground	
44	2nd Lane0_N	Negative eDP differential data input	
45	2nd Lane0_P	Positive eDP differential data input	
46	GND	Ground	
47	2nd AUX_CH_P	Positive AUX Channel differential data input	
48	2nd AUX_CH_N	Negative AUX Channel differential data input	
49	GND	Ground	

50	HPD	Hot plug detection	
51	GND	Ground	



Note 3-1: Input signals of port 1 to port 4 clocks shall be the same timing.

3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

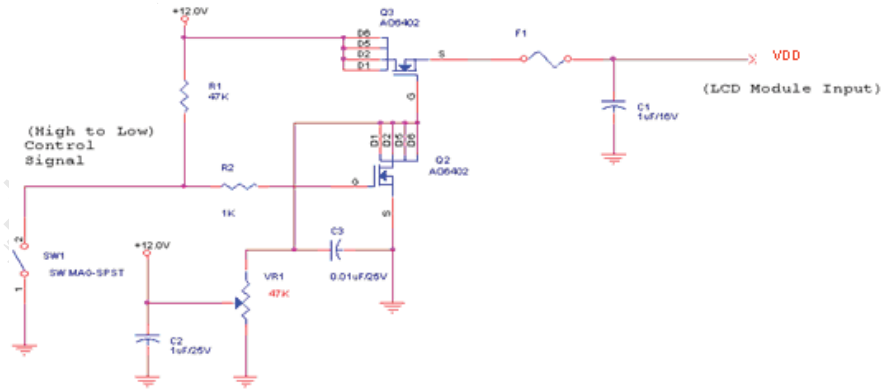
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25°C

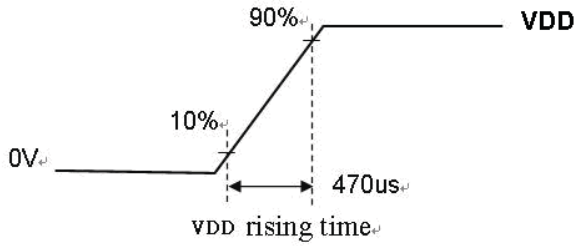
3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.71	1.75	[A]	VDD= 12.0V, White pattern, Fv=144Hz
			0.65	1.53		VDD= 12.0V, White pattern, Fv=120Hz
PDD	VDD Power Consumption	-	8.57	21.68	[Watt]	VDD= 12.0V , White pattern, Fv=144Hz
			7.80	18.36		VDD= 12.0V, White pattern, Fv=120Hz
IRush	Inrush Current	-	-	3	[A]	***Note 3-2***
VDDrp	Allowable VDD Ripple Voltage	-	-	VDD*5%	[mV]	VDD= 12.0V, White pattern, Fv=144Hz

Note 3-2: Inrush Current measurement:

Test circuit:



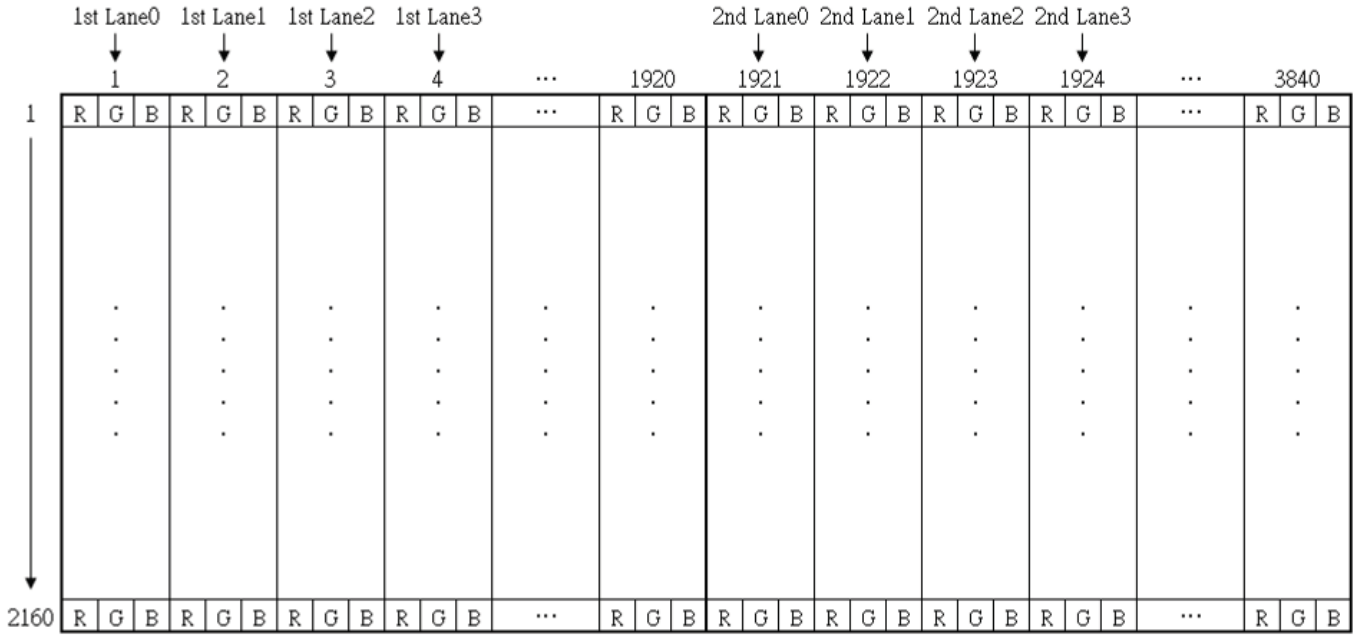


The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.



Note 3-3: The module use 8-Lanes eDP interface.

1st port:

1st Lane0：1+4n pixel

1st Lane1：2+4n pixel

1st Lane2：3+4n pixel

1st Lane3：4+4n pixel

2nd port:

2nd Lane0：1921+4n pixel

2nd Lane1：1922+4n pixel

2nd Lane2：1923+4n pixel

2nd Lane3：1924+4n pixel

n=0~479

3.4.2 eDP Data Format

1st Lane0	1st Lane1	1st Lane2	1st Lane3
R1-7:0	R2-7:0	R3-7:0	R4-7:0
G1-7:0	G2-7:0	G3-7:0	G4-7:0
B1-7:0	B2-7:0	B3-7:0	B4-7:0
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-7:0	G6-7:0	G7-7:0	G8-7:0
B5-7:0	B6-7:0	B7-7:0	B8-7:0
R9-7:0	R10-7:0	R11-7:0	R12-7:0
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-7:0	B10-7:0	B11-7:0	B12-7:0
.	.	.	.
.	.	.	.
.	.	.	.

2nd Lane0	2nd Lane1	2nd Lane2	2nd Lane3
R1921-7:0	R1922-7:0	R1923-7:0	R1924-7:0
G1921-7:0	G1922-7:0	G1923-7:0	G1924-7:0
B1921-7:0	B1922-7:0	B1923-7:0	B1924-7:0
R1925-7:0	R1926-7:0	R1927-7:0	R1928-7:0
G1925-7:0	G1926-7:0	G1927-7:0	G1928-7:0
B1925-7:0	B1926-7:0	B1927-7:0	B1928-7:0
R1929-7:0	R1930-7:0	R1931-7:0	R1932-7:0
G1929-7:0	G1930-7:0	G1931-7:0	G1932-7:0
B1929-7:0	B1930-7:0	B1931-7:0	B1932-7:0
.	.	.	.
.	.	.	.
.	.	.	.

3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.1 support 5.4Gbps)

a. DisplayPort main link signal:

DisplayPort main link					
		Min	Typ	Max	unit
Frequency	Main link Frequency	-	5.4	-	Gbps
UI	Unit Interval	-	185	-	ps
VCM	RX input DC Common Mode Voltage	-	0	-	[Volt]
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	70	-	-	[mVolt]
Down_Spread_Freq	Link clock down spread frequency	30	-	33	KHz
Down_Spread_Amplitude	Link clock down spread amplitude	-	-	0.5	%

Point	Time (UI)	Voltage (V)
1	0.310	0
2	0.375~0.625	35mV
3	0.690	0
4	0.375~0.625	-35mV

Figure 5.55.2 Downstream Device EYE Mask at Receiver Connector for HBR2

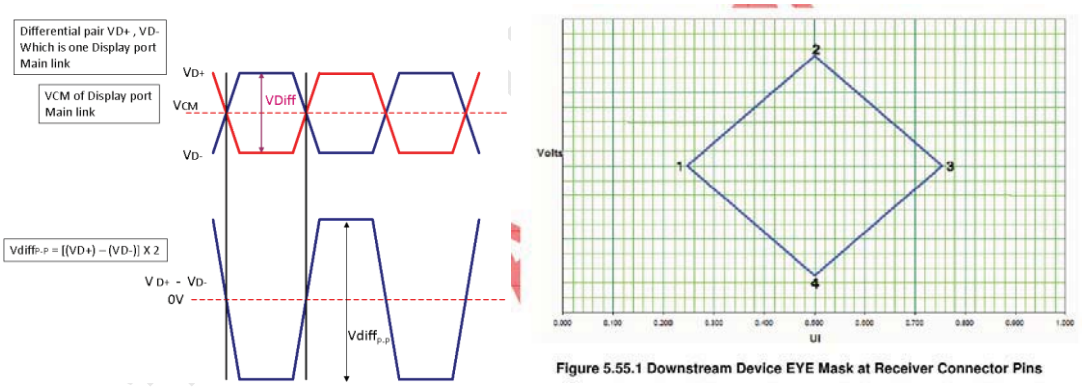
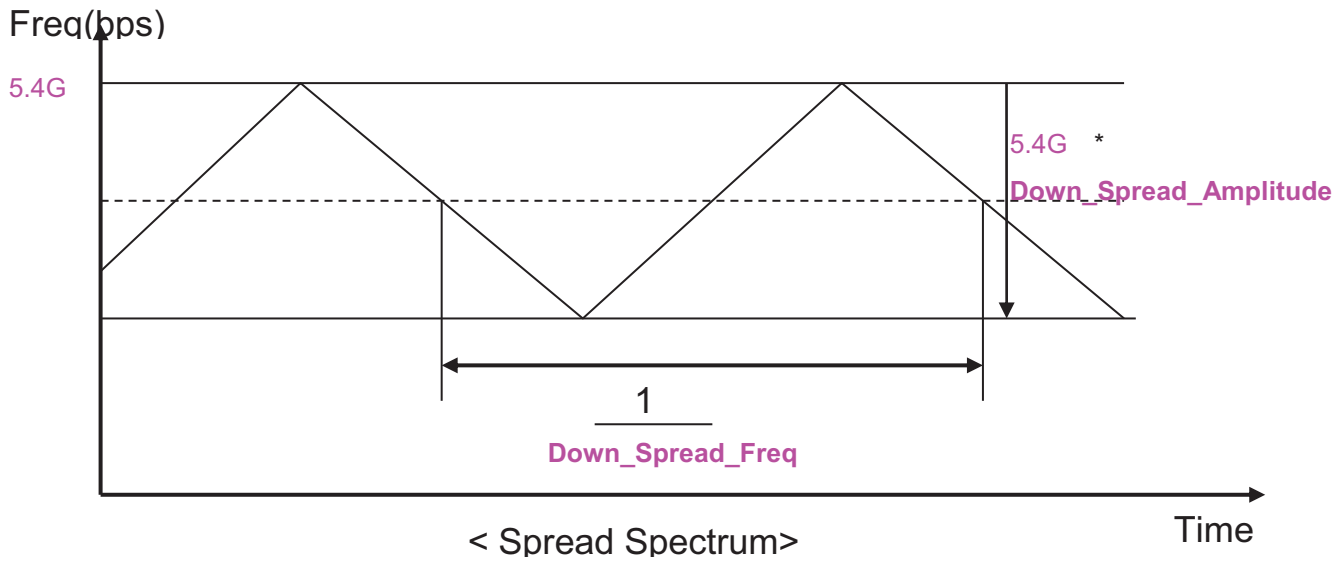
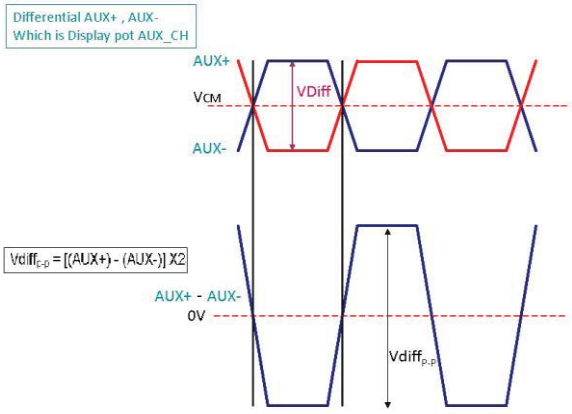


Figure 5.55.1 Downstream Device EYE Mask at Receiver Connector Pins



b. DisplayPort AUX_CH signal:

DisplayPort AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	2.0	V
$VDiff_{P-P}$	AUX Peak-to-peak voltage at a receiving device	0.27	-	1.36	V



c. DisplayPort VHPD signal:

DisplayPort VHPD					
		Min	Typ	Max	unit

VHPD	HPD Voltage	2.25	-	3.6	V

d. Intra-Pair skew

LRX-SKEW-INTRA_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTRA_PAIR	Lane Intra-pair Skew Tolerance	-	-	50	ps

e. Inter-Pair Skew

LRX-SKEW-INTER_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTER_PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	ps

3.4.5 Input Timing Specification

The input timing is shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	2180	2200	6735	Th	
Tdisp (v)		Active	2160	2160	2160	Th	
Tblk (v)		Blanking	20	40	4575	Th	
Fv		Frequency	47	120	145	Hz	***Note 3-4*** ***Note 3-7***
Th	Horizontal Section	Period	2000	2100	3520	Tclk	
Tdisp (h)		Active	1920	1920	1920	Tclk	
Tblk (h)		Blanking	80	180	1600	Tclk	
Fh		Frequency	180	264	317	kHz	***Note 3-5***
Tclk	Pixel Clock	Period	1.581	1.804	2.778	ns	1/Fclk
Fclk		Frequency	360	554	633	MHz	***Note 3-6***
Link Rate per Lane				5.4		Gbps	5.4

Note 3-4: The optimal Vertical Frequency is 119~145 Hz for best picture quality.

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.)
Fh (Typ.) = Fclk (Typ.) / Th (Typ.)
Fh (Max.)= Fclk (Max.) / Th (Min.)

Note 3-6: The equation is listed as following. Please don't exceed the above recommended value.

1st Lane N & 2nd Lane N skew < 200ns

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)

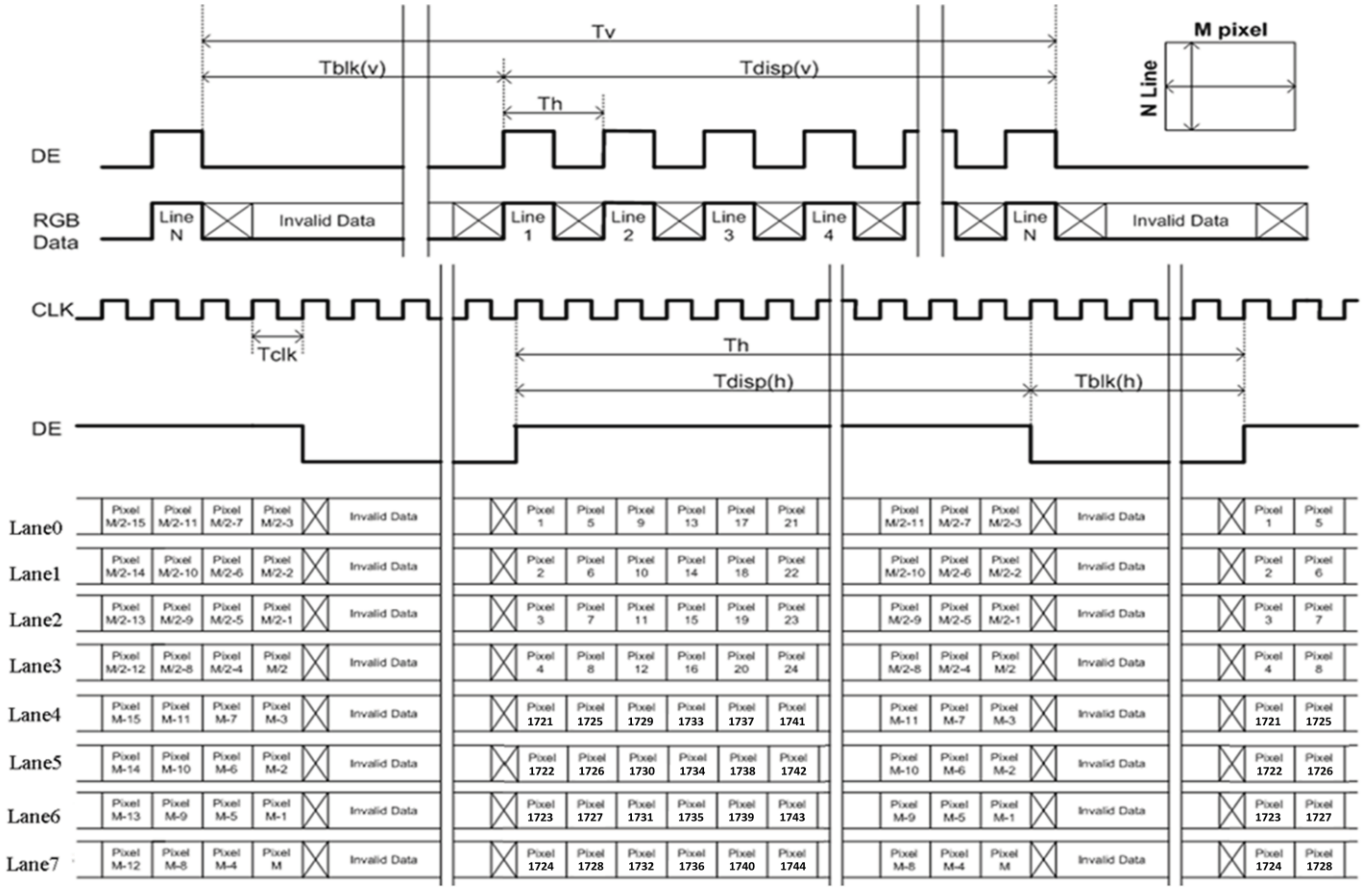
Fclk (Min.)≦Fv x Th x Tv ≦ Fclk (Max.)

Note 3-7: The equation is listed as following. Please don't exceed the above recommended value.

Fv =Fclk(Typ.) / (Tv x Th)

3.4.6 Input Timing Diagram

(Lane0~7 eDP data:1, 2, 3, 4, 1721, 1722, 1723, 1724)



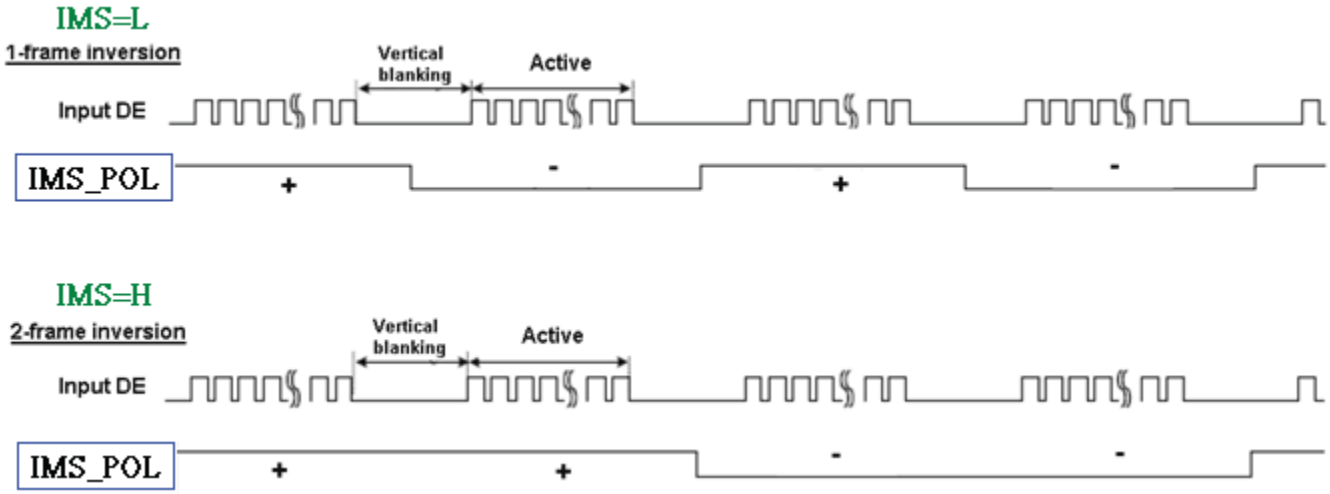
3.4.7 3D Control

3.4.7.1. 3D control I/O Characteristics

Pin #	Symbol	I/O	Buffer	Description	Remark
CN2_pin 30	IMS_POL	O	4mA	Frame Inversion polarity Index IMS=L :1-frame inversion IMS=H :2-frame inversion	***Note 3-8***
CN3_pin 30	IMS	I	IPL*	3D enable control signal	

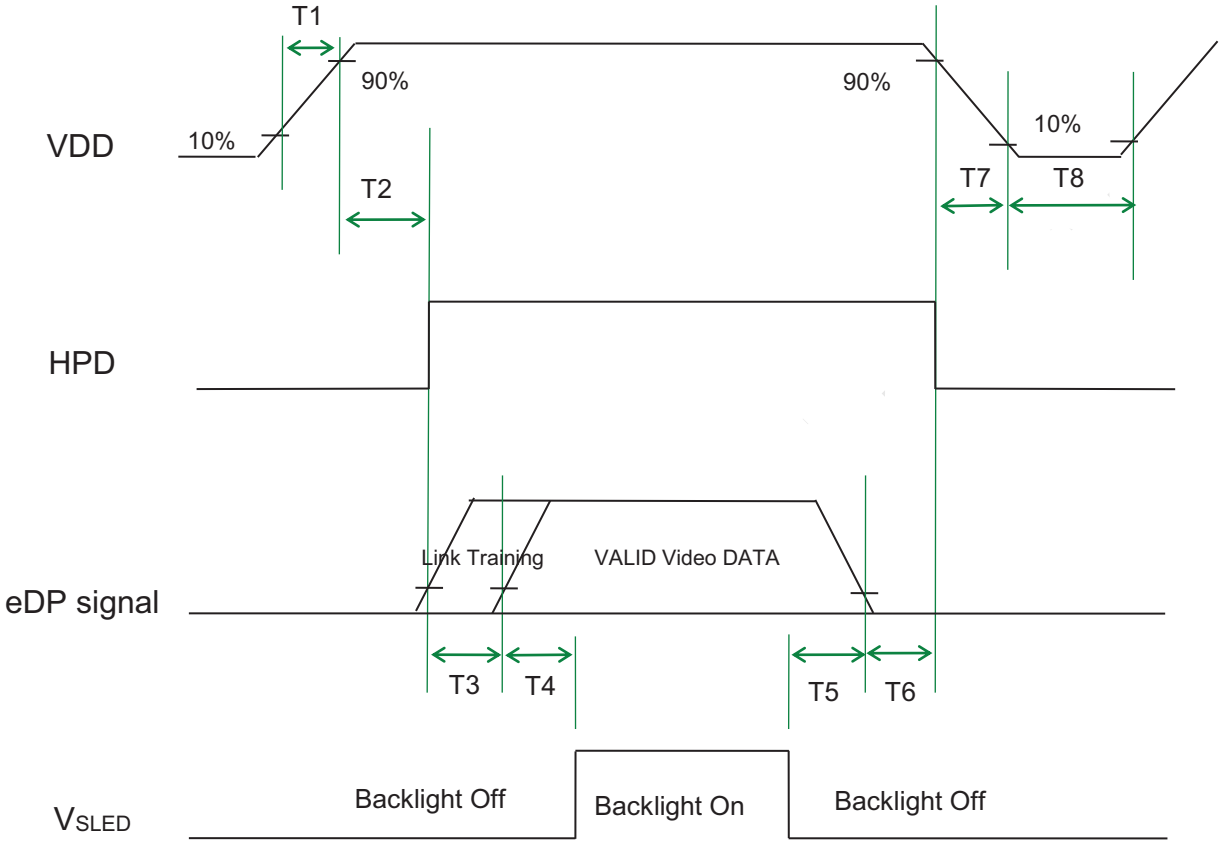
* IPL : internal pull low

Note 3-8



3.5 Power ON/OFF Sequence

VDD power,eDP signal and backlight on/off sequence are as following. eDP signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

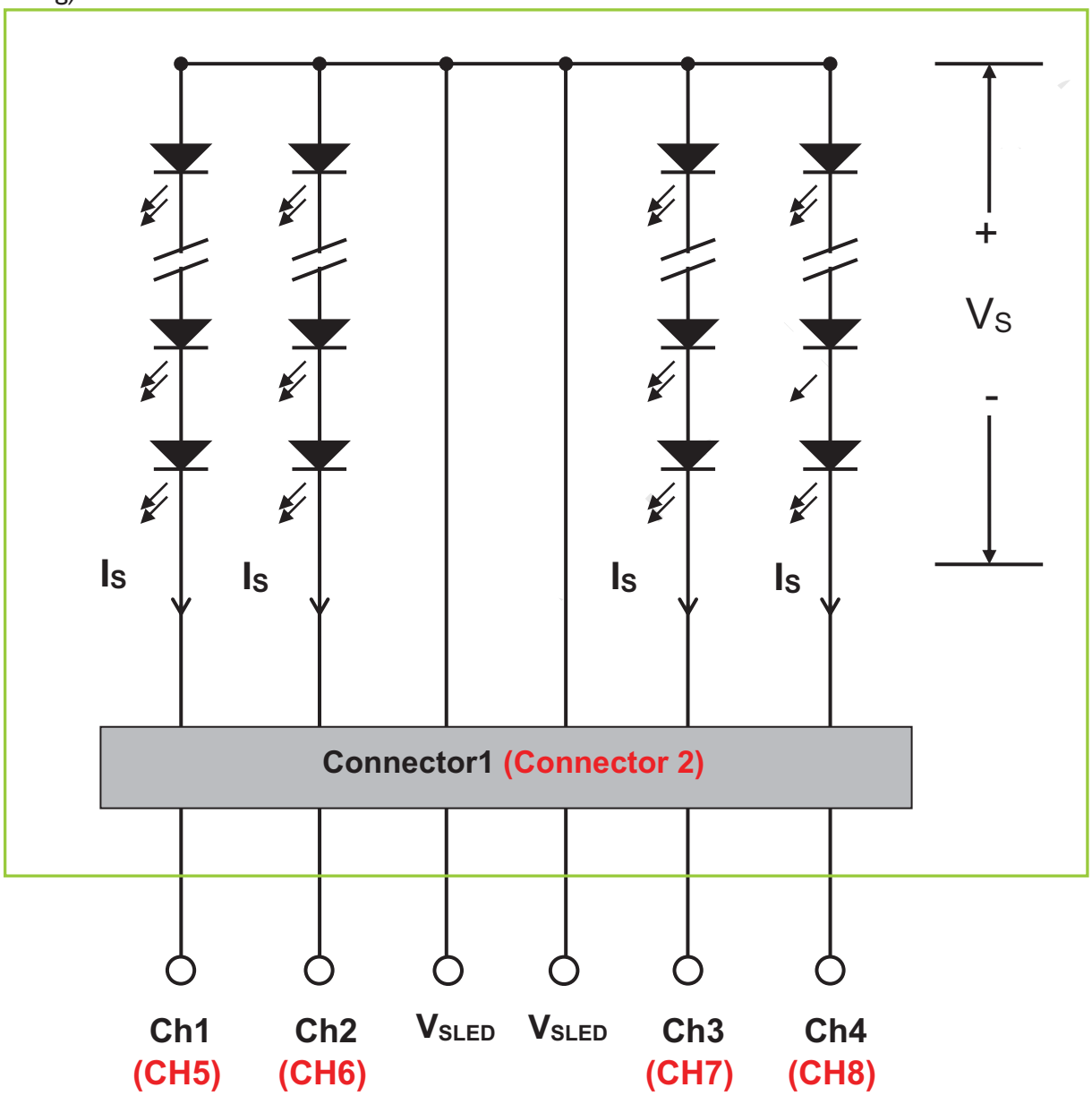
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	***Note 3-9***
T4	500	-	-	[ms]	
T5	100	-	-	[ms]	
T6	0		50	[ms]	***Note 3-10*** ***Note 3-11***
T7	0	-	200	[ms]	***Note 3-11*** ***Note 3-12***
T8	1000	-	-	[ms]	

Note 3-9: During T3 period , eDP link training time by customer's system.
Note 3-10: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.
Note 3-11: During T6 and T7 period , please keep the level of input eDP signals with Hi-Z state.
Note 3-12: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 27.0 inch Backlight Unit. Each LED light bar includes 1pcs LED light bar in Backlight Unit. Each LED light bar includes 112pcs LED package. (8 strings and 14 pcs LED of one string).



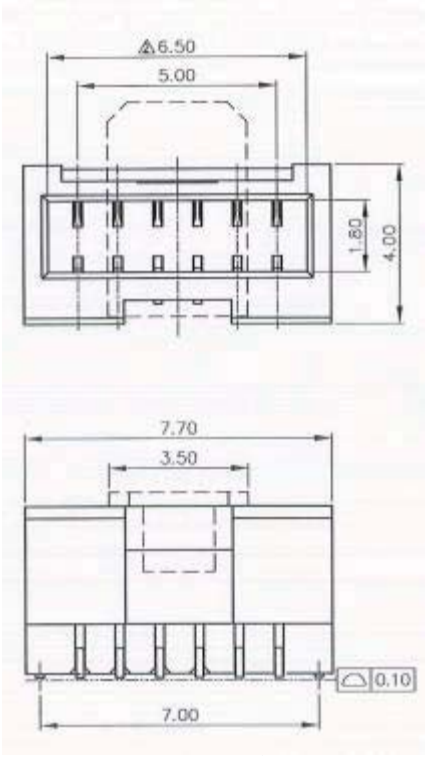
4.2 Interface Connection

4.2.1 Connector Type

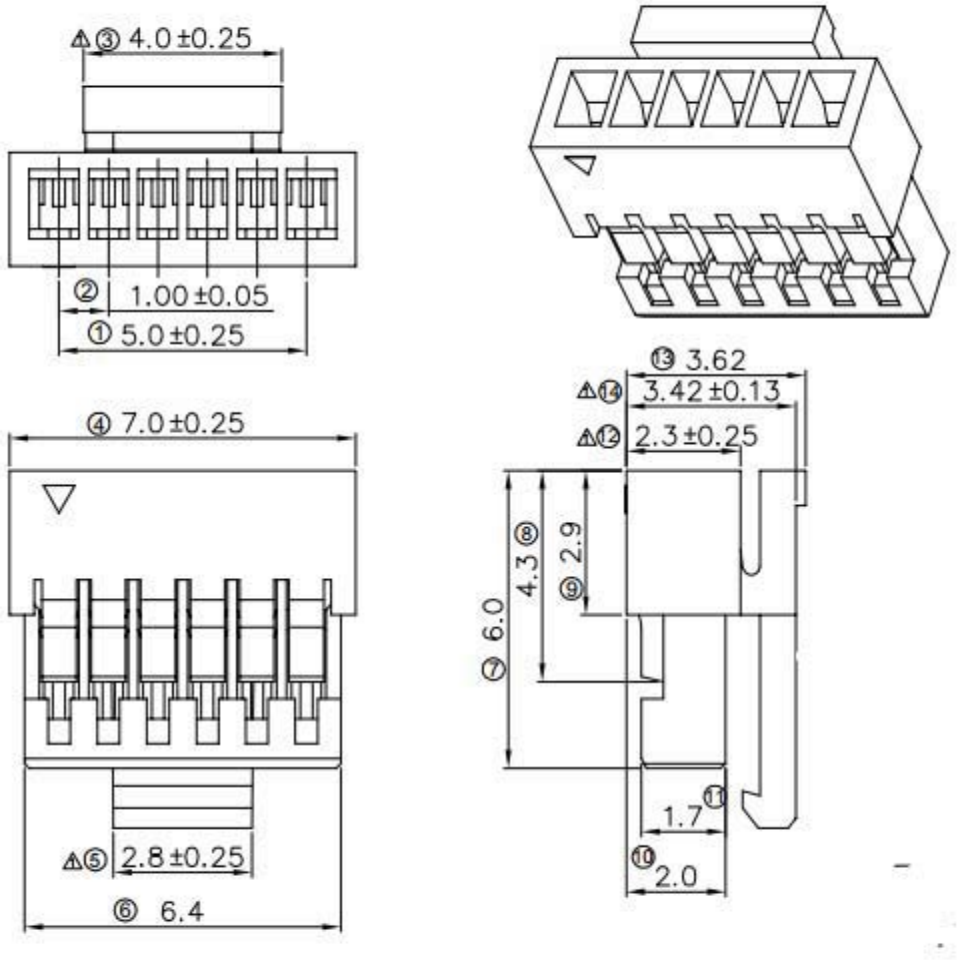
Backlight Connector	Manufacturer	ENTERY
	Part Number	3709K-Q06C-04L
Mating Connector	Manufacturer	ENTERY
	Part Number	H112K-P06N-13B (Locked type)

Backlight Connector dimension:

H x V x D=7.7 x 4 x 4.65 ,Pitch =0.75(unit=mm)



Mating Connector dimension:



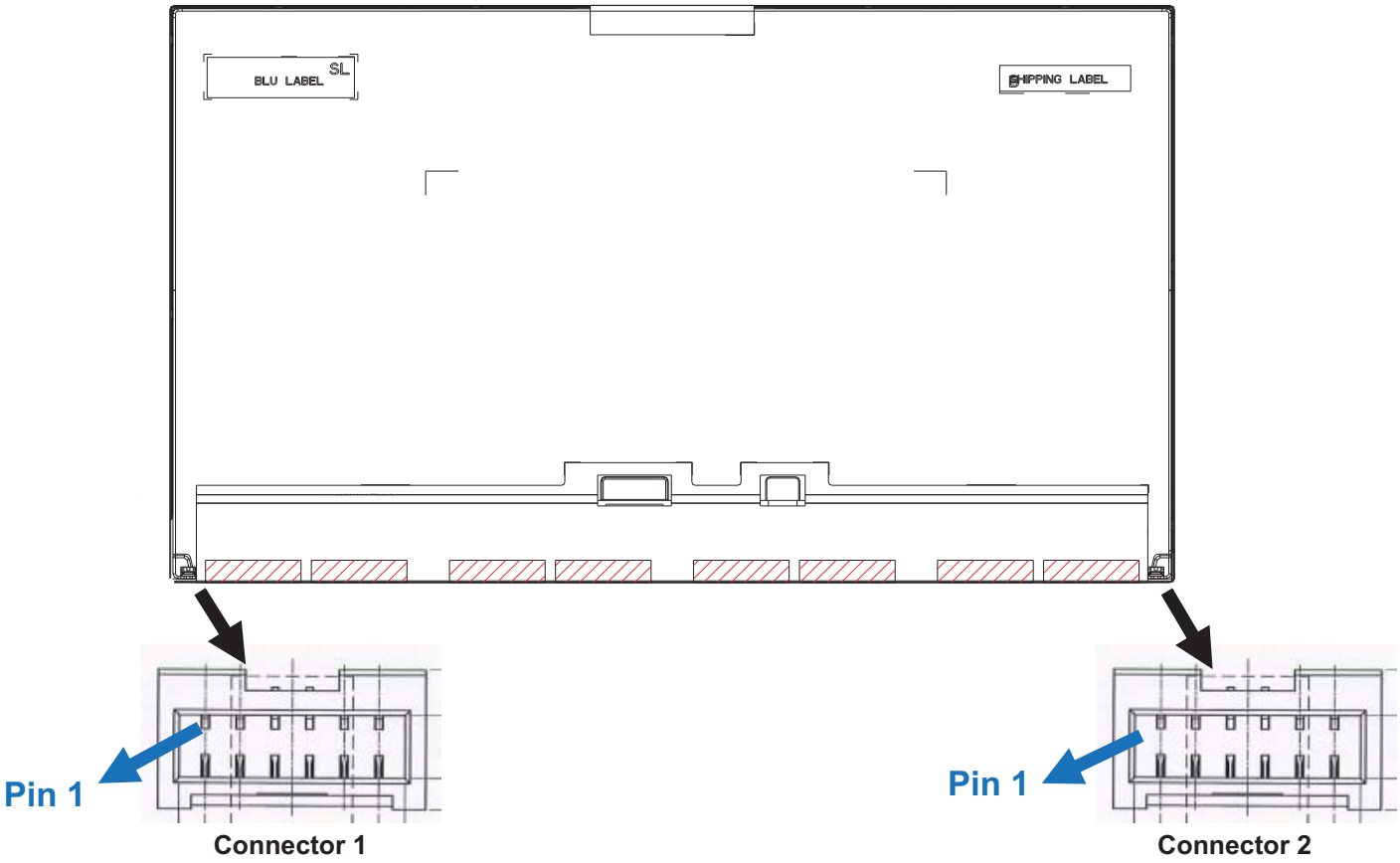
4.2.2 Connector Pin Assignment

Connector 1

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	

Connector 2

Pin#	Symbol	Description	Remark
1	Ch5	LED Current Feedback Terminal (Channel 5)	
2	Ch6	LED Current Feedback Terminal (Channel 6)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch7	LED Current Feedback Terminal (Channel 7)	
6	Ch8	LED Current Feedback Terminal (Channel 8)	



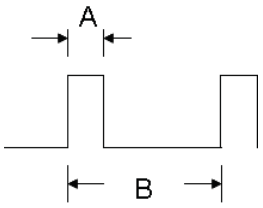
4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25°C)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	150	[mA]	100% duty ratio
			300	[mA]	Duty ratio≦ 10% Pulse time=10 ms



Duty ratio= (A / B) X 100% ; (A: Pulse time, B: Period)

4.3.2 Recommended Operating Condition

(Ta=25°C)

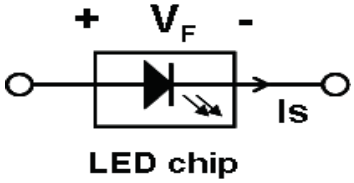
Symbol	Description	Min.	Typ.	Max.	Unit	Remark
Is	LED String Current		90	99	[mA]	@HDR off 100% duty ratio of LED chip; ***Note 4-7***
Is	LED String Current		100	110	[mA]	@HDR on 100% duty ratio of LED chip; ***Note 4-7 & Note 4-8***
Vs	LED String Voltage	39.2	44.8	47.6	[Volt]	Is=90mA @ 100% duty ratio; ***Note 4-1&Note 4-5***
ΔVs	Maximum Vs Voltage Deviation of light bar			2.8	[Volt]	Is=90mA @ 100% duty ratio; ***Note 4-2***
P_{BLU}	LED Light Bar Power Consumption		32.3	34.3	[Watt]	@HDR off ***Note 4-3***
P_{BLU}	LED Light Bar Power Consumption		35.8	38.1	[Watt]	@HDR on ***Note 4-3***
LT_{LED}	LED Life Time	30000			[Hour]	***Note 4-4***

OVP	Over Voltage Protection in system board	110% Vs(Max.)			[Volt]	***Note 4-5***

Note 4-1: Vs (Typ.) = V_F (Typ.) X LED No. (one string);

a. V_F: LED chip forward voltage, V_F (Min.)=2.8V, V_F(Typ.)=3.2V, V_F(Max.)=3.4V

b. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F(Max.);



Note 4-2: ΔVs (Max.) = ΔV_F X LED No. (one string);

a. ΔV_F: LED chip forward voltage deviation (0.2V , each Bin of LED V_F)

Note 4-3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 8 (8 is total String No. of BLU)

P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 8

Note 4-4: Definition of life time:

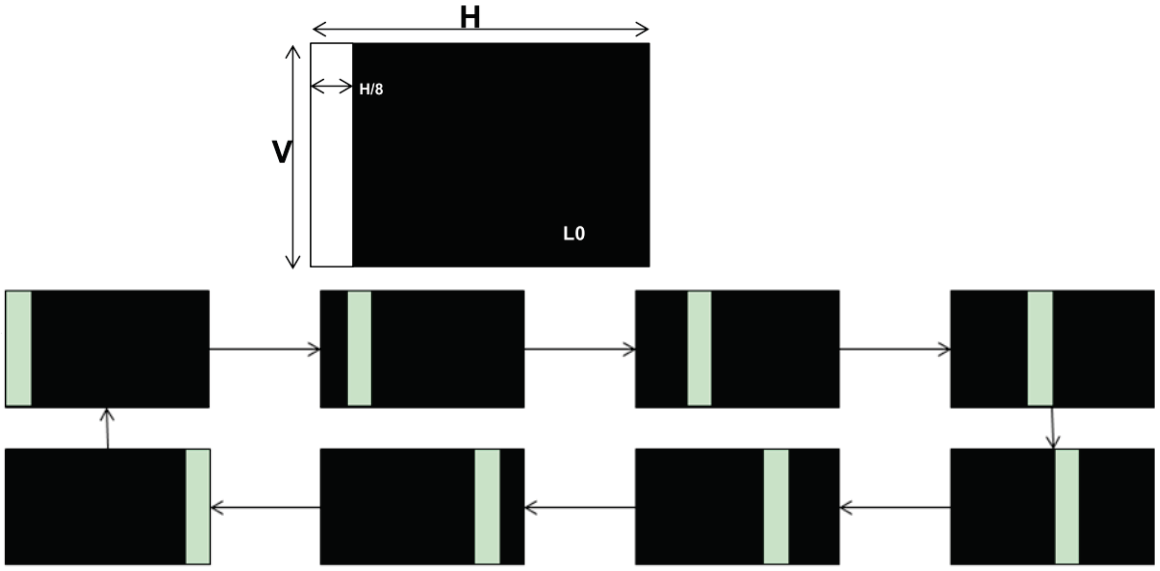
a. Brightness of LED becomes to 50% of its original value

b. Test condition: i. Is = 100mA and 25℃ (Room Temperature)

ii. Aging pattern: bar flow is shown below

iii. Measurement position: center of full screen with L255 pattern

iv. Per pattern flow time:35mins



Note 4-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over

voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

Note 4-6: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency

Note 4-7 Ensure that the LED light bar is not subjected either forward or reverse voltage while monitor set is on standby mode or not in use.

Note 4-8: Peak brightness 400nits can be measured with Is= 100mA (typ.) at L255 pattern at center of full screen. The specifications for guarantee remains under the normal operating condition specified in section 2-2. Specifications and condition for evaluation test and mass production shall be applied with conditions specified in section 2-2.

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	***Note 5-1***
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	***Note 5-2***
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed No data lost
Self-recoverable
No hardware failures.

ESD discharged points should avoid display area and periphery front bezel of display area.

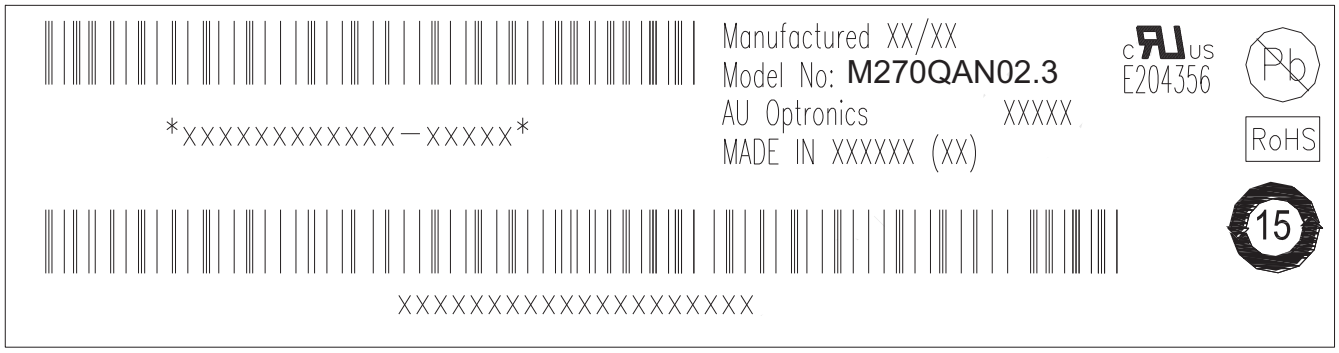
Suggest points were 4 side parallel edge of display area surface.

Metal front bezel must cover half area of BM (black matrix) and metal front bezel must connect with metal back bezel to protect source IC of panel by ESD damaged.

Note5-3: Result Evaluation Criteria: TFT-LCD panels test should take place after gradually cooling enough at room temperature. In the normal application, there should be no particular problems that may affect the display function.

6 Shipping Label

The label is on the panel as shown below:



Note 6-1: For Pb Free products, AUO will add Pb for identification.

Note 6-2: For RoHS compatible products, AUO will add RoHS for identification.

Note 6-3: For China RoHS compatible products, AUO will add 15 for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

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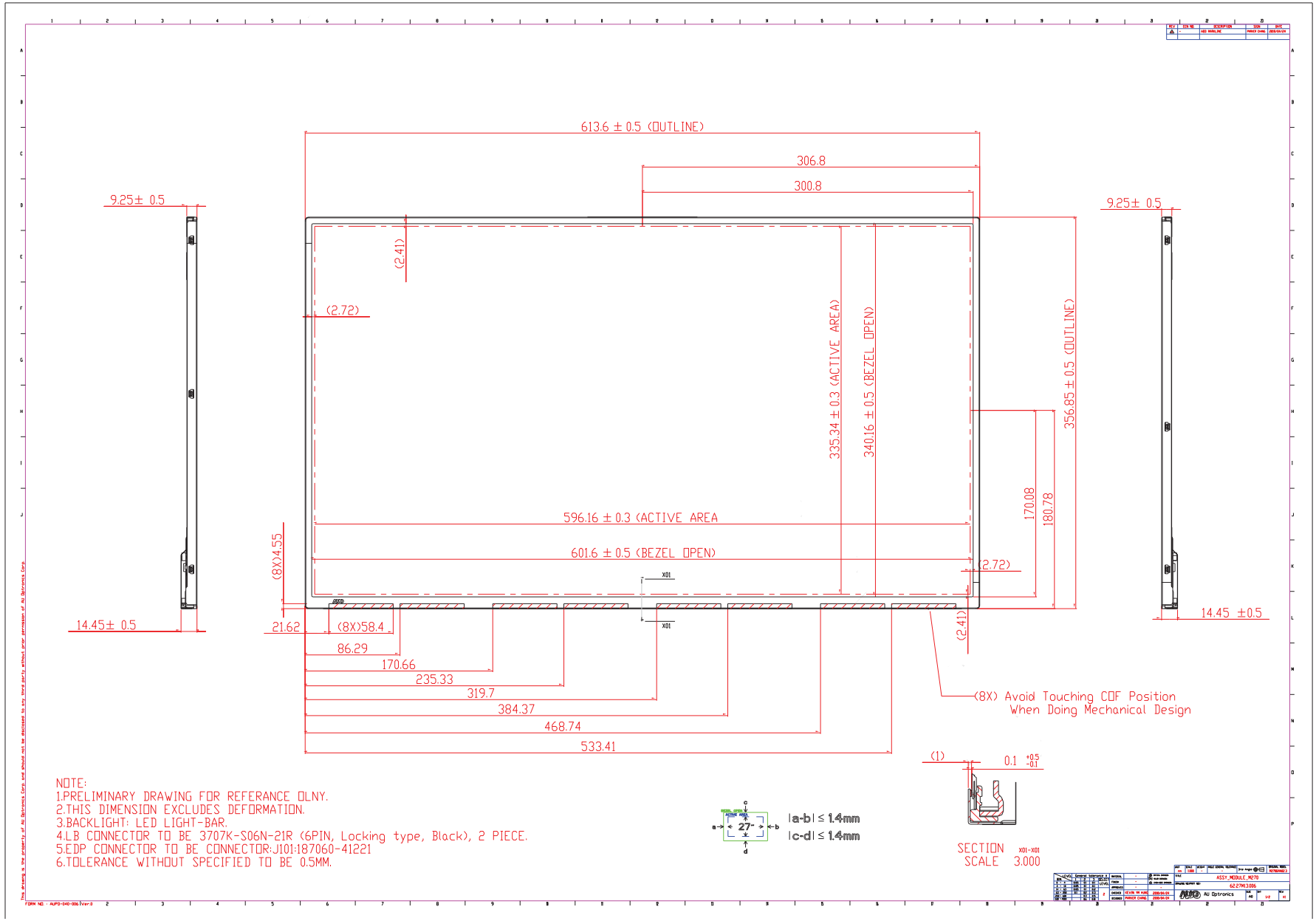
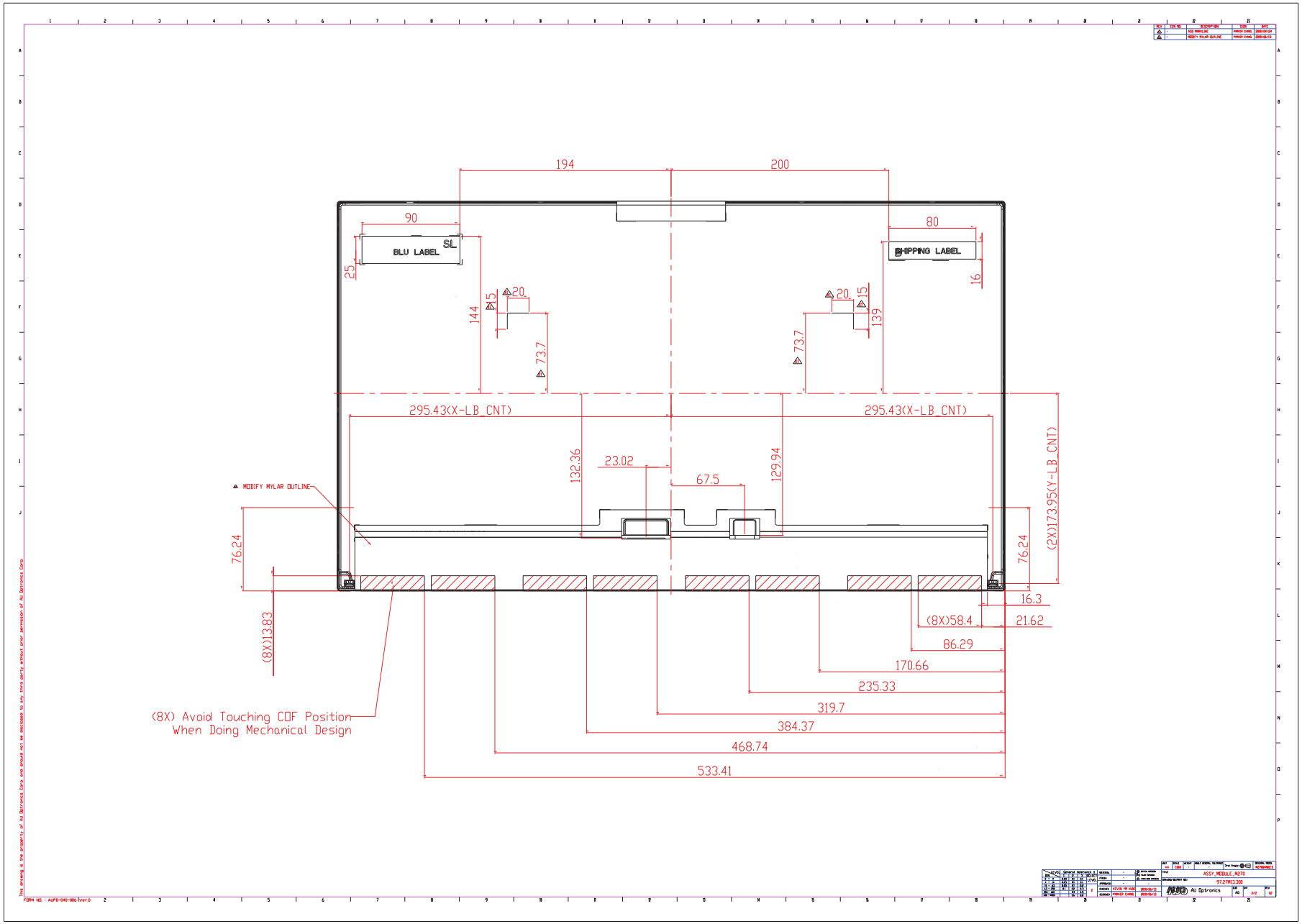
7 Mechanical Characteristics

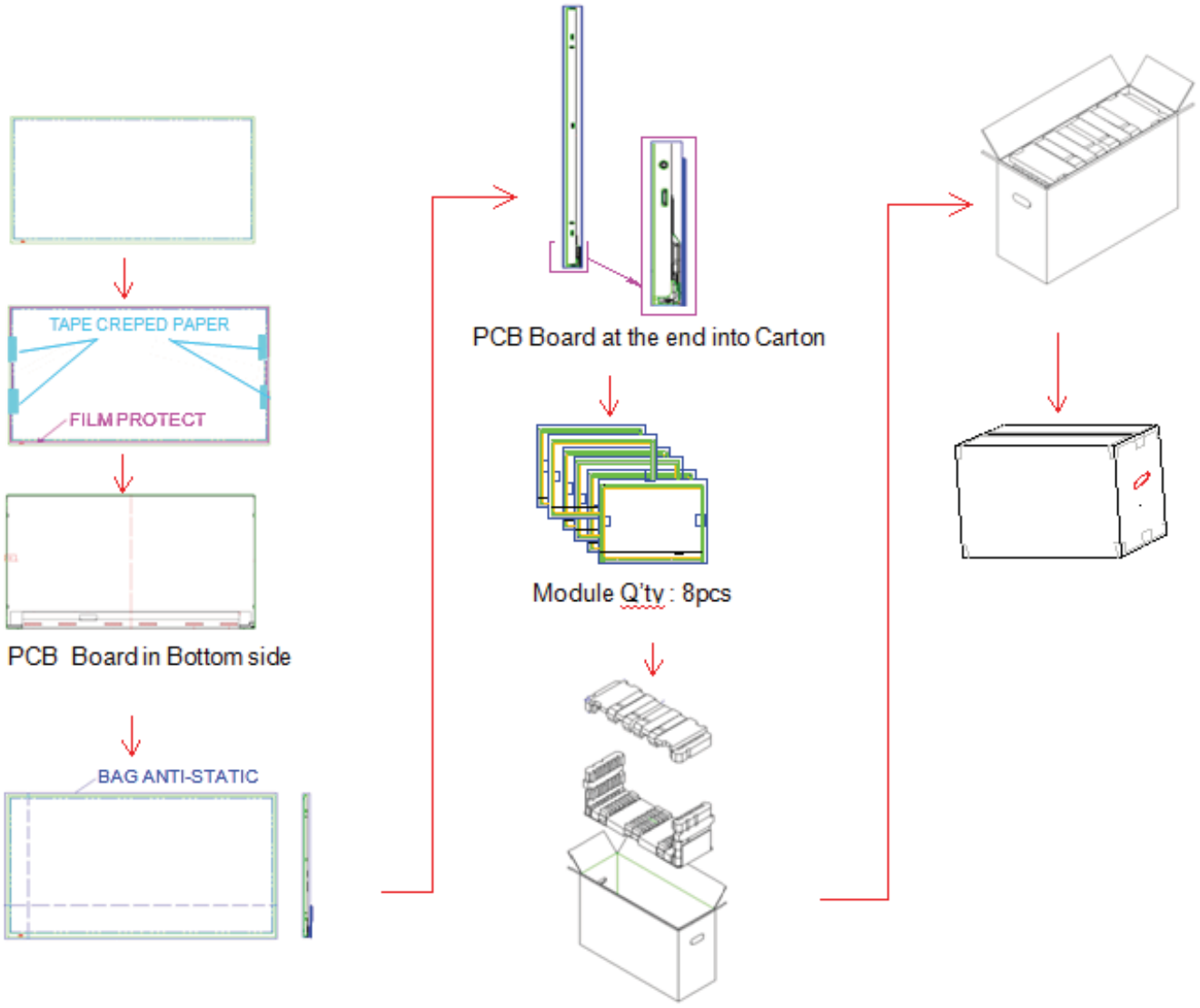


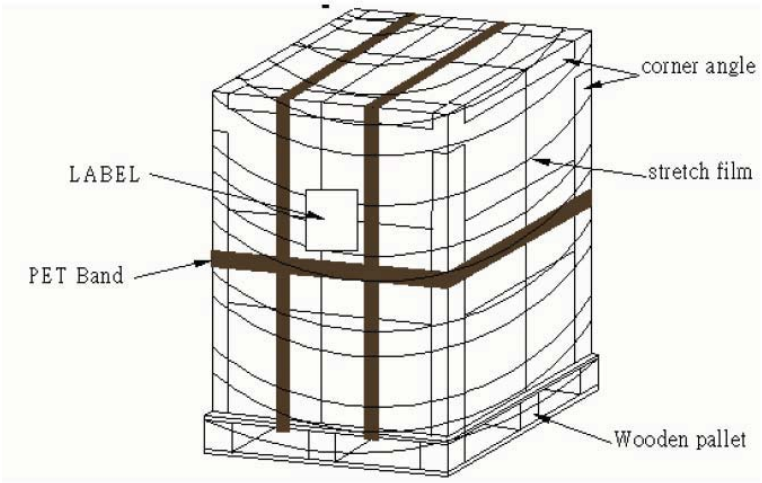

194
200
90
80
SL
BLU LABEL
SHIPPING LABEL
25
16
144
15
20
73.7
139
295.43(X-LB_CNT)
295.43(X-LB_CNT)
132.36
23.02
67.5
129.94
(2X)173.95(Y-LB_CNT)
MODIFY MYLAR OUTLINE
76.24
76.24
16.3
(8X)58.4
21.62
(8X)113.83
86.29
170.66
235.33
319.7
384.37
468.74
533.41
(8X) Avoid Touching COF Position
When Doing Mechanical Design
ASSY_MODULE_M270
AU Optronics

Ver 0.1

8 Packing SpecificationAUO-General ral

8.1 Packing Flow





8.2 Pallet and shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight (kg)	
Panel	1	613.6(H)mm × 356.85(V)mm × 14.45(D)mm	2.511	
Cushion	1	-	0.9	
Box	1	702(L)mm x 264(W)mm x 456(H)mm	1.2	without Panel & cushion
Packing Box	8pcs/Box	702(L)mm x 264(W)mm x 456(H)mm	22.188	with panel & cushion
Pallet	1	1070(L)mm x 740(W)mm x 132(H)mm	14.8	
Pallet after Packing	8boxes/pallet	1070(L)mm x 740(W)mm x 1086(H)mm	192.304	

9 Design Guide for System

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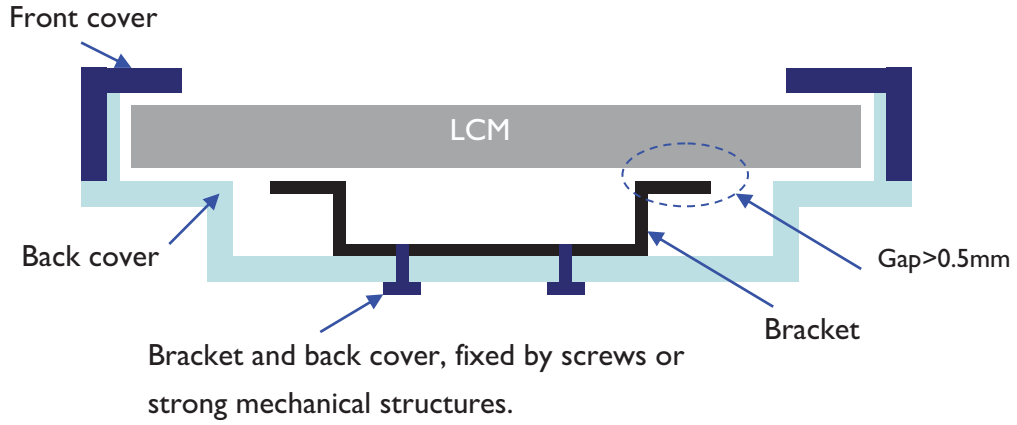
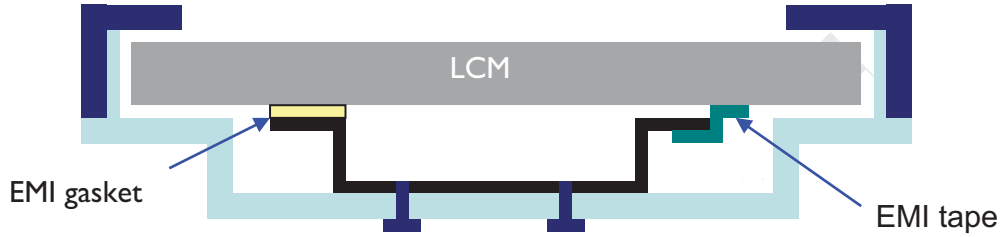
9.1 The gap between LCM and system rear bracket should be bigger than 0.5mm.

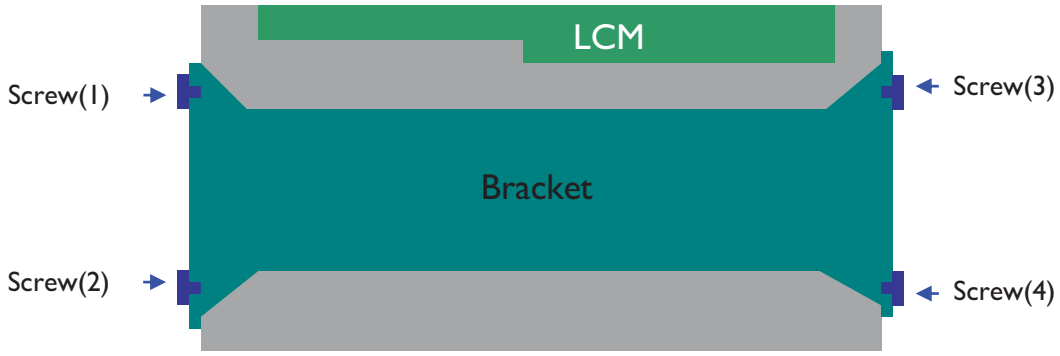
9.2 The system bracket should be fixed on back cover firmly.



9.3 The EMI gasket should be uniform and not push panel strongly.



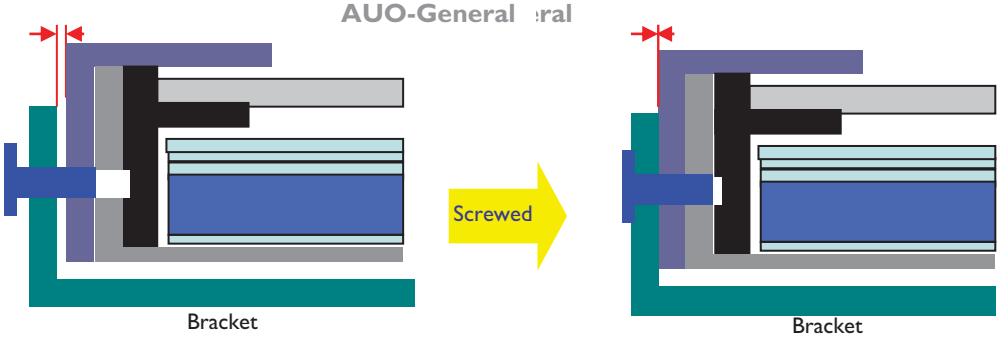
9.4 For stable assembly, the system bracket should use 4 screws to fix system and panel by dual sides.



9.5 The system bracket and panel should be in parallel with having no gap after inserting screws.

Proper and Parallel gap	0 gap and no mechanical damage

AUO-General ral



9.6 Avoid scratching LCM, the rib on system front-cover should not exceed the bottom edge of LCM's front-bezel.