**Doc. Number:**

☐ Tentative Specification

☐ Preliminary Specification

■ Approval Specification

# MODEL NO.: N080ICE
# SUFFIX: GB1 Rev.C8

**Customer:**

**APPROVED BY** **SIGNATURE**

**Name / Title**

Note :

Please return 1 copy for your confirmation with your signature and comments.

| Approved By | Checked By | Prepared By |
|---|---|---|
| | Tsoyu Chu | PING.FAN |

# CONTENTS

REVISION HISTORY

| Version | Date | Page | Description |
|---|---|---|---|
| V0 | Oct, 23, 2014 | All | Spec Ver.0.0 was first issued. |
| V1 | FEB.03.2015 | 32 | Update outline drawing |
| V2 | FEB.06.2015 | 32 | Update outline drawing |
| | | | |
| | | | |

# 1. GENERAL DESCRIPTION

## 1.1 OVERVIEW

N080ICE-GB0 is a 8” (8” diagonal) TFT Liquid Crystal Display module with LED Backlight unit and **31 pins MIPI** interface. This module supports 800 x 1280 WXGA mode.

## 1.2 GENERAL SPECIFICATI0NS

| Item | Specification | Unit | Note |
|---|---|---|---|
| Screen Size | 8” diagonal | | |
| Driver Element | a-si TFT active matrix | - | - |
| Pixel Number | 800 x R.G.B. x 1280 | pixel | - |
| Pixel Pitch | 0.13455 (H) x 0.13455 (V) | mm | - |
| Pixel Arrangement | RGB vertical stripe | - | - |
| Display Colors | 16,777,216 (8bit color depth) | color | - |
| Transmissive Mode | Normally black | - | - |
| Surface Treatment | Hard coating | - | - |
| Luminance, White | 350 | Cd/m2 | |
| Power Consumption | *Total 1.63 W (Max.) ( panel 0.3 W (Max.), BL 1.33W (Max.))* | | (1) |

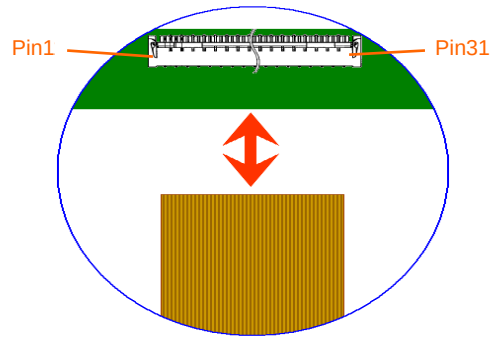
Note (1) The specified power consumption (with converter efficiency) is under the conditions at **VCI = 3.3 V, VDDI= 1.8V, fv = 60 Hz, Brightness = 350nits, $I_{F\_LED}$ = 21mA** and Ta = 25 ± 2 ºC, whereas **white** pattern is displayed.

# 2. MECHANICAL SPECIFICATIONS

| Item | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Module Size | Horizontal (H) | 114.38 | 114.58 | 114.78 | mm | (1) |
| | Vertical (V) | 183.89 | 184.09 | 184.29 | mm | |
| | Thickness (T) | | | 2.7 mm w/o PCBA<br>4.5 with PCBA | mm | |
| CF Polarizer | Horizontal | 110.24 | 110.44 | 110.64 | mm | |
| | Vertical | 175.42 | 175.62 | 175.82 | mm | |
| Active Area | Horizontal | 107.54 | 107.64 | 107.74 | mm | |
| | Vertical | 172.12 | 172.22 | 172.32 | mm | |
| Weight | | - | - | 94 | g | |

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

## 2.1 CONNECTOR TYPE




Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **I- PEX: 20613-031E-01**

# 3. ABSOLUTE MAXIMUM RATINGS

## 3.1 ABSOLUTE RATINGS OF ENVIRONMENT

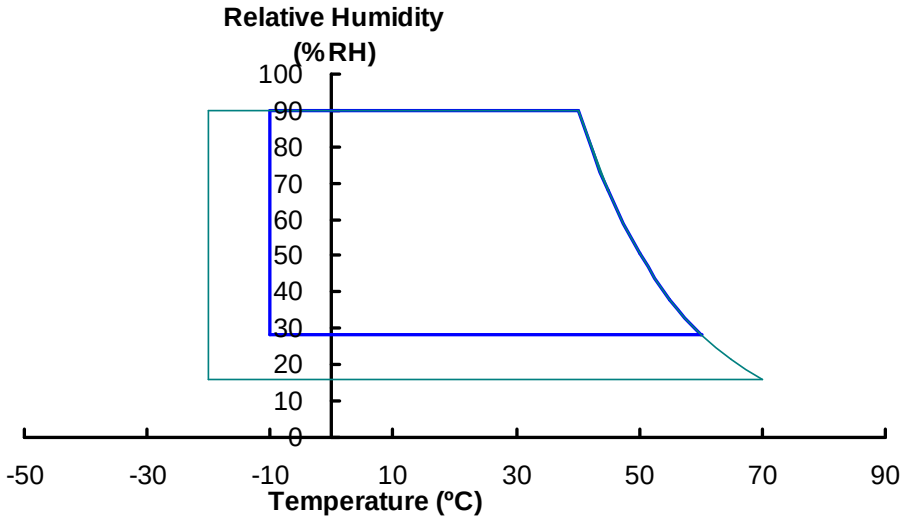
| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Storage Temperature | $T_{ST}$ | -20 | +70 | ºC | (1) |
| Operating Ambient Temperature | $T_{OP}$ | -10 | +60 | ºC | (1), (2) |

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be -10 ºC min. and 70 ºC max.




## 3.2 ELECTRICAL ABSOLUTE RATINGS

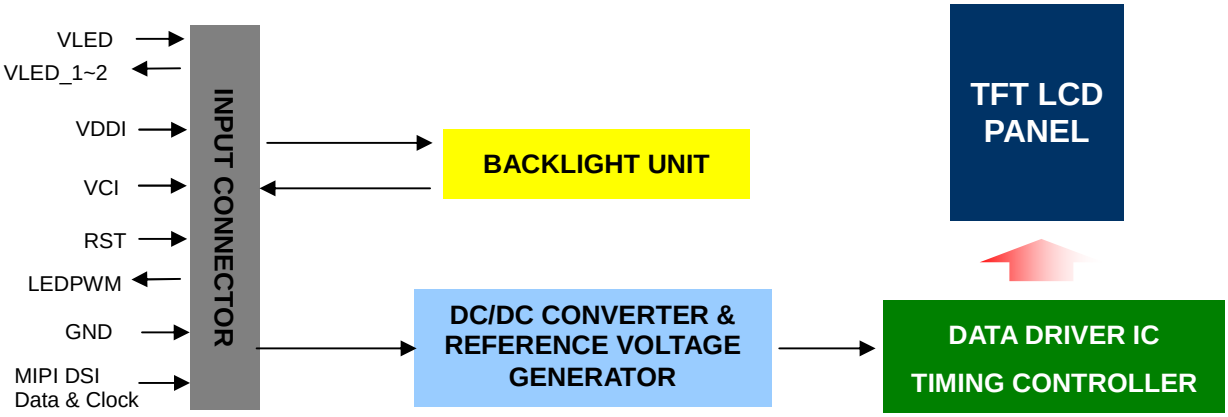
### 3.2.1 TFT LCD MODULE

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| **Power Supply Voltage** | **VCI** | **-0.3** | **+5.0** | **V** | (1) |
| | **VDDI** | **-0.3** | **+2.0** | **V** | (1) |

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

# 4. ELECTRICAL SPECIFICATIONS

## 4.1 FUNCTION BLOCK DIAGRAM




## 4.2. INTERFACE CONNECTIONS

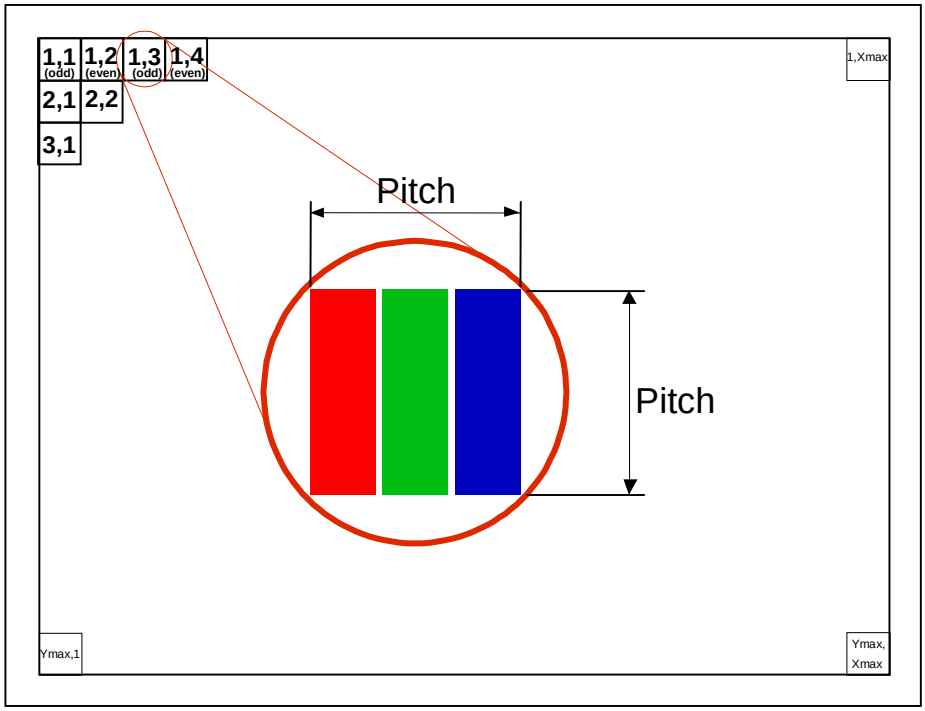
PIN ASSIGNMENT

| Pin | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | ID | - | No Connection | |
| 2 | GND | P | Ground | |
| 3 | NC | - | No Connection | |
| 4 | D2_P | I | MIPI differential data2 input (Positive) | |
| 5 | LED3 | P | Cathode 3 for light bar | |
| 6 | D2_N | I | MIPI differential data2 input (Negative) | |
| 7 | LED2 | P | Cathode 2 for light bar | |
| 8 | GND | P | Ground | |
| 9 | LED1 | P | Cathode 1 for light bar | |
| 10 | D1_P | I | MIPI differential data1 input (Positive) | |
| 11 | GND | P | Ground | |
| 12 | D1_N | I | MIPI differential data1 input (Negative) | |
| 13 | VLED | P | Anode for light bar | |
| 14 | GND | P | Ground | |
| 15 | VLED | P | Anode for light bar | |
| 16 | CLK_P | I | MIPI differential clock input (Positive) | |
| 17 | NC(MTP) | P | No connection, please keep it floating | |
| 18 | CLK_N | I | MIPI differential clock input (Negative) | |
| 19 | VCI | P | 3.3V input | |
| 20 | GND | P | Ground | |
| 21 | VCI | P | 3.3V input | |
| 22 | D0_P | I | MIPI differential data0 input (Positive) | |

| | | | | |
|---|---|---|---|---|
| 23 | Hsync | O | Per scan line signal for noise sensing of TP. If not used, please keep it floating. | |
| 24 | D0_N | I | MIPI differential data0 input (Negative) | |
| 25 | VDDI | P | 1.8V input | |
| 26 | GND | P | Ground | |
| 27 | VDDI | P | 1.8V input | |
| 28 | D3_P | I | MIPI differential data3 input (Positive) | |
| 29 | RESX | I | Device reset signal | |
| 30 | D3_N | I | MIPI differential data3 input (Negative) | |
| 31 | LEDPWM | O | PWM control signal for LED driver (CABC) | |

Note (1) The first pixel is odd as shown in the following figure.

Note (2) Normal operation/BIST pattern selection. (Control by MIPI LP Command)



## 4.3 ELECTRICAL CHARACTERISTICS

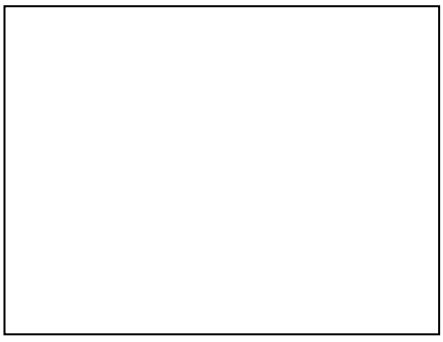
### 4.3.1 LCD ELETRONICS SPECIFICATION

| Item | | Symbol | Values | | | Unit | Remark |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power supply voltage | | VCI | 3.0 | 3.3 | 3.6 | V | |
| | | VDDI | 1.7 | 1.8 | 1.9 | V | |
| VDDI High level input voltage | | $V_{IH2}$ | 0.7 VDDI | - | VDDI | V | For I/O circuit |
| VDDI Low level input voltage | | $V_{IL2}$ | 0 | - | 0.3 VDDI | V | |
| Power Supply Current | White | $I_{VCI}$ | - | 50 | 60 | mA | Note (2) |
| | | $I_{VDDI}$ | - | 45 | 55 | mA | |
| Power consumption | | PLCD | - | - | 300 | mW | Note (3) |

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) The specified power supply current is under the conditions at VCI = 3.3 V, VDDI = 1.8 V, Ta = 25 ± 2 ºC, DC Current and $f_v$ = 60 Hz, whereas a power dissipation check pattern below is displayed.

b. White Pattern



Active Area

Note (3) The power consumption is specified at the white pattern with the maximum current

### 4.3.2 LED CONVERTER SPECIFICATION

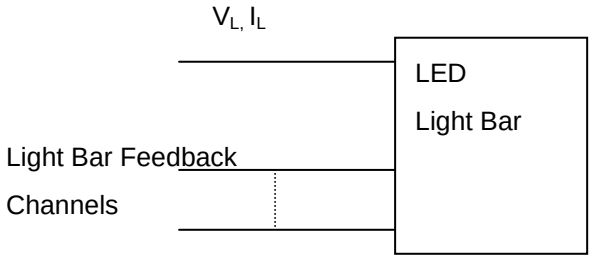
**N/A**

### 4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| LED Light Bar Power Supply Voltage | $V_L$ | 18.9 | 20.3 | 21 | V | (1)(2)(Duty100%) |
| LED Light Bar Power Supply Current | $I_L$ | - | 63 | - | mA | |
| Power Consumption | $P_L$ | - | 1.28 | 1.33 | W | (3) |
| LED Life Time | $L_{BL}$ | 15000 | - | - | Hrs | (4) |

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :

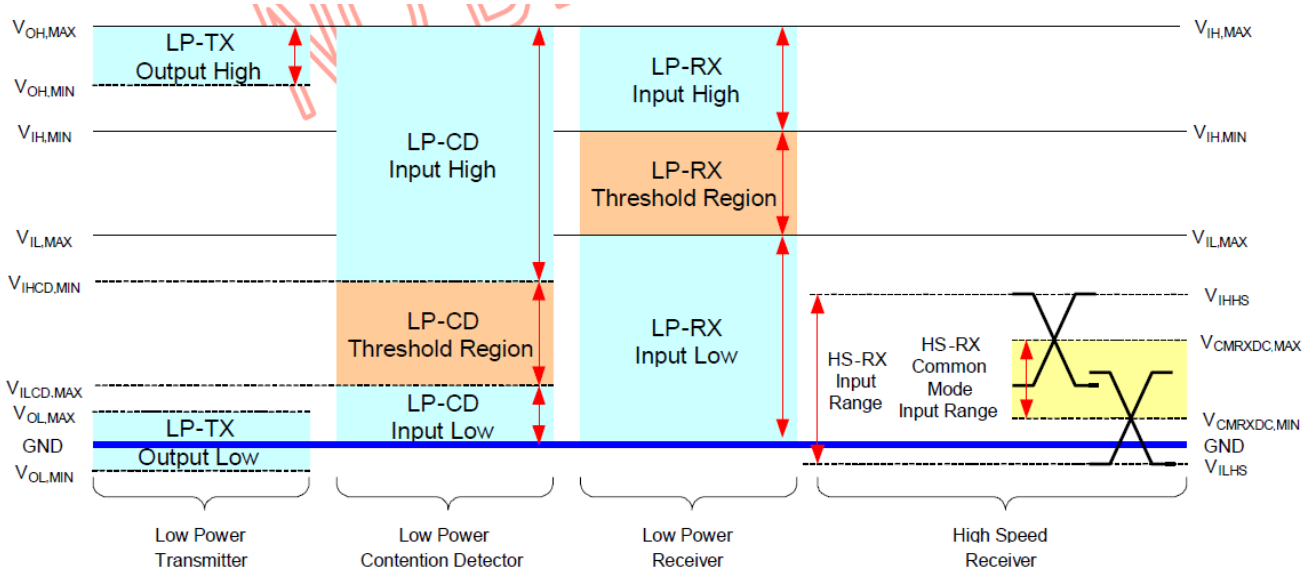



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 $^{o}$C and $I_L$ = 21 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

## 4.4 MIPI DSI INPUT SIGNAL TIMING SPECIFICATIONS



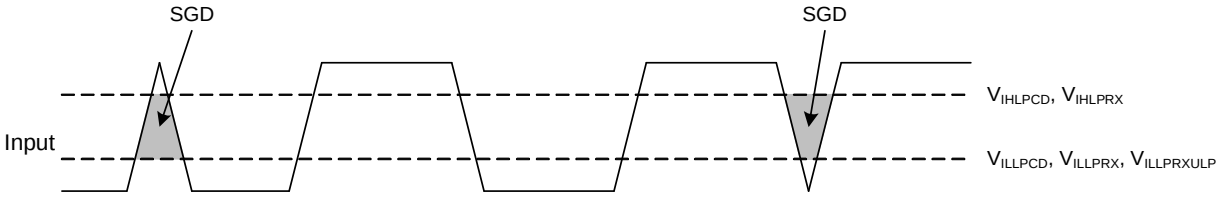

**MIPI DC Diagram**

### 4.4.1 DC Electrical Characteristic

#### 4.4.1.1DC Characteristics for DSI LP Mode

| Parameter | Symbol | Conditions | Specification | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Logic high level input voltage | $V_{IHLPCD}$ | LP-CD | 450 | - | 1350 | mV |
| Logic low level input voltage | $V_{ILLPCD}$ | LP-CD | 0 | - | 200 | mV |
| Logic high level input voltage | $V_{IHLPRX}$ | LP-RX (CLK, D0, D1) | 880 | - | 1350 | mV |
| Logic low level input voltage | $V_{ILLPRX}$ | LP-RX (CLK, D0, D1) | 0 | - | 550 | mV |
| Logic low level input voltage | $V_{ILLPRXULP}$ | LP-RX (CLK ULP mode) | 0 | - | 300 | mV |
| Logic high level output voltage | $V_{OHLPTX}$ | LP-TX (D0) | 1.1 | - | 1.3 | V |
| Logic low level output voltage | $V_{OLLPTX}$ | LP-TX (D0) | -50 | - | 50 | mV |
| Logic high level input current | $I_{IH}$ | LP-CD, LP-RX | - | - | 10 | μA |
| Logic low level input current | $I_{IL}$ | LP-CD, LP-RX | -10 | - | - | μA |
| Input pulse rejection | SGD | DSI-CLK+/-, DSI-Dn+/- (Note 3) | - | - | 300 | Vps |

*Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).*
*Note 2) DSI high speed is off.*
*Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.*

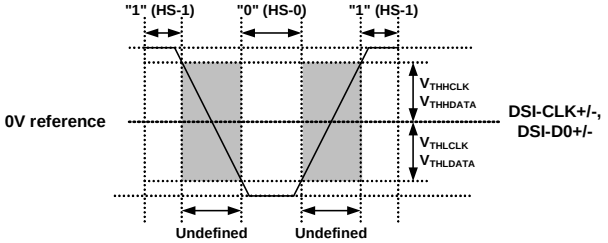


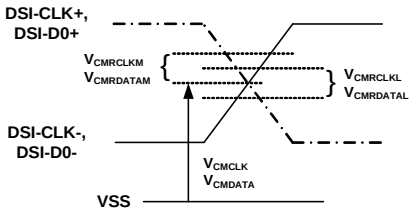

***Spike/Glitch rejection-DSI***

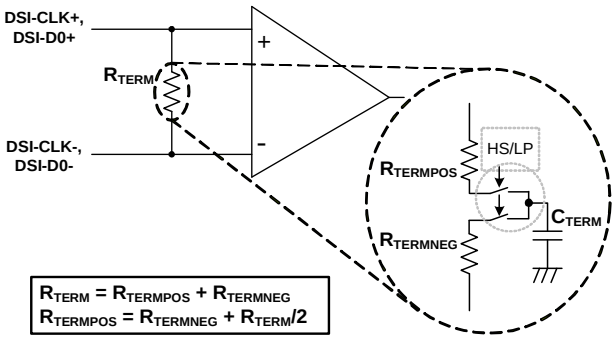
### 4.4.1.2DC Characteristics for DSI HS Mode

| Parameter | Symbol | Conditions | Specification | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Input voltage common mode range | $V_{CMCLK}$ $V_{CMDATA}$ | DSI-CLK+/-, DSI-Dn+/- (Note2, 3) | 70 | - | 330 | mV |
| Input voltage common mode variation (≤ 450MHz) | $V_{CMRCLKL}$ $V_{CMRDATAL}$ | DSI-CLK+/-, DSI-Dn+/- (Note 4) | -50 | - | 50 | mV |
| Input voltage common mode variation (≥ 450MHz) | $V_{CMRCLKM}$ $V_{CMRDATAM}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 100 | mV |
| Low-level differential input voltage threshold | $V_{THLCLK}$ $V_{THLDATA}$ | DSI-CLK+/-, DSI-Dn+/- | -70 | - | - | mV |
| High-level differential input voltage threshold | $V_{THHCLK}$ $V_{THHDATA}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 70 | mV |
| Single-ended input low voltage | $V_{ILHS}$ | DSI-CLK+/-, DSI-Dn+/- (Note 3) | -40 | - | - | mV |
| Single-ended input high voltage | $V_{IHHS}$ | DSI-CLK+/-, DSI-Dn+/- (Note 3) | - | - | 460 | mV |
| Differential input termination resistor | $R_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- | 80 | 100 | 125 | Ω |
| Single-ended threshold voltage for termination enable | $V_{TERM-EN}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 450 | mV |
| Termination capacitor | $C_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- | - | - | 14 | pF |

*Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).*
*Note 2) Includes 50mV (-50mV to 50mV) ground difference.*
*Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$ .*
*Note 4) Without 50mV (-50mV to 50mV) ground difference.*
*Note 5) Dn=D0, D1, D2 and D3.*






***Differential voltage range, termination resistor and Common mode voltage***

## 4.4.2 AC Electrical Characteristics

### 4.4.2.1 MIPI DSI Timing Characteristics

#### 4.4.2.1.1 High Speed Mode

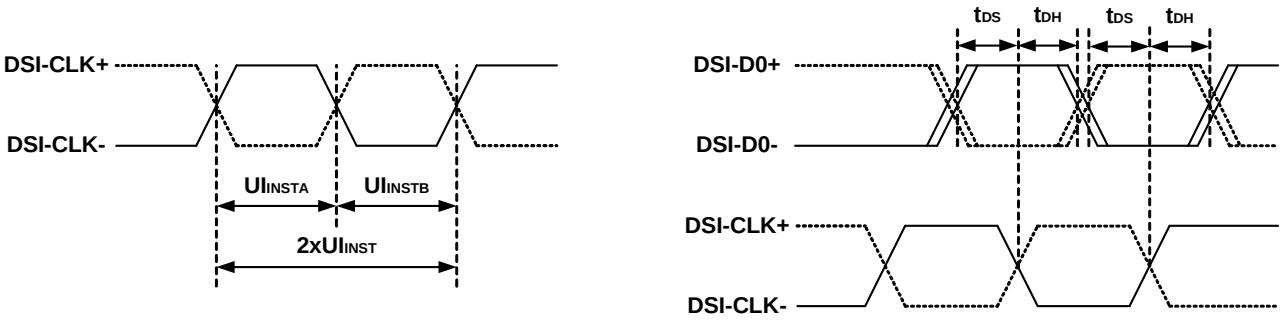
(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*** ,Ta = -30 to 70℃)

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| DSI-CLK+/- | 2xUI$_{INST}$ | Double UI instantaneous | 4 | - | 8 | ns | 4 Lane (Note 2) |
| | | | 3 | - | 8 | ns | 3 Lane (Note 2) |
| | | | 2.352 | - | 8 | ns | 2 Lane (Note 3) |
| DSI-CLK+/- | UI$_{INSTA}$<br>UI$_{INSTB}$ | UI instantaneous halfs<br>(UI = UI$_{INSTA}$ = UI$_{INSTB}$) | 2 | - | 4 | ns | 4 Lane (Note 2) |
| | | | 1.5 | - | 4 | ns | 3 Lane (Note 2) |
| | | | 1.176 | - | 4 | ns | 2 Lane (Note 3) |
| DSI-Dn+/- | t$_{DS}$ | Data to clock setup time | 0.15xUI | - | - | ps | |
| DSI-Dn+/- | t$_{DH}$ | Data to clock hold time | 0.15xUI | - | - | ps | |
| DSI-CLK+/- | t$_{DRTCLK}$ | Differential rise time for clock | 150 | - | 0.3xUI | ps | |
| DSI-Dn+/- | t$_{DRTDATA}$ | Differential rise time for data | 150 | - | 0.3xUI | ps | |
| DSI-CLK+/- | t$_{DFTCLK}$ | Differential fall time for clock | 150 | - | 0.3xUI | ps | |
| DSI-Dn+/- | t$_{DFTDATA}$ | Differential fall time for data | 150 | - | 0.3xUI | ps | |

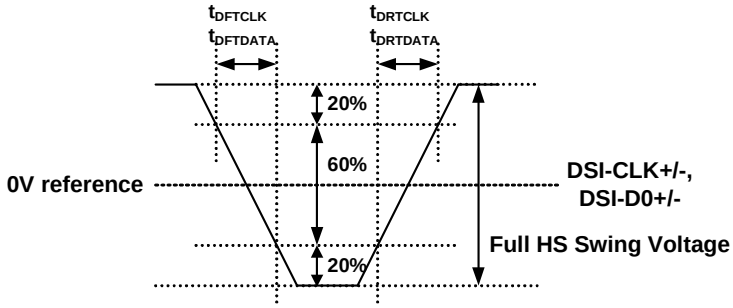
*Note 1) Dn = D0, D1, D2 and D3.*

*Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.*

*Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.*




***DSI clock channel timing***

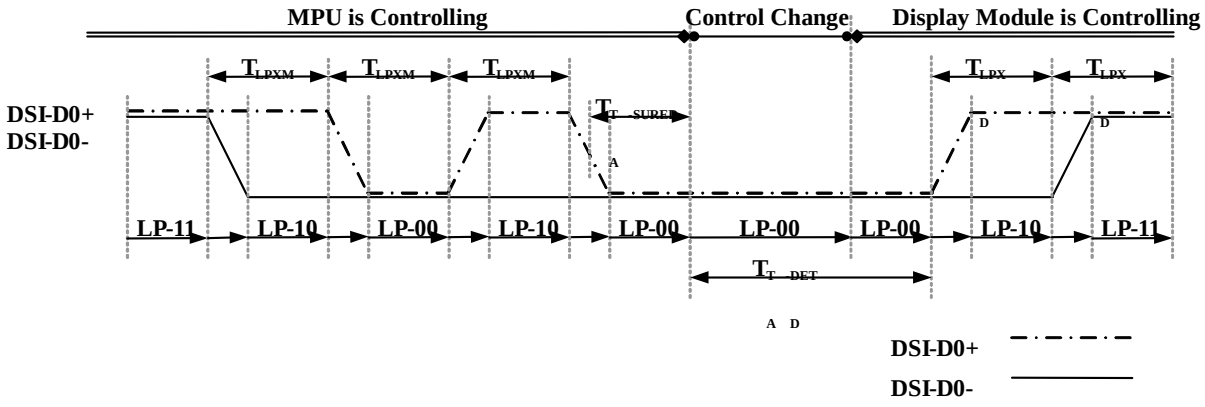



***Rising and fall time on clock and data channel***

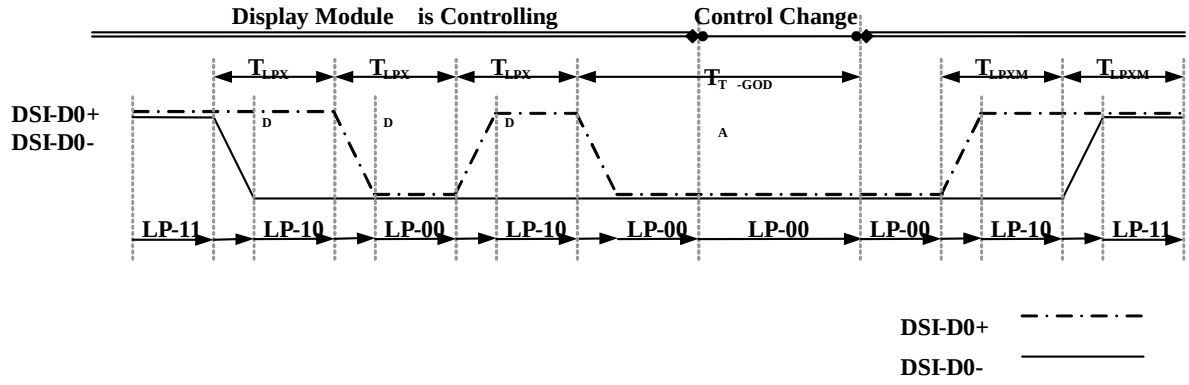
### 4.4.2.1.2 Low Power Mode

(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*** ,Ta = -30 to 70℃)

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| DSI-D0+/- | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module | 50 | - | 75 | ns | Input |
| DSI-D0+/- | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU | 50 | - | 75 | ns | Output |
| DSI-D0+/- | $T_{TA-SURED}$ | Time-out before the MPU start driving | $T_{LPXD}$ | - | $2xT_{LPXD}$ | ns | Output |
| DSI-D0+/- | $T_{TA-GETD}$ | Time to drive LP-00 by display module | $5xT_{LPXD}$ | - | - | ns | Input |
| DSI-D0+/- | $T_{TA-GOD}$ | Time to drive LP-00 after turnaround request - MPU | $4xT_{LPXD}$ | - | - | ns | Output |




***Bus Turnaround (BAT) from MPU to display module Timing***




***Bus Turnaround (BAT) from display module to MPU Timing***

### 4.4.2.1.3 DSI Bursts

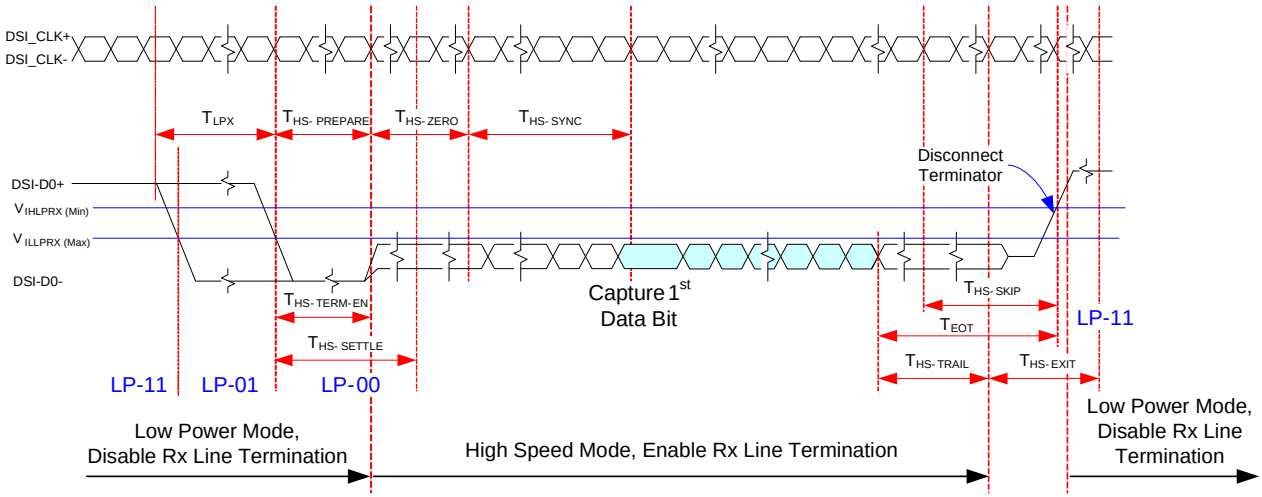
(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*,Ta = -30 to 70℃)

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| Low Power Mode to High Speed Mode Timing | | | | | | | |
| DSI-Dn+/- | $T_{LPX}$ | Length of any low power state period | 50 | - | - | ns | Input |
| DSI-Dn+/- | $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 40+4xUI | - | 85+6xUI | ns | Input |
| DSI-Dn+/- | $T_{HS-TERM-EN}$ | Time to enable data receiver line termination measured from when Dn crosses $V_{ILMAX}$ | - | - | 35+4xUI | ns | Input |
| High Speed Mode to Low Power Mode Timing | | | | | | | |
| DSI-Dn+/- | $T_{HS-SKIP}$ | Time-out at display module to ignore transition period of EoT | 40 | - | 55+4xUI | ns | Input |
| DSI-Dn+/- | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | - | ns | Input |
| DSI-Dn+/- | $T_{HS-TRAIL}$ | Time to drive flipped differential state after last payload data bit of a HS transmission burst | 60+4xUI | - | - | ns | Input |
| High Speed Mode to/from Low Power Mode Timing | | | | | | | |
| DSI-CLK+/- | $T_{CLK-POS}$ | Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode | 60+52xUI | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | - | ns | Input |
| DSI-CLK+/- | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 38 | - | 95 | ns | Input |
| DSI-CLK+/- | $T_{CLK-TERM-EN}$ | Time-out at clock lane display module to enable HS | - | - | 38 | ns | Input |

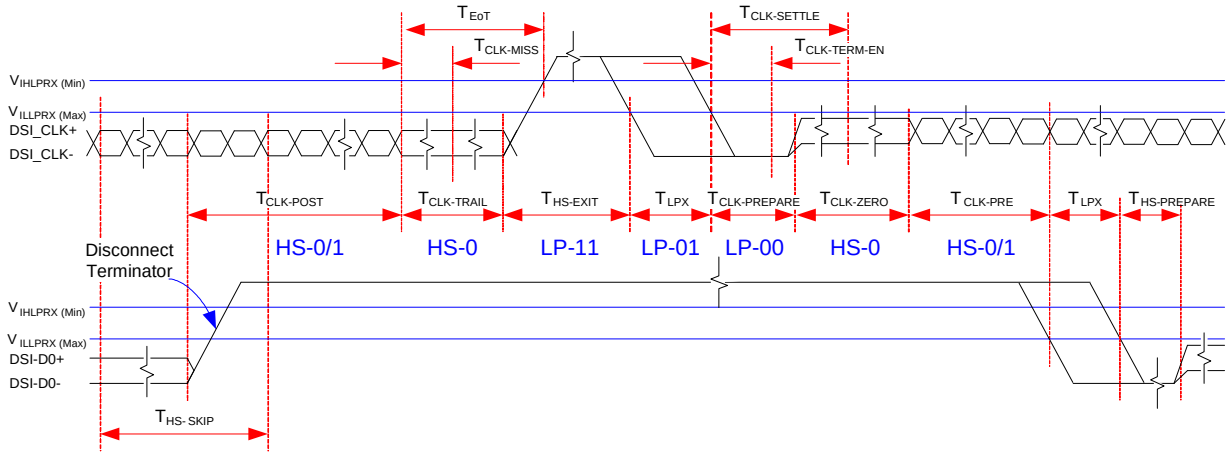
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | transmission | | | | | |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | Minimum lead HS-0 drive period before starting clock | 300 | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode | 8xUI | - | - | ns | Input |

*Note 1) Dn = D0, D1, D2 and D3.*

*Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.*

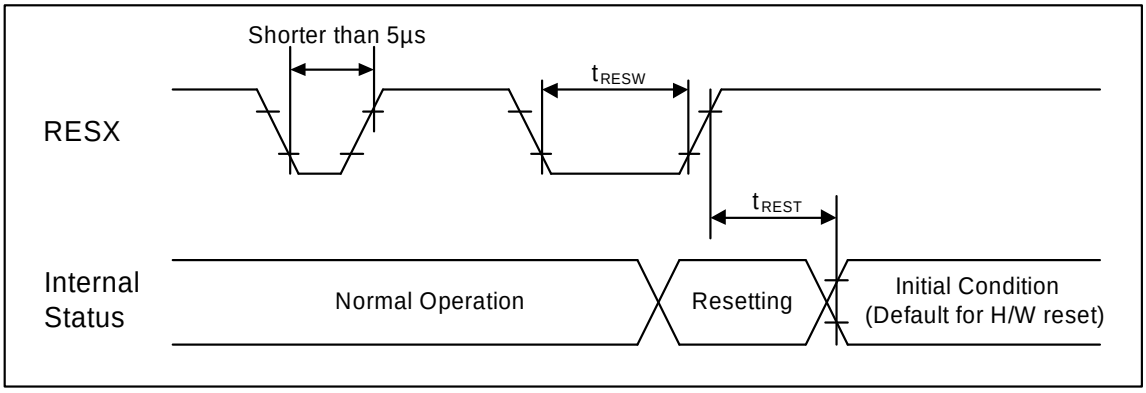



***Data lanes-Low Power Mode to/from High Speed Mode Timing***




***Clock lanes- High Speed Mode to/from Low Power Mode Timing***

4.4.2.2 Reset Input Timing




***Reset input timing***

**(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*,Ta** = -30 to 70℃)

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| RESX | $t_{RESW}$ | Reset "L" pulse width (Note 1) | 10 | - | - | µs | |
| | $t_{REST}$ | Reset complete time (Note 2) | - | - | 5 | ms | When reset applied during Sleep In Mode |
| | | | - | - | 120 | ms | When reset applied during Sleep Out Mode and Note 5 |

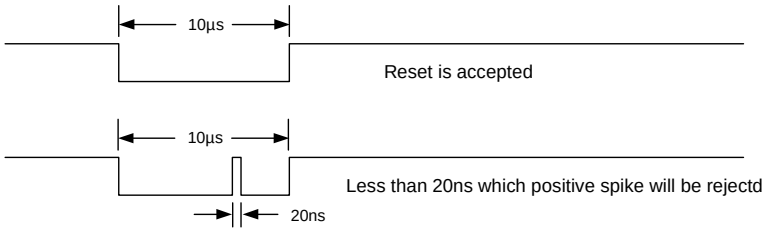
*Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.*

| *RESX Pulse* | *Action* |
|---|---|
| *Shorter than 5µs* | *Reset Rejected* |
| *Longer than 10µs* | *Reset* |
| *Between 5µs and 10µs* | *Reset Start* |

*Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.*

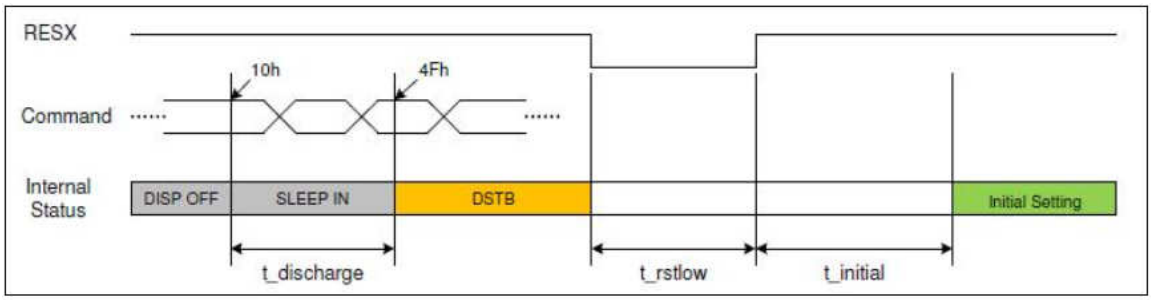
*Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time ($t_{REST}$) within 5ms after a rising edge of RESX.*

*Note 4) Spike Rejection also applies during a valid reset pulse as shown below:*




*Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec*

4.4.2.3 Deep Standby Mode Timing




(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V***,Ta = -30 to 70℃)

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| RESX | $t_{discharge}$ | Sleep in into DSTB delay time | - | - | 100 | ms | |
| | $t_{rstlow}$ | Reset low pulse | 3 | - | - | ms | |
| | $t_{initial}$ | Reset high to initial setting delay time | - | - | 120 | ms | |

*Note 1)* $t_{\_discharge}$ *suggested delay time over 100ms.*

Note 2) $t_{\_initial}$ suggested delay time over 120ms..

### 4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Note: The product only supports Video Mode operation.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

#### 4.5.1 MIPI Lane Configuration

| | MCU (Master) Display Module (Slave) |
|---|---|
| Clock Lane+/- | Unidirectional Lane<br>■ Clock Only<br>■ Escape Mode(ULPS Only) |
| Data Lane0+/- | Bi-directional Lane<br>■ Forward High-Speed<br>■ Bi-directional Escape Mode<br>■ Bi-directional LPDT |
| Data Lane1+/- | Unidirectional<br>■ Forward High speed |
| Data Lane2+/- | Unidirectional<br>■ Forward High speed |
| Data Lane3+/- | Unidirectional<br>■ Forward High speed |

The connection between host device and display module is as reference.

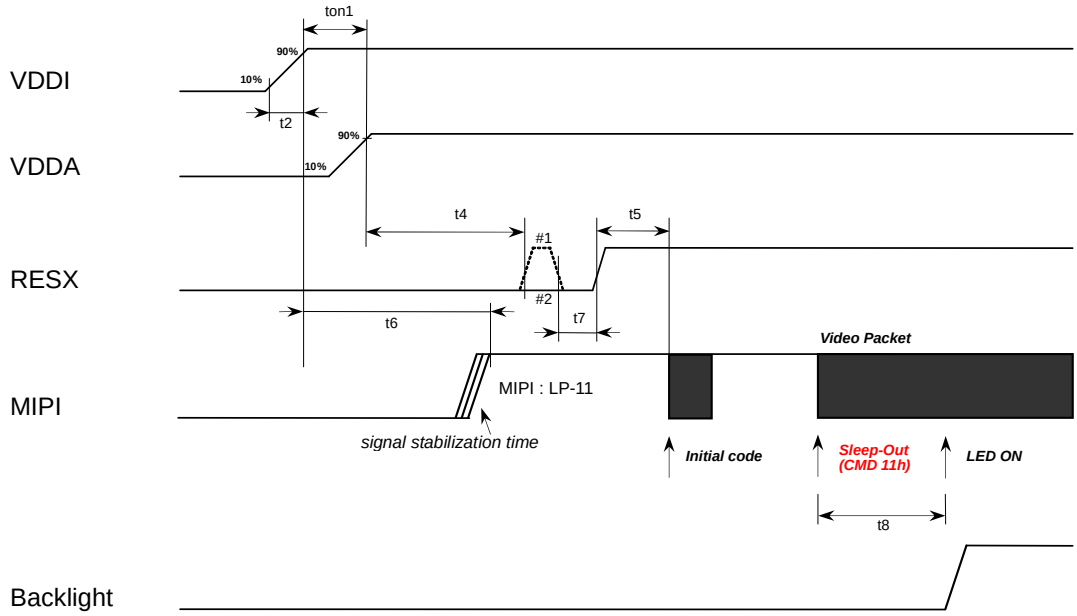
Note: Usually, we suggest host can use non-continuous clock mode & non-burst mode with sync events to transmit the video stream to enhance ESD ability.

### 4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram**.**

**a. Power on:**

***VDDI=1.7~1.9V, VCI(VDDA)=3.0 to 3.6V,***



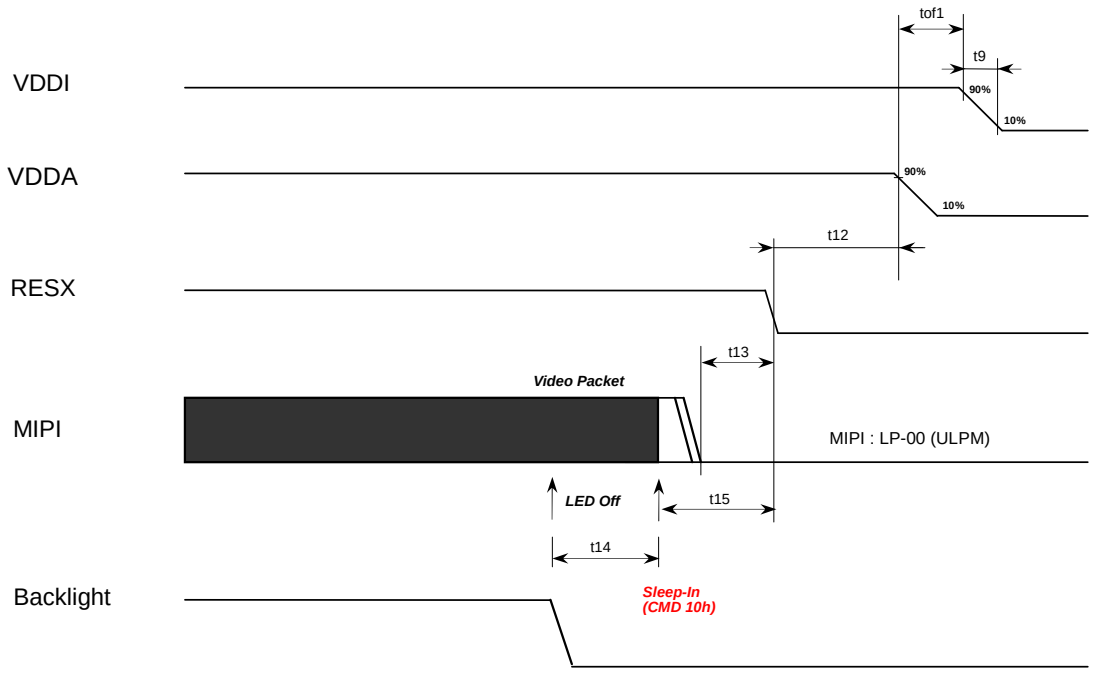

*Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

*Note 2: Reset signal H to L to H (#1) is better than only L to H (#2).*

| Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| ton1 | 0 | | | ms | |
| t2 | | No limit | | μs | |
| t4 | 40 | | | ms | |
| t5 | 20 | | | ms | |
| t6 | 0 | | t4 | ms | |
| t7 | 10 | | | μs | |
| t8 | 8 | | | VS | Keep data more than 8 frames (VS) |

## b. Power off:

***VDDI=1.7~1.9V, VCI=3.0 to 3.6V,***




*Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

| Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| t9 | 150 | - | - | ms | |
| tof1 | 0 | - | - | ms | |
| t12 | 0 | - | - | ms | |
| t13 | 0 | - | - | ms | |
| t14 | 0 | - | - | ms | |
| t15 | 100 | - | - | ms | |

# 5. OPTICAL CHARACTERISTICS

## 5.1 TEST CONDITIONS

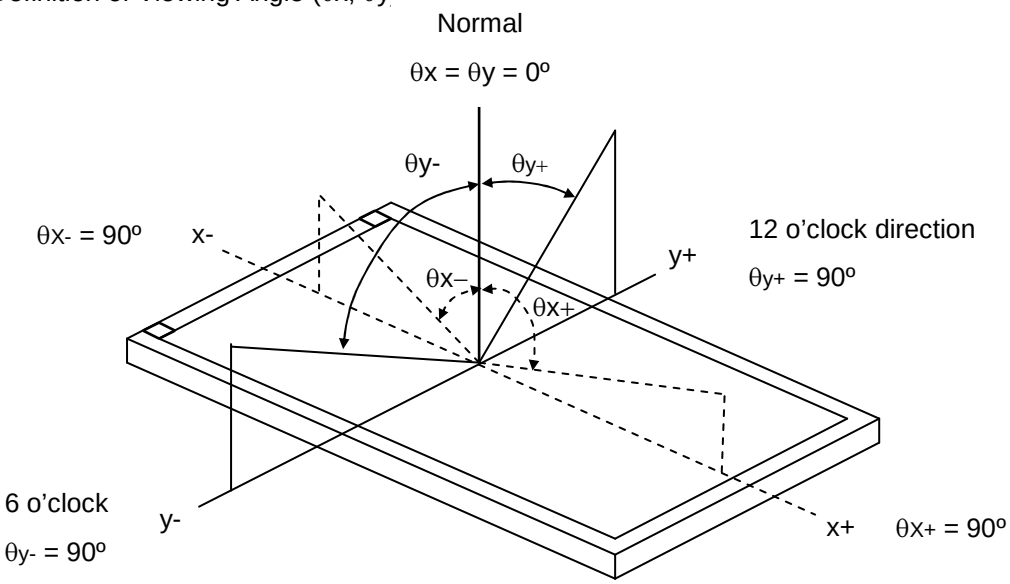
| Item | Symbol | Value | Unit |
|---|---|---|---|
| Ambient Temperature | Ta | 25±2 | °C |
| Ambient Humidity | Ha | 50±10 | %RH |
| Supply Voltage | VDDI | 1.8 | V |
| | VCI | 3.3 | V |
| Input Signal | According to typical value in "3. ELECTRICAL CHARACTERISTICS" | | |
| LED Light Bar Input Current | $I_L$ | 21 | mA |

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

## 5.2 OPTICAL SPECIFICATIONS

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | $\theta_x$=0°, $\theta_Y$ =0° CS-2000 R=G=B=255 Gray scale | 600 | 800 | - | - | (2), (5) ,(7) |
| Response Time | | $T_{R+}T_F$ | | - | 25 | 30 | ms<br>ms | (3) ,(7) |
| CP Luminance of White | | $L_{CP}$ | | 300 | 350 | - | Cd/m$^2$ | (4), (6) ,(7) |
| | White | Wx | | Typ – 0.03 | 0.313 | Typ + 0.03 | - | (4), (6) ,(7) |
| | | Wy | | | 0.329 | | - | |
| | Red | Rx | | | 0.618 | | | |
| | | Ry | | | 0.340 | | | |
| | Green | Gx | | | 0.344 | | | |
| | | Gy | | | 0.300 | | | |
| | Blue | Bx | | | 0.160 | | | |
| | | By | | | 0.074 | | | |
| NTSC | | | | 55 | 60 | % | | (2), (5) ,(7) |
| White Variation | | 5 point | $\theta_x$=0°, $\theta_Y$ =0° | 80 | | | % | (5), (6) ,(7) |
| | | 13 point | | 67 | | | | |
| Flicker | | | | | | -30 | dB | (8) |
| Crosstalk | | | | | | 2 | % | (9) |
| Viewing Angle | Horizontal | θx+ | CR > 10 | 85 | 89 | - | Deg. | (1),(5) , (7) |
| | | θx- | | 85 | 89 | | | |
| | Vertical | θx+ | | 85 | 89 | - | | |
| | | θx- | | 85 | 89 | | | |

Note (1) Definition of Viewing Angle (θx, θy)




Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

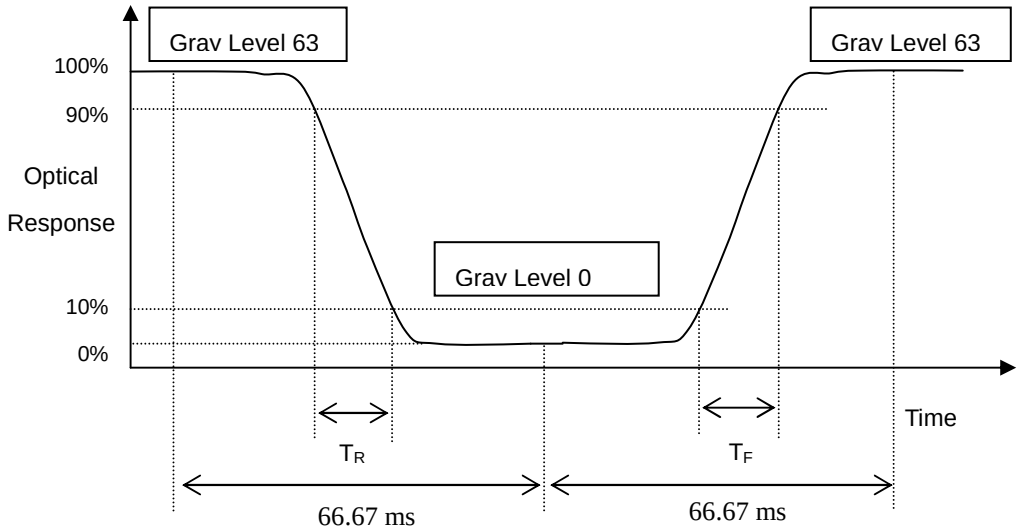
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time ($T_R$, $T_F$):




Note (4) Definition of Center Point Luminance of White ($L_{CP}$):

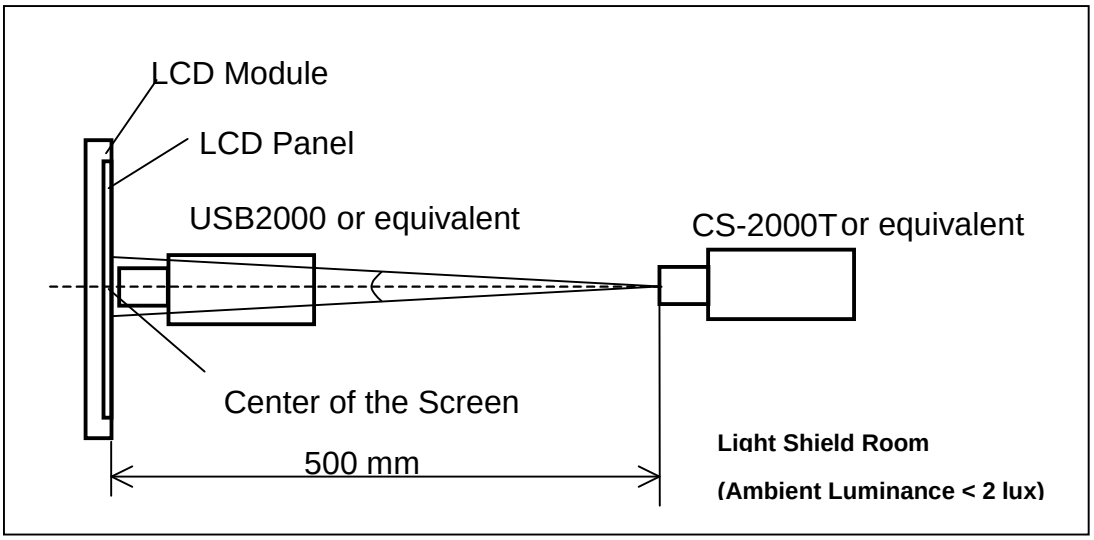
Measure the luminance of gray level 63 at center point

$L_{CP}$ = L(5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

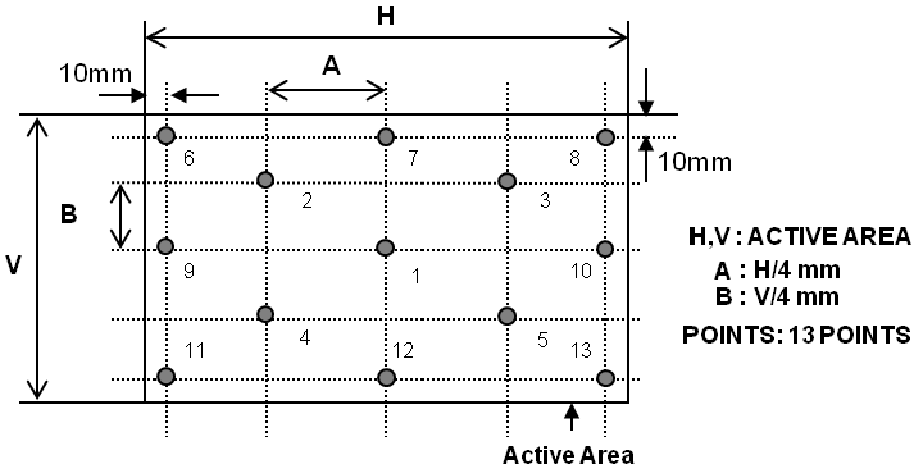



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 13 points

$\delta W_{13p}$ = {Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%

Active area




Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note(8) Flicker

No visual flicker will be allowed. The flicker level should be measured on GS127, The output signal is measured by Minolta CA210 immediately while Vcom is optimized. The flicker is

essentially a ratio of the Amplitude in the frequency spectrum at 30 Hz (A30) and 0 Hz (A0), i.e.,

$$F = 20 \text{ Log } (A30 / A0).$$

Note(9) Crosstalk

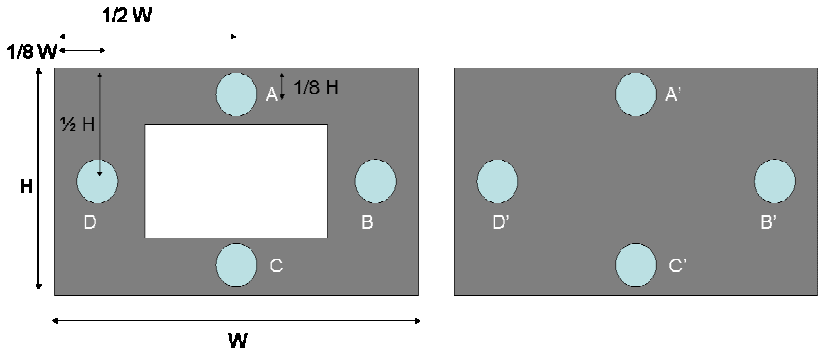
No visual cross-talk will be allowed. Two luminance values are measured at the same position (i.e. A and A'). The cross-talk, is defined as,

$$C(A, B, C, D)=| (L(A', B', C', D') – L(A, B, C, D))/L(A, B, C, D) | • 100\%,$$

Where, L(A, B, C, D) = Luminance in Position A, B, C, D

L(A', B', C', D') = Luminance in Position A', B', C', D'

Crosstalk=max (C(A), C(B), C(C), C(D))




Background : GS 127

Center Pattern: GS 255, 50%(W) x 50%(H).

## 6. RELIABILITY TEST ITEM

| Test Item | Test Condition | Note |
|---|---|---|
| High Temperature Storage Test | 70ºC, 240 hours | (1) (2) |
| Low Temperature Storage Test | -20ºC, 240 hours | |
| Thermal Shock Storage Test | -20ºC, 0.5hour←→70℃, 0.5hour; 100cycles, 1hour/cycle | |
| High Temperature Operation Test | 60ºC, 240 hours | |
| Low Temperature Operation Test | -10ºC, 240 hours | |
| High Temperature & High Humidity Storage Test | 60ºC, RH 90%, 240hours | |
| ESD Test (Operation) | Condition 1 : Contact Discharge, ±8KV<br>Condition 2 : Air Discharge, ±12KV | (1) |
| Shock (Non-Operating) | 220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z | (1)(3) |
| Vibration (Non-Operating) | 1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z | (1)(3) |

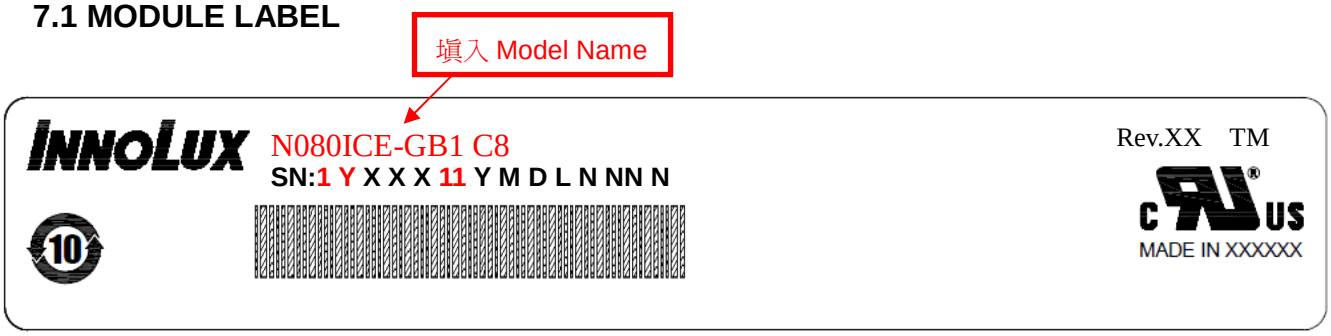
Note (1) criteria : Normal display image with no mura and extra line defect.
(should be checked with 6% ND filter and within 45° viewing angle from vertical)

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

## 7. PACKING

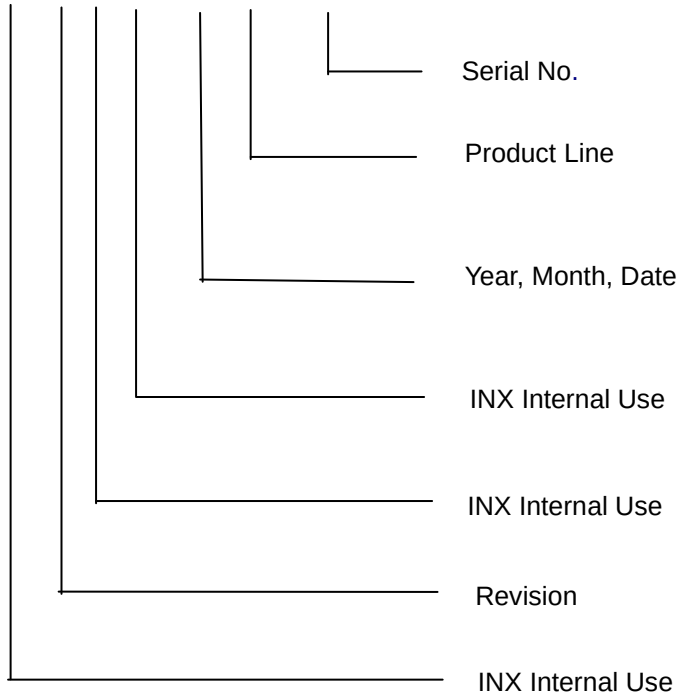
### 7.1 MODULE LABEL




(a) Model Name: **N080ICE-GB1 C8**

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N




(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL factory code stands for panel manufactured by Innolux satisfying UL requirement. Marking as follows rule :

"LEOO" for Ningbo NA
"VIRO" for Ningbo NB,NC
"CANO" for Ningbo ND
"GEMN" for Tainan LCM1,LCM4
" " for Tainan J001

## 7.2 CARTON

(1) Box Dimensions : 489(L)*382(W)*275(H)
(2) 60 Modules/Carton

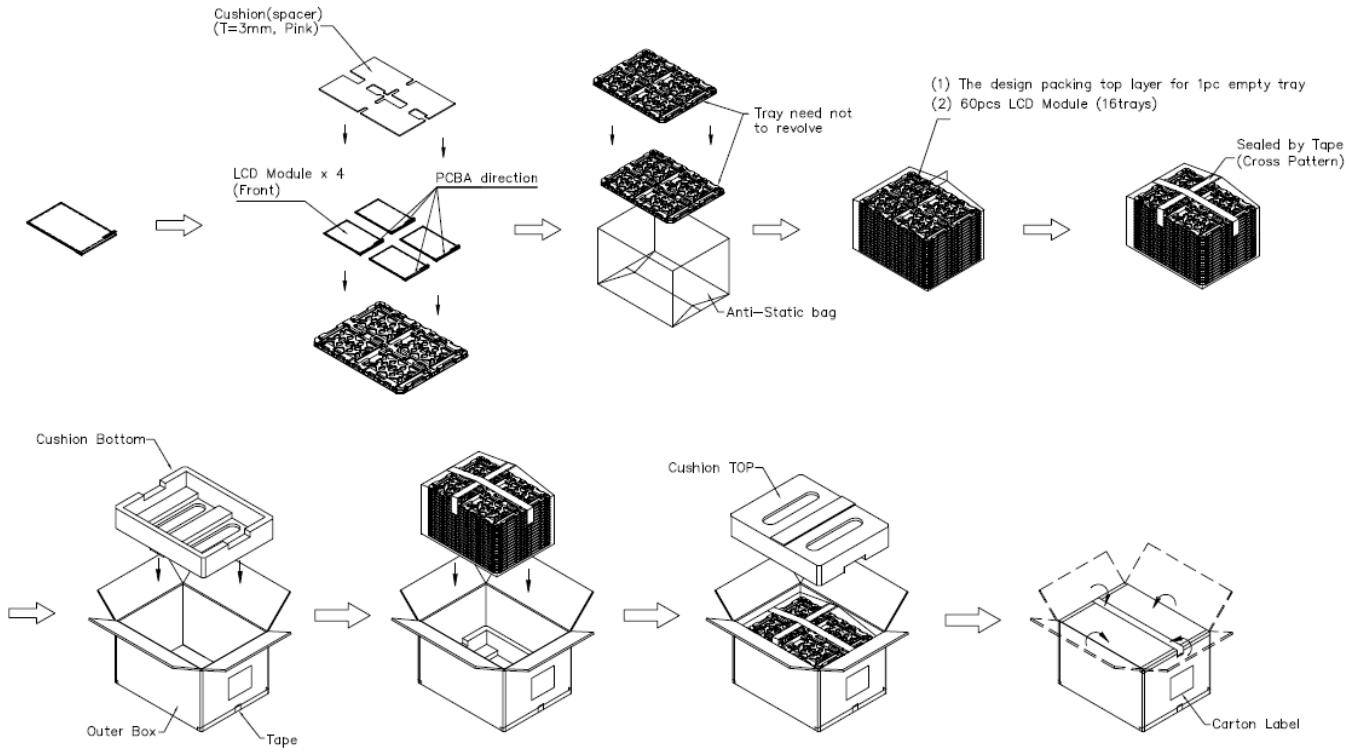



**Figure. 7-1 Packing method**

### 7.3 PALLET

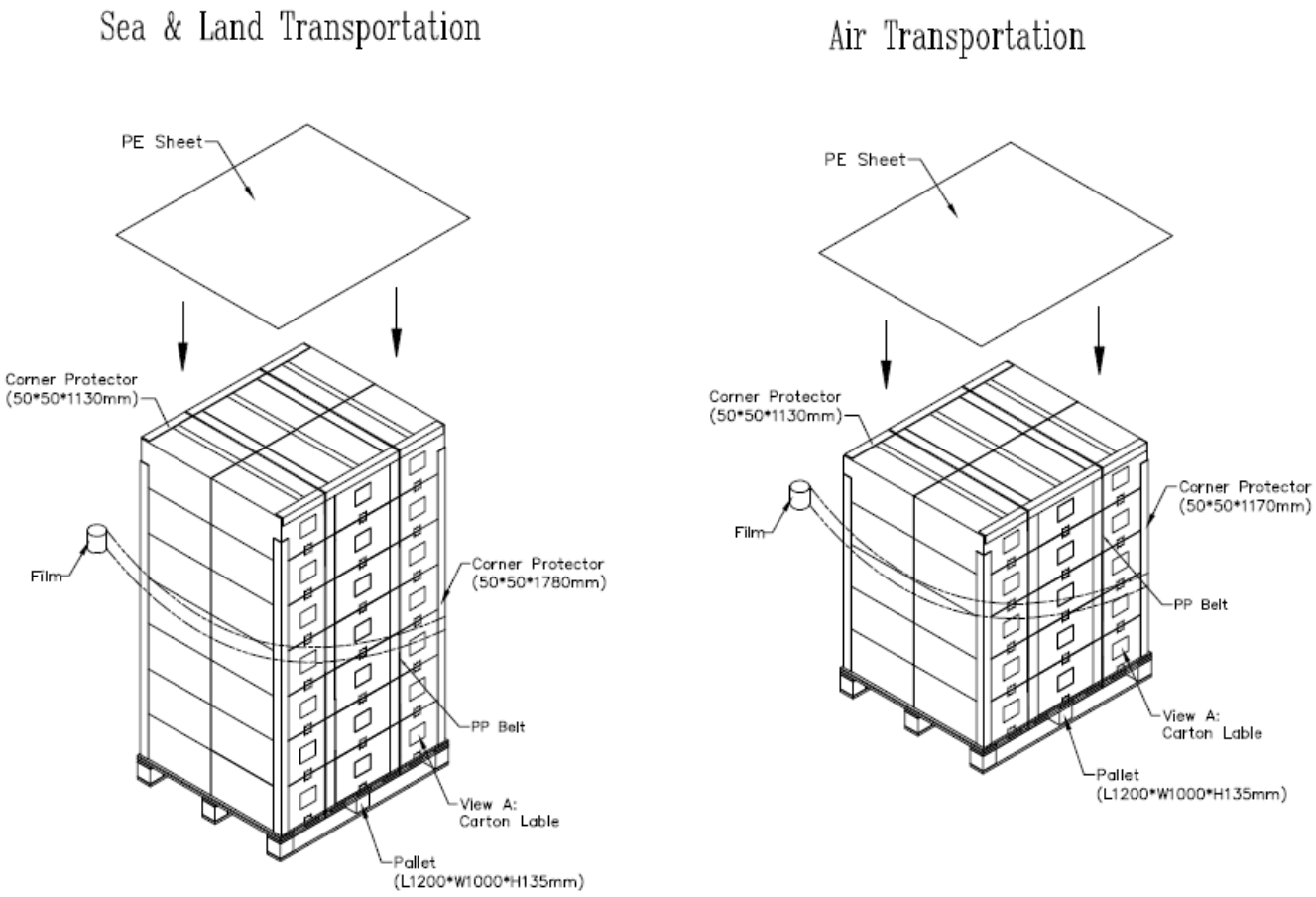



**Figure. 7-2 Packing method**

## 7.4 Un-Packing

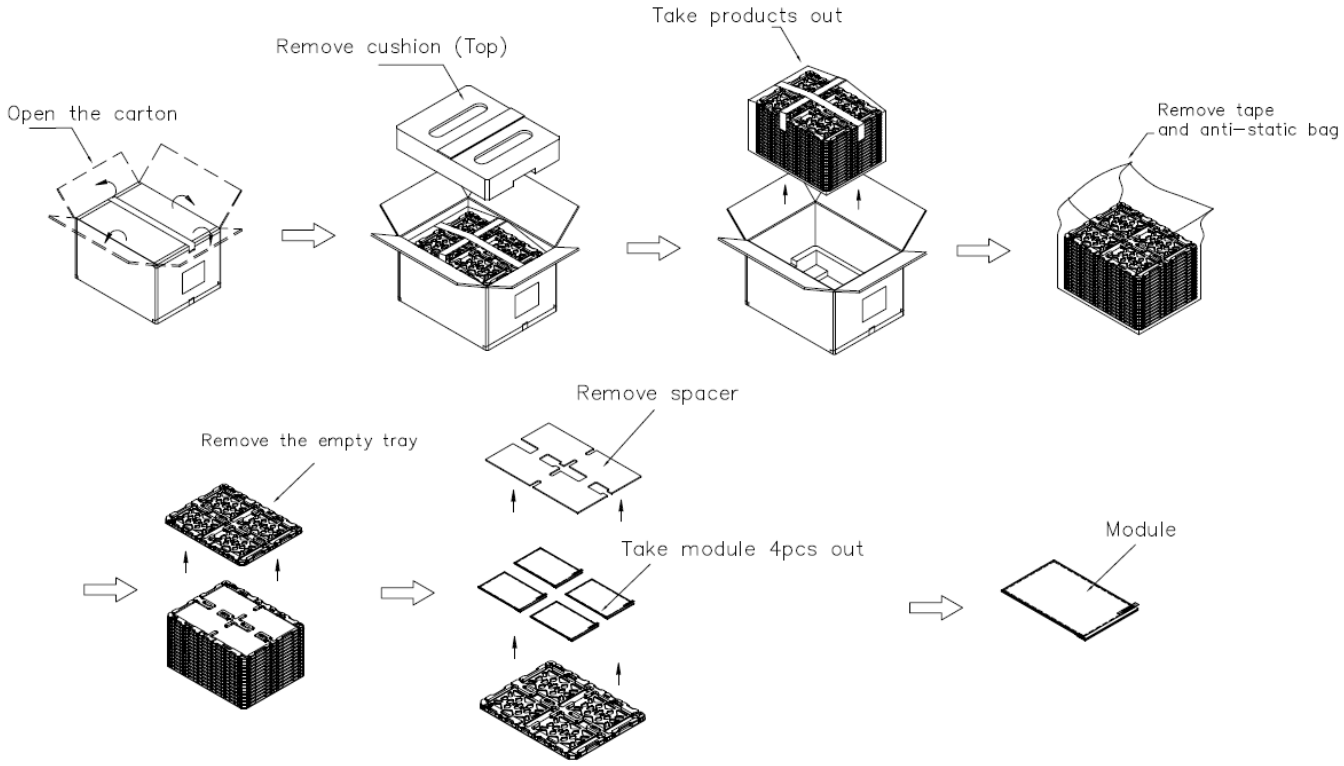



**Figure. 7-3 Un-Packing method**

# 8. PRECAUTIONS

## 8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

## 8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

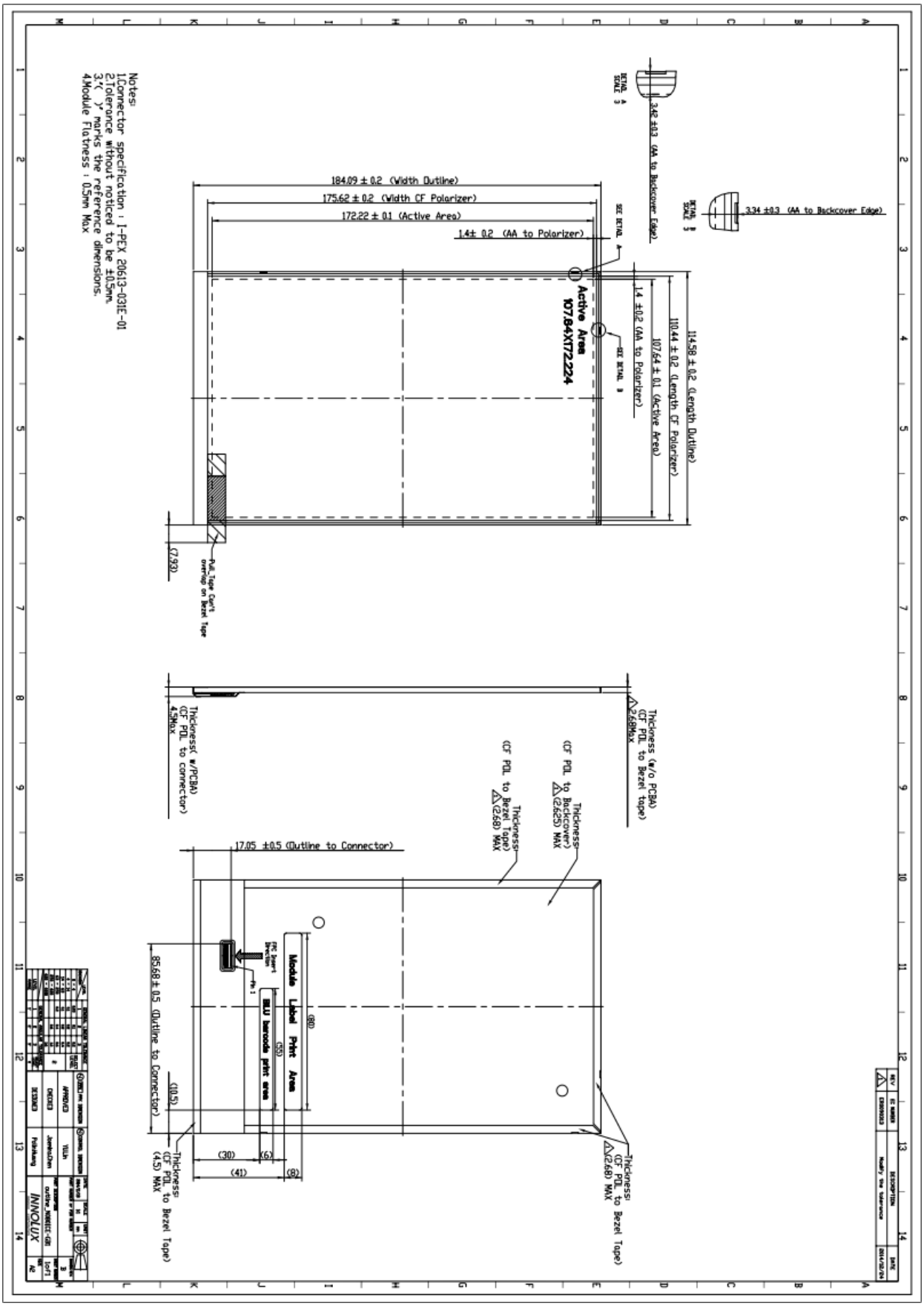
## 8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

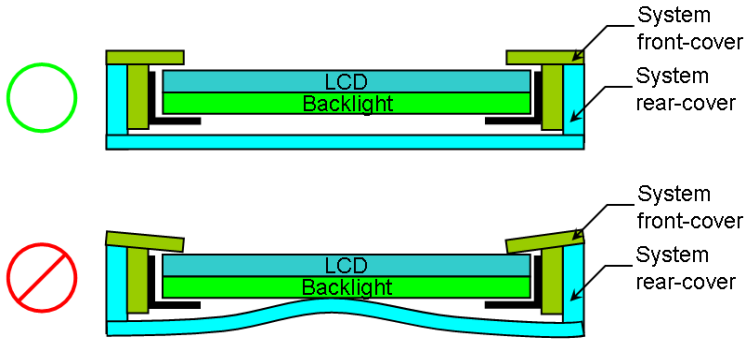
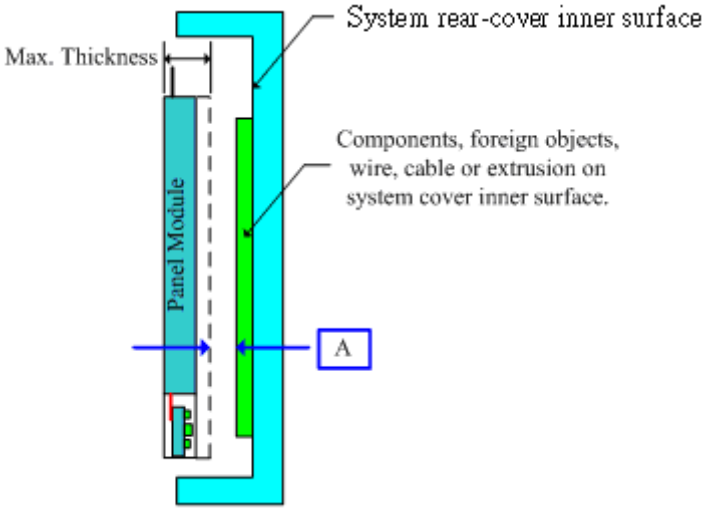
(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

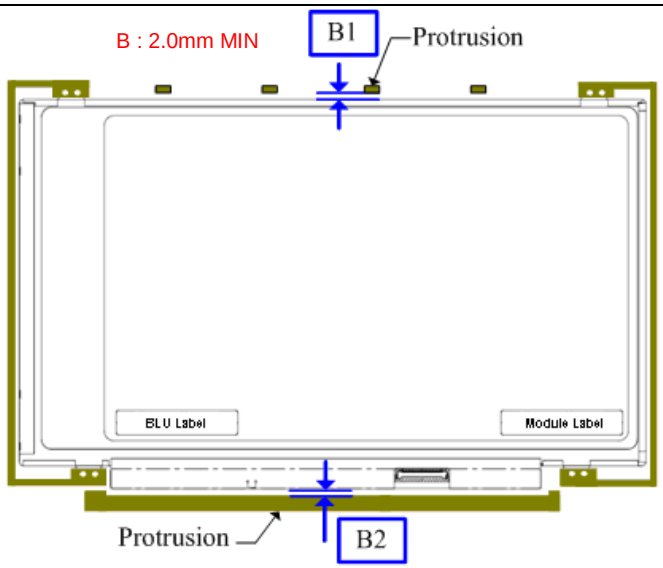
(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the backlight unit.

## Appendix. OUTLINE DRAWING (Label position will be updated as requirement)

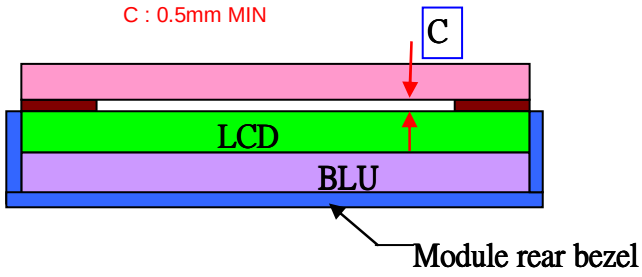


Appendix II. SYSTEM COVER DESIGN GUIDANCE

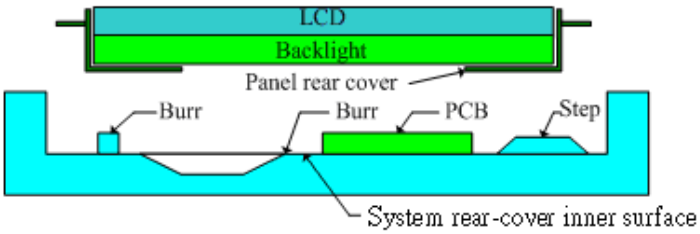
| | |
|---|---|
| **1.** | **Permanent deformation of system cover after reliability test** |
| |  |
| Definition | System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. |
| **2.** | **Design gap A between panel & any components on system rear-cover** |
| |  |
| Definition | Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Flatness of panel and system rear-cover should be taken into account for gap design. |
| **3** | **Design gap B1 & B2 between panel & protrusions** |



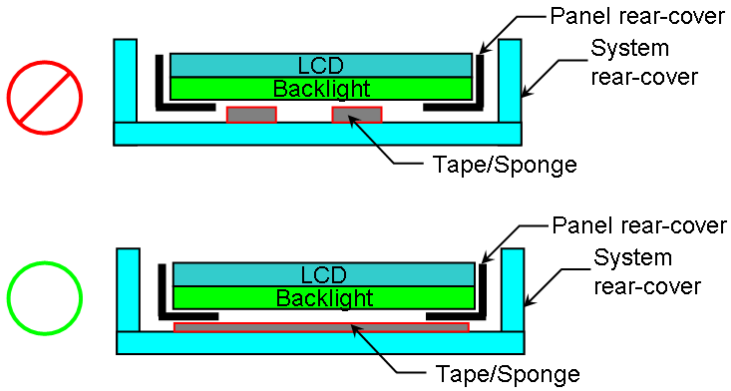

| | |
|---|---|
| Definition | Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. |
| **4** | **Design gap C between touch panel & panel surface.** |



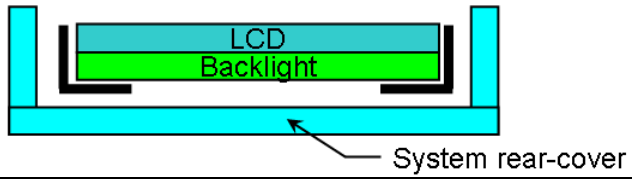

| | |
|---|---|
| Definition | Air gap design between touch panel & panel surface is needed to prevent pooling, newton ring or glass broken. Compression ration of double side tape may cause pooling issue or newton ring. This phenomenon is obvious during pooling inspection procedure.<br>To remain sufficient gap between touch panel and panel surface is recommended. |
| **5** | **System rear-cover inner surface examination** |



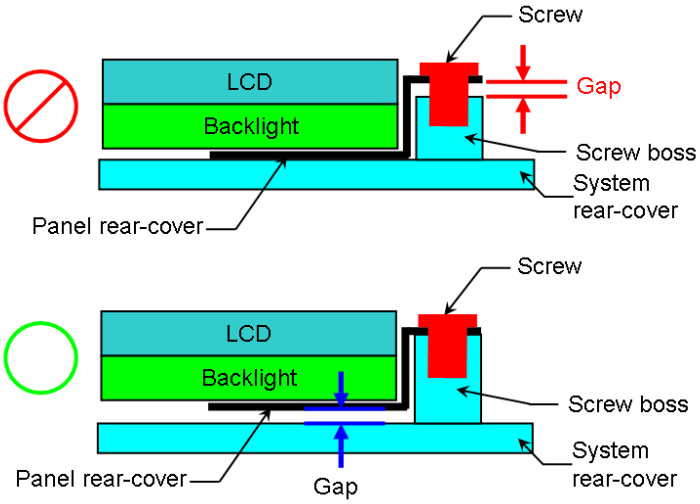

| | |
|---|---|
| Definition | Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test. |
| **6** | **Tape/sponge design on system inner surface** |



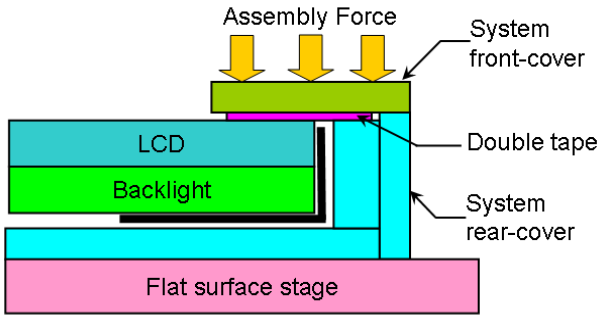

| | |
|---|---|
| Definition | To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location. |
| **7** | **Material used for system rear-cover** |




| | |
|---|---|
| Definition | System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test.<br>Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference. |
| **8** | **Screw boss height design** |




| | |
|---|---|
| Definition | Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur. |
| **9** | **Assembly SOP examination for touch panel with double side tape design** |




| | |
|---|---|
| Definition | To prevent panel crack during touch panel assembly process with double tape design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly. |