Doc. Number:

■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: N133FGE
SUFFIX: L31

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
楊竣傑 2011-09-15 20:21:56 CST	陳逸銘 2011-09-08 10:34:40 CST	阮經綸 2011-08-31 10:45:46 CST

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
0.0	Aug.17, 2011	All	Tentative spec Ver.0.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N133FGE-L31 is a 13.3" (13.3" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1600 x 900 HD+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	13.3 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1600 x R.G.B. x 900	pixel	-
Pixel Pitch	0.18375 (H) x 0.18375 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Anti-Glare, Haze 14%	-	-
Luminance, White	300	Cd/m2	
Power Consumption	TBD		(1)

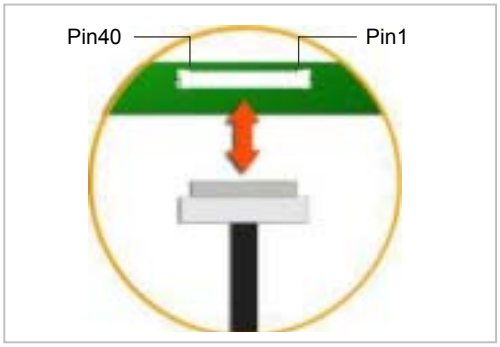
Note (1) The specified power consumption is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and fv = 60 Hz, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	305.8	306.3	306.8	mm	(1)
	Vertical (V) (W/ PCBA)	187.7	188.2	188.7	mm	
	Thickness (T) (W/ PCBA)	NA	NA	3	mm	
	Thickness (T) (W/O PCBA)	NA	2.48	2.68		
Active Area	Horizontal	293.7	294	294.3	mm	
	Vertical	165.075	165.375	165.675	mm	
Weight		-	200	210	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12 or FOXCONN GS13401-1110A-7H or equivalent

User's connector Part No: IPEX-20453-040T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

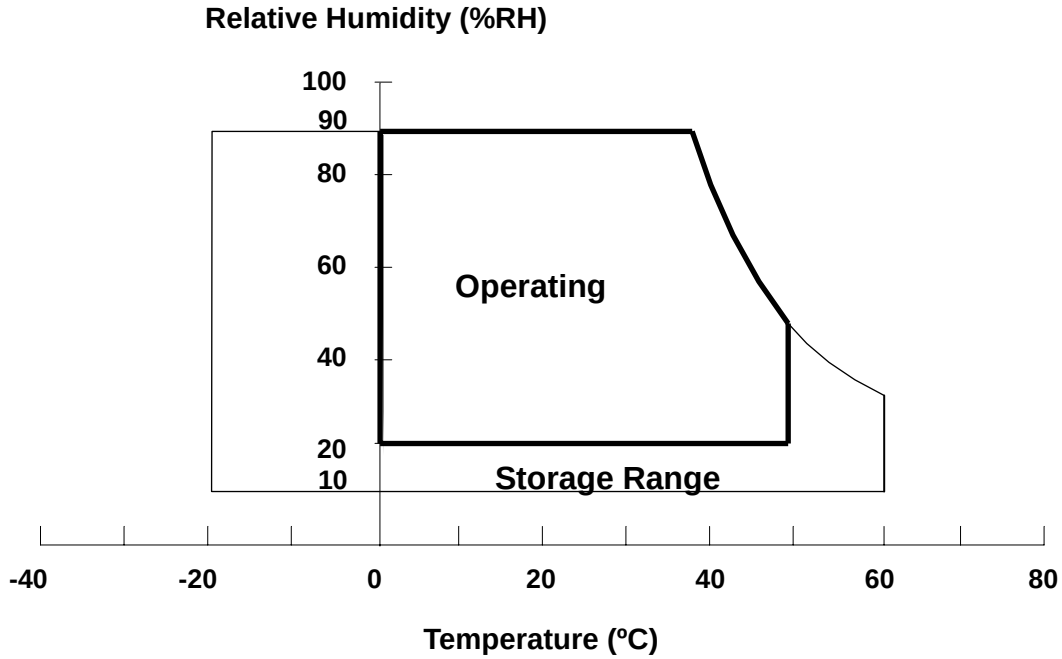
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

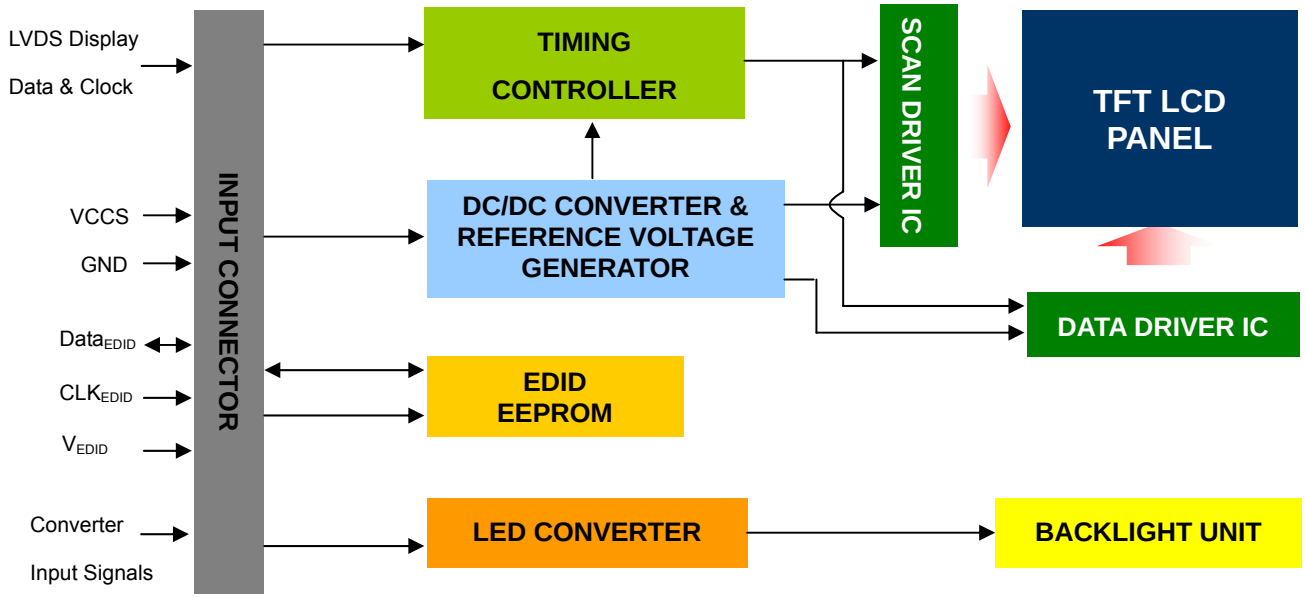
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	(25)	V	
Converter Control Signal Voltage	LED_PWM,	-0.3	(5)	V	
Converter Control Signal Voltage	LED_EN	-0.3	(5)	V	

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



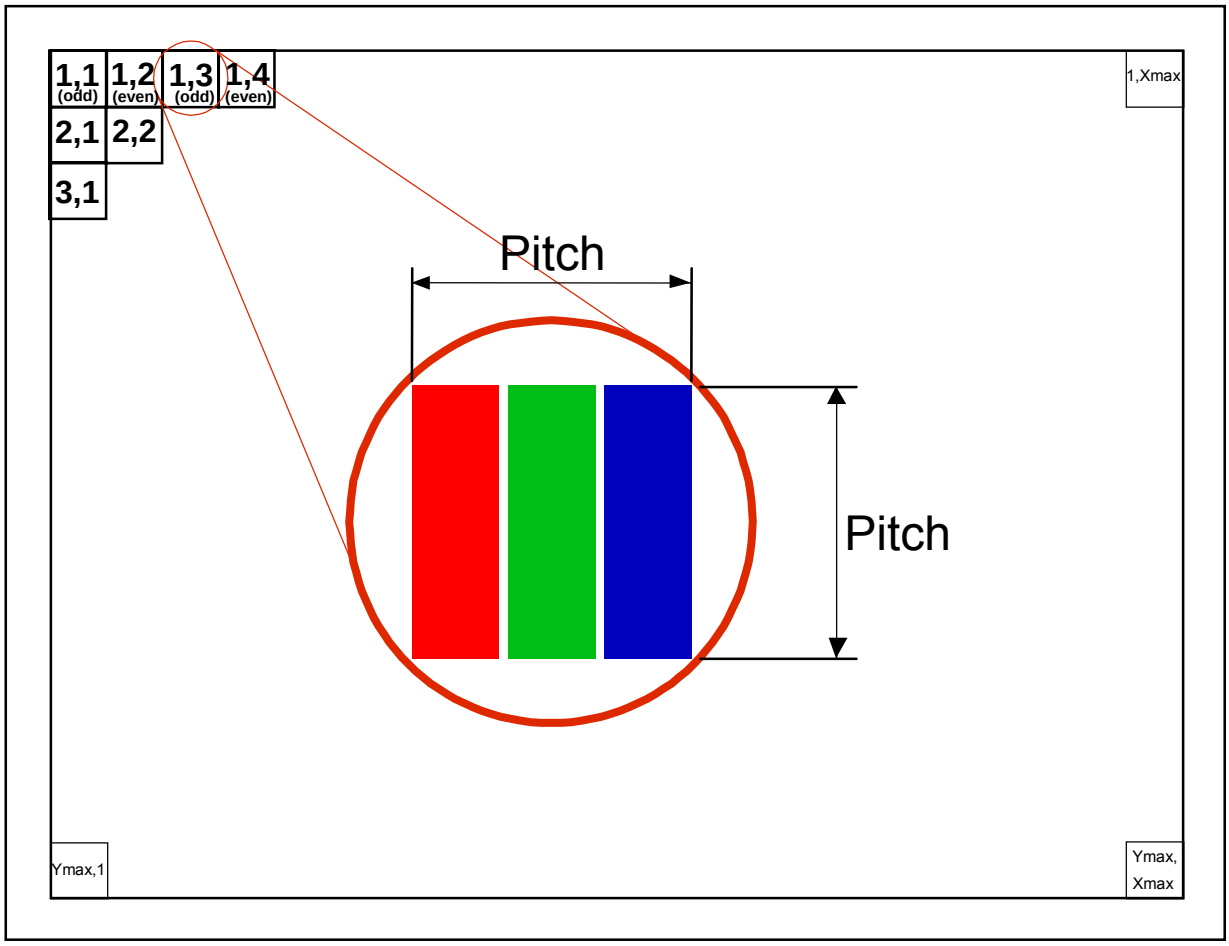
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserve)	
2	VCCS	Power Supply (3.3V typ.)	
3	VCCS	Power Supply (3.3V typ.)	
4	VEDID	DDC 3.3V power	
5	NC	No Connection (Reserved for CMI test)	
6	CLKEDID	DDC clock	
7	DATAEDID	DDC data	
8	RXO0-	LVDS Differential Data Input (Odd)	R0-R5, G0
9	RXO0+	LVDS Differential Data Input (Odd)	
10	VSS	Ground	
11	RXO1-	LVDS Differential Data Input (Odd)	G1~G5, B0, B1
12	RXO1+	LVDS Differential Data Input (Odd)	
13	VSS	Ground	
14	RXO2-	LVDS Differential Data Input (Odd)	B2-B5,HS,VS, DE
15	RXO2+	LVDS Differential Data Input (Odd)	
16	VSS	Ground	
17	RXOC-	LVDS Clock Data Input (Odd)	LVDS CLK
18	RXOC+	LVDS Clock Data Input (Odd)	
19	VSS	Ground	
20	RXE0-	LVDS Differential Data Input (Even)	R0-R5, G0
21	RXE0+	LVDS Differential Data Input (Even)	
22	VSS	Ground	
23	RXE1-	LVDS Differential Data Input (Even)	G1~G5, B0, B1

24	RXE1+	LVDS Differential Data Input (Even)	
25	VSS	Ground	
26	RXE2-	LVDS Differential Data Input (Even)	B2-B5,HS,VS, DE
27	RXE2+	LVDS Differential Data Input (Even)	
28	VSS	Ground	
29	RXEC-	LVDS Clock Data Input (Even)	LVDS CLK
30	RXEC+	LVDS Clock Data Input (Even)	
31	LED_GND	LED Ground	
32	LED_GND	LED Ground	
33	LED_GND	LED Ground	
34	NC	No Connection (Reserve)	
35	LED_PWM	PWM Control Signal of LED Converter	
36	LED_EN	Enable Control Signal of LED Converter	
37	NC	No Connection (Reserve)	
38	LED_VCCS	LED Power Supply	
39	LED_VCCS	LED Power Supply	
40	LED_VCCS	LED Power Supply	

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

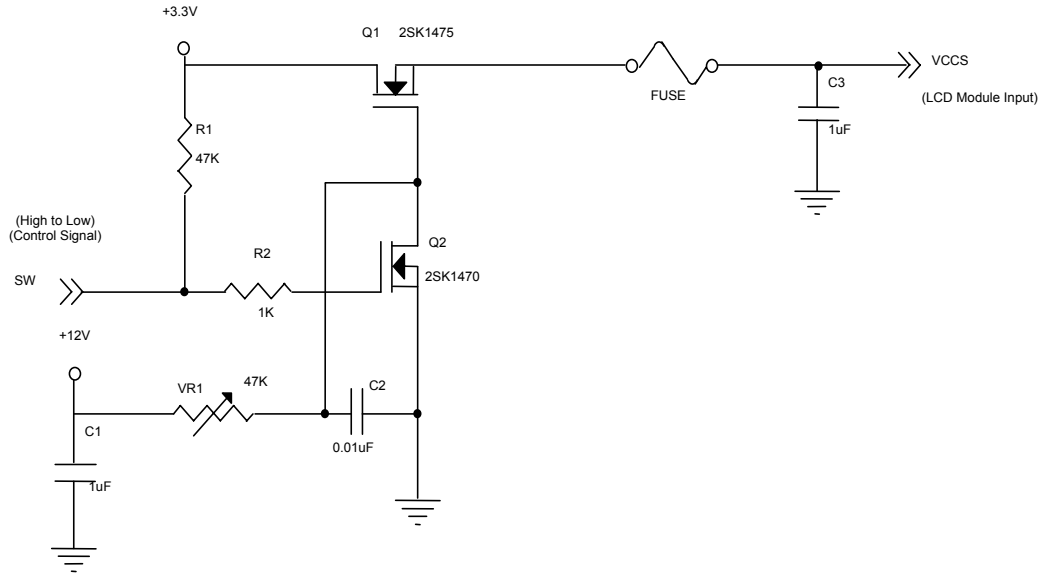
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc		(TBD)	(TBD)	(3)a	(3)a
	Black			(TBD)	(TBD)	(3)b	(3)b

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

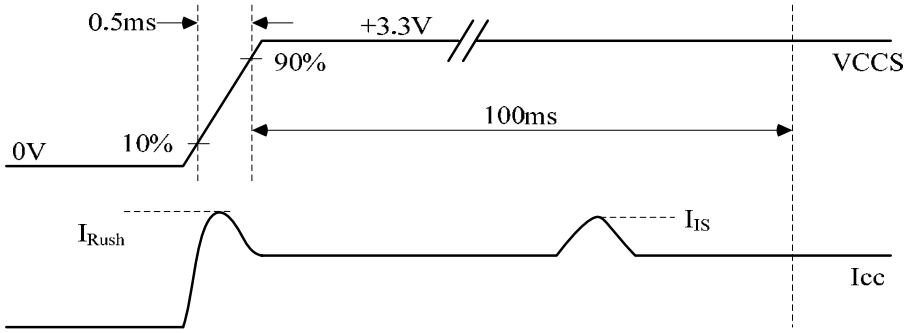
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

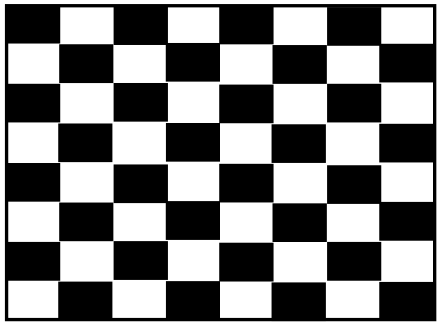


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. Black Pattern

Active Area

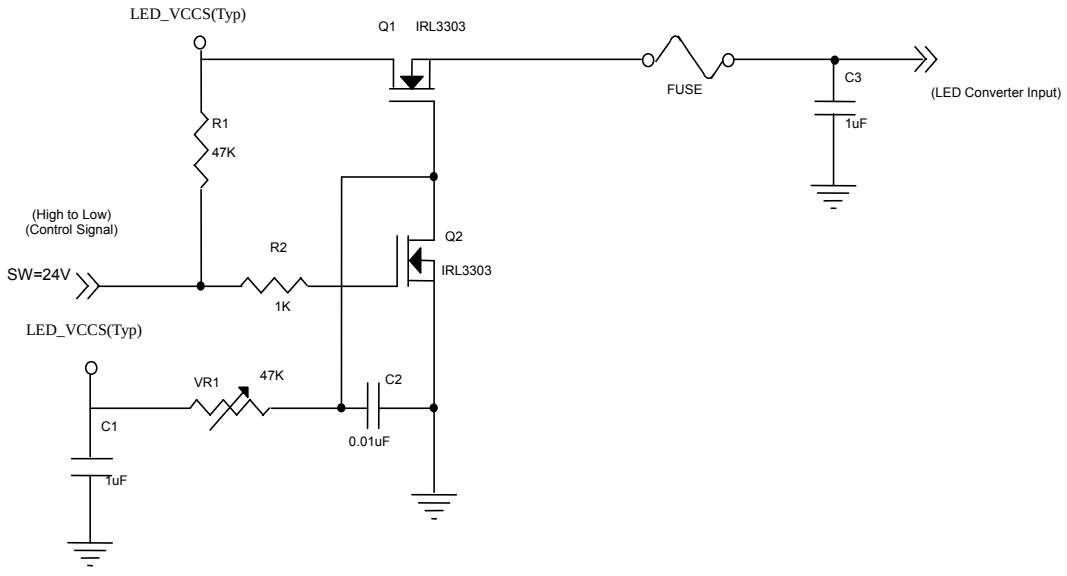
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	(6.0)	(12.0)	(21.0)	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	(1.5)	A	(1)
EN Control Level	Backlight On		(2.3)	-	(5.0)	V	
	Backlight Off		(0)	-	(0.5)	V	
PWM Control Level	PWM High Level		(2.3)	-	(5.0)	V	
	PWM Low Level		(0)	-	(0.5)	V	
PWM Control Duty Ratio			(10)	-	(100)	%	
			(5)	-	(100)	%	(2)
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	(100)	mV	
PWM Control Frequency		f_{PWM}	(190)	-	(2K)	Hz	(3)
LED Power Current	LED_VCCS =Typ.	ILED	(132)	(165)	(185)	mA	(4)

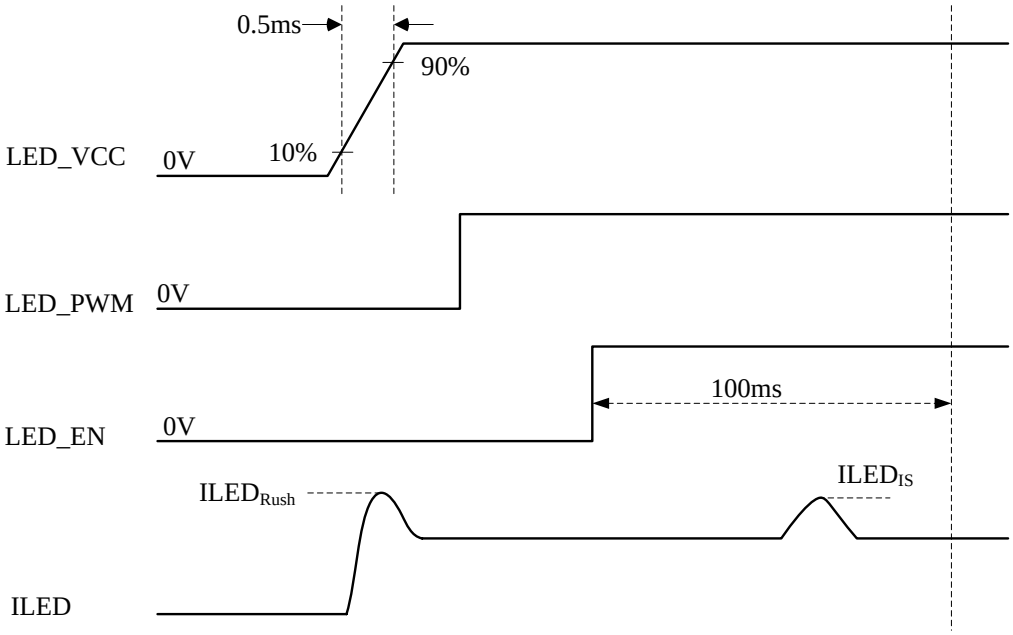
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it’s a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

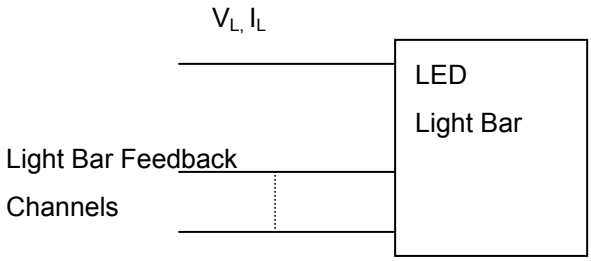
Note (4) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	25	29	30	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	57	60	63	mA	
Power Consumption	P_L	1.425	1.74	1.89	W	(3)
LED Life Time	L_{BL}	15,000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 ^oC and I_L = 15 mA(Per EA) until the brightness becomes $\leqq$ 50% of its original value.

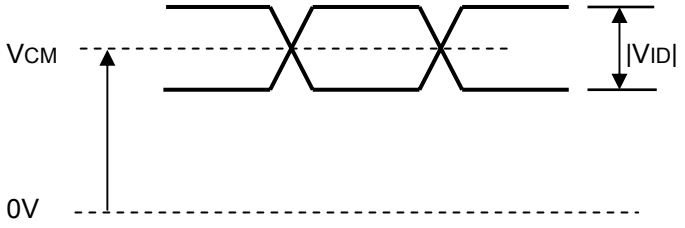
4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 LVDS DC SPECIFICATIONS

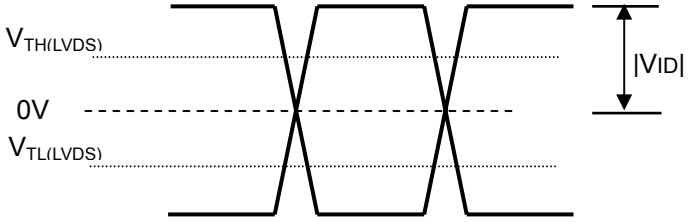
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), V_{CM}=1.2V
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1) V_{CM}=1.2V
LVDS Common Mode Voltage	V_{CM}	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	$\|V_{ID}\|$	100	-	600	mV	(1)
LVDS Terminating Resistor	R_T	-	100	-	Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.

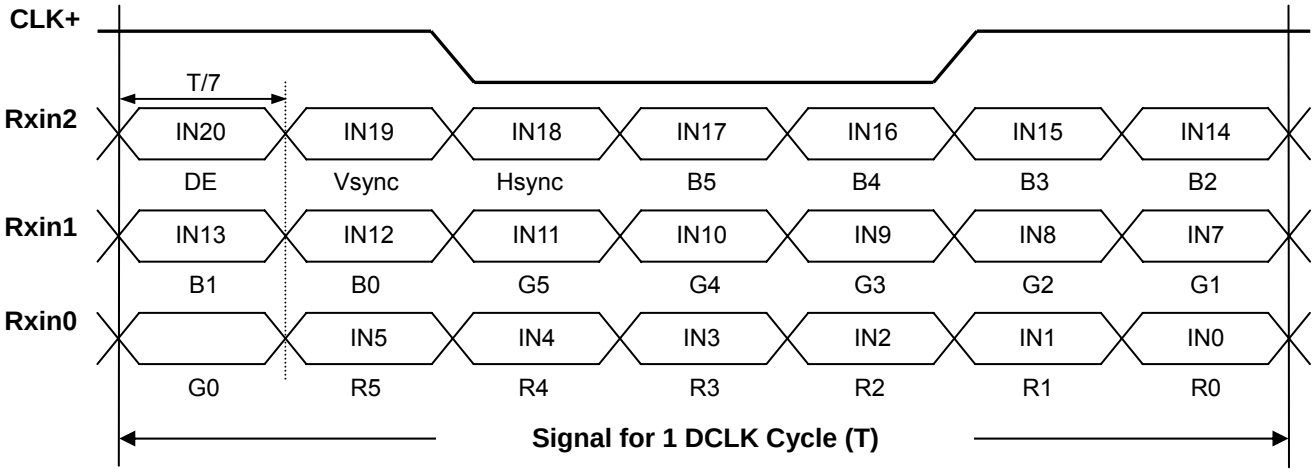
Single Ended



Differential



4.4.2 LVDS DATA FORMAT



4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

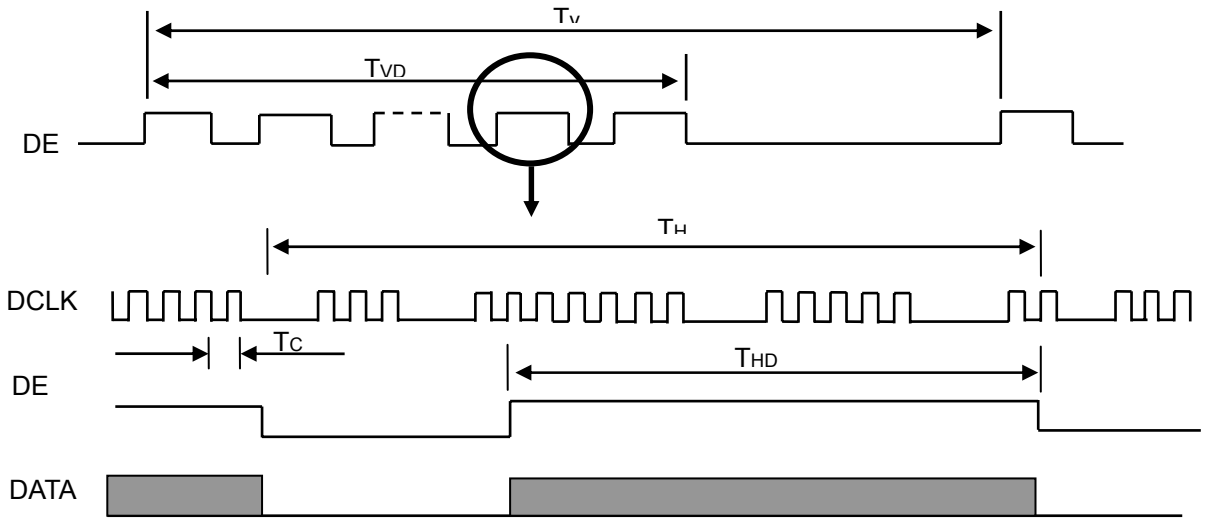
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(32.50)	(48.89)	(53.78)	MHz	-
DE	Vertical Total Time	TV	(TBD)	926	(TBD)	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	-
	Horizontal Total Time	TH	(TBD)	1760	(TBD)	Tc	-
	Horizontal Active Display Period	THD	1600	1600	1600	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

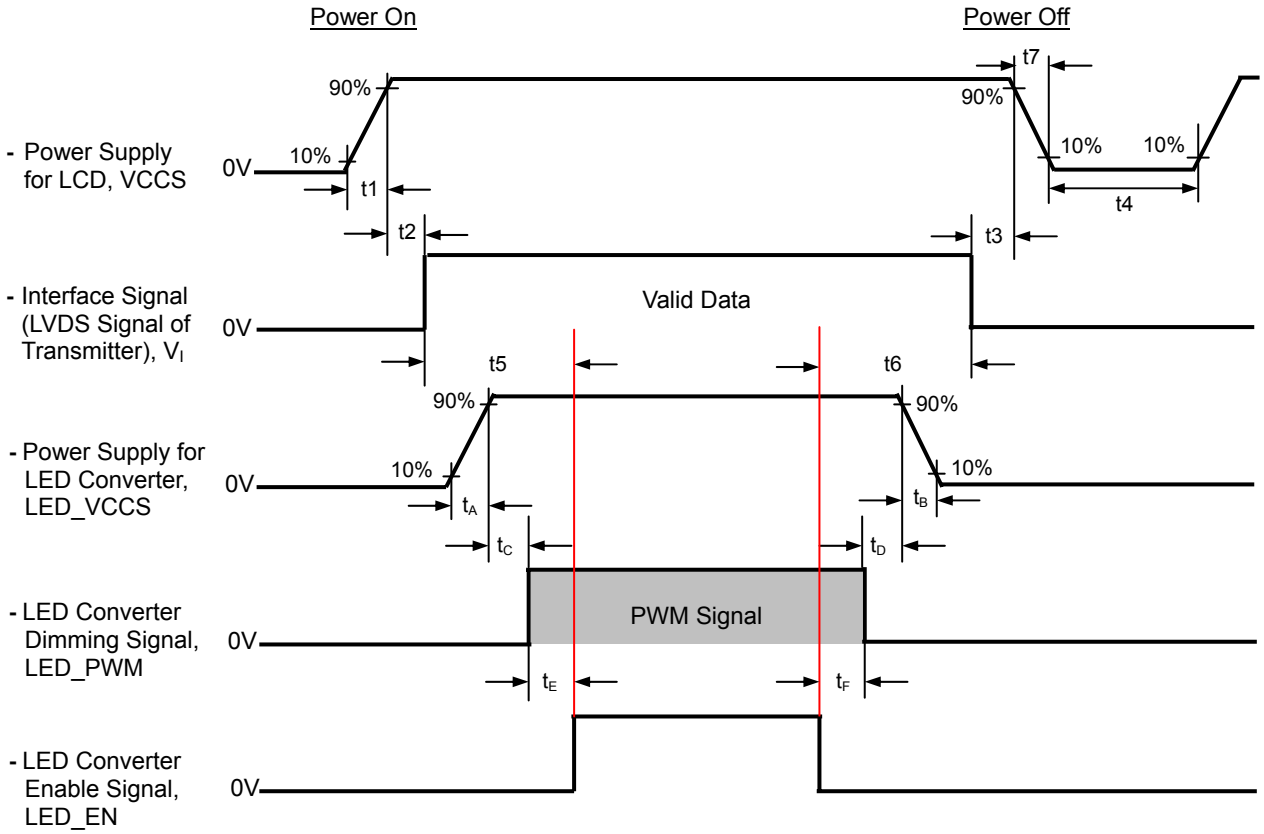
INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t1	(0.5)	-	(10)	ms	
t2	(0)	-	(50)	ms	
t3	(0)	-	(50)	ms	
t4	(500)	-	-	ms	
t5	(200)	-	-	ms	
t6	(200)	-	-	ms	
t7	(0.5)	-	(10)	ms	
t_A	(0.5)	-	(10)	ms	
t_B	(0)		(10)	ms	
t_C	(10)	-	-	ms	
t_D	(10)	-	-	ms	
t_E	(10)	-	-	ms	
t_F	(10)	-	-	ms	



Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

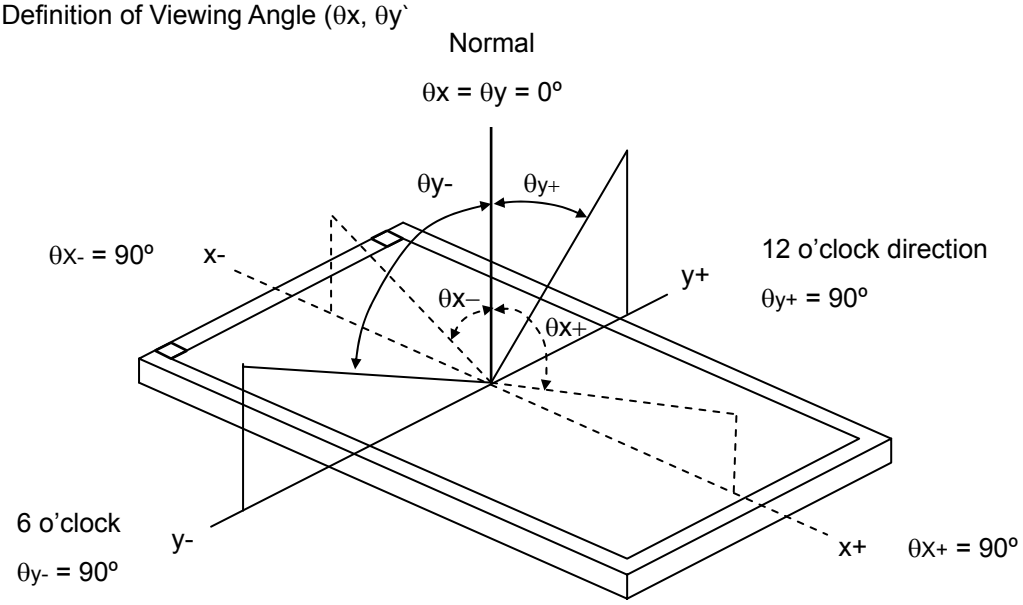
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	60	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	300	500	-	-	(2), (5), (7)
Response Time		T_R		-	3	4	ms	(3), (7)
		T_F		-	7	12	ms	
Average Luminance of White		L_{AVE}		260	300	-	cd/m^2	(4), (6), (7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.648	Typ + 0.03	-	(1), (7)
		Ry			0.332		-	
	Green	Gx			0.324		-	
		Gy			0.629		-	
	Blue	Bx			0.155		-	
		By			0.135		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45		Deg.	(1), (5), (7)
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		
Brightness Full width at Half-maximum		Horizontal	1/2 L_{AVE}	45			Deg.	(1), (5), (7)
		Vertical		23				
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	70	-	-	%	(5), (6),

Note (1) Definition of Viewing Angle (θx, θy`



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

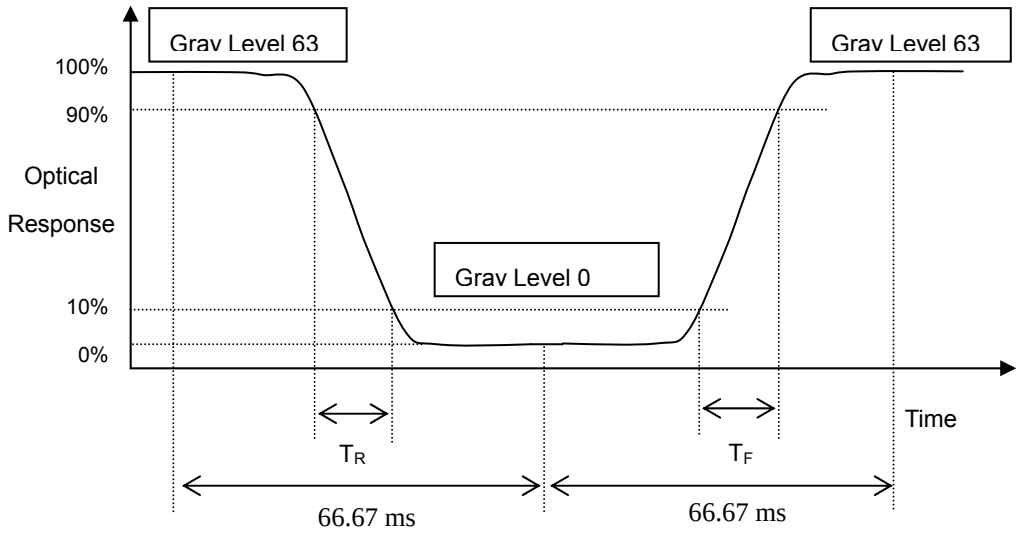
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

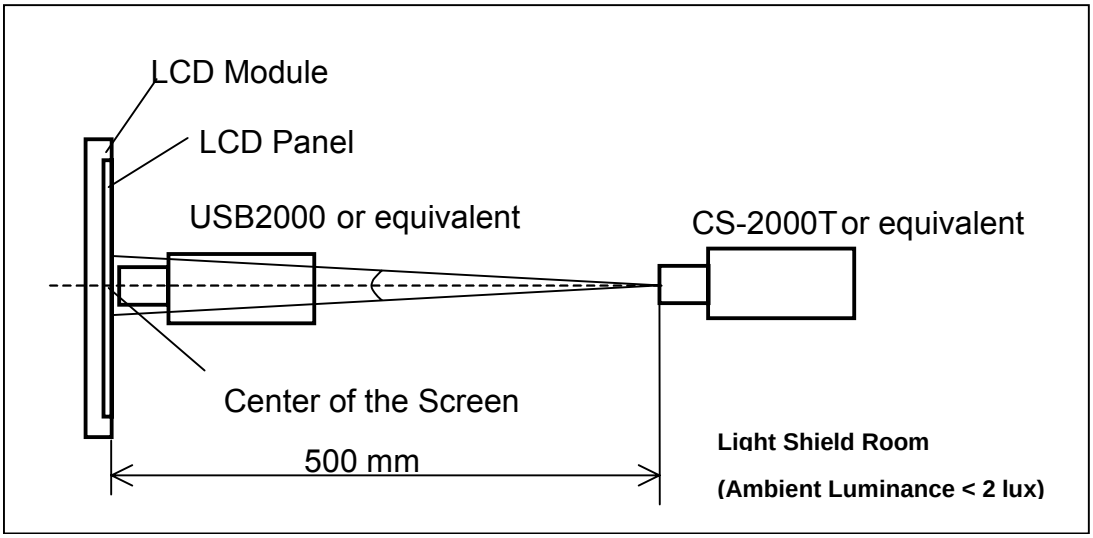
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

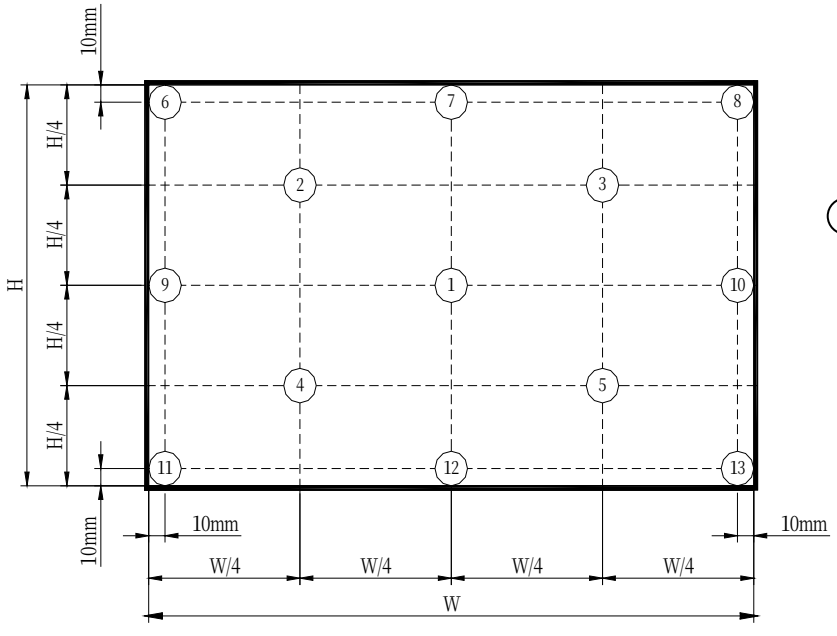
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Minimum [L (1)~L (5)] / Maximum [L (1)~ L (5)]}*100%



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N133FGE - L31

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- CMI Internal Use
- Revision
- CMI Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

(e) UL logo: “XXXX” is factory ID

7.2 CARTON

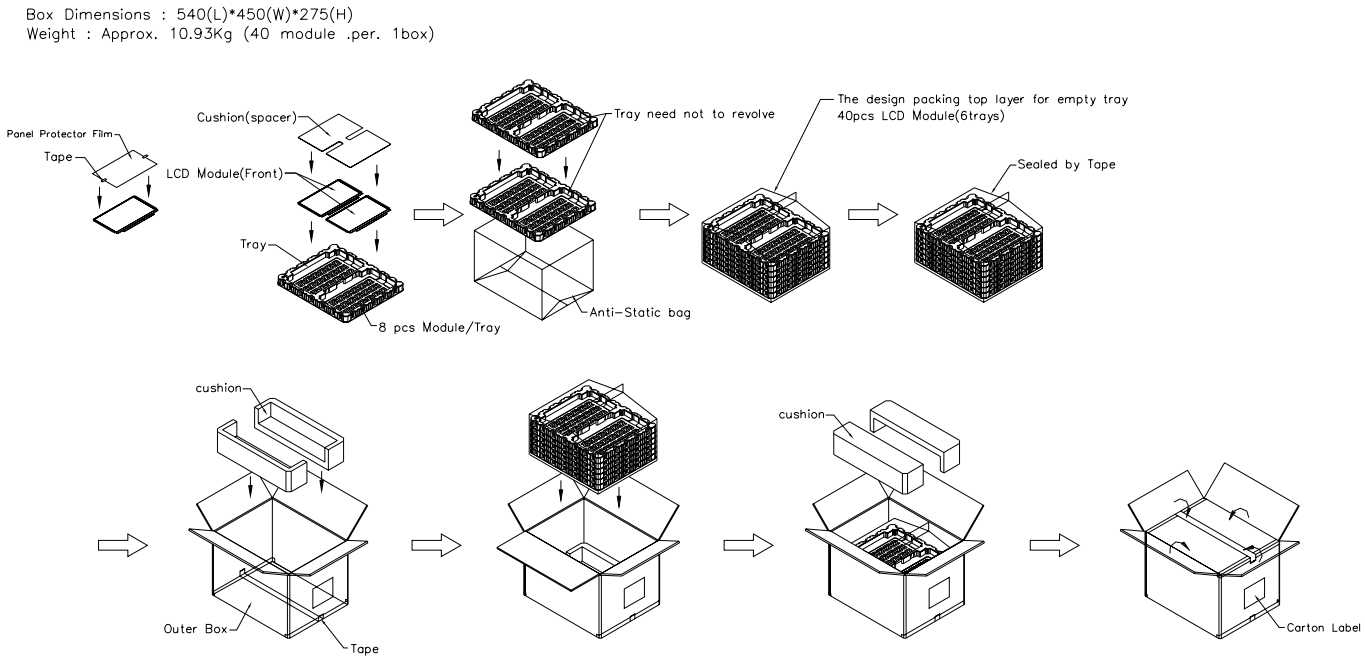


Figure. 7-2 Packing

7.3 PALLET

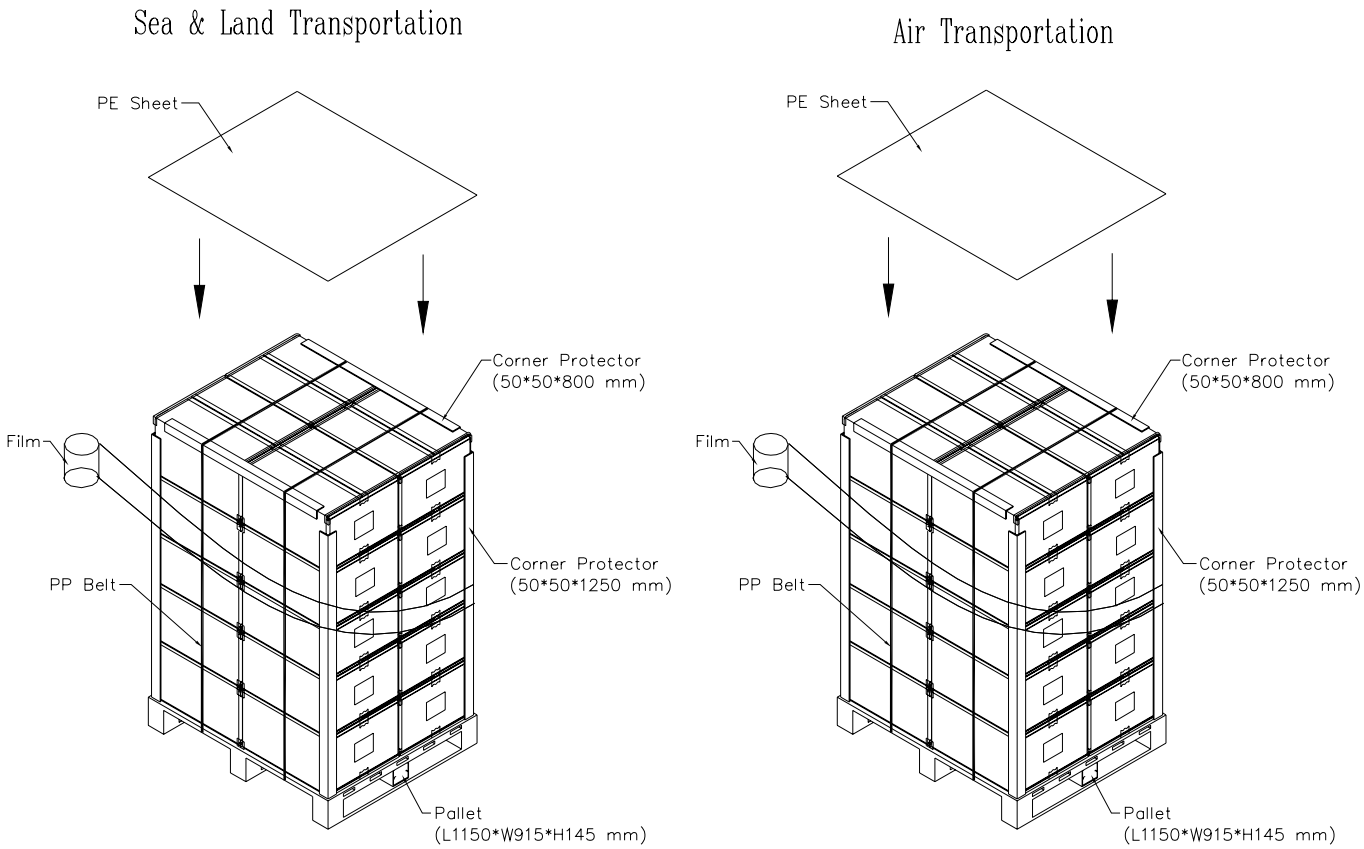


Figure. 7-3 Packing

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

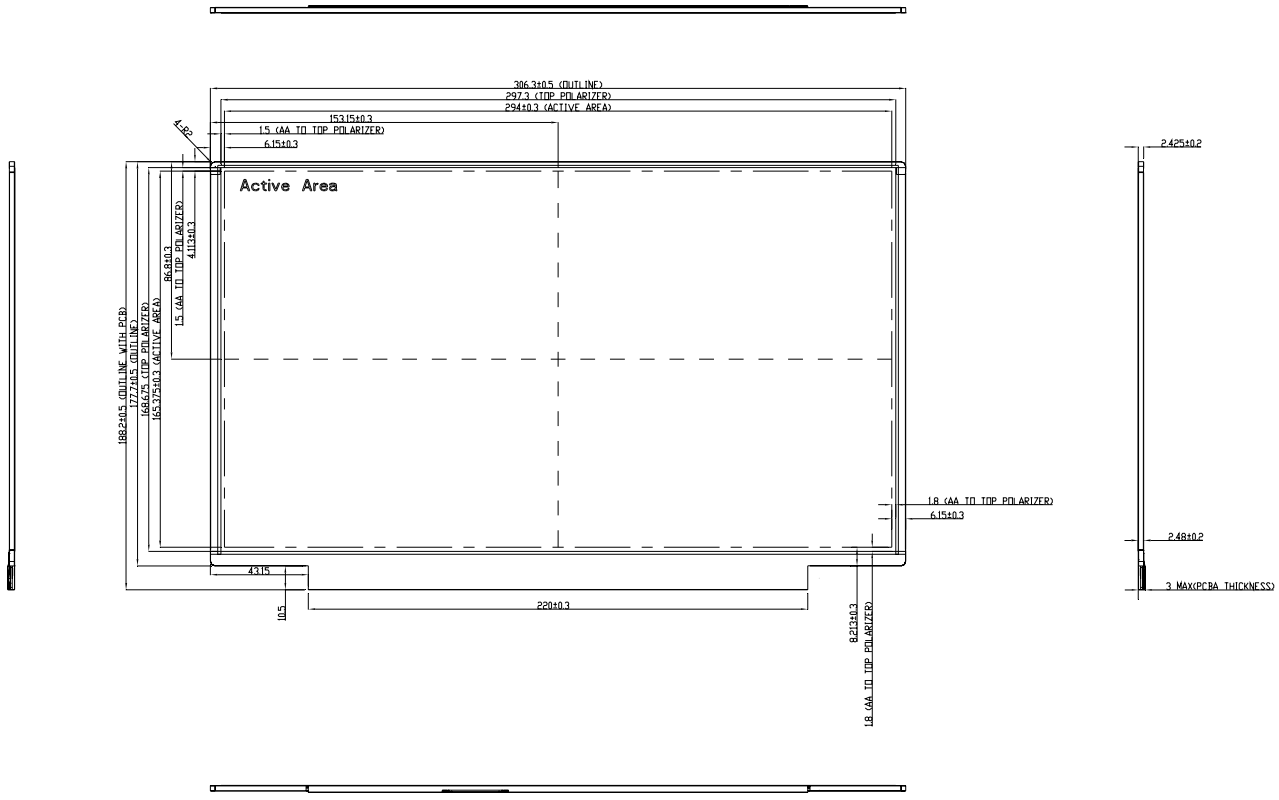
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

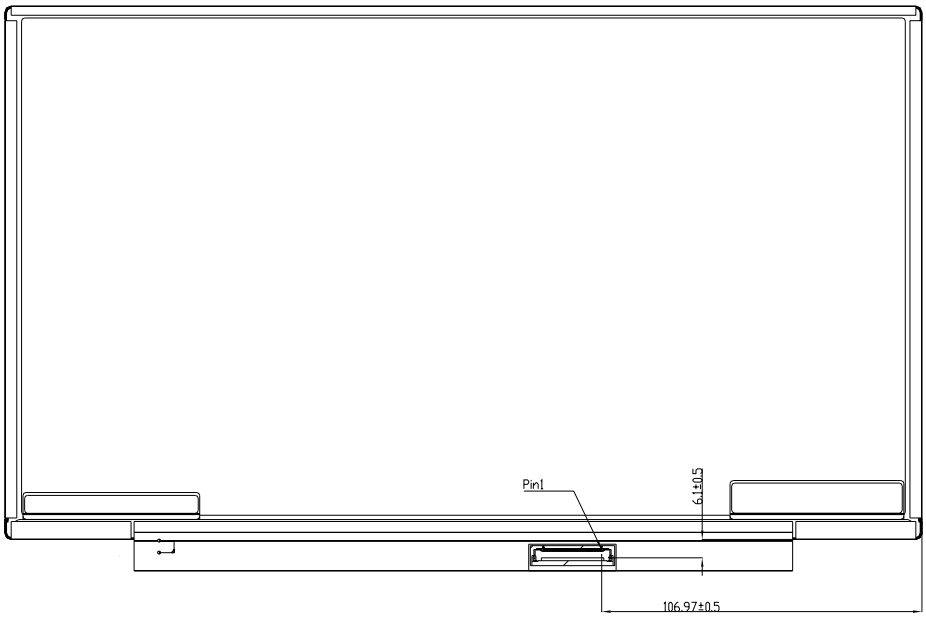
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMN”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AE	10101110
10	0A	ID product code (N133FGE-L31)	40	01000000
11	0B	ID product code (hex LSB first; N133FGE-L31)	13	00010011
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	02	00000010
17	11	Year of manufacture (fixed year code)	16	00010110
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Max H image size (“ 29.40cm”)	1D	00011101
22	16	Max V image size (“16.53 cm”)	10	00010000
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“Active off, RGB Color”)	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	CF	11001111
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	15	00010101
27	1B	Rx=0.659	A8	10101000
28	1C	Ry=0.332	55	01010101
29	1D	Gx=0.331	54	01010100
30	1E	Gy=0.616	9D	10011101
31	1F	Bx=0.148	26	00100110
32	20	By=0.044	0B	00001011
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (100.22 MHz”, According to VESA CVT Rev1.1)	26	00100110
55	37	# 1 Pixel clock (hex LSB first)	27	00100111
56	38	# 1 H active (“1600”)	40	01000000
57	39	# 1 H blank (“160”)	A0	10100000
58	3A	# 1 H active : H blank (“1600 : 160”)	60	01100000
59	3B	# 1 V active (”900”)	84	10000100
60	3C	# 1 V blank (”50”)	32	00110010
61	3D	# 1 V active : V blank (”900 :50”)	30	00110000
62	3E	# 1 H sync offset (”48”)	30	00110000
63	3F	# 1 H sync pulse width ("32”)	20	00100000
64	40	# 1 V sync offset : V sync pulse width (”6 : 10”)	6A	01101010
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 6 : 10”)	00	00000000
66	42	# 1 H image size (”294 mm”)	26	00100110
67	43	# 1 V image size (”165 mm”)	A5	10100101
68	44	# 1 H image size : V image size (”294 : 165”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	1A	00011010
72	48	Detailed timing description # 2 Pixel clock (83.60 MHz”, According to VESA CVT Rev1.1)	A8	10101000
73	49	# 2 Pixel clock (hex LSB first)	20	00100000
74	4A	# 2 H active (“1600”)	40	01000000
75	4B	# 2 H blank (“160”)	A0	10100000
76	4C	# 2 H active : H blank (“1600 : 160”)	60	01100000
77	4D	# 2 V active (”900”)	84	10000100
78	4E	# 2 V blank (”50”)	32	00110010
79	4F	# 2 V active : V blank (”900 :50”)	30	00110000
80	50	# 2 H sync offset (”48”)	30	00110000
81	51	# 2 H sync pulse width ("32”)	20	00100000
82	52	# 2 V sync offset : V sync pulse width (”6 : 10”)	6A	01101010
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 6 : 10”)	00	00000000
84	54	# 2 H image size (”294 mm”)	26	00100110
85	55	# 2 V image size (”165 mm”)	A5	10100101

86	56	# 2 H image size : V image size (”294 : 165”)	10	00010000
87	57	# 2 H boarder (”0”)	00	00000000
88	58	# 2 V boarder (”0”)	00	00000000
89	59	# 2 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	1A	00011010
90	5A	Detailed timing description # 3 Pixel clock (66.88 MHz”, According to VESA CVT Rev1.1)	20	00100000
91	5B	# 3 Pixel clock (hex LSB first)	1A	00011010
92	5C	# 3 H active (“1600”)	40	01000000
93	5D	# 3 H blank (“160”)	A0	10100000
94	5E	# 3 H active : H blank (“1600 : 160”)	60	01100000
95	5F	# 3 V active (”900”)	84	10000100
96	60	# 3 V blank (”50”)	32	00110010
97	61	# 3 V active : V blank (”900 :50”)	30	00110000
98	62	# 3 H sync offset (”48”)	30	00110000
99	63	# 3 H sync pulse width ("32”)	20	00100000
100	64	# 3 V sync offset : V sync pulse width (”6 : 10”)	6A	01101010
101	65	# 3 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 6 : 10”)	00	00000000
102	66	# 3 H image size (”294 mm”)	26	00100110
103	67	# 3 V image size (”165 mm”)	A5	10100101
104	68	# 3 H image size : V image size (”294 : 165”)	10	00010000
105	69	# 3 H boarder (”0”)	00	00000000
106	6A	# 3 V boarder (”0”)	00	00000000
107	6B	# 3 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	1A	00011010
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name“N133FGE-L31”, ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 2 1st character of name (“N”)	4E	01001110
114	72	# 2 2nd character of name (“1”)	31	00110001
115	73	# 2 3rd character of name ("3”)	33	00110011
116	74	# 2 4th character of name (“3”)	33	00110011
117	75	# 2 5th character of name (“F”)	46	01000110
118	76	# 2 6th character of name (“G”)	47	01000111
119	77	# 2 7th character of name (“E”)	45	01000101
120	78	# 2 8th character of name (“-”)	2D	00101101
121	79	# 2 9th character of name (“L”)	4C	01001100
122	7A	# 2 Ath character of name (“3”)	33	00110011
123	7B	# 2 Bth character of name (“1”)	31	00110001
124	7C	# 2 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with “Blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	6C	01101100

Appendix. OUTLINE DRAWING





NOTES:
1.FLATNESS 0.5 mm MAX
2.'< >' MARKS THE REFERENCE DIMENSIONS.
3.LCD MODULE INPUT CONNECTOR: 20455-040E-12 (I-PEX) OR EQUIVALENT
4.IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAM OR OTHER FOREIGN OBJECTS OVER COF DRIVER IC, TCON AND VR LOCATION.