TFT LCD Preliminary Specification

MODEL NO.: N156B6-L3D

Customer : _____

Approved by : _____

Note :

核准時間	部門	審核	角色	投票
2010-05-20 17:24:11	NB 產品管理處	楊 2010.05.20 竣 傑	Director	Accept

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 0.0	Feb.3, 2010	All	All	Tentative spec 0.0 was first issued for N156B6-L3D
Ver. 1.0	Apr.29, 2010	All	All	Preliminary spec 1.0 was first issued for N156B6-L3D
Ver.1.1	May.11.2010	32	11.2	Carton label delete CMO logo

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N156B6-L3D is a 15.6” (15.547” diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 2Ch LVDS 40 pin interface. This module supports 1366 x 768 HD mode and can display 262,144 colors. The optimum viewing angle is at 6 o’clock direction.

1.2 FEATURES

- HD (1366 x 768 pixels) resolution
- 3.3V LVDS (Low Voltage Differential Signaling) interface
- WLED
- LED converter embedded
- 120Hz frame rate

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	344.232 (H) x 193.536 (V) (15.547” diagonal)	mm	(1)
Bezel Opening Area	348.43 (H) x 197.74 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.252 (H) x 0.252 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	358.8	359.3	359.8	mm	(1)
	Vertical(V)	209	209.5	210	mm	
	Thickness(T)	-	5.9	6.2	mm	
Weight		---	485	500	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

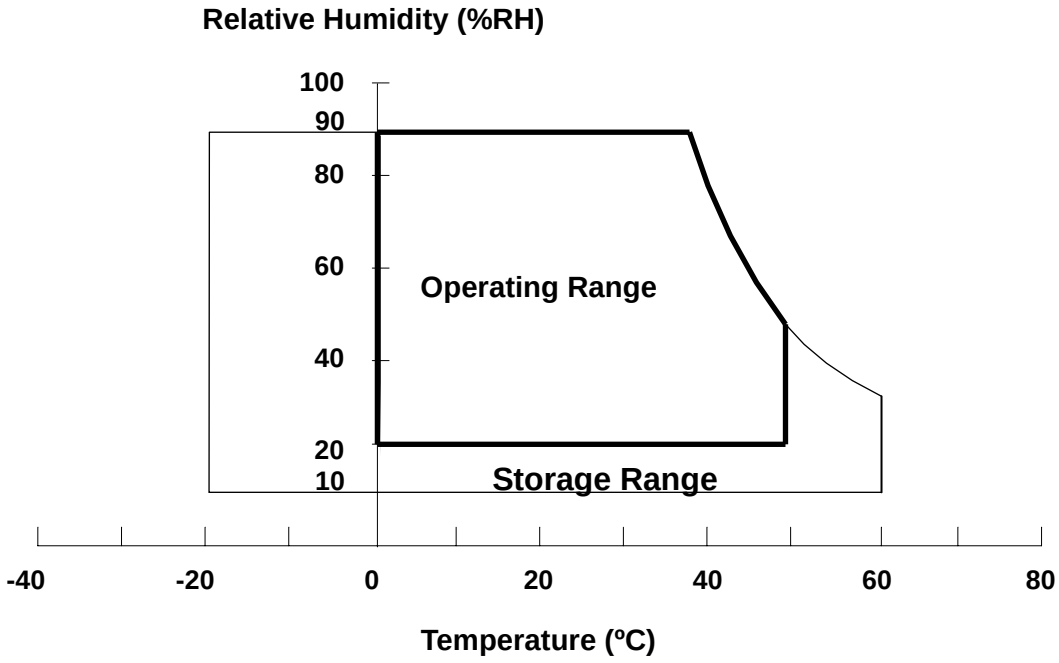
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 50 ºC max.

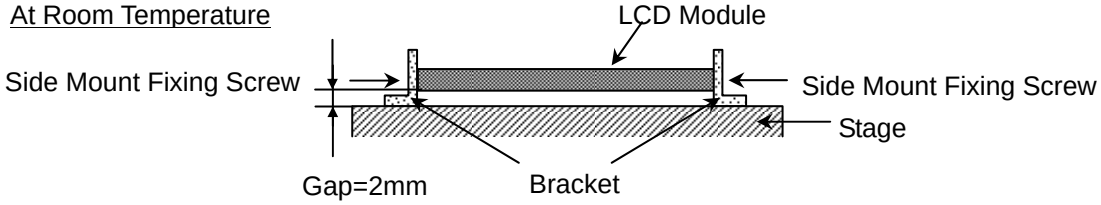


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10~500 Hz, 0.5hr/cycle 1cycle for X,Y,Z

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_I	-0.3	V_{CC}+0.3	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

2.2.2 BACKLIGHT UNIT

Item	Value		Unit	Note
	Min	Max.		
LED Light Bar Power Supply Voltage	-45	31.5	V_{DC}	(1), (2)
LED Light Bar Power Supply Current	0	180	mA_{DC}	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to Section 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

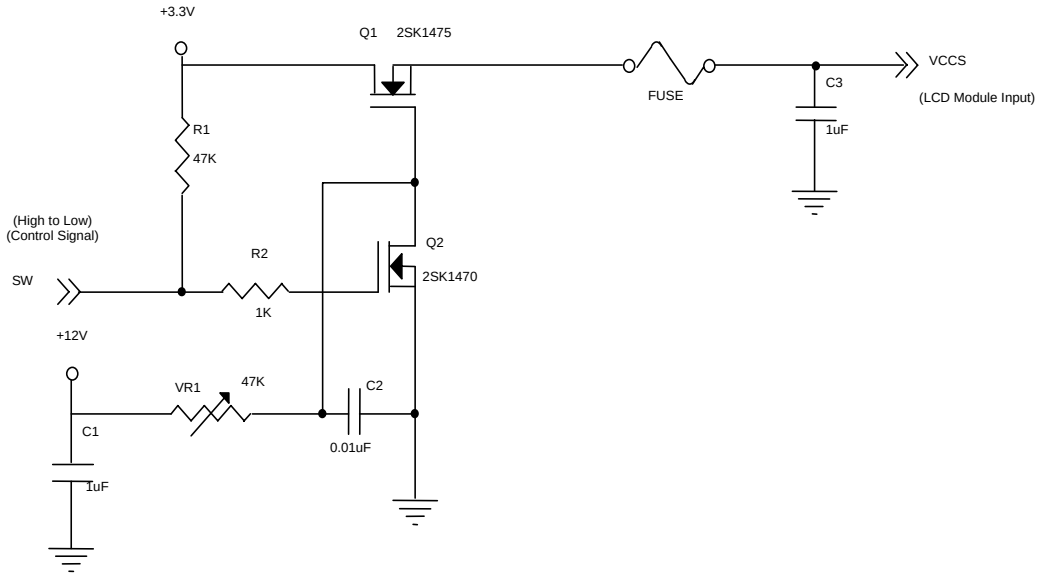
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.2	3.3	3.46	V	-
Ripple Voltage		V_{RP}	-	50	-	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.5	A	(2)
Power Supply Current	White	Icc	-	690	820	mA	60Hz,(3)a
	Black		-	770	950	mA	60Hz,(3)b
Power Supply Current	White	Icc		910	1100	mA	120Hz,(3)a
	Black			1150	1500	mA	120Hz,(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(4), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(4) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(4)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100	-	600	mV	(4)
LVDS Terminating Resistor		R_T	-	100	-	Ohm	-

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

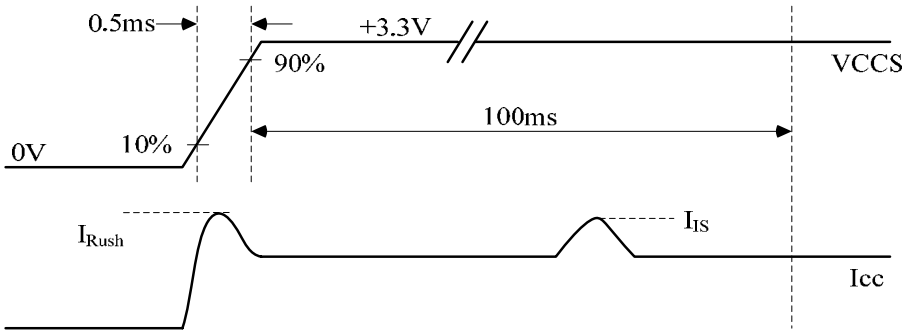
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

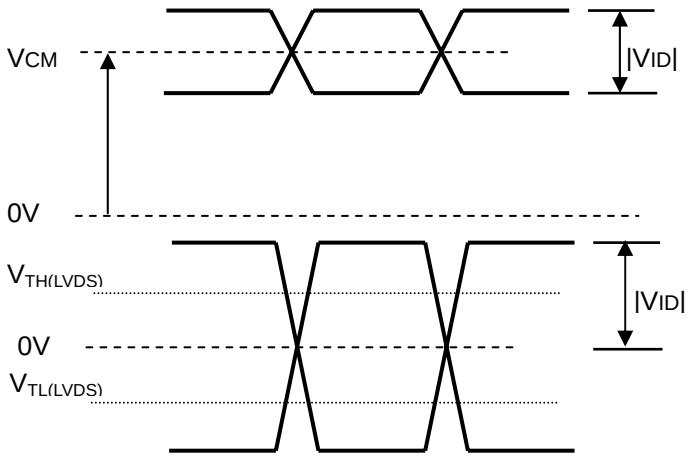
b. Black Pattern

Active Area

Note (4) The parameters of LVDS signals are defined as the following figures.

Single Ended

Differential

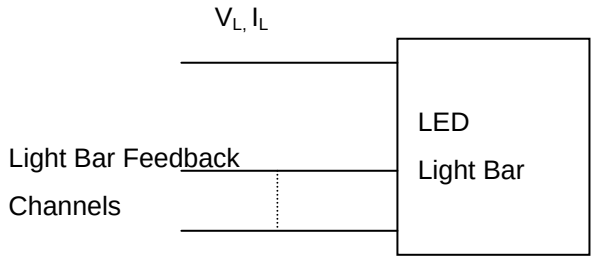


3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar input Voltage	V_L	25.2	28.8	31.5	V	(1) Duty 100%
LED Light Bar input Current	I_L	114	120	126	mA	
Power Consumption	P_L	2.872	3.456	3.969	W	(3) I_L= 120 mA Duty=100%
LED Life Time	L_{BL}	15000			Hrs	(4)

Note (1) LED light bar configuration is shown as below.



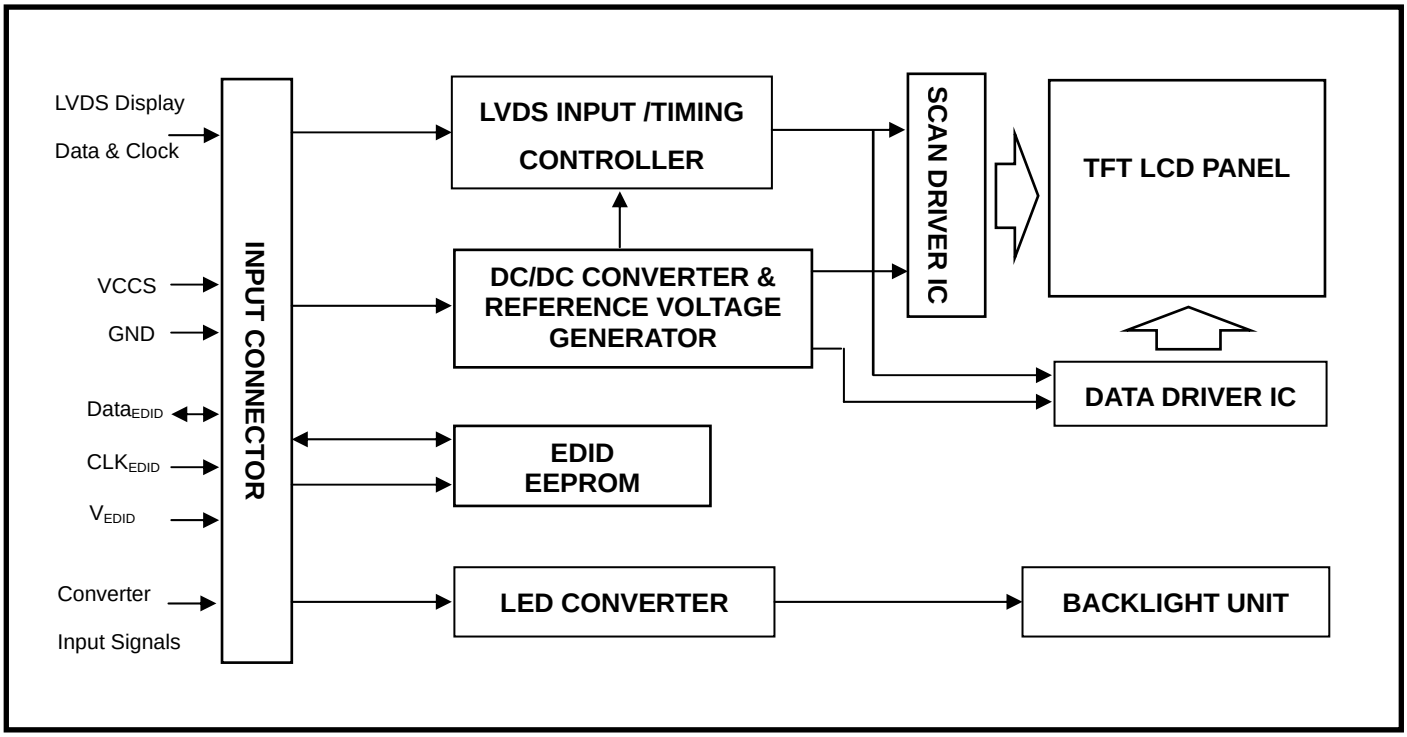
Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2°C and I_L = 20.0mA (Per EA) until the brightness becomes ≦ 50% of its original value.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

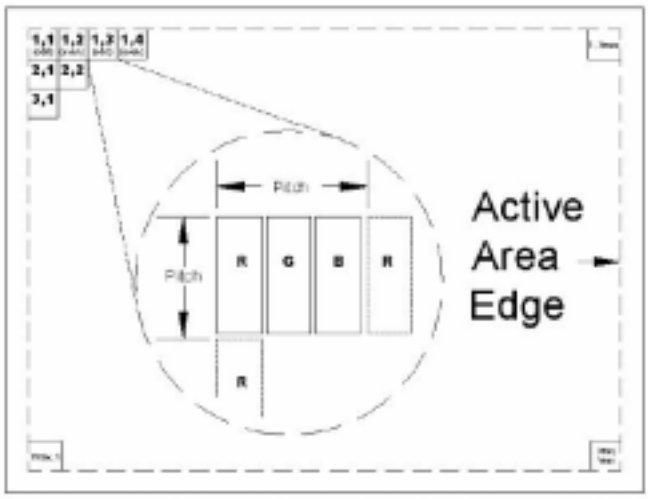
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vccs	Power Supply +3.3 V (typical)		
2	Vccs	Power Supply +3.3 V (typical)		
3	Vccs	Power Supply +3.3 V (typical)		
4	V_{EDID}	DDC 3.3V Power		
5	NC	Non-Connection (Reserved for CMO)		
6	CLK_{EDID}	DDC Clock		
7	$DATA_{EDID}$	DDC Data		
8	RXO0-	LVDS Differential Data Input (Odd)	Negative	R0-R5, G0
9	RXO0+	LVDS Differential Data Input (Odd)	Positive	
10	Vss	Ground		
11	RXO1-	LVDS Differential Data Input (Odd)	Negative	G1~G5, B0, B1
12	RXO1+	LVDS Differential Data Input (Odd)	Positive	
13	Vss	Ground		
14	RXO2-	LVDS Differential Data Input (Odd)	Negative	B2-B5,HS,VS, DE
15	RXO2+	LVDS Differential Data Input (Odd)	Positive	
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RxE0-	LVDS Differential Data Input (Even)	Negative	R0-R5, G0
21	RxE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground		
23	RxE1-	LVDS Differential Data Input (Even)	Negative	G1~G5, B0, B1
24	RxE1+	LVDS Differential Data Input (Even)	Positive	
25	Vss	Ground		
26	RxE2-	LVDS Differential Data Input (Even)	Negative	B2-B5,HS,VS, DE
27	RxE2+	LVDS Differential Data Input (Even)	Positive	
28	Vss	Ground		
29	RXEC-	LVDS Clock Data Input (Even)	Negative	
30	RXEC+	LVDS Clock Data Input (Even)	Positive	
31	LED_GND	LED Ground		
32	LED_GND	LED Ground		
33	LED_GND	LED Ground		
34	NC	Non-Connection (Reserved for CMO)		
35	LED_PWM	PWM Control Signal of LED Converter		
36	LED_EN	Enable Control Signal of LED Converter		
37	NC	Non-Connection (Reserved for CMO)		
38	LED_VCCS	LED Power		
39	LED_VCCS	LED Power		
40	LED_VCCS	LED Power		

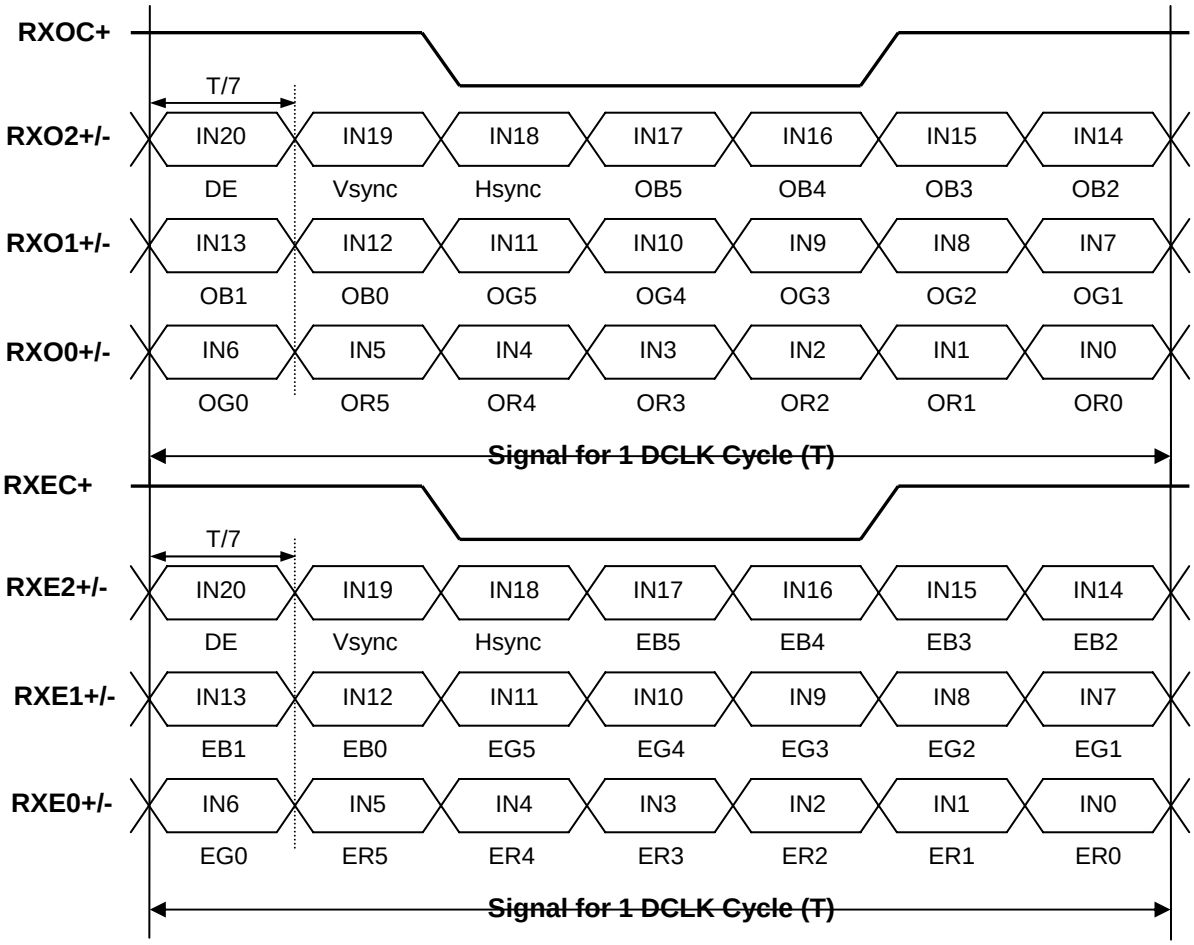
Note (1) Connector Part No.: IPEX-20455-040E-12、5-2069716-3 or equivalent

Note (2) User's connector Part No: IPEX-20453-040T-01 or equivalent

Note (3) The first pixel is odd as shown in the following figure.



5.2 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N156B6-L3D)	98	10011000
11	0B	ID product code (hex LSB first; N156B6-L3D)	15	00010101
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed “00H”)	09	00001001
17	11	Year of manufacture (fixed “00H”)	13	00010011
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Max H image size (“34.42cm”)	22	00100010
22	16	Max V image size (“19.35cm”)	13	00010011
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“Active off, RGB Color”)	0A	00001010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	D1	11010001
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	F5	11110101
27	1B	Red-x (Rx = “0.624”)	93	10010011
28	1C	Red-y (Ry = “0.342”)	5D	01011101
29	1D	Green-x (Gx = ”0.320”)	59	01011001
30	1E	Green-y (Gy = ”0.588”)	90	10010000
31	1F	Blue-x (Bx = ”0.162”)	26	00100110
32	20	Blue-y (By = ”0.088”)	1D	00011101
33	21	White-x (Wx = ”0.313”)	50	01010000
34	22	White-y (Wy = ”0.329”)	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001

41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“75.45MHz”, According to VESA CVT Rev1.1)	79	01111001
55	37	# 1 Pixel clock (hex LSB first)	1D	00011101
56	38	# 1 H active (“1366”)	56	01010110
57	39	# 1 H blank (“194”)	C2	11000010
58	3A	# 1 H active : H blank (“1366 :194”)	50	01010000
59	3B	# 1 V active (”768”)	00	00000000
60	3C	# 1 V blank (”38”)	26	00100110
61	3D	# 1 V active : V blank (”768 :38”)	30	00110000
62	3E	# 1 H sync offset (”31”)	1F	00011111
63	3F	# 1 H sync pulse width ("65”)	41	01000001
64	40	# 1 V sync offset : V sync pulse width (”4 : 12”)	4C	01001100
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”31: 65 : 4 : 12”)	00	00000000
66	42	# 1 H image size (”344 mm”)	58	01011000
67	43	# 1 V image size (”194 mm”)	C2	11000010
68	44	# 1 H image size : V image size (”344 : 194”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 1 Pixel clock (“125.74MHz”, According to VESA CVT Rev1.1)	1E	00011110
73	49	# 1 Pixel clock (hex LSB first)	31	00110001
74	4A	# 1 H active (“1366”)	56	01010110
75	4B	# 1 H blank (“194”)	C2	11000010
76	4C	# 1 H active : H blank (“1366 :194”)	50	01010000
77	4D	# 1 V active (”768”)	00	00000000
78	4E	# 1 V blank (”38”)	26	00100110
79	4F	# 1 V active : V blank (”768 :38”)	30	00110000
80	50	# 1 H sync offset (”31”)	1F	00011111
81	51	# 1 H sync pulse width ("65”)	41	01000001
82	52	# 1 V sync offset : V sync pulse width (”4 : 12”)	4C	01001100
83	53	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”31: 65 : 4 : 12”)	00	00000000
84	54	# 1 H image size (”344 mm”)	58	01011000

85	55	# 1 V image size (”194 mm”)	C2	11000010
86	56	# 1 H image size : V image size (”344 : 194”)	10	00010000
87	57	# 1 H boarder (”0”)	00	00000000
88	58	# 1 V boarder (”0”)	00	00000000
89	59	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
90	5A	Detailed timing description # 1 Pixel clock (“138.31MHz”, According to VESA CVT Rev1.1)	07	00000111
91	5B	# 1 Pixel clock (hex LSB first)	36	00110110
92	5C	# 1 H active (“1366”)	56	01010110
93	5D	# 1 H blank (“194”)	C2	11000010
94	5E	# 1 H active : H blank (“1366 :194”)	50	01010000
95	5F	# 1 V active (”768”)	00	00000000
96	60	# 1 V blank (”38”)	26	00100110
97	61	# 1 V active : V blank (”768 :38”)	30	00110000
98	62	# 1 H sync offset (”31”)	1F	00011111
99	63	# 1 H sync pulse width ("65”)	41	01000001
100	64	# 1 V sync offset : V sync pulse width (”4 : 12”)	4C	01001100
101	65	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”31: 65 : 4 : 12”)	00	00000000
102	66	# 1 H image size (”344 mm”)	58	01011000
103	67	# 1 V image size (”194 mm”)	C2	11000010
104	68	# 1 H image size : V image size (”344 : 194”)	10	00010000
105	69	# 1 H boarder (”0”)	00	00000000
106	6A	# 1 V boarder (”0”)	00	00000000
107	6B	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
108	6C	Detailed timing description # 1 Pixel clock (“150.89MHz”, According to VESA CVT Rev1.1)	F1	11110001
109	6D	# 1 Pixel clock (hex LSB first)	3A	00111010
110	6E	# 1 H active (“1366”)	56	01010110
111	6F	# 1 H blank (“194”)	C2	11000010
112	70	# 1 H active : H blank (“1366 :194”)	50	01010000
113	71	# 1 V active (”768”)	00	00000000
114	72	# 1 V blank (”38”)	26	00100110
115	73	# 1 V active : V blank (”768 :38”)	30	00110000
116	74	# 1 H sync offset (”31”)	1F	00011111
117	75	# 1 H sync pulse width ("65”)	41	01000001
118	76	# 1 V sync offset : V sync pulse width (”4 : 12”)	4C	01001100
119	77	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”31: 65 : 4 : 12”)	00	00000000
120	78	# 1 H image size (”344 mm”)	58	01011000
121	79	# 1 V image size (”194 mm”)	C2	11000010
122	7A	# 1 H image size : V image size (”344 : 194”)	10	00010000
123	7B	# 1 H boarder (”0”)	00	00000000
124	7C	# 1 V boarder (”0”)	00	00000000
125	7D	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
126	7E	Extension flag	00	00000000

127	7F	Checksum	B3	10110011

6. CONVERTER SPECIFICATION

6.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings
LED_VCCS	-0.3~28V
LED_PWM	-0.3V~5.5V
LED_EN	-0.3V~5.5V

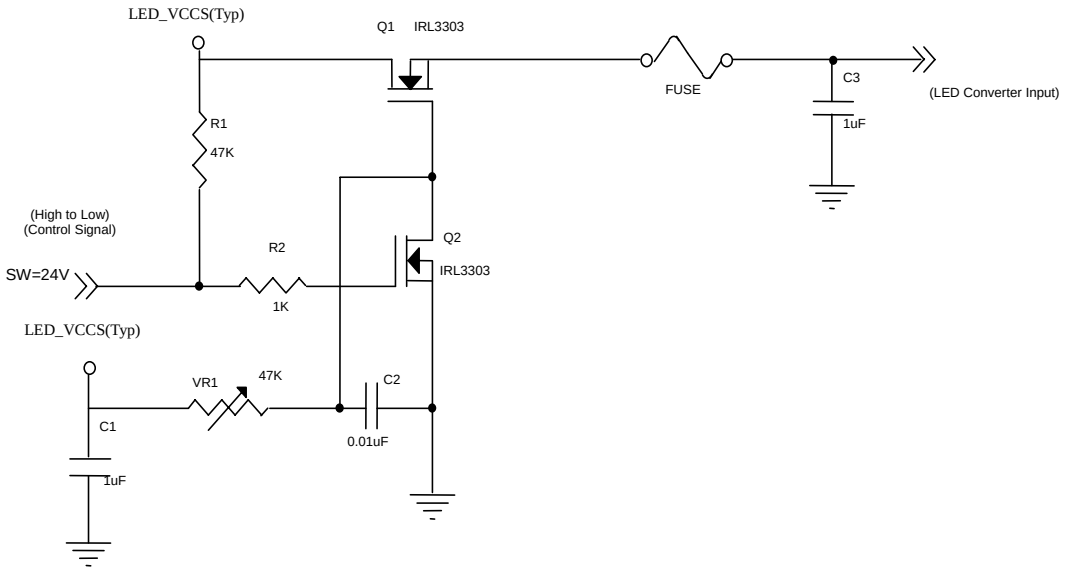
6.2 RECOMMENDED OPERATING RATINGS

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	6	12.0	21.0	V	-
Converter Rush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
Converter Initial Stage Current		$ILED_{IS}$	-	-	1.5	A	(1)
EN Control Level	Backlight On		2.3	-	5	V	-
	Backlight Off		0	-	0.5	V	-
PWM Control Level	PWM High Level		2.3	-	5	V	-
	PWM Low Level		0	-	0.5	V	-
PWM Control Duty Ratio			10	10	-	100	-
			5	5	-	100	(2)
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	-	100	-
PWM Control Frequency		f_{PWM}	190	210	2K	Hz	(3)
LED Power Current	LED_VCCS =Min.	ILED	532	678	827	mA	(4)
	LED_VCCS =Typ.		266	339	413	mA	(4)
	LED_VCCS =Max.		152	194	236	mA	(4)

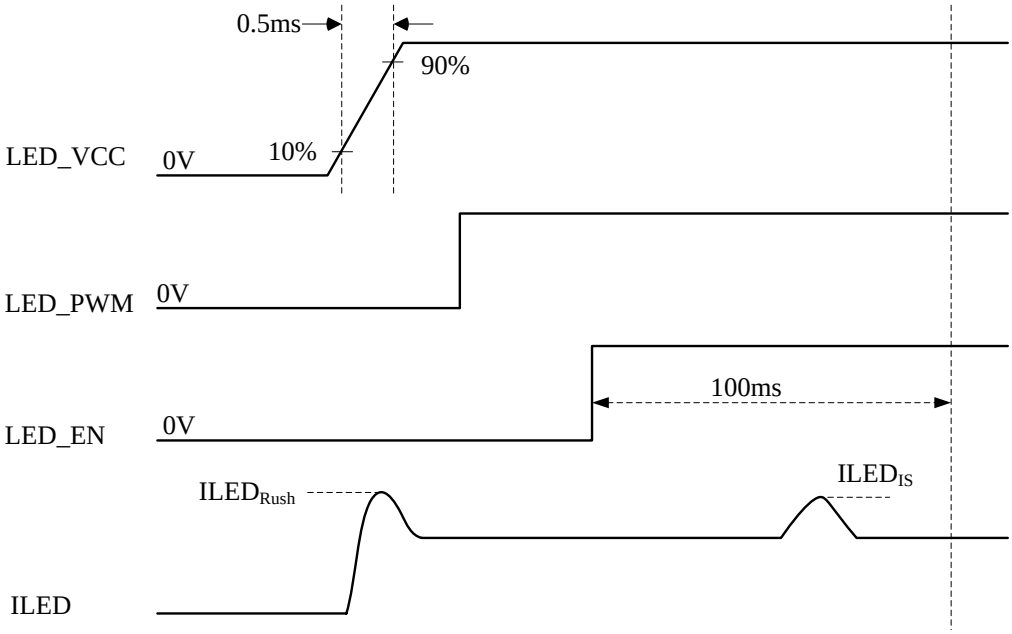
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it’s a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.4) * f \leq f_{PWM} \leq (N + 0.6) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (4) The specified LED power supply current is under the conditions at “LED_VCCS = Min., Typ., Max.”, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

7. INTERFACE TIMING

7.1 INPUT SIGNAL TIMING SPECIFICATIONS

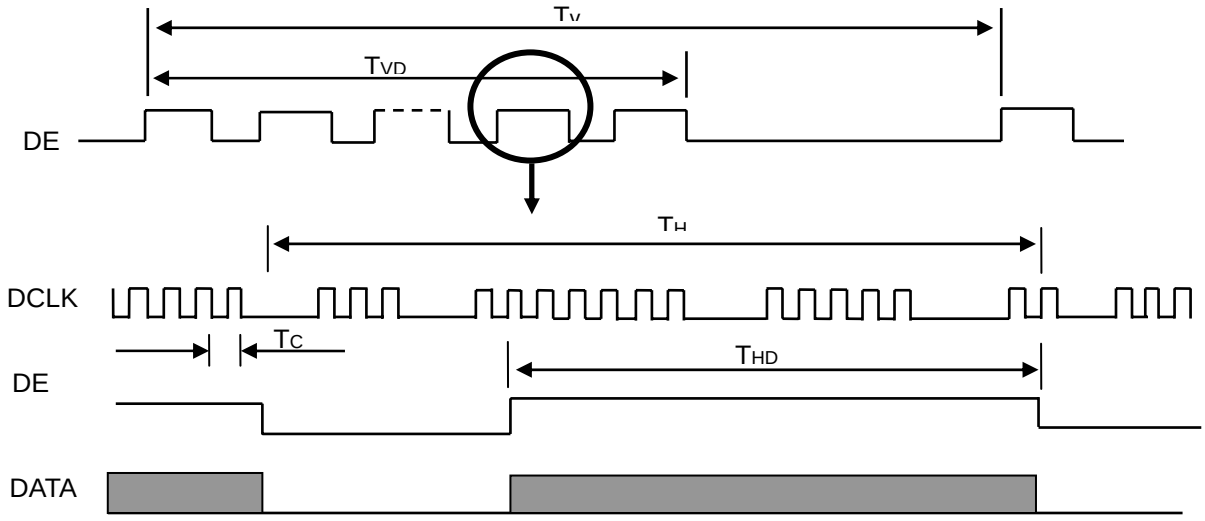
The input signal timing specifications are shown as the following table and timing diagram**.**

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	TBD	37.7	TBD	MHz	60Hz, (2)
		1/Tc	TBD	62.9	TBD	MHz	100Hz, (2)
		1/Tc	TBD	69.2	TBD	MHz	110Hz, (2)
		1/Tc	TBD	75.4	TBD	MHz	120Hz, (2)
DE	Vertical Total Time	TV	798	806	854	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	38	TV-TVD	TH	-
	Horizontal Total Time	TH	1512	1560	1608	Tc	(2)
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	194	TH-THD	Tc	(2)

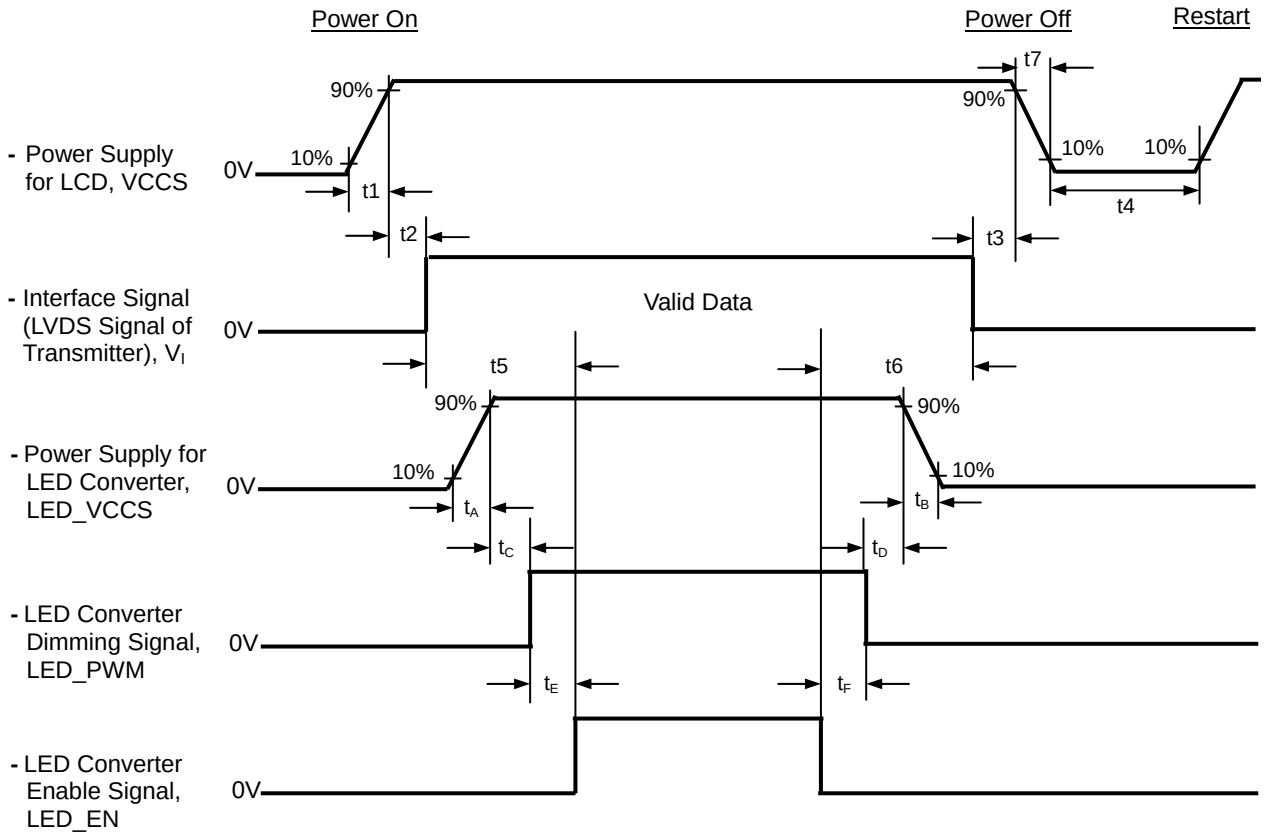
Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 2 channels LVDS input.

INPUT SIGNAL TIMING DIAGRAM



7.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$0.5 \leqq t1 \leqq 10$ ms

$0 \leqq t2 \leqq 50$ ms

$0 \leqq t3 \leqq 50$ ms

$t4 \geqq 500$ ms

$t5 \geqq 700$ ms

$t6 \geqq 200$ ms

$0.5 \leqq t7 \leqq 10$ ms

$0.5 \leqq t_A \leqq 10$ ms

$0 < t_B \leqq 10$ ms

$t_C \geqq 10$ ms

$t_D \geqq 10$ ms

$t_E \geqq 10$ ms

$t_F \geqq 10$ ms

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD VCCS to 0 V.

Note (3) The Backlight converter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight converter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Please follow the LED converter power sequence as above. If the customer could not follow, it might cause backlight flash issue during display ON/OFF or damage the LED backlight controller

8. OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

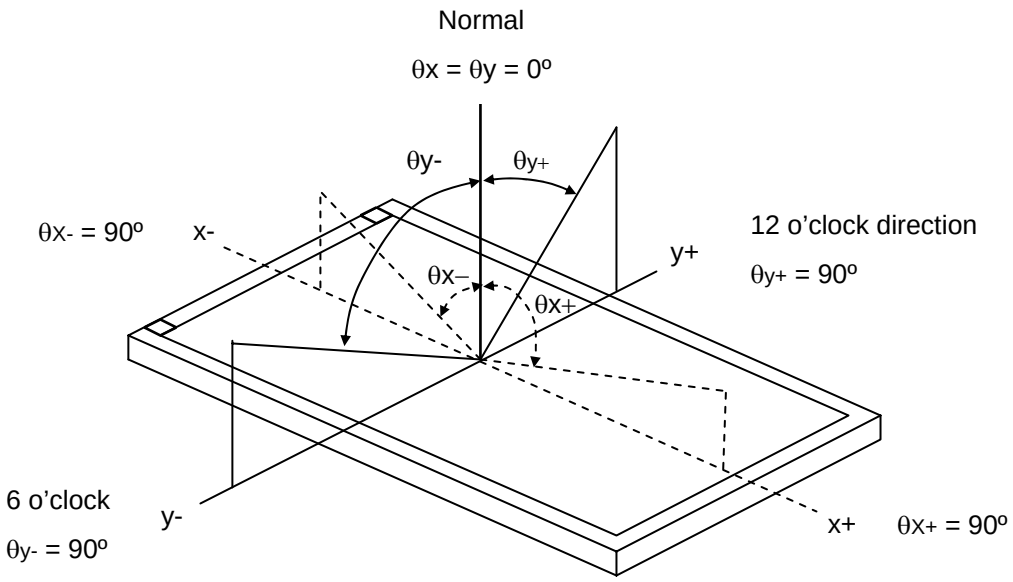
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	120	mA

The measurement methods of optical characteristics are shown in Section 8.2. The following items should be measured under the test conditions described in Section 8.1 and stable environment shown in Note (5).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	400	500	-	-	(2), (5),(7)
Response Time		T_R		-	2	4	ms	(3),(7)
		T_F		-	4	8	ms	
Average Luminance of White		L_{AVE}		185	220	-	cd/m^2	(4), (6),(7)
Color Chromaticity	Red	Rx		Typ –0.03	0.624	Typ +0.03	-	(1),(7)
		Ry			0.342		-	
	Green	Gx			0.320		-	
		Gy			0.588		-	
	Blue	Bx			0.162		-	
		By			0.088		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	35	40		Deg.	(1),(5) (7)
		θ_x-		35	40	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		35	40	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80	-	-	%	(5),(6) (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

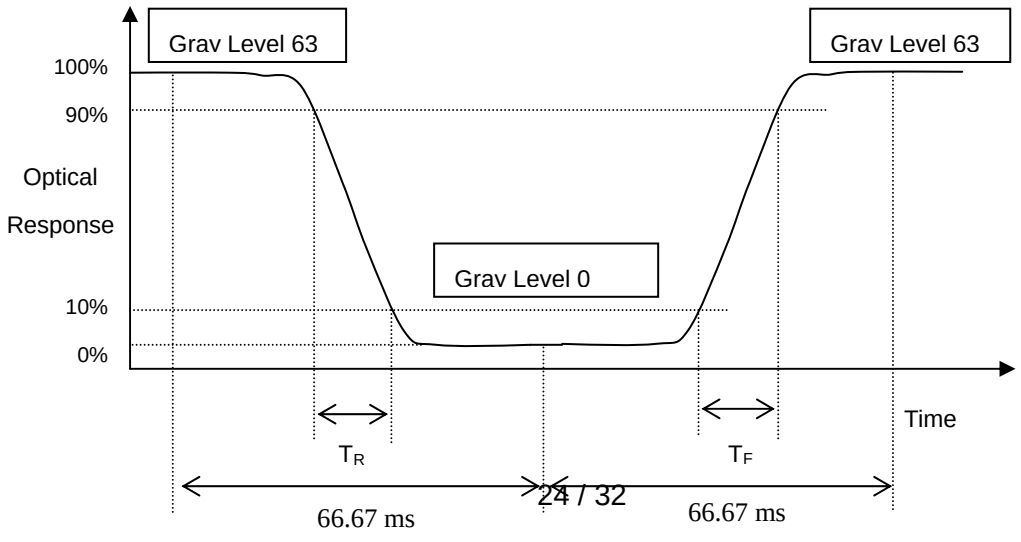
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

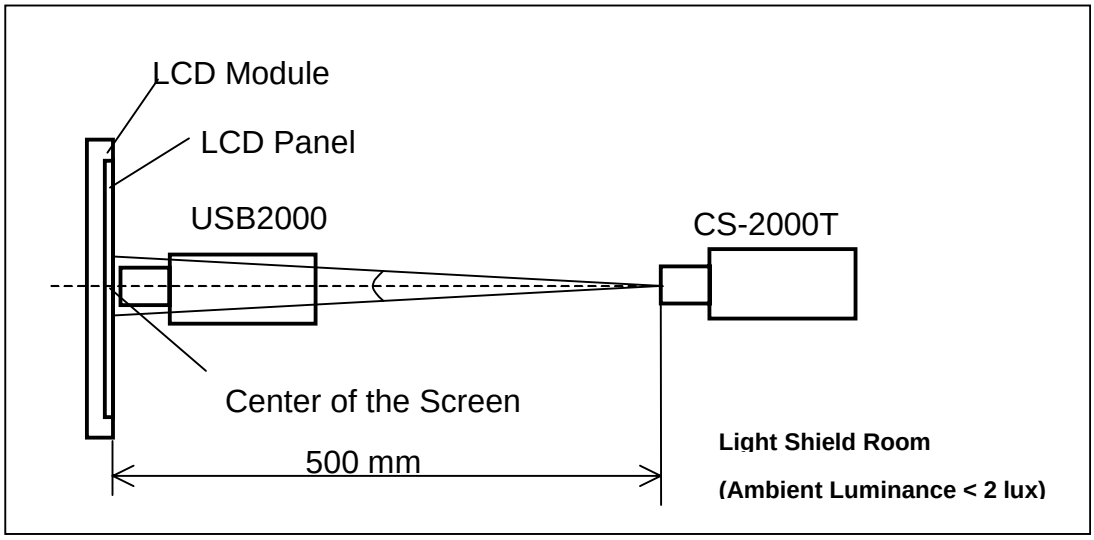
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

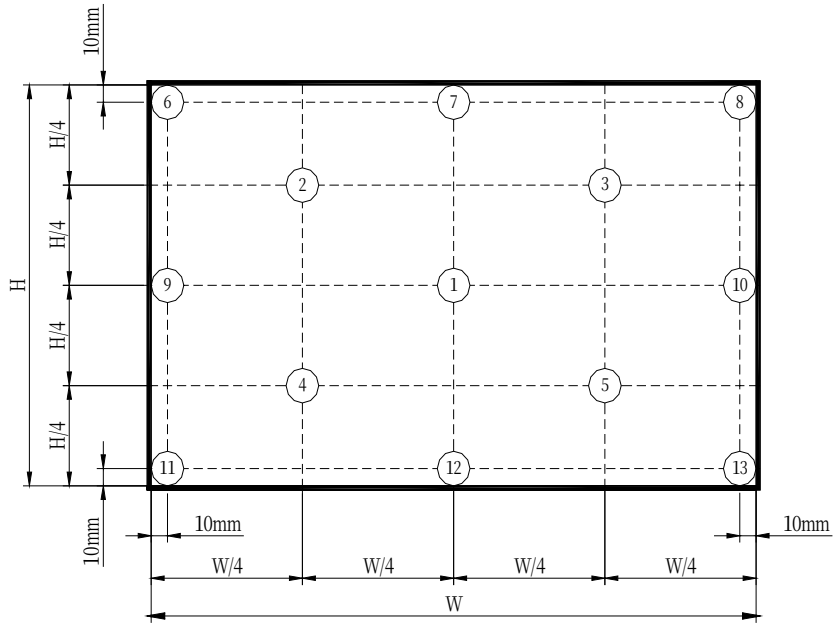
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Minimum [L (1), L (2), L (3), L (4), L (5)] / Maximum [L (1), L (2), L (3), L (4), L (5)]}*100%



Ⓧ : Test Point

X=1 to 13

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

9. PRECAUTIONS

9.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

10. PACKING

10.1 CARTON

(1) Box Dimensions : 489(L)*382(W)*320(H)
(2) 20 modules/Carton

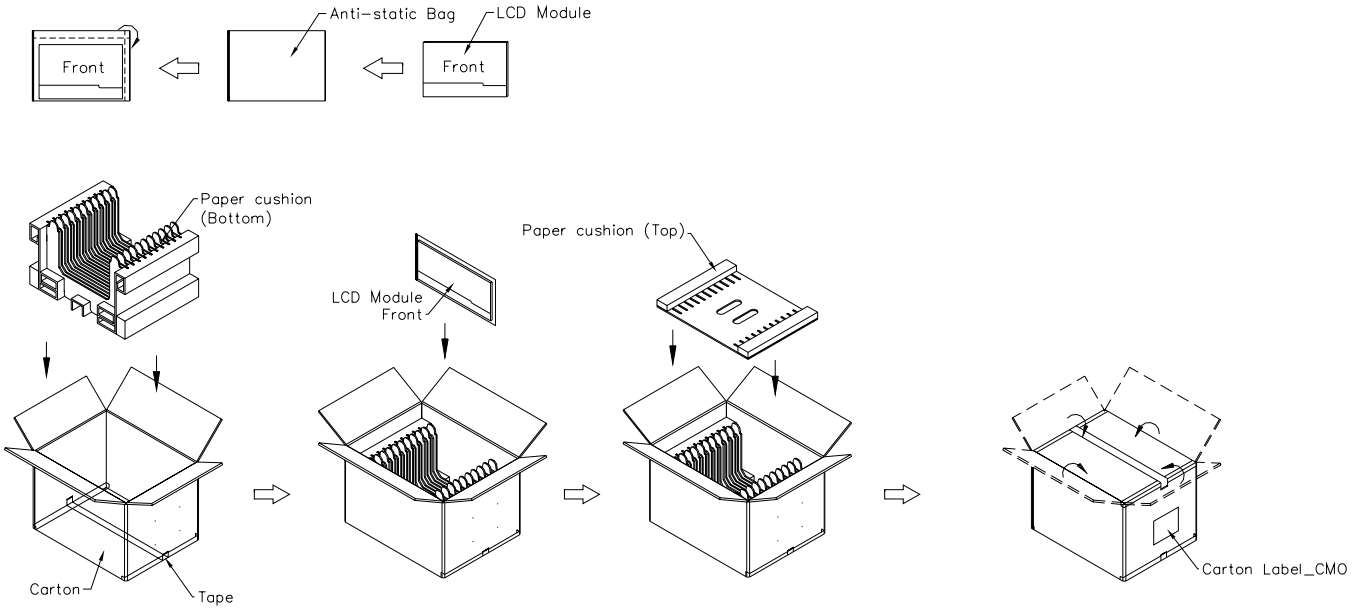


Figure. 10-1 Packing method

10.2 PALLET

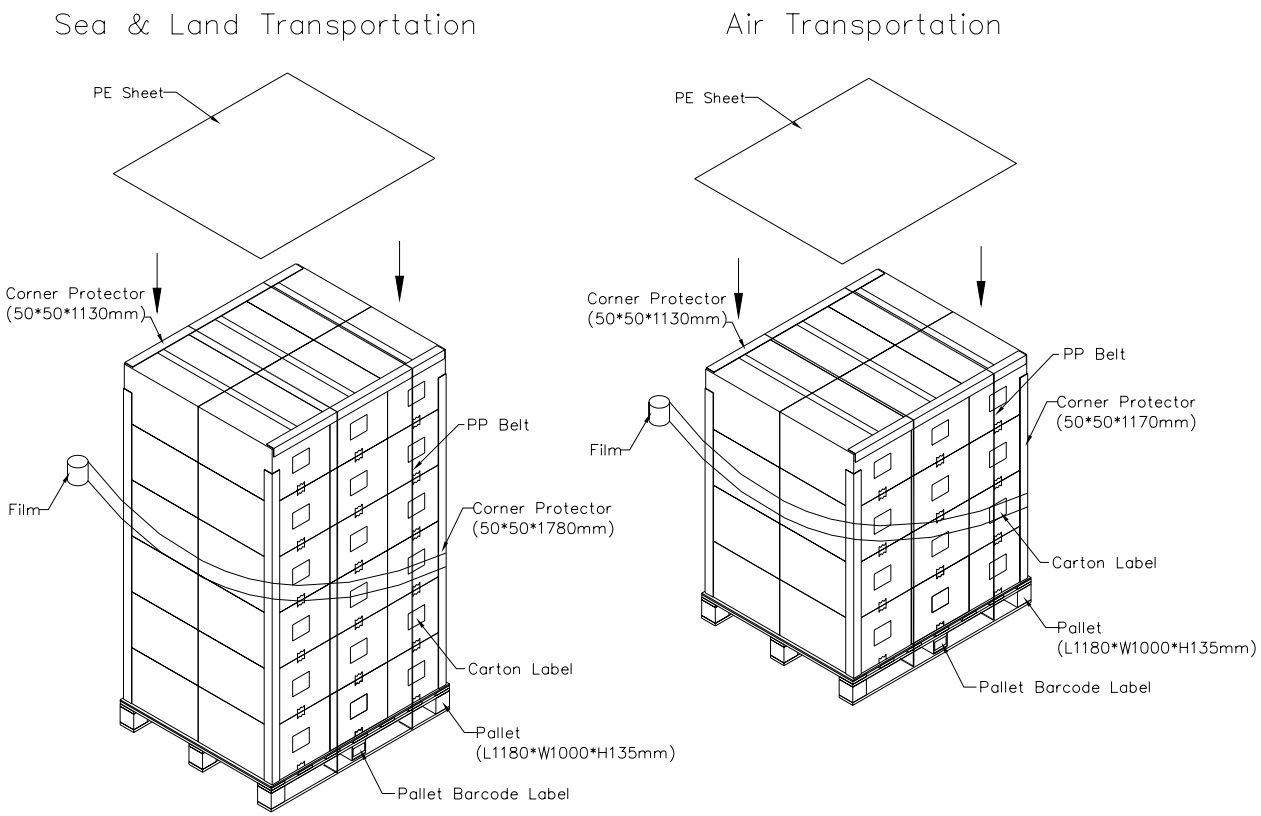


Figure. 10-2 Packing method

11. DEFINITION OF LABELS

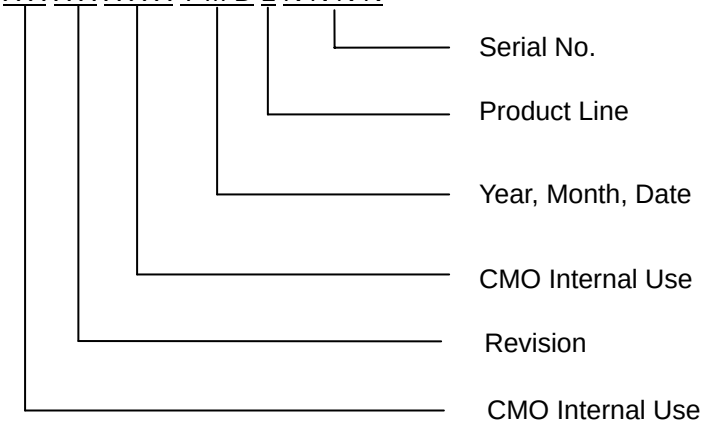
11.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N156B6 - L3D

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL logo: “AAAA” especially stands for panel manufactured by CMO China satisfying UL requirement. “LEOO” and “COCKN” is the CMO’s UL factory code for Ningbo factory..

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

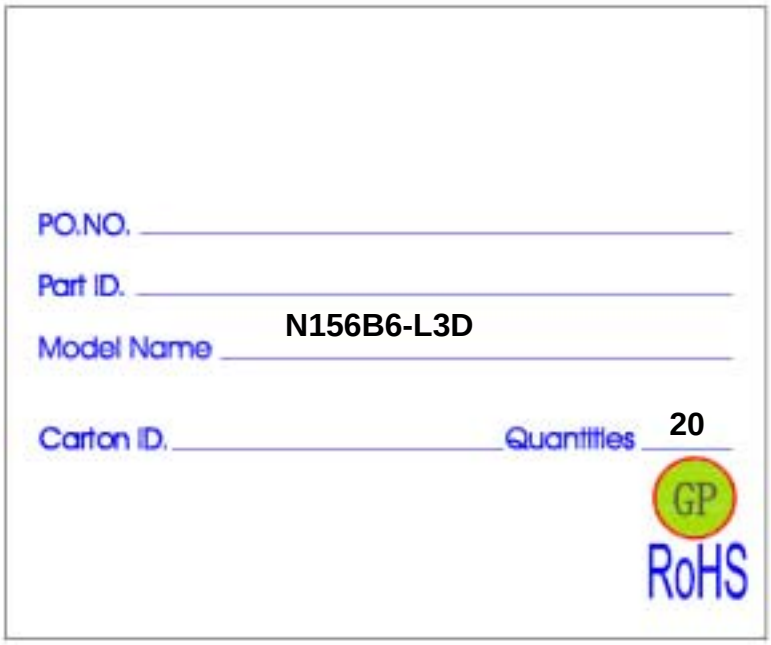
Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

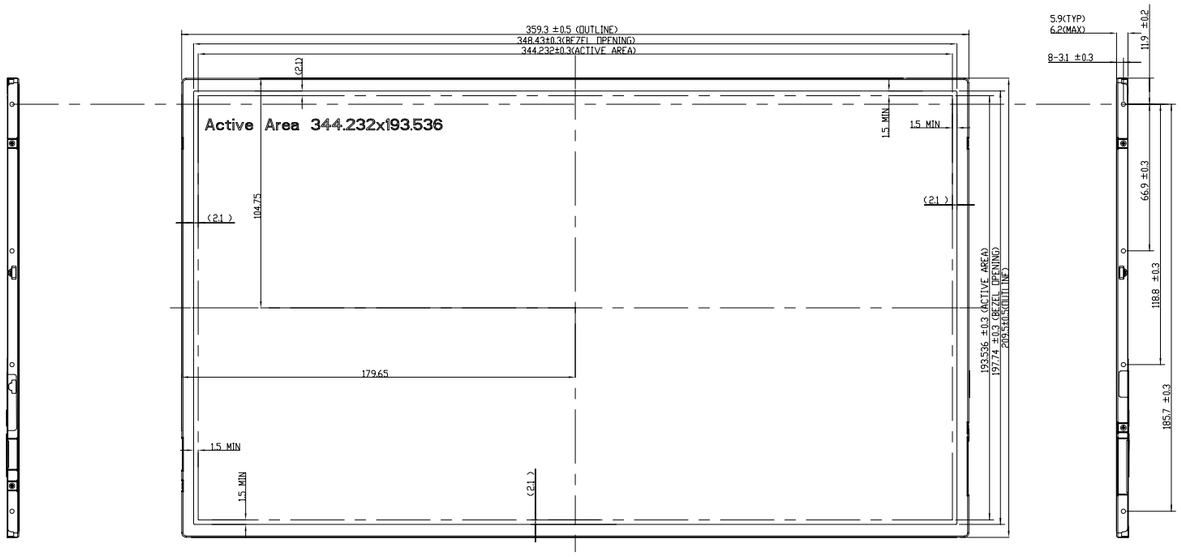
(b) Revision Code: cover all the change

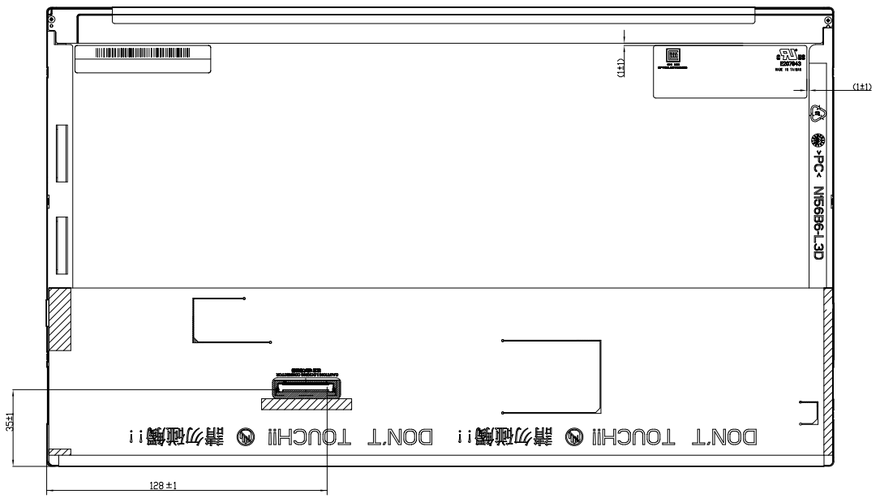
(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

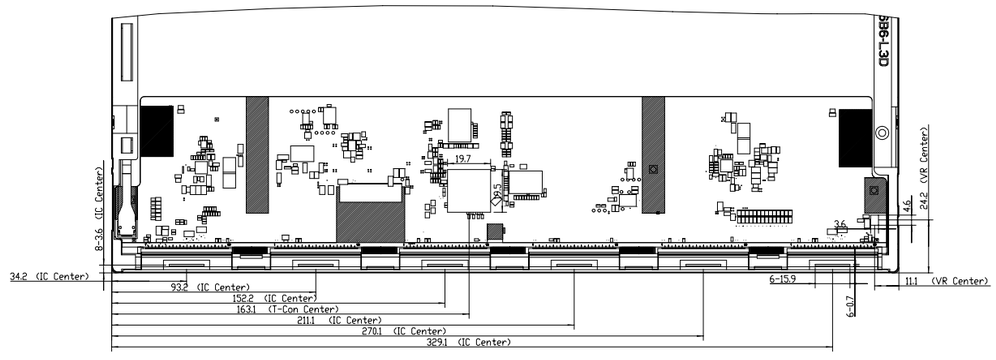
11.2 CARTON LABEL







NOTES:
1. MAX. SCREW DEPTH: 2.6 mm.
2. MAX. SCREW TORQUE: 2 kgf-cm.
3. LCD MODULE INPUT CONNECTOR : IPEX-20455-040E-12 , S-2069716-3 OR EQUIVALENT
4. GAP BETWEEN BEZEL AND PANEL: 0.5mm MAX.
5. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAM OR OTHER FOREIGN OBJECTS OVER TCON AND VR LOCATION.
6. MODULE FLATNESS 0.5mm MAX.
7. '( )' MARKS THE REFERENCE DIMENSIONS.



Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	Outline_Drawing_N156B6-L3D					2D REV.	I.0
						3D REV.	I.0
Approved	Shunnan	Drawing No.	N156A41021				
Checked	Poshen	Part No.	NA				
Drawer	Andy Lee	Material	NA			Sheet	1 / 1 A0
Designer	Andy Lee	Date	12-Feb-2010	Scale	1:1	Unitmm	

CHI MEI OPTOELECTRONICS CORP.