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NE156QUM-N63 V5.0

Preliminary Product Specification

Rev. P0

HEFEI XINSHENG OPTOELECTRONICS TECHNOLOGY CO.,LTD

REVISION HISTORY

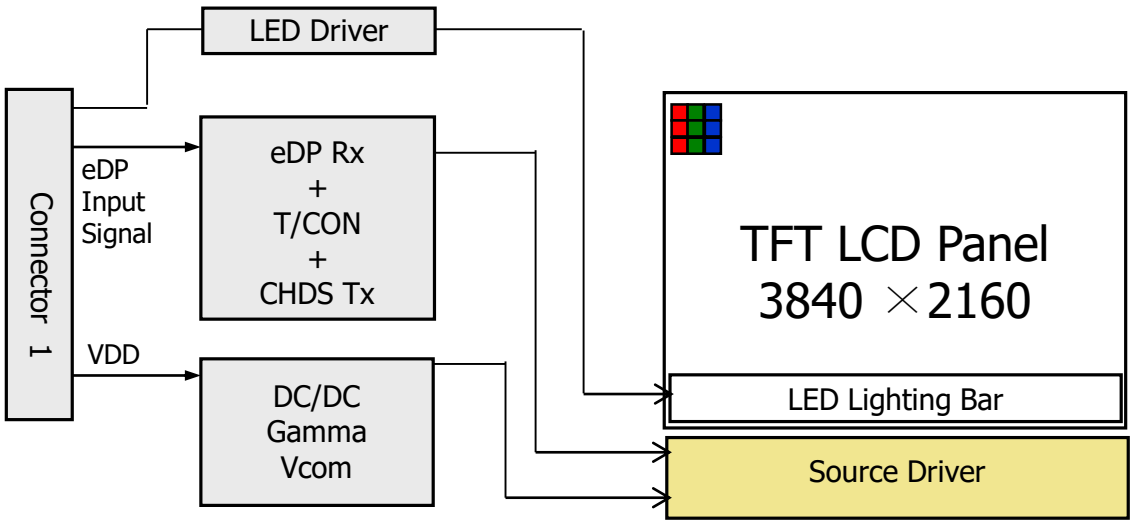
REV.	ECN No.	DESCRIPTION OF CHANGES	DATE	PREPARED
P0	-	Initial Release	2018.05.24	马睿

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NE156QUM-N63 V5.0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.6 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical Stripe and this module can display 16,777,216 colors. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED Driver for back-light driving is built in this model.
All input signals are eDP 1.4a interface compatible.



1.2 Features

- 4 lane eDP Interface with 5.4Gbps Link Rates
- Thin and light weight
- 8-bit color depth, display 16.7M colors
- Single LED Lighting Bar. (Down side/Horizontal Direction)
- Green Product (RoHS & Halogen free product)
- On board LED Driving circuit
- Low driving voltage and low power consumption
- On board EDID chip

1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NE156QUM-N63. (listed in Table 1.)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.2176 (H) ×193.6224 (V)	mm	
Number of pixels	3840 (H) ×2160 (V)	pixels	
Pixel pitch	0.08964(H) X 0.08964 (V)	mm	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M	colors	
Display mode	Normally Black		
Dimensional outline	350.66±0.3(H)*216.45±0.5(V) (W/PCB)*2.6(Max)	mm	
Weight	320 (max)	g	
Surface treatment	AG		
Back-light	Lower Down side, 1-LED Lighting Bar type		Note 1
Power consumption	P_D : 1.4 (max.)	W	@ mosaic
	P_{BL} :4.05(max)	W	
	P_{total} :5.45 （max）	W	@ mosaic

Notes : 1. LED Lighting Bar (60*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

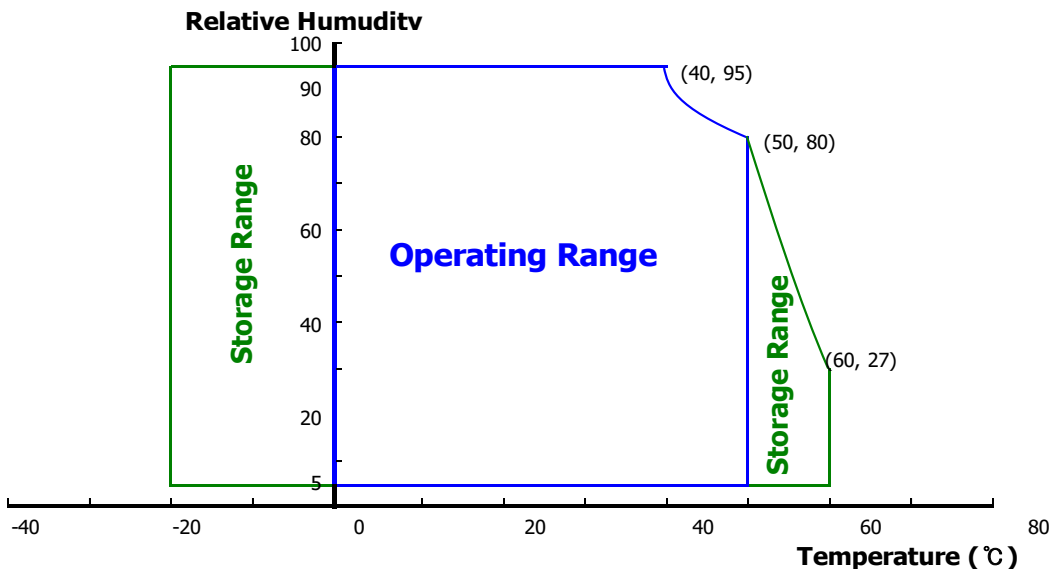
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings> Ta=25+/-2˚C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
Logic Supply Voltage	V_{IN}	V_{ss}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	℃	Note 2
Storage Temperature	T_{ST}	-20	+60	℃	

Notes : 1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 ^{O}C ≥ Ta)
Maximum wet - bulb temperature at 39 ^{O}C or less. (Ta > 40 ^{O}C) No condensation.



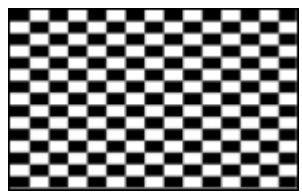
3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical specifications > Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V_{RF}	-	90	100	mV	At V_{DD} = 3.3V
Power Supply Current	I_{DD}	-	409	-	mA	Note 1
Differential Input Voltage	V_{ID}	200	400	600	mV	
Power Consumption	P_D	-	1.35	1.4	W	Note 1
	P_{BL}	-	3.95	4.05	W	Note 2
	P_{total}	-	5.3	5.45	W	Note 1

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for 3.3V at 25℃ @mosaic.



2. Calculated value for reference ($V_{LED} \times I_{LED}$)

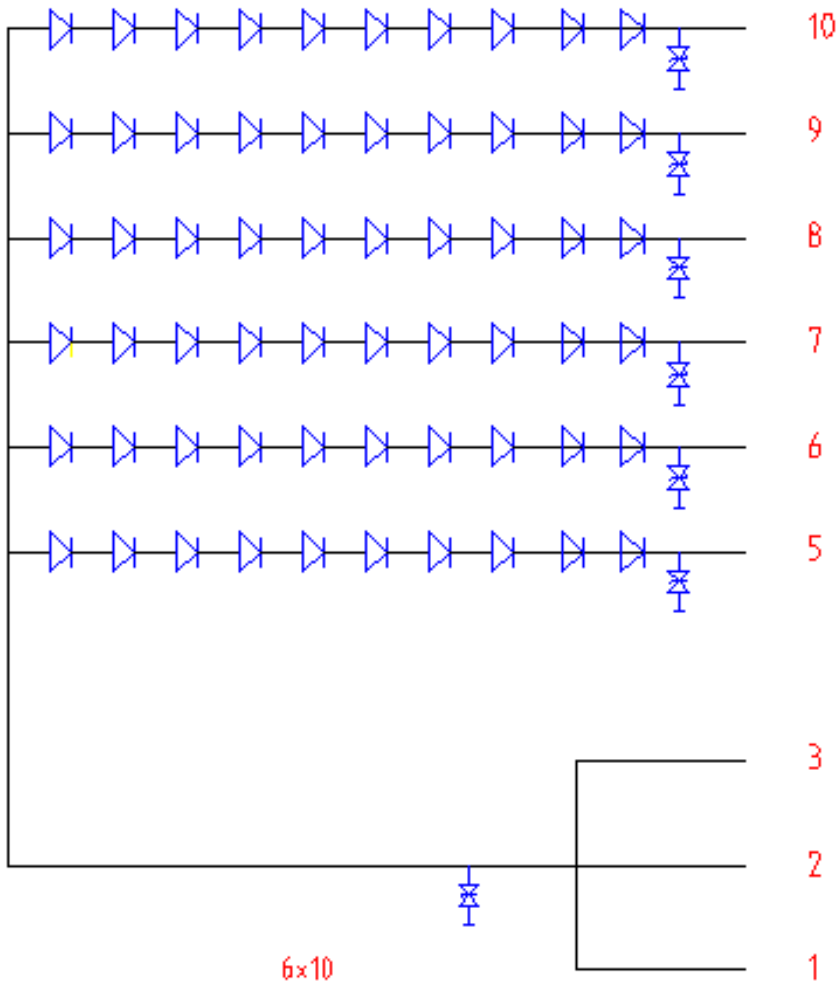
3.2 Backlight Unit

< Table 4. LED Driving guideline specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	2.9	V	-
LED Forward Current		I_F	-	20.3	-	mA	-
LED Power Consumption		P_{LED}		-	3.53	W	Note 1
LED Life-Time		N/A	15,000	-	-	Hour	I_F = 19mA
Power supply voltage for LED Driver		V_{LED}	5	12	21	V	
EN Control Level	Backlight on		2.5		5.0	V	
	Backlight off		0		1.0	V	
PWM Control Level	PWM High Level		2.5		5.0	V	
	PWM Low Level		0		0.1	V	
PWM Control Frequency		F_{PWM}	200	-	2,000	Hz	
Duty Ratio		-	1	-	100	%	Note3

Notes : 1. Power supply voltage12V for LED Driver
Calculator Value for reference $I_F \times V_F \times 60 / \text{efficiency} = P_{LED}$
2. The LED Life-time define as the estimated time to 50% degradation of initial luminous.
3. 1% duty cycle is achievable with a dimming frequency less than 1KHz.

3.3 LED structure



4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	85	-	Deg.	Note 1
		Θ_9		-	85	-	Deg.	
	Vertical	Θ_{12}		-	85	-	Deg.	
		Θ_6		-	85	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	700	1000			Note 2
Luminance of White	5 Points	Y_w	Θ = 0° I_{LED} = 19mA	289	340	-	cd/m^2	Note 3
White Luminance uniformity	5 Points	ΔY5		80%	-	-		Note 4
	13 Points	ΔY13		63%	70%	-		
White Chromaticity		x_w	Θ = 0°	0.283	0.313	0.343		Note 5
		y_w		0.299	0.329	0.359		
Reproduction of color	Red	x_R	Θ = 0°	-0.03	0.644	+0.03		
		y_R			0.336			
	Green	x_G			0.300			
		y_G			0.612			
	Blue	x_B			0.151			
		y_B			0.069			
Gamut					72		%	
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	25	30	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state .
(see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.
(see FIGURE 2 and FIGURE 3).

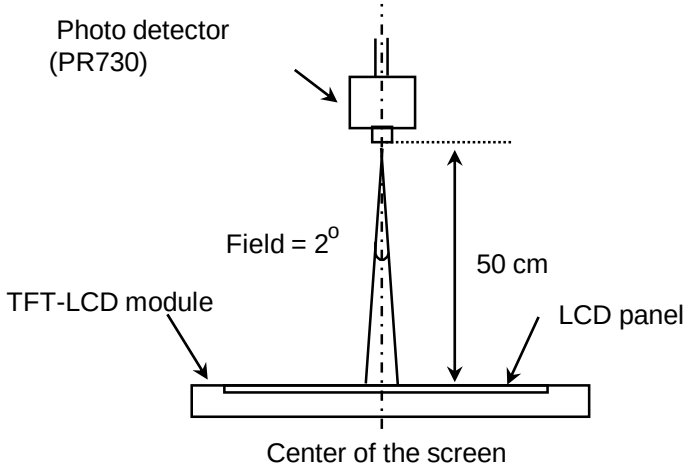
5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as FIGURE 4 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.
(See FIGURE 5).

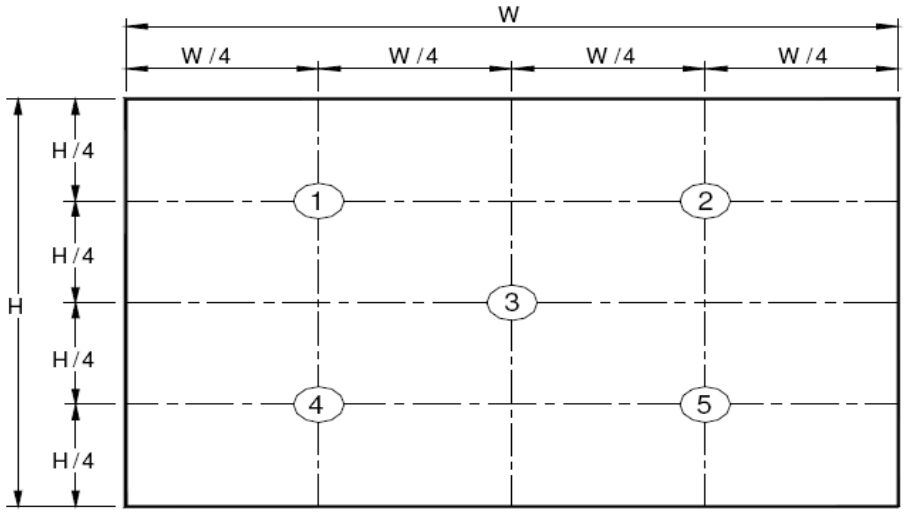
4.3 Optical measurements

Figure 1. Measurement Set Up



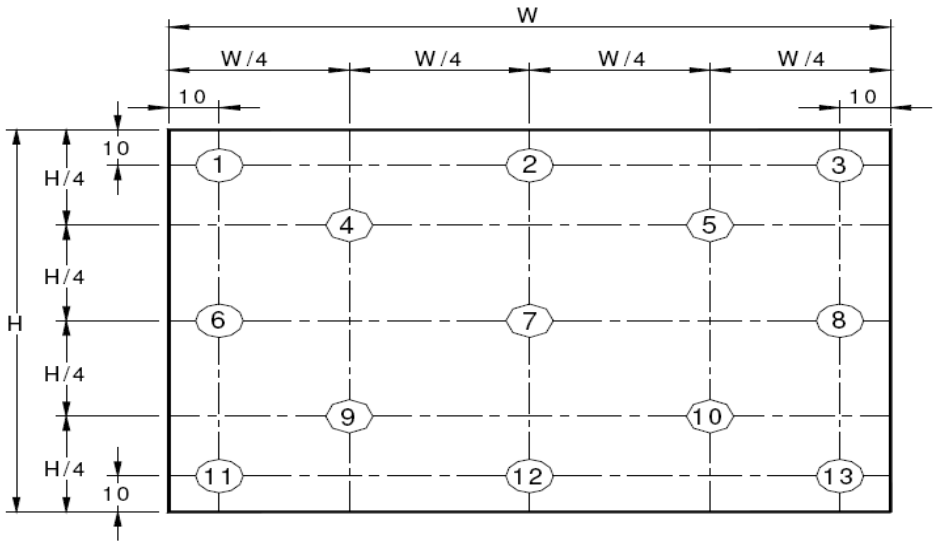
Optical characteristics measurement setup

Figure 2. White Luminance and Uniformity Measurement Locations (5 points)



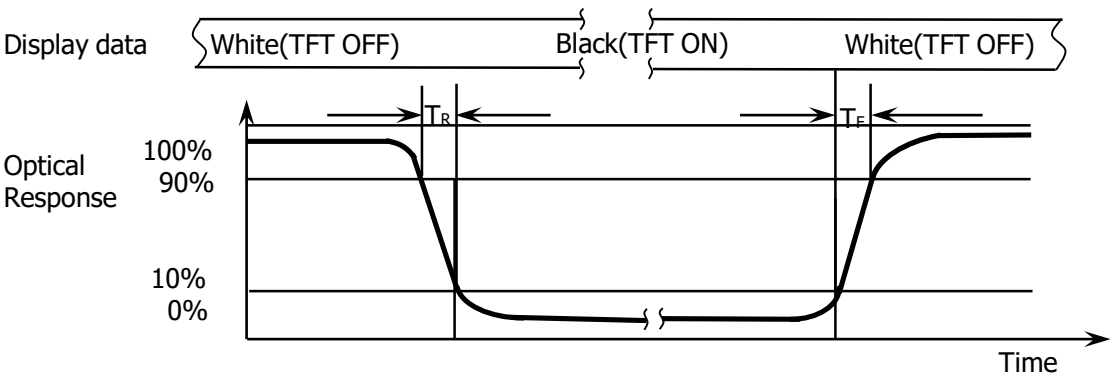
Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

Figure 3. Uniformity Measurement Locations (13 points)



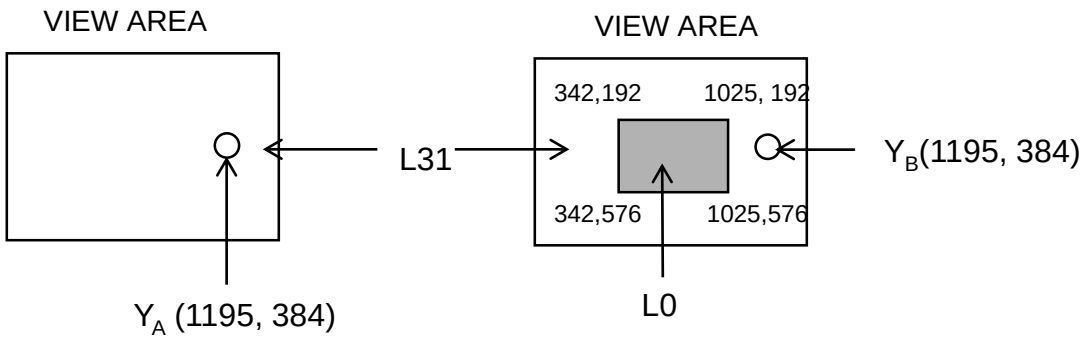
The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see FIGURE 2) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see FIGURE 3).(W&H is AA area side).

Figure 4. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 4 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Td and 90% to 10% is Tr.

Figure 5. Cross Modulation Test Description



$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns

Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark (Refer to FIGURE 5).

5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

The electronics interface connector is IPEX-20455-040E-66.

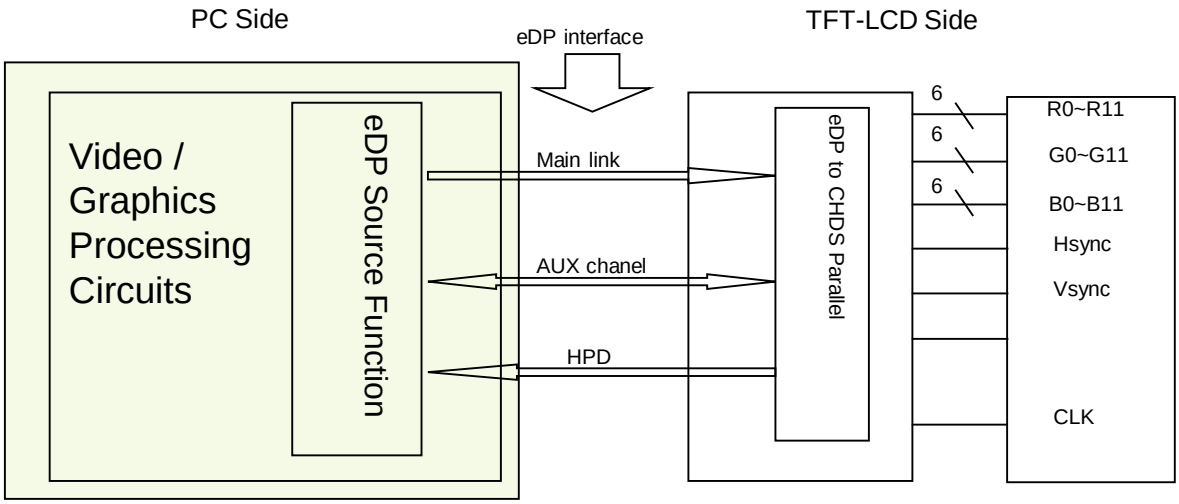
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Pin No.	Symbol	Description	I/O
1	NC(G_SYNC)	Reserved for LCD manufacturer’ s use	P
2	H_GND	High Speed Ground	-
3	Lane3_N	eDP RX channel 3 negative	O
4	Lane3_P	eDP RX channel 3 positive	O
5	H_GND	High Speed Ground	-
6	Lane2_N	eDP RX channel 2 negative	O
7	Lane2_P	eDP RX channel 2 positive	O
8	H_GND	High Speed Ground	-
9	Lane1_1N	eDP RX channel 1 negative	O
10	Lane1_1P	eDP RX channel 1 positive	O
11	H_GND	High Speed Ground	-
12	Lane1_0N	eDP RX channel 0 negative	O
13	Lane1_0P	eDP RX channel 0 positive	O
14	H_GND	High Speed Ground	-
15	AUX_CH_P	True Signal Auxiliary Channel	I/O
16	AUX_CH_N	Complement Signal Auxiliary Channel	I/O
17	H_GND	High Speed Ground	-
18	LCD_VCC	3.3VDC	P
19	LCD_VCC	3.3VDC	P
20	LCD_VCC	3.3VDC	P
21	LCD_VCC	3.3VDC	P
22	BIST	VDC LCD Panel Self Test Enable（max2.5VDC)	-
23	LCD_GND	LCD logic and driver ground	-
24	LCD_GND	LCD logic and driver ground	-
25	LCD_GND	LCD logic and driver ground	-

Pin No.	Symbol	Description	I/O
26	LCD_GND	LCD logic and driver ground	-
27	HPD	HPD signal pin	I/O
28	BL_GND	Backlight ground	-
29	BL_GND	Backlight ground	-
30	BL_GND	Backlight ground	-
31	BL_GND	Backlight ground	-
32	BL_ENABLE	3.3VDC from system	I/O
33	BL_PWM	PWM Input	I/O
34	NC(H_SYNC)	Reserved for LCD manufacturer’s use	I/O
35	NC(DBC)	Reserved for LCD manufacturer’s use	I/O
36	BL_PWR	12VDC	P
37	BL_PWR	12VDC	P
38	BL_PWR	12VDC	P
39	BL_PWR	12VDC	P
40	NC(COLOUR ENIN)	Reserved for LCD manufacturer’s use	I/O

5-2. eDP Interface



Note. Transmitter : CRX1200A.
Transmitter is not contained in Module.

5.3.eDP Input signal

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

5.4 Back-light & LCM Interface Connection

Interface Connector: **MSK24022P10**

<Table 7. Pin Assignments for the BLU & LCM Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	LED2	LED cathode connection
2	Vout	LED anode connection	7	LED3	LED cathode connection
3	Vout	LED anode connection	8	LED4	LED cathode connection
4	NC	No Connection	9	LED5	LED cathode connection
5	LED1	LED cathode connection	10	LED6	LED cathode connection

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NE156QUM-N63 V5.0 is operated by the DE only.

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	355.52	533.25	586.6	MHz
	High Time	Tch	-	*4/7*	-	Tc
	Low Time	Tcl	-	*3/7*	-	Tc
Frame Period		Tv	*3900*	*4000*	*4050*	lines
			-	*60*	-	Hz
			25	*16.7*	*15.15*	ms
Vertical Display Period		Tvd	-	*2160*	-	lines
One line Scanning Period		Th	*2180*	*2222*	*2240*	clocks
Horizontal Display Period		Thd	-	*3840*	-	clocks

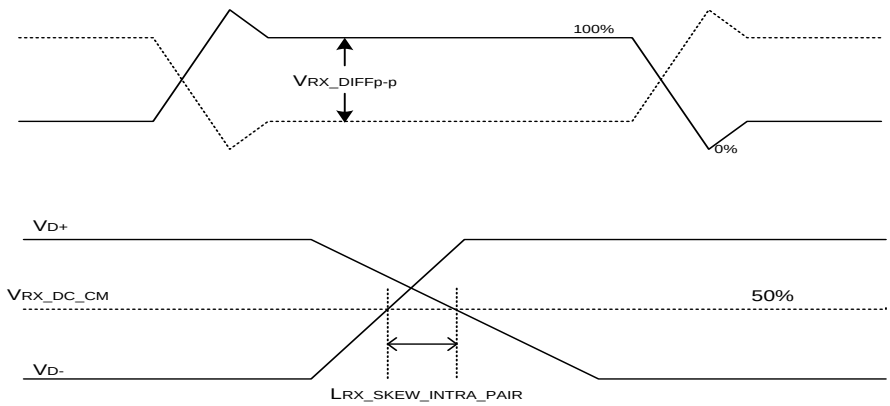
Note※: This Module can support low frame refresh rate 60Hz & 40Hz.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 8.

<Table 8. eDP Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock	ssc		0.5		%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	100	0	1320	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	-	GND	-	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	100	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	150	ps	

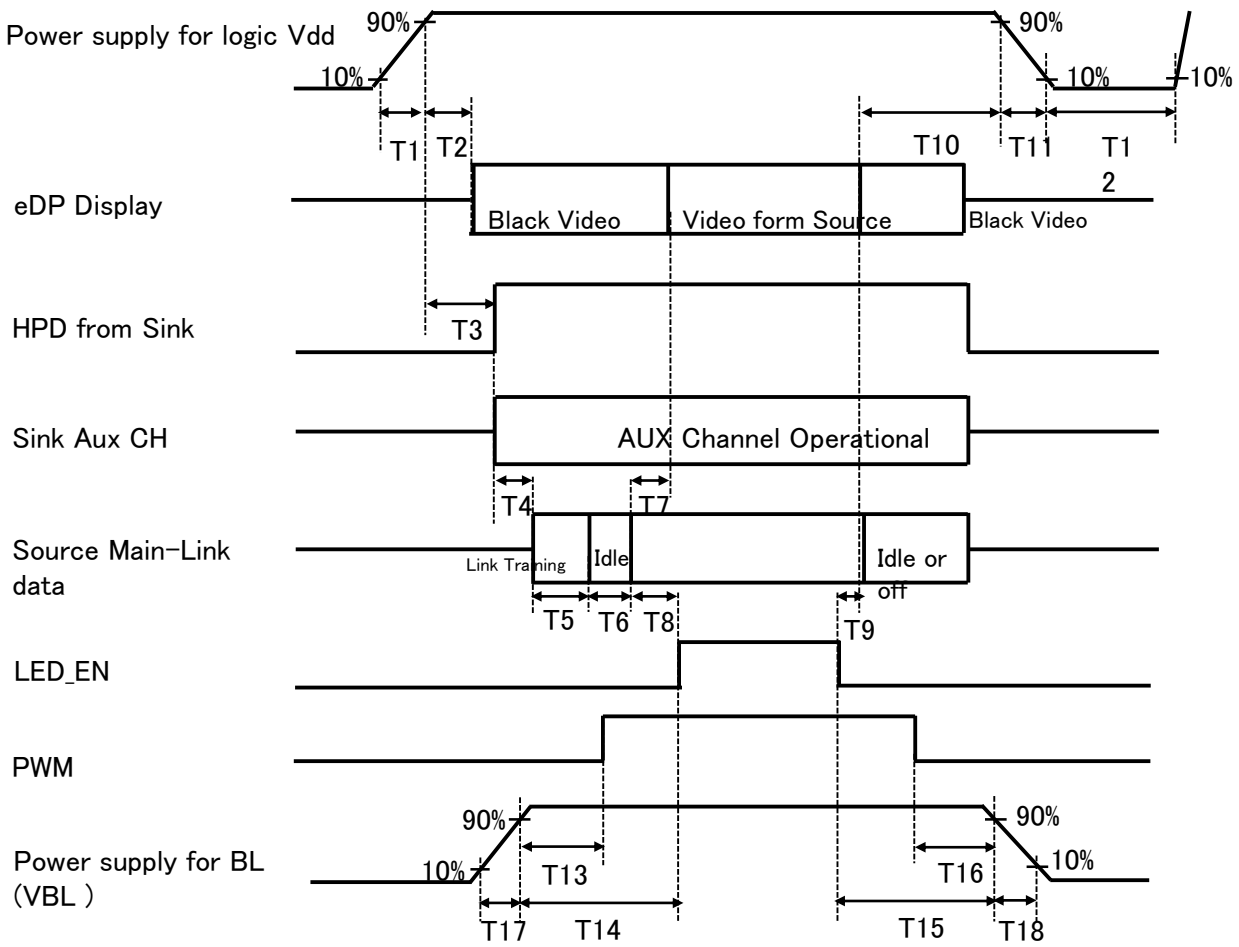


7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▿	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▿	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▿	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▿	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off seq uence shall be as shown in below



- 0.5ms ≤ T1 ≤ 10 ms
- 0ms ≤ T2 ≤ 200 ms
- 0ms ≤ T3 ≤ 200 ms
- 0ms ≤ T13
- 0ms ≤ T14
- 0ms ≤ T17
- 0ms ≤ T7 ≤ 50ms
- 0ms ≤ T10 ≤ 500 ms
- 0 ms ≤ T11 ≤ 10 ms
- 150ms ≤ T12
- 0ms ≤ T15
- 0ms ≤ T16
- 0ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

Connector Name /Description	For Signal Connector
Manufacturer	I-PEX
Type/ Part Number	IPEX-20455-040E-66
Mating housing/ Part Number	IPEX-20455-040T or equivalent

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

FIGURE 6 shows mechanical outlines for the model NE156QUM-N63.
Other parameters are shown in Table 9.

<Table 9. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.2176 (H) ×193.6224(V)	
Number of pixels	3840 (H) X 2160 (V) (1 pixel = R + G + B dots)	
Pixel pitch	0.08964 (H) X 0.08964 (V)	mm
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M	
Display mode	Normally Black	
Dimensional outline	350.66±0.3(H)*216.45±0.5(V) (W/PCB)*2.6(Max)	mm
Weight	320(Max)	gram
Back Light	Connector :MSK24022P10	
	LED, Horizontal-LED Array type	

10.2 Mounting

See FIGURE 6.

10.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an AG coating to minimize reflection and a coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 10. Reliability test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240 hrs
4	High temperature operation test	Ta = 50 ℃, 240 hrs
5	Low temperature operation test	Ta = 0 ℃, 240 hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle
7	Vibration test (non-operating)	1.5G, 10~500Hz,Half Sine X,Y,Z / Sweep rate : 1 hour
8	Shock test (non-operating)	220G, Half Sine Wave 2msec ±X,±Y,±Z Once for each direction
9	Electro-static discharge test (non-operating)	Air : 150 pF, 330Ω, 15 KV Contact : 150 pF, 330Ω, 8 KV

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

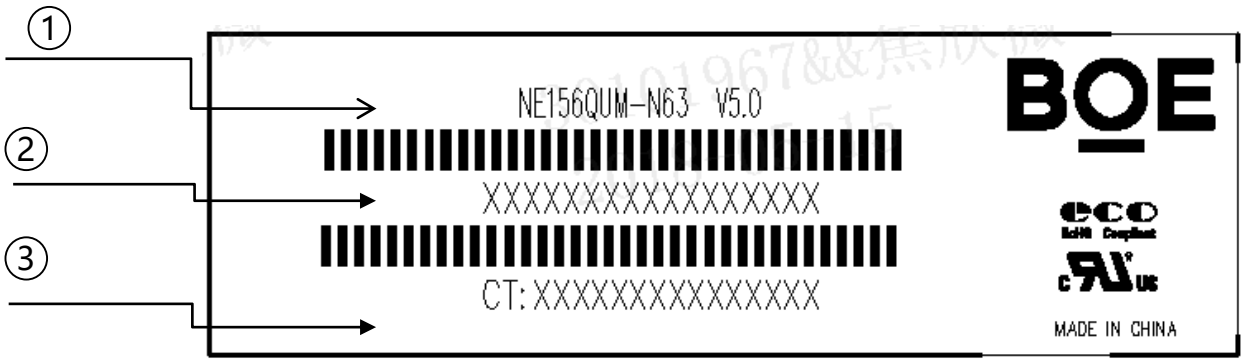
(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) MDL label



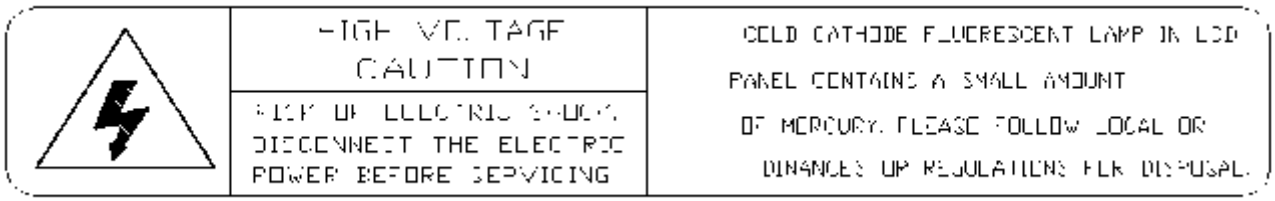
序列号标注部分需打印, 说明如下:

1. **FG-CODE(前12位)**
2. **MDL ID 及其条形码**
3. **CT码及其条形码**

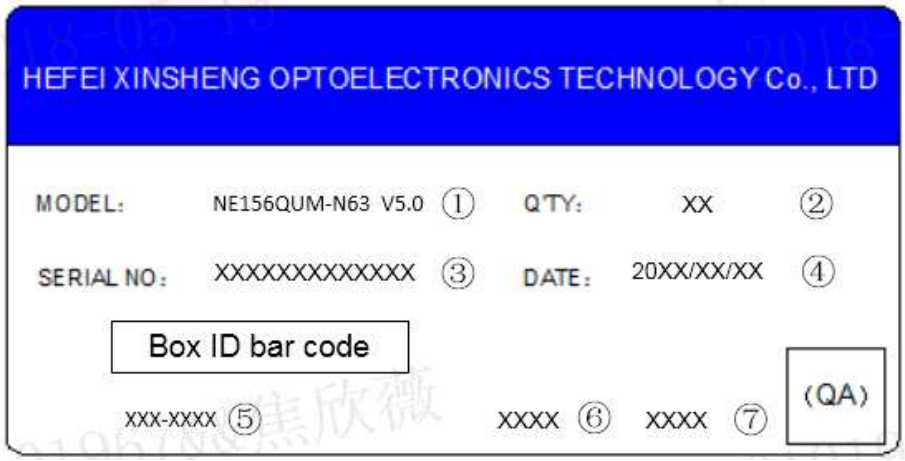
Total Size:80×25mm

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	S	L	S	5	1	2	3	5	9	4	2	0	0	0	1	D	B
Description	Model Code /GBN		Grade	Line	Year		Month	Model Extension Code (Last 4 Digits Of FGCOD)				Serial No 00001-ZZZZZZ					

(2) High voltage caution label



(3) Box label



Serial number marked part needs to print, As follows

1. FG-CODE
2. Product Quantity
3. Box ID
4、Packing Date
5. Customer Part No.--Empty
6. the last four numbers FG-Code
7. Vendor Code --- Empty

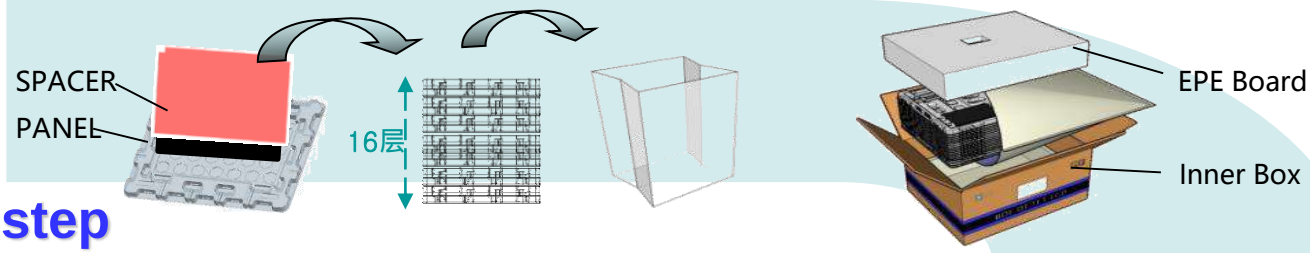
Total Size:110×55mm

Box ID编码规则如下：

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	S	L	S	5	1	2	3	D	0	0	0	6	8
Description	Products GBN		Grade	Line	Year		Month	Revision Code	Serial No				

15.0 PACKING INFORMATION

15.1 Packing order



step 1

-. 将1pcs MDL放入Tray中,每个MDL放置1pcs Spacer（置于顶部）

-.将15EA装满 MDL & Spacer的Tray依次堆叠,其上放置1EA空Tray,并将堆码16EA Tray放置于PE Bag中

-.容量:1pcs/Tray

Step 2

-.将装满Tray的PE Bag放入Inner Box上下放置EPE Board

-. 容量: 15pcs MDL/Inner Box

step 3

-. 将 4EA Box码放于Pallet上,共堆叠3层

堆码高度:1015mm (包含Pallet高度)

-.单Pallet用8ea纸护角防护,捆扎带固定,缠绕膜包裹

-.容量: 4 EA Box/层,共3层,180pcs MDL/Pallet

15.2 Notes

- Box Dimension: 540mm*410mm*295mm
- Package Quantity in one Box: 15 pcs
- Total Weight of One Box: 10.8 kg
- Pallet 四边及打包带位置放置纸护角

16.0 MECHANICAL OUTLINE DIMENSION

Figure 6. TFT-LCD Module Outline Dimension (Front View)

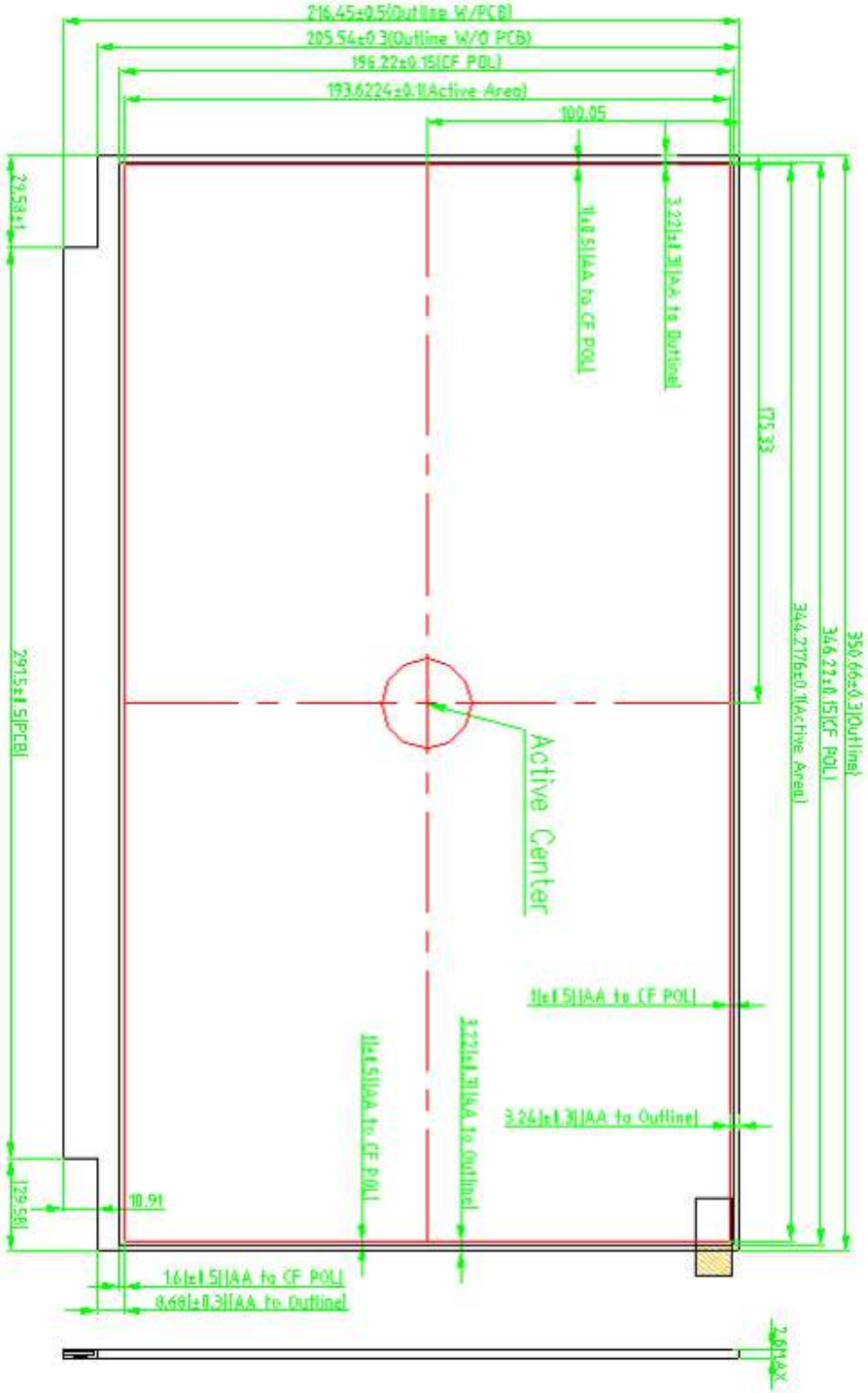
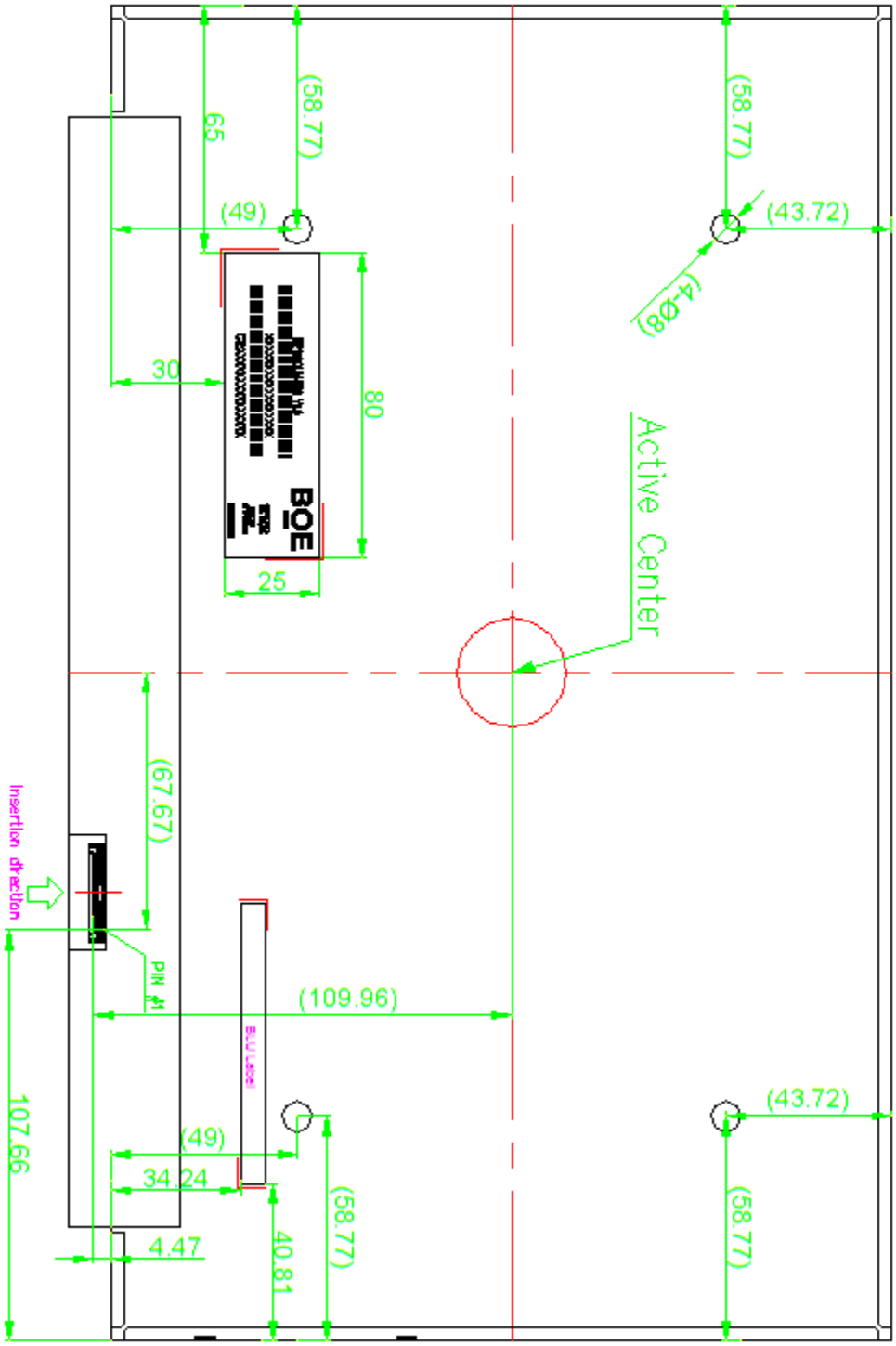


Figure 7. TFT-LCD Module Outline Dimensions (Rear view)



17.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	F4	244		2036	ID = 2036
0B		07	7			
0C	32-bit serial No.	00	0			
0D		00	0			
0E		00	0			
0F		00	0			
10	Week of manufacture	01	1		1	
11	Year of Manufacture	1C	28		2018	Manufactured in 2018
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	A5	165		-	
15	Max H image size	22	34		34	34 cm (Approx)
16	Max V image size	13	19		19	19 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	02	2			RGB display, Preferred Timming mode
19	Red/Green low bits	7B	123		-	Red / Green Low Bits
1A	Blue/White low bits	80	128		-	Blue / White Low Bits
1B	Red x high bits	A6	166	665	0.65	Red (x) = 10100110 (0.65)
1C	Red y high bits	54	84	335	0.328	Red (y) = 01010100 (0.328)
1D	Green x high bits	4D	77	310	0.303	Green (x) = 01001101 (0.303)
1E	Green y high bits	9B	155	619	0.605	Green (y) = 10011011 (0.605)
1F	Blue x high bits	26	38	154	0.151	Blue (x) = 00100110 (0.151)
20	BLue y high bits	11	17	68	0.067	Blue (y) = 00010001 (0.067)
21	White x high bits	50	80	320	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	336	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	
26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			

17.0 EDID Table

2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	4D	77		533.3	533.25MHz Main clock
37		D0	208			
38		00	0		3840	Hor Active = 3840
39		A0	160		160	Hor Blanking = 160
3A		F0	240		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		70	112		2160	Ver Active = 1080
3C		3E	62		62	Ver Blanking = 62
3D		80	128		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		A5	165		10	V sync Offset = 10 line
41		00	0		5	V Sync Pulse width : 5 line
42		58	88		344	Horizontal Image Size = 344 mm (Low 8 bits)
43		C2	194		194	Vertical Image Size = 194 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		-	Refer to right table
48	Detailed timing/monitor descriptor #2	DE	222		355.5	355.5MHz Main clock
49		8A	138			
4A		00	0		3840	Hor Active = 3840
4B		A0	160		160	Hor Blanking = 160
4C		F0	240		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		70	112		2160	Ver Active = 2160
4E		3E	62		62	Ver Blanking = 62
4F		80	128		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50		30	48		48	Hor Sync Offset = 48
51		20	32		32	H Sync Pulse Width = 32
52		A5	165		10	V sync Offset = 10 line
53		00	0		5	V Sync Pulse width : 5 line
54		58	88		344	Horizontal Image Size = 344 mm (Low 8 bits)
55		C2	194		194	Vertical Image Size = 194 mm (Low 8 bits)
56		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0		0	Hor Border (pixels)
58		00	0		0	Vertical Border (Lines)
59		1A	26		-	

17.0 EDID Table

5A	Detailed timing/monitor descriptor #3	00	0			Nvidia nvDPS Lowest refresh rate that does not cause any visual/optical side effect
5B		00	0			
5C		00	0			
5D		00	0			
5E		00	0			
5F		00	0			
60		00	0			
61		00	0			
62		00	0			
63		00	0			
64		00	0			
65		00	0			
66		00	0			
67		00	0			
68		00	0			
69		00	0			
6A		00	0			
6B		00	0			
6C	Detailed timing/monitor descriptor #4	00	0		0	Detailed Timing Description #4
6D		00	0		0	Flag
6E		00	0		0	Reserved
6F		02	2			For Brightness Table and Power consumption
70		00	0		0	Flag
71		0B	11		11	PWM % [7:0] @ Step 0
72		2F	47		47	PWM % [7:0] @ Step 5
73		FF	255		255	PWM % [7:0] @ Step 10
74		0F	15		15	Nits [7:0] @ Step 0
75		3C	60		60	Nits [7:0] @ Step 5
76		AA	170		170	Nits [7:0] @ Step 10
77		23	35		1400	Panel Electronics Power @32x32 Chess Pattern=1400
78		11	17		715	Backlight Power @60 nits=715
79		32	50		4050	Backlight Power @Step 10=4050
7A		AA	170		170	Nits @ 100% PWM Duty =170
7B		00	0		0	Flags
7C		00	0		0	Flags
7D		00	0		0	Flags
7E	Extension flag	00	0			
7F	Checksum	2C	44	44	-	