NEC

TFT COLOR LCD MODULE

Type: NL10276AC30-01
38cm (15.0 Type), XGA

SPECIFICATIONS

(First Edition)

PRELIMINARY

This document is preliminary. All information in this document are subject to change Without prior notice.

NEC Corporation
Display Device Operations Unit
Color LCD Division
Application Engineering Department

Approved	T. Fukuda	Jun. 10, 1998
Checked	Z. Ishii	Jun. 10, 1998
Prepared	T. Kusanagi	Jun. 10, 1998

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Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

CONTENTS

1. DESCRIPTION

NL10276AC30-01 is a TFT(thin film transistor) active matrix color liquid crystal display(LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276AC30-01 has a built-in backlight with an inverter.

The 38cm(15.0 Type) diagonal display area contains 1024 × 768 pixels and can display full-color (more than 16 million colors simultaneously).Also, it has wide viewing angle and multi-scan function. Therefore, this module calls Super Fine TFT.

2. FEATURES

- Ultra-wide viewing angle
- Low reflection
- High luminance
- Analog RGB signals
- Multi-scan function: e.g., XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC
- Incorporated edge type backlight (Four lamps, Inverter)
- Lamp holder replaceable (Part No. 150LHS01)

3. APPLICATIONS

- Desk-top type of PC
- Engineering work station

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

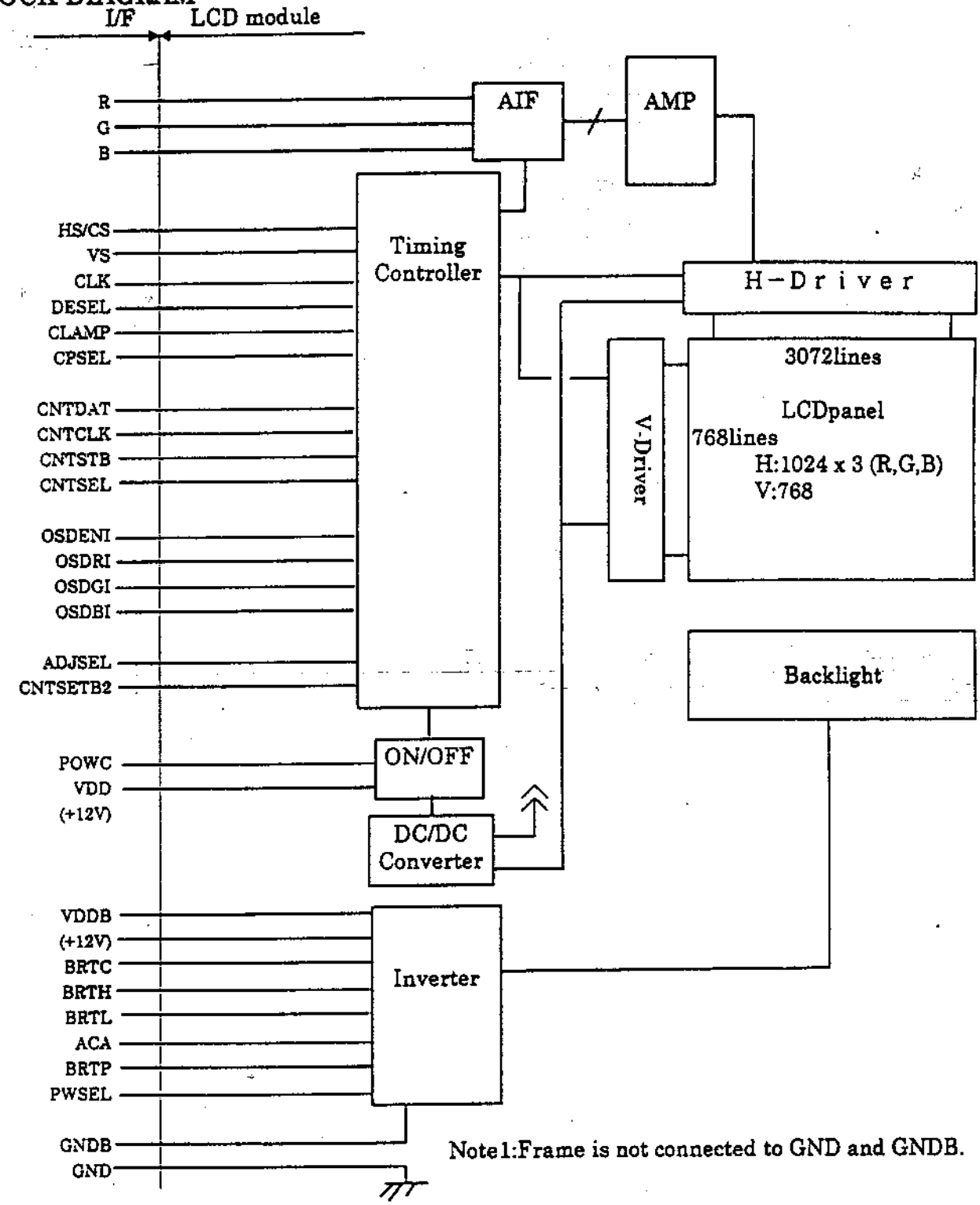
Display area	304.128(H) × 228.096(V)mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1024 × 768
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.297(H) × 0.297(V)mm
Module size	350.0(H) × 265.0(V) × 24.0(D)mm
Weight	1680g (typ.)
Contrast ratio	150:1 (typ., perpendicular)

Viewing angle (more than the contrast ratio of 10:1)
- Horizontal: 85° (typ. , left side, right side)
- Vertical: 85° (typ. , up side, down side)

Designed viewing direction
- Optimum grayscale (γ =2.2): perpendicular

Polarizer Pencil-hardness	3H (min. at JIS K5400)
Color gamut	35%(typ., At center, To NTSC)
Response time	44ms(typ.), " black " to " white "
Luminance	180cd/m^2(typ.)
Signal system	Analog RGB signals, Synchronous signals(Hsync and Vsync), CLK
Supply voltage	12V, 12V (Logic/LCD driving, Backlight)
Backlight	Edge light type: Four cold cathode fluorescent lamps with an inverter [Replaceable parts] · Lamp holder: 150LHS01 · Inverter: 150PW011
Power consumption	24W (typ.)

6. BLOCK DIAGRAM



Note1:Frame is not connected to GND and GNDB.

7. SPECIFICATIONS

7.1. GENERAL SPECIFICATIONS

Item	Contents	Unit
Module size	350.0±0.6 (H) x 265.0±0.6 (V) x 24.0 (max.)(D)	mm
Display area	304.128 (H) x 228.096 (V)	mm
Number of dots	1024 x 3 (H) x 768 (V)	dots
Pixel pitch	0.297 (H) x 0.297 (V)	mm
Dot pitch	0.099 (H) x 0.297 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	full color	color
Weight	1720 (max.)	g

7.2. ABSOLUTE MAXMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta=25℃
	VDDB	-0.3 to +14	V	
Logic input voltage	Vin1	-0.3 to +5.5	V	Ta=25℃ VDD=12V
R,G, B input voltage	Vin2	-6.0 to +6.0	V	
CLK input voltage	Vin3	-7.0 to +7.0	V	
BRTL input voltage	Vin4	-0.3 to +1.5	V	
Storage temp.	Tst	-20 to +60	℃	–
Operating temp.	Top	0 to +50	℃	Module surface note 1
Humidity (no condensation)	≦95% relative humidity			Ta≦40 ℃
	≦85% relative humidity			40<Ta≦50 ℃
	Absolute humidity shall not exceed Ta=50℃, 85% relative humidity level.			Ta>50 ℃

note 1: Measured at the display area

7.3. ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving, Backlight (Ta=25℃)

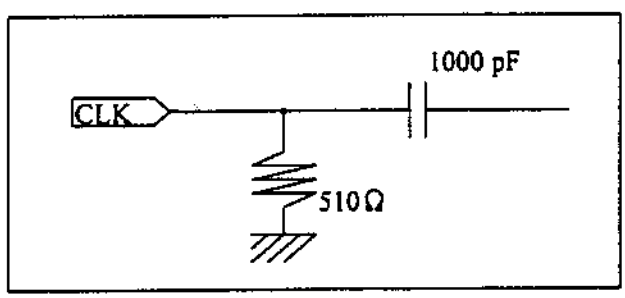
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	11.4	12.0	12.6	V	for Logic and LCD driving
	VDDB	11.4	12.0	12.6	V	for backlight
Logic input " L " voltage 1	ViL1	0	–	0.6	V	for BRTP
Logic input " H " voltage 1	ViH1	4.5	–	5.25	V	
Logic input " L " voltage 2	ViL2	0	–	0.8	V	Logic except BRTP
Logic input " H " voltage 2	ViH2	2.2	–	5.25	V	
Input CLK voltage	ViCLK	0.6	–	1.0	Vp-p	CLK
Input DC voltage level	ViDCCLK	-4.5	–	+4.5	V	
Logic input " L " current 1	IiL1	-10	–	–	μA	HS, VS
Logic input " H " current 1	IiH1	–	–	160	μA	
Logic input " L " current 2	IiL2	-1400	–	–	μA	CNTSEL, CPSEL, POWC, ADJSEL
Logic input " H " current 2	IiH2	–	–	10	μA	
Logic input " L " current 3	IiL3	-1.0	–	–	mA	BRTC, BRTL, ACA, PWSEL
Logic input " H " current 3	IiH3	–	–	0.8	mA	
Logic input " L " current 4	IiL4	-1.0	–	–	mA	BRTP
Logic input " H " current 4	IiH4	–	–	10	mA	
Logic input " L " current 5	IiL5	-10	–	–	μA	Logic except above input
Logic input " H " current 5	IiH5	–	–	10	μA	
Supply current note 1	IDD	–	570	800	mA	VDD=12.0V
	IDDB	–	1430	1600	mA	VDDB=12.0V (Max.luminance)

Note 1: Pixel checkered pattern

(2) Video signal (R, G, B) input (Ta=25℃)

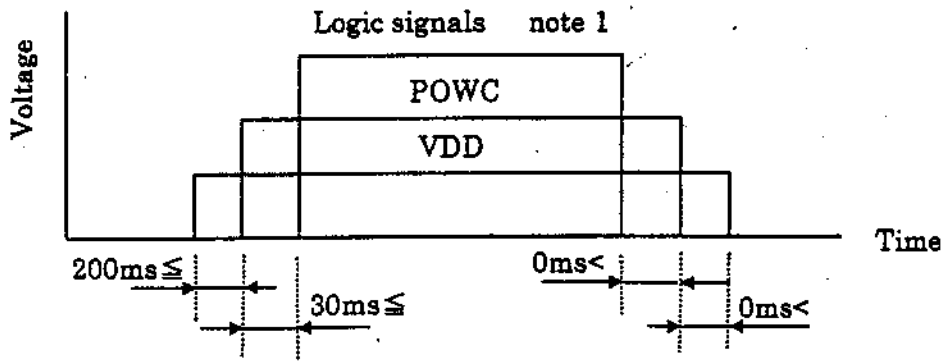
Item	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white - black)	0 (black)	0.7 (white)	0.9	Vp-p	Need to adjust contrast if input more 0.7Vp-p
DC input level (black)	-3.5	–	+3.5	V	–

(3) CLK input equivalent circuit



7.4. CAUTIONS ABOUT POWER SUPPLY

(1) Cautions at Power-on



note 1: Synchronous signal, Control signals, CLK

CAUTION
Wrong power sequence may damage to the module.

a) Logic signals (synchronous signals and control signals) should be "0" voltage (V), when VDD is not input. If higher than 0.3 V is input to signal lines, the internal circuit will be damaged.

b) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, Vsync is not input more than 90 ms typically. As the display data are unstable in this period, the display is disordered. But the backlight works correctly even this period. So the backlight ON/OFF should be controlled by BRTC signal.

c) The backlight ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals.

d) Keep POWC signal "L" more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.

e) Analog RGB input are independent from this power supply sequence.

f) 12V for backlight should be started up within 80ms, otherwise, the protection circuit makes the backlight turn off

(2)Ripple of supply voltage

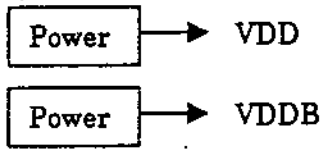
Please note that the ripple at the input connector of the module should be within the values shown in this table. If the ripple would be beyond these values, the noise might appear on the screen.

	VDD (for logic and LCD driver)	VDDB (for backlight)
Acceptable range	≦ 100mVp-p	≦ 200mVp-p

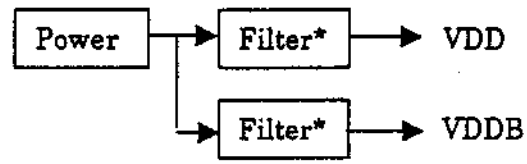
note 1:The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



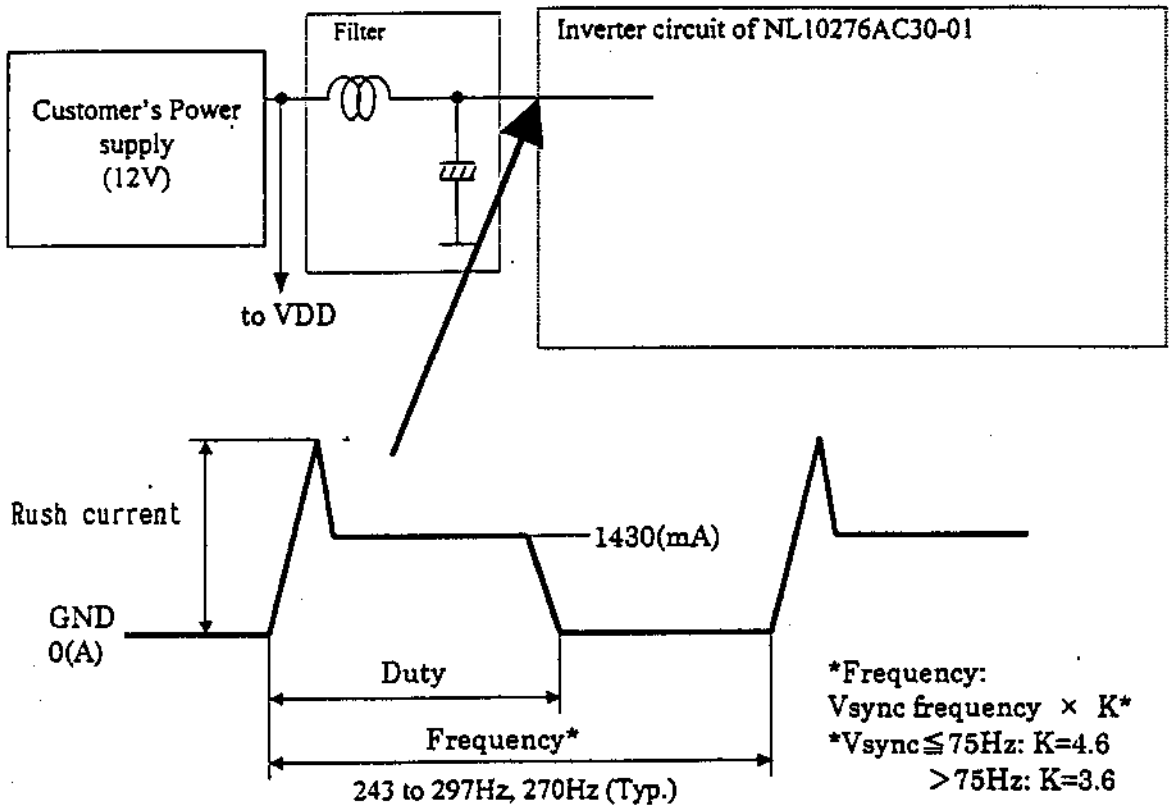
b) Put the filter



Filter*(reference value)
L = 10 μH to 100 μH
C = 10 μF to 100 μF

(3)Inverter current wave

In the luminance control mode, the rush current below flows into the inverter of the module. The duty cycle varies from 100% through 20% depending on the luminance control level. This might cause the noise on the screen. Please evaluate the appropriate value of the capacitor in the filter to eliminate the noise.



*Frequency:
Vsync frequency × K*
*Vsync≦75Hz: K=4.6
>75Hz: K=3.6

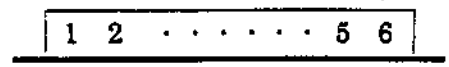
7.5. INTERFACE PIN CONNECTION

(1) CN1

Part No. : MRF03-6R-SMT(coaxial type)
Adaptable socket : MRF03-2×6P-1.27(For cable type) or
MRF03-6PR-SMT(For board to board type)
Supplier : HIROSE ELECTRIC CO., LTD.
Coaxial cable : UL20537PF75VLAS
Supplier : HITACHI CO., LTD.
note 1: A coaxial cable shield should be connected with GND.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync
3	R	6 ▼	CLK

Figure from socket view



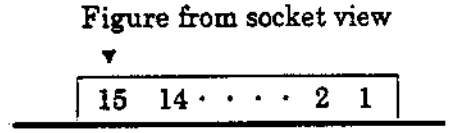
(2) CN3

Part No. : IL-Z-15PL-SMTY
Adaptable socket : IL-Z-15S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDD	9	GND
2	VDD	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	CLAMP
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15 ▼	GND
8	CNTSTB		

Note 1:N.C.(No connection) should be open.

Figure from socket view



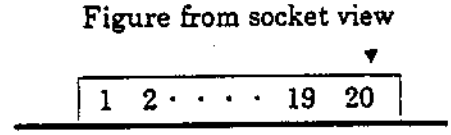
(3) CN4

Part No. : DF14A-20P-1.25H
Adaptable socket : DF14-20S-1.25C
Supplier : HIROSE ELECTRIC CO., LTD

Pin No.	Symbol	Pin No.	Symbol
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20 ▼	N.C.

Note 1:N.C.(No connection) should be open.

Figure from socket view



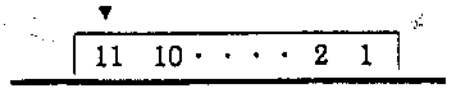
(4) CN201

Part No. : IL-Z-11PL-SMTY
Adaptable socket : IL-Z-11S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDDB	7	ACA
2	VDDB	8	BRTC
3	VDDB	9	BRTH
4	GNDB	10	BRTL
5	GNDB	11 ▼	N.C.
6	GNDB		

Note 1:N.C.(No connection) should be open.

Figure from socket view



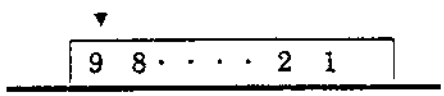
(5) CN202

Part No. : IL-Z-9PL-SMTY
Adaptable socket : IL-Z-9S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GNDB	6	BRTL
2	GNDB	7	BRTP
3	ACA	8	GNDB
4	BRTC	9 ▼	PWSEL
5	BRTH		

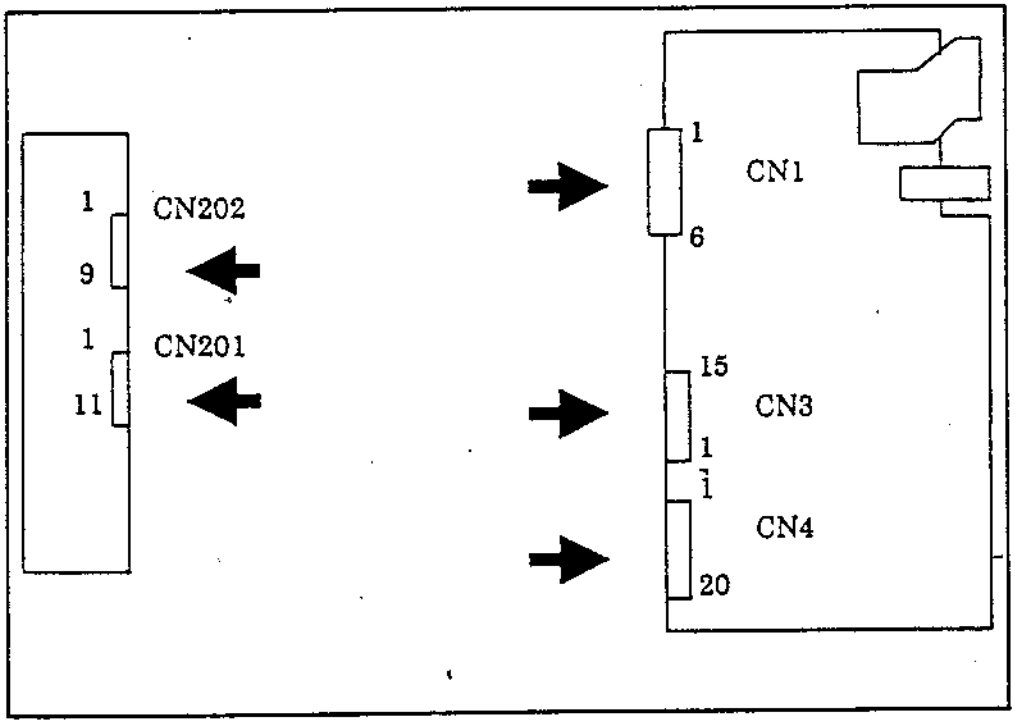
Note 1:N.C.(No connection) should be open.

Figure from socket view



Caution: Choice CN201 or CN202 and use one.

《Rear view》



7.6. PIN FUNCTION

Symbol	I/O	Logic	Description
CLK	Input	Positive	Dot clock input. (ECL level) This timing-signal is for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	–	Red video signal input (0.7Vp-p, 75Ω)
G	Input	–	Green video signal input (0.7Vp-p, 75Ω)
B	Input	–	Blue video signal input (0.7Vp-p, 75Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "Open": Logic and LCD power are on. "L": Logic and LCD power are off. When POWC is "L", serial communication data is clear. Please set again. note 1
CNTSEL	Input	–	Display control signal in case of serial communications. (TTL level) "H" or "Open" : Default , "L" : External control Serial communications are set up by external control.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in 7.7 FUNCTIONS.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTDAT is mentioned in 7.7 FUNCTIONS.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTDAT is mentioned in 7.7 FUNCTIONS.
CPSEL	Input	–	CLAMP function select signal "H" or "Open": Default , "L" : External control
CLAMP	Input	Negative	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L".
ADJSEL	Input	Positive	Contrast, brightness select control signal (TTL level)
CNTSTB2	Input	Positive	Latch pulse2 for display control data Detail of CNTDAT is mentioned in 7.7 FUNCTIONS
OSDRI	Input	–	Input OSD-R data Detail of CNTDAT is mentioned in 7.8.5 OSD FUNCTIONS
OSDGI	Input	–	Input OSD-G data Detail of CNTDAT is mentioned in 7.8.5 OSD FUNCTIONS
OSDBI	Input	–	Input OSD-B data Detail of CNTDAT is mentioned in 7.8.5 OSD FUNCTIONS
OSDENI	Input	Positive	Enable signal for OSD Detail of CNTDAT is mentioned in 7.8.5 OSD FUNCTIONS

Note 1: When POWC is "L" logic input signal is all "0V". If input more than "0.3V", inside circuits of the LCD module may be broken.

Symbol	I/O	Logic	Description
ACA	Input	Positive	Luminance control signal (TTL level) "H" or "Open" : Normal luminance "L" : Low luminance (1/2 of normal luminance)
BRTC	Input	Positive	Backlight ON/OFF control signal (TTL level) "H" or "Open" : Backlight ON, "L": Backlight OFF
BRTH BRTL	Input	–	Variable resistor control or Voltage control See the detail below function select
BRTP	Input	–	Luminance control signal
PWSEL	Input	Positive	Select the control of luminance (TTL level) See the detail in next page
VDD	–	–	Power supply for Logic and LCD driving +12V (±5%)
VDDB	–	–	Power supply for backlight. +12V (±5%)
GND	–	–	Signal ground for Logic and LCD driving (Connect to a system ground)
GNDB	–	–	Ground for backlight. GNDB is not connected to the frame ground of LCD module.

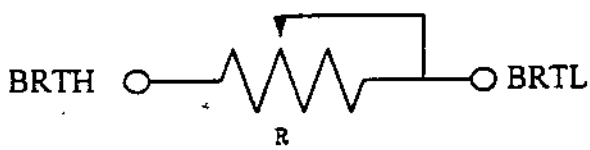
Note1: Frame ground, system ground (GND) and backlight ground (GNDB) are not connected in the module.

Note2: 12V for backlight should be started up within 80ms, otherwise, the protection circuit makes the backlight turn off.

[Function select]

Form	Terminal	How to adjust	
BRTP signal =Valid	PWSEL="L"	Luminance can be controlled by BRTP-signal. See More detail of 7.8.6 **OUTSIDE CONTROL FOR LUMINANCE**	
BRTP signal =should be open	PWSEL= "H" or "Open"	Volume	Please connect BRTP and BRTL. Note 1
		Voltage	BRTH is "0V", and BRTL input voltage controls brightness. When BRTL input voltage is "1V" the luminance become maximum, and when BRTL input voltage is "0V", the luminance becomes minimum

Note 1: The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor correspond to the mimimum of luminance.



Mating variable resistor:
10KΩ ±5% , B curve

Maximun luminance(100%) : R=10 KΩ
Minimum luminance (20%) : R= 0Ω

7.7. FUNCTIONS

This LCD module has following functions by serial data input (table 1)

(1) Control Display position (VERTICAL):	See table 3
(2) Control Display position (HORIZONTAL):	See table 6
(3) Control CLK delay:	See table 4
(4) Change CLK fall/rise synchronous:	See table 5
(5) Contrast control:	See table 9, 10 and 7.8.4 COLOR CONTROL FUNCTION AND GRAPH IMAGE
(6) Sub-Contrast control:	
(7) Sub-Brightness control:	

Set up the following items to work the above functions

(A) Expansion mode:	See table 2 and 7.8 EXPANSION FUNCTION
(B) CLK counts of horizontal period:	See table 7
(C) CLK frequency range:	See table 8

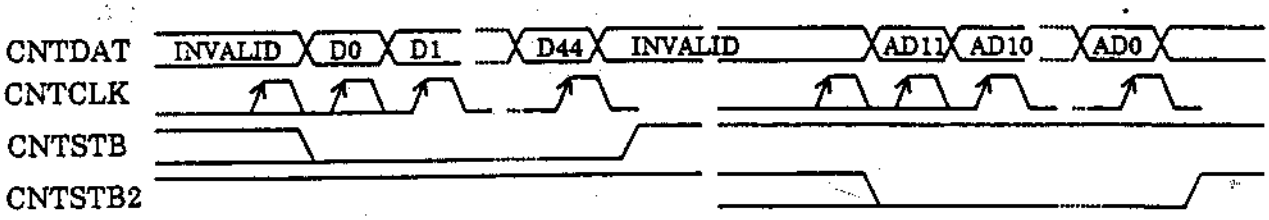
7.7.1. HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is "L", the above functions((1)-(4), (A)-(C))are valid. (CNTSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions((1)-(4), (A)-(C)) are effective.

If ADJSEL is "L", the above functions((5)-(7))are valid. (ADJSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB2. Once, the data is latched, the above functions((5)-(7)) are effective.

Please keep CNTSTB/2 to be "L" during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

7.7.2. SERIAL COMMUNICATION TIMING AND WAVEFORM



Parameter	Symbol	Min.	Max.	Unit	Remark
CLK pulse-width	Twck	50	–	ns	CNTCLK
CLK frequency	Fclk	–	5	MHz	
DATA set-up-time	Tdst	50	–	ns	CNTDAT
DATA hold-time	Tdhl	50	–	ns	
Latch pulse-width	Twlp	50	–	ns	CNTSTB, CNTSTB2
Latch set-up-time	Tlst	50	–	ns	
Rise / fall time	Tr , Tf	–	50	ns	CNT xxx

SERIAL COMMUNICATION WAVEFORM

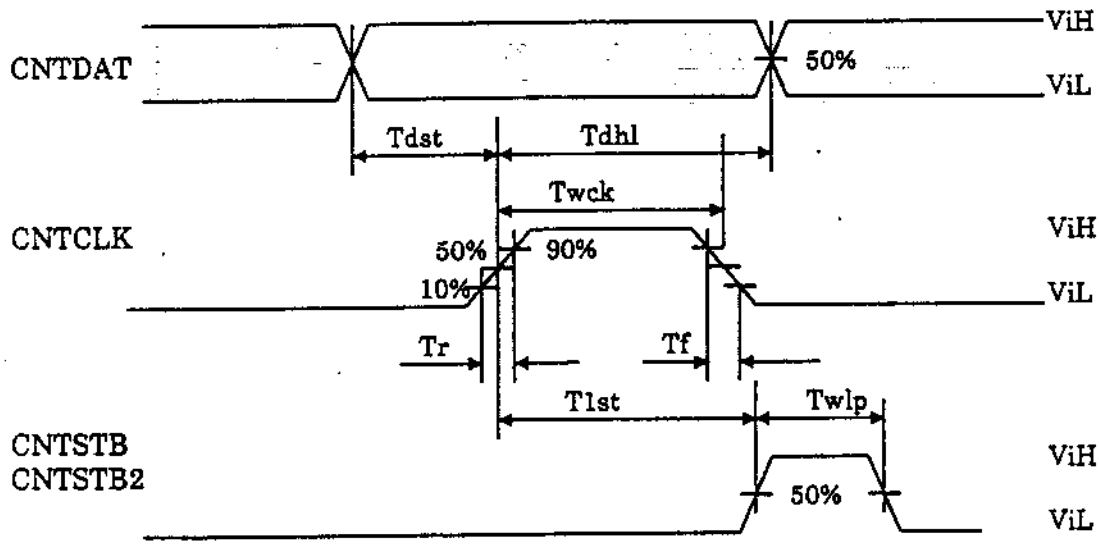


Table 1. CNTDAT Composition

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19	DELAY2	CLK delay	
D20	DELAY1	CLK delay	
D21	DELAY0	CLK delay (LSB)	
D22	CKS	CLK reverse signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	CLK count of horizontal period (MSB)	See table 7
D33	HSE9	CLK count of horizontal period	
D34	HSE8	CLK count of horizontal period	
D35	HSE7	CLK count of horizontal period	
D36	HSE6	CLK count of horizontal period	
D37	HSE5	CLK count of horizontal period	
D38	HSE4	CLK count of horizontal period	
D39	HSE3	CLK count of horizontal period	
D40	HSE2	CLK count of horizontal period	
D41	HSE1	CLK count of horizontal period	
D42	HSE0	CLK count of horizontal period (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	

Continue to next page

Table 1. CNTDAT Composition (continuation)

DATA	DATA name	Function	
AD11	DAA0	Color adjust select data (LSB)	See table 10
AD10	DAA1	Color adjust select data	
AD9	DAA2	Color adjust select data	
AD8	DAA3	Color adjust select data (MSB)	
AD7	DAD7	Color adjust data (MSB)	See table 9
AD6	DAD6	Color adjust data	
AD5	DAD5	Color adjust data	
AD4	DAD4	Color adjust data	
AD3	DAD3	Color adjust data	
AD2	DAD2	Color adjust data	
AD1	DAD1	Color adjust data	
AD0	DAD0	Color adjust data (LSB)	

Table 2. Display mode (VEX3 to VEX0 : 4bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	XGA	Standard note 1
0	0	0	1	1.25	SVGA	See 7.8.3 DISPLAY IMAGE
0	0	1	0	1.6	PC98,VGA,TEXT	
0	0	1	1	—	Prohibit	
0	1	0	0	—	Prohibit	
0	1	0	1	—	Prohibit	
0	1	1	0	—	Prohibit	
0	1	1	1	—	Prohibit	
1	0	0	0	—	Prohibit	
1	0	0	1	1.2	832 x 624(MAC)	
1	0	1	0	—	Prohibit	
1	0	1	1	—	Prohibit	
1	1	0	0	—	Prohibit	
1	1	0	1	—	Prohibit	
1	1	1	0	—	Prohibit	
1	1	1	1	—	Prohibit	

note 1: When CNTSEL is "H" or "Open" , display mode is XGA.

Table 3. Vertical position (VD10 to VD0 : 11bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] note 1
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 note 2

note 1: This is horizontal line number for effective VIDEO signal from Vsync-fall.
note 2: The maximum vertical position is Vsync total.
note 3: When CNTSEL is "H" or "Open", vertical position is fixed at 35[H].

Table 4. CLK delay (DELAY6 to DELAY0 : 7bit)

DELAY[6..0]	Delay	Unit	DELAY[6..0]	Delay	Unit	DELAY[6..0]	Delay	Unit
00H	11.1	ns	30H	23.6	ns	60H	36.0	ns
01H	11.3	ns	31H	23.8	ns	61H	36.3	ns
02H	11.6	ns	32H	24.1	ns	62H	36.6	ns
03H	11.8	ns	33H	24.3	ns	63H	36.8	ns
04H	12.1	ns	34H	24.6	ns	64H	37.1	ns
05H	12.3	ns	35H	24.8	ns	65H	37.3	ns
06H	12.6	ns	36H	25.1	ns	66H	37.6	ns
07H	12.8	ns	37H	25.3	ns	67H	37.8	ns
08H	13.1	ns	38H	25.6	ns	68H	38.1	ns
09H	13.4	ns	39H	25.8	ns	69H	38.4	ns
0AH	13.6	ns	3AH	26.1	ns	6AH	38.7	ns
0BH	13.9	ns	3BH	26.4	ns	6BH	38.9	ns
0CH	14.1	ns	3CH	26.6	ns	6CH	39.2	ns
0DH	14.4	ns	3DH	26.8	ns	6DH	39.4	ns
0EH	14.6	ns	3EH	27.1	ns	6EH	39.7	ns
0FH	14.9	ns	3FH	27.4	ns	6FH	39.9	ns
10H	15.2	ns	40H	27.7	ns	70H	40.2	ns
11H	15.5	ns	41H	28.0	ns	71H	40.4	ns
12H	15.7	ns	42H	28.3	ns	72H	40.7	ns
13H	16.0	ns	43H	28.5	ns	73H	41.0	ns
14H	16.2	ns	44H	28.8	ns	74H	41.2	ns
15H	16.5	ns	45H	29.0	ns	75H	41.4	ns
16H	16.7	ns	46H	29.3	ns	76H	41.7	ns
17H	17.0	ns	47H	29.5	ns	77H	42.0	ns
18H	17.3	ns	48H	29.8	ns	78H	42.3	ns
19H	17.5	ns	49H	30.1	ns	79H	42.5	ns
1AH	17.8	ns	4AH	30.3	ns	7AH	42.8	ns
1BH	18.1	ns	4BH	30.6	ns	7BH	43.1	ns
1CH	18.3	ns	4CH	30.8	ns	7CH	43.3	ns
1DH	18.6	ns	4DH	31.1	ns	7DH	43.5	ns
1EH	18.8	ns	4EH	31.3	ns	7EH	43.8	ns
1FH	19.1	ns	4FH	31.6	ns	7FH	44.0	ns
20H	19.4	ns	50H	31.9	ns			
21H	19.6	ns	51H	32.1	ns			
22H	19.9	ns	52H	32.4	ns			
23H	20.2	ns	53H	32.7	ns			
24H	20.4	ns	54H	32.9	ns			
25H	20.7	ns	55H	33.2	ns			
26H	20.9	ns	56H	33.4	ns			
27H	21.2	ns	57H	33.7	ns			
28H	21.5	ns	58H	34.0	ns			
29H	21.7	ns	59H	34.3	ns			
2AH	22.0	ns	5AH	34.5	ns			
2BH	22.3	ns	5BH	34.8	ns			
2CH	22.5	ns	5CH	35.0	ns			
2DH	22.7	ns	5DH	35.3	ns			
2EH	23.0	ns	5EH	35.5	ns			
2FH	23.3	ns	5FH	35.8	ns			

note 1: When CNTSEL is "H" or "Open", DELAY[6..0] is fixed at 00H.

note 2: This delay value is typical value at Ta=25℃. By changing ambient temperature and power supply, the delay will be changed.

Please set up a preferable display position. See the following references.

① Variation of CLK delay by temperature drift. (as reference) The temperature constant of CLK delay is 0.2%/℃.

Calculated example:

In case of delay time is 20ns at Ta=25℃;

(a) In case Ta rising to 50℃.

Increase of delay time → (50℃ − 25℃) × 0.002 × 20ns = +1ns

So, the total delay time is 21 ns at Ta=50℃.

(b) In case Ta falling to 0℃.

Decrease of delay time → (0℃ − 25℃) × 0.002 × 20ns = -1ns

So, the total delay time is 19 ns at Ta=0℃.

② Variation of CLK delay time against each LCD module. (as reference)

−10.5% to +14.4%

	MOD setting			
	0,0	0,1	1,0	1,1
The upper limit of CLK delay; DELAY[6..0]	Prohibit	59H	6BH	7FH

Table 5. CLK reverse signal (CKS)

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK 
1	DATA is sampled on falling edge of CLK 

note 1: When CNTSEL is "H" or "Open", CKS is "0".

Table 6. Display horizontal position (HD8 to HD0 : 9bit)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] note 1
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

note 1: This is CLK number from Hsync-fall to effecting VIDEO signal.
note 2: When CNTSEL is "H" or "Open", Horizontal position is set at 296[CLK].

Table 7. CLK count of horizontal period (HSE10 to HSE0 : 11bit)

HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK count note 1
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

note 1: This is CLK number from Hsync to next Hsync.
note 2: When CNTSEL is "H" or "Open", CLK count is set at 1344[CLK].
note 3: This CLK count must be equal to CLK count of input signal.

Table 8. CLK frequency select (MOD1 to MOD0 : 2bit)

MOD1	MOD0	CLK frequency [MHz]
0	0	Prohibit
0	1	$65 < f \leqq 80$
1	0	$50 < f \leqq 65$
1	1	$20 < f \leqq 50$

note 1: Set up the MOD1 and MOD0 complying with input CLK frequency.
note 2: When CNTSEL is "H" or "Open", CLK frequency is set 65 to 80MHz.

Table 9. Color control data (DAD7 to DAD0 : 8bit)

DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0	Adjusting value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Note 1: Adjust value for selecting function above table.10.
Note 2: Different D/A-range depend on function selected.
Note 3: See more detail 7.8.4. Color control function and graph image.

Table 10. Color adjust select data (DAA3 to DAA0 : 4bit)

DAA3	DAA2	DAA1	DAD0	Function
0	0	0	0	Prohibit
0	0	0	1	Main contrast
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	0	1	1	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

Note 1: See more detail 7.8.4. Color control function and graph image.

7.8. EXPANSION FUNCTION
7.8.1. HOW TO USE EXPANSION MODE

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 1.6 times vertically and horizontally, VGA screen image can be displayed fully on the screen of XGA resolution.

This LCD module has the function of expanding vertical direction as shown in Table 1. And expanding horizontal direction is possible by setting input CLK frequency which is equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

The below image is display example, HD and VD is set to most suitable frequency.

Please adopt this mode after evaluating display quality, because the appearance of expansion mode is happened to become bad some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal note 1
XGA	1024 x 768	1	1
SVGA	800 x 600	1.25	1.25
VGA	640 x 480	1.6	1.6
VGA text	720 x 400	1.6	1.4
PC9801	640 x 400	1.6	1.6
MAC	832 x 624	1.2	1.2

note 1: The horizontal magnification multiples the input clock(CLK).

Input CLK = system CLK × horizontal magnification

Example:

In case of XGA and VGA, CLK frequency can be decided as follows.

XGA: (system CLK(65MHz)) × 1.0=65MHz

VGA: (system CLK(25.175MHz)) × 1.6=40.28MHz

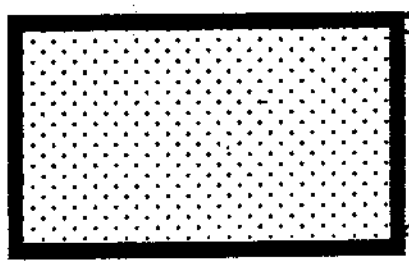
7.8.2. SETTING SERIAL DATA

Input signal								Module serial data setting		
Mode	System CLK [M Hz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count number [CLK]	DSP * [CLK]	Count number [H]	DSP * [H]	Calculation formula		
				(A)	(B)	—	(C)	(A) x Ver. mag.	(B) x Hor. mag.	=(C)
XGA (1024 x 768)	65 75 78.75	48.363 56.476 60.023	60.004 70.069 75.029	1344 1328 1312	296 280 272	806 806 800	35 35 31	(A) x 1	(B) x 1	
MAC (832x624)	57.283	49.725	74.5	1152	288	667	42	(A)x1.2	(B)x1.2	
SVGA (800 x 600)	36 40 50 49.5	35.156 37.879 48.077 46.875	56.25 60.317 72.188 75	1024 1056 1040 1056	200 216 184 240	625 628 666 666	24 27 29 24	(A) x 1.25	(B) x 1.25	=(C)
VGA (640 x 480)	25.175 31.5 31.5 30.24	31.469 37.861 37.5 35.0	59.94 72.809 75 66.667	800 832 840 864	144 168 184 160	525 520 500 525	35 31 19 42	(A) x 1.6	(B) x 1.6	
VGA text (720 x 400)	28.322 31.5	31.469 37.927	70.087 85.04	900 936	153 180	449 446	37 45	(A) x 1.4	(B) x 1.4	
PC9801 (640 x 400)	21.053	24.827	56.432	848	144	440	33	(A) x 1.6	(B) x 1.6	443

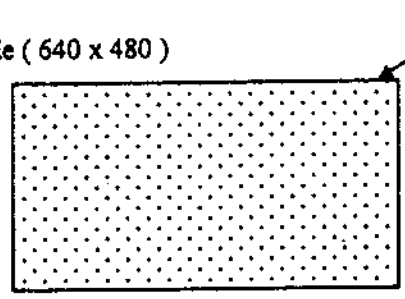
*: DSP = Display Start Period. DSP is total of "pulse-width" and "back-porch".
Note 1: HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.
Note 2: The pulse-width of Hsync, Vsync and back-porch are the same as XGA-mode. (Standard-mode).
Note 3: HSE see CLK number of table 7.
Note 4: HD see horizontal position of table 6.
Note 5: VD see vertical position of table 3.

7.8.3. DISPLAY IMAGE

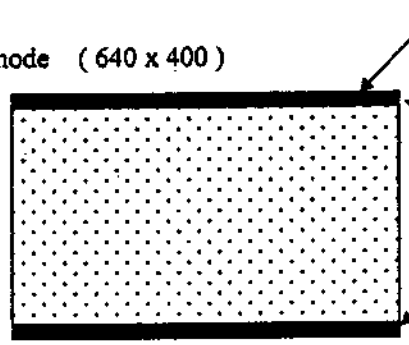
1) SVGA mode (800 x 600)



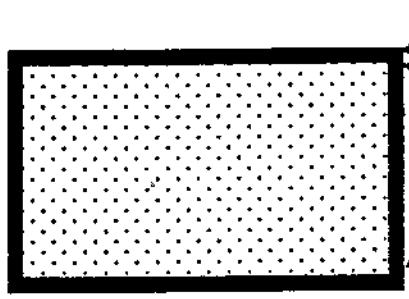
2) VGA mode (640 x 480)



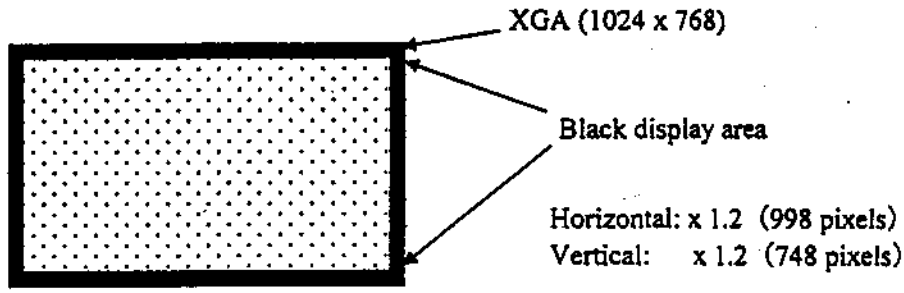
3) PC9801 mode (640 x 400)



4) VGA text mode (720 x 400)



5) 832 x 624 MAC mode (832 x 624)



7.8.4. COLOR CONTROL FUNCTION AND GRAPH IMAGE

This LCD module can adjust the following functions by serial data input (table.1)

(1) Main contrast:
(2) Sub-contrast each R,G,B:
(3) Sub-brightness each R,G,B:

} **See table 9, 10 and 7.8.4 Color control function and graph image**

(1) Main contrast

Main contrast is adjusted R/G/B contrast at the same time. Contrast control the amplitude of input video signal.

Default value: 128, Valid range: 78 to 198
Contrast minimum: 198
Contrast maximum: 78
ADJSEL="H" or "Open" : Maincontrast=128

(2) Sub-contrast R,G,B

Sub-contrast can adjust each R/G/B. Contrast control the amplitude of input video signal.

Default value: 128, Valid range: 78 to 198
Contrast minimum: 198
Contrast maximum: 78
ADJSEL="H" or "Open" : Maincontrast=128

(3) Sub-brightness R,G,B

Sub-brightness can adjust each R/G/B. Brightness adjust the black level of input video signal.

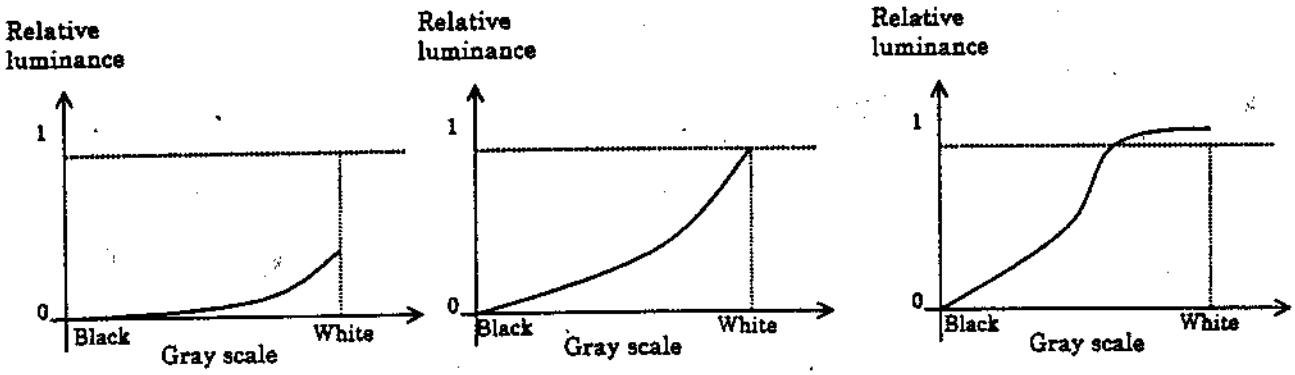
Default value: 128, Valid range: 55 to 163
Brightness minimum: 55
Brightness maximum: 163
ADJSEL="H" or "Open" : Maincontrast=128

Note1: If use to go over above valid range, LCD module will be not destroy. However LCD will be inferiority. Please keep value of valid range.

Note2: Although set up the same value for each LCD, color will be caused the different. And also, will be afraid to deviate values from optical characteristics. Please adopt this functions evaluating display quality.

《GRAPH IMAGE》

・Main contrast & Sub contrast



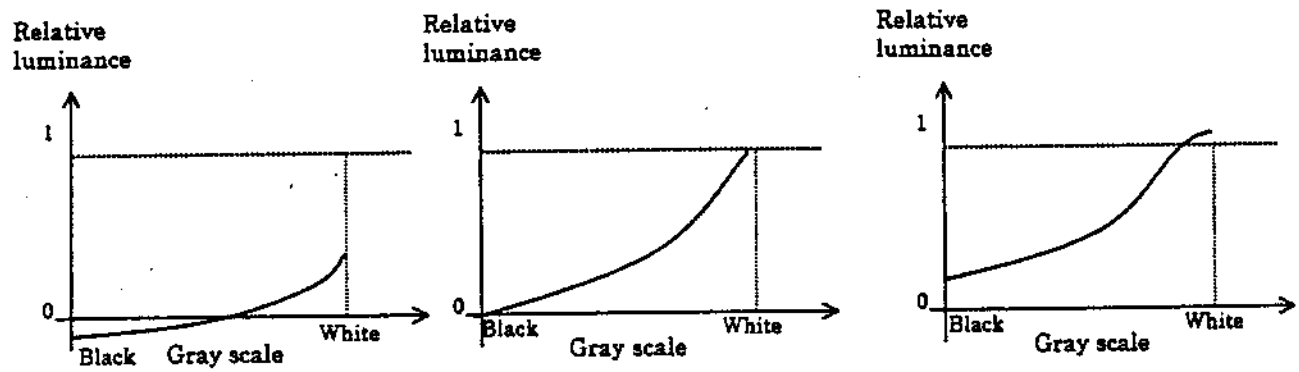
Main contrast

MAX ◄——— DEFAULT ———► MIN

Sub contrast

MAX ◄——— DEFAULT ———► MIN

・Sub brightness



Sub brightness

MIN ◄——— DEFAULT ———► MAX

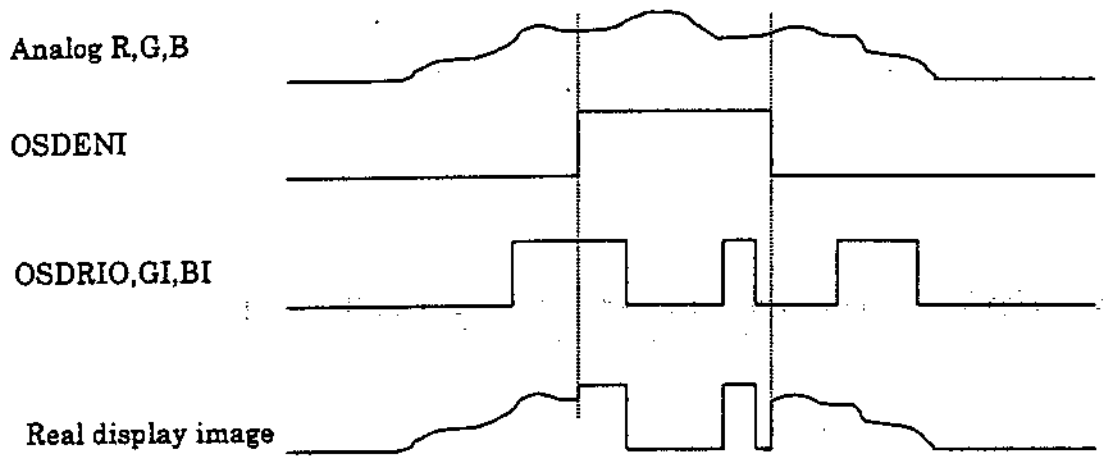
7.8.5. OSD FUNCTION

OSD (On Screen Display) is the function to display the other digital data on the input analog input data. Possible to display 1 bit data for each R/G/B color (8 colors). OSD valid for the period of OSDENI

OSDRI, OSDGI, OSDBI: digital data for OSD
OSDENI="H": OSD signal is valid
OSDENI="L": OSD signal is not valid

OSD is the sub-display for function-control and the display quality will be not guarantee. Please adopt the OSD image evaluating display quality.

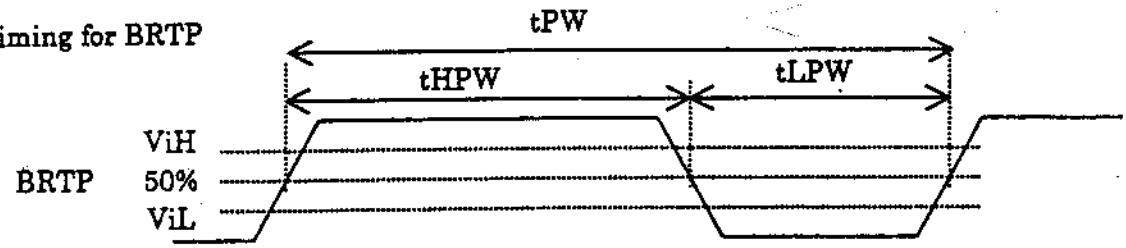
《OSD image》



7.8.6. OUTSIDE CONTROL FOR LUMINANCE

Outside control is valid, when PWSEL="L" and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.
Duty=100%: luminance is maximum.
Duty=20%: luminance is minimum.

Timing for BRTP



Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Frequency	1/tPW	185	–	340	Hz	–
Pulse-width	tHPW/tPW	20	–	100	%	at max. luminance (100%)
Input voltage	ViL	–	–	0.6	V	–
	ViH	4.5	–	–	V	–

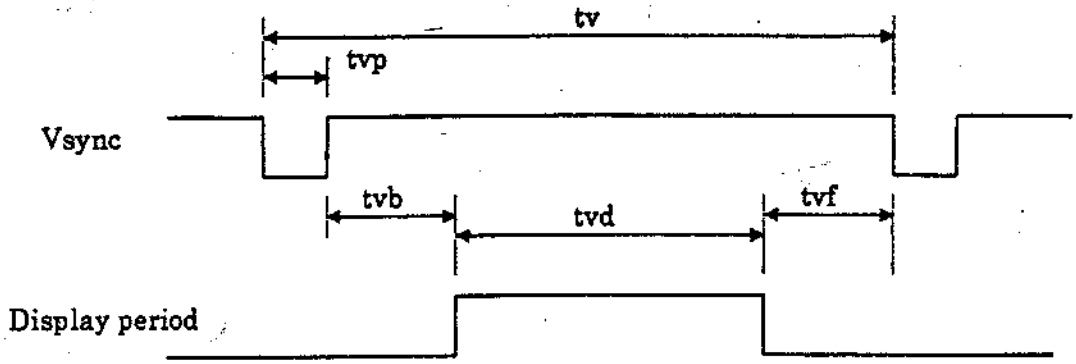
Regarding set up for frequency, please refer to the below method.
Set up frequency = Vsync frequency × (n+0.25) or (n+0.75)
Please adopt the frequency evaluating the display quality, because the display will be disturbed depend on frequency.

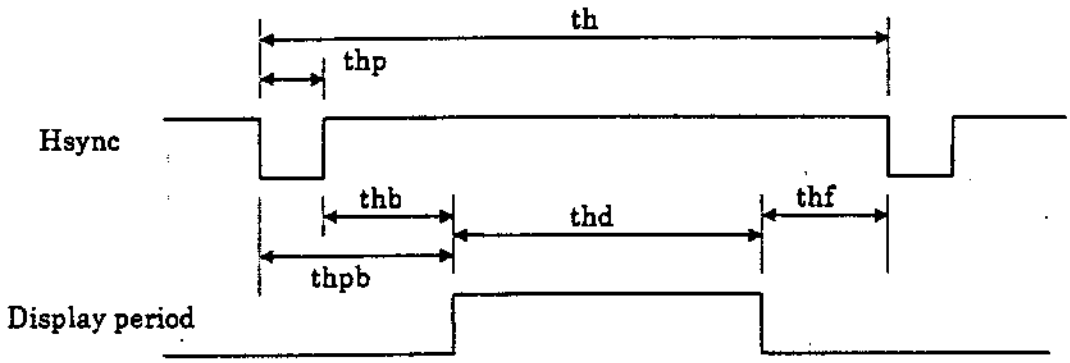
7.9. INPUT SIRIAL TIMINGS

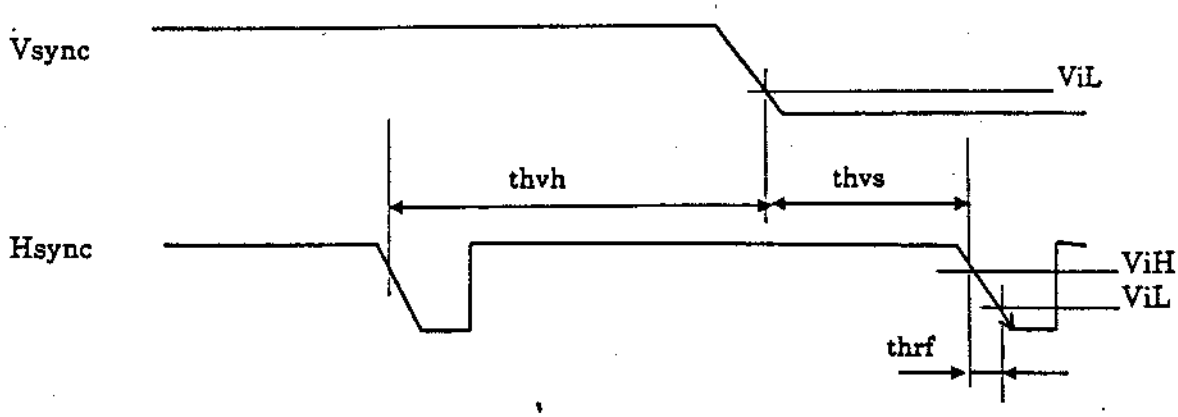
7.9.1. XGA MODE (STANDARD)

	Name	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK	Frequency	1/tc	52.0 —	65.0 15.385	80.0 —	MHz ns	XGA standard
	Rise / Fall	tcrf	—	—	10	ns	—
	Pulse-width	tcl/t c	0.4	0.5	0.6	—	—
Hsync	Period	th	16.0 —	20.677 1344	22.7 —	µs CLK	48.363kHz (typ.)
	Display	thd	— —	15.754 1024	— —	µs CLK	—
	Front-porch	thf	— 10	0.369 24	— —	µs CLK	—
	Pulse-width	thp	— 16	2.092 136	— —	µs CLK	—
	Back-porch	thb	1.0 44	2.462 160	— —	µs CLK	note1
	Pulse-width +Back-porch	thpb	1.8	—	—	µs	—
	Vsync — Hsync timing	thvh	3	—	—	CLK	—
		thvs	1	—	—	CLK	—
	Rise / Fall	thrf	—	—	10	ns	—
Vsync	Period	tv	13.3 —	16.665 806	18.5 —	ms H	60.004Hz (typ.)
	Display	tvd	— —	15.880 768	— —	µs H	—
	Front-porch	tvf	— 1	62.031 3	— —	µs H	—
	Pulse-width	tvp	— 2	124.06 6	— —	µs H	—
	Back-porch	tvb	— 5	599.63 29	— —	µs H	—
Analog R,G,B	—	tda	4	—	—	ns	—

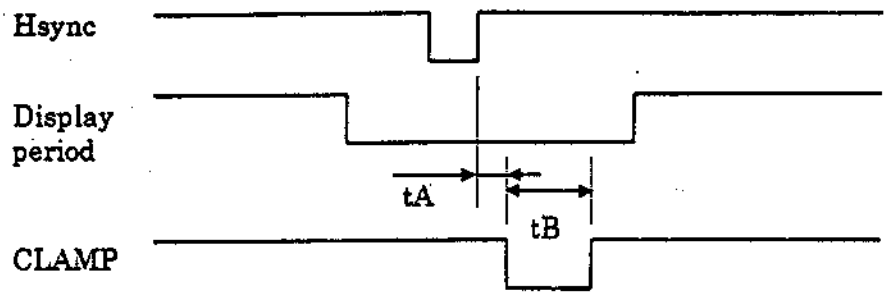
note1: Minimum values of Back-porch (thb) must be satisfied with both 1.0 µs and 44 CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
ViL
thvh
thvs
Hsync
ViH
ViL
thrf

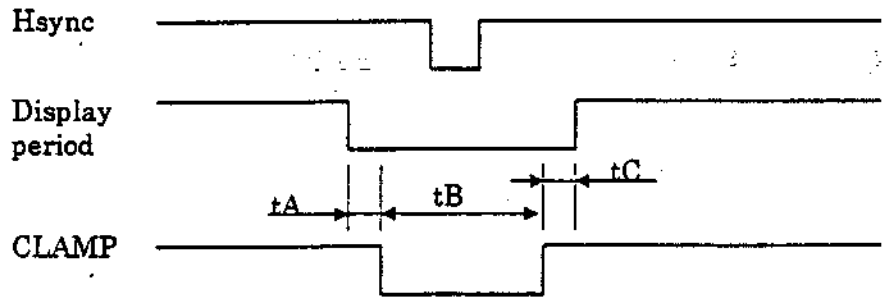
7.9.2. TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD2	tA [CLK]	tB [ns]
0	0	Prohibit	
0	1	2	27
1	0		20
1	1		15

note1: Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

7.9.3. TIMING FOR INPUTING CLAMP SIGNAL FROM OUTSIDE



Item	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	–	–	μs	–
tB	0.3	–	–	μs	–
tC	0.2	–	–	μs	–

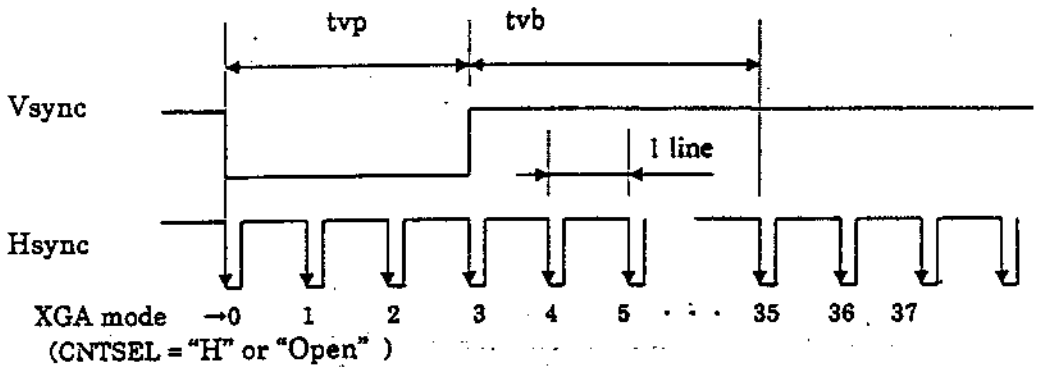
note 1: Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

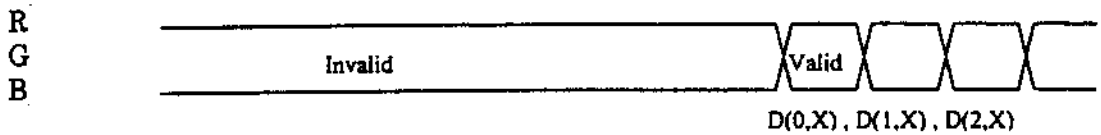
7.10.INPUT SIGNAL AND DISPLAY POSITION

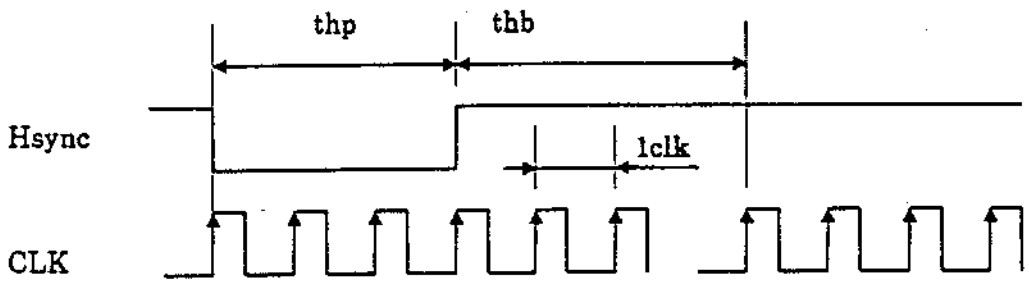
XGA standard timing

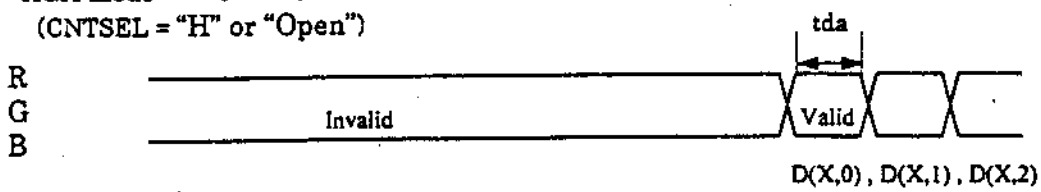
Pixels

D(0,0)	D(0,1)	D(0,2)	· · · · · ·	D(0.1023)
D(1,0)	D(1,1)	D(1,2)	· · · · · ·	D(1,1023)
D(2,0)	D(2,1)	D(2,2)	· · · · · ·	D(2,1023)
·	·	·		·
·	·	·		·
·	·	·		·
·	·	·		·
D(767,0)	D(767,1)	D(767,2)	· · · · · ·	D(767,1023)









note 1: tda should be more than 4ns

7.11. OPTICAL CHARACTERISTICS

(Ta = 25℃, VDD = 12V, VDDB = 12V) note 1

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio	CR	Perpendicular	TBD	150	—	—	note 2
Luminance	Lvmax	White	150	180	—	cd/m^2	—
Luminance uniformity	—	White	—	1.1	1.30	—	note 3

Reference data

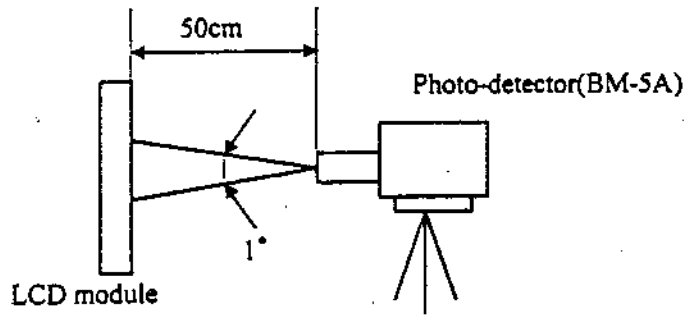
(Ta = 25℃, VDD = 12V, VDDB = 12V) note 1

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing angle range	θR	CR > 10, θU=0°, θD=0° white/black		70	85	—	deg.	note 4
	θL			70	85	—	deg.	
	θU	CR > 10, θR=0°, θL=0° white/black		70	85	—	deg.	
	θD			70	85	—	deg.	
Color gamut	C	at center, to NTSC		35	48	—	%	—
Luminance control range	—	Maximum luminance: 100%	ACA=L	—	30 to 100	—	%	—
			ACA=H		60 to 100			
Response time	Ton	black to white		—	44	80	ms	note 5
	Toff	White to black		—	47	80	ms	note 5

note 1: The luminance is measured after 20 minutes from the module works, with all pixels in "white". The typical value is measured after luminance saturation.
Display mode: VESA XGA-75Hz
RGB input voltage: 0.7Vp-p
Contrast: Default value

note 2: The contrast ratio is calculated by using the following formula.

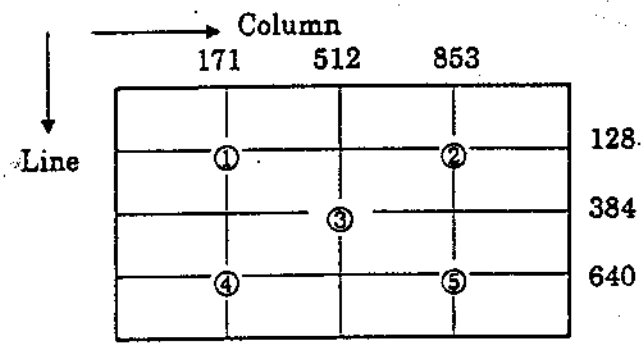
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$



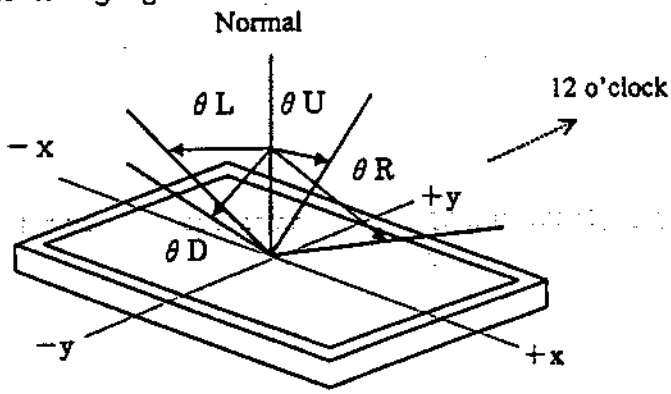
note 3: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

The luminance is measured at near the five points shown below.

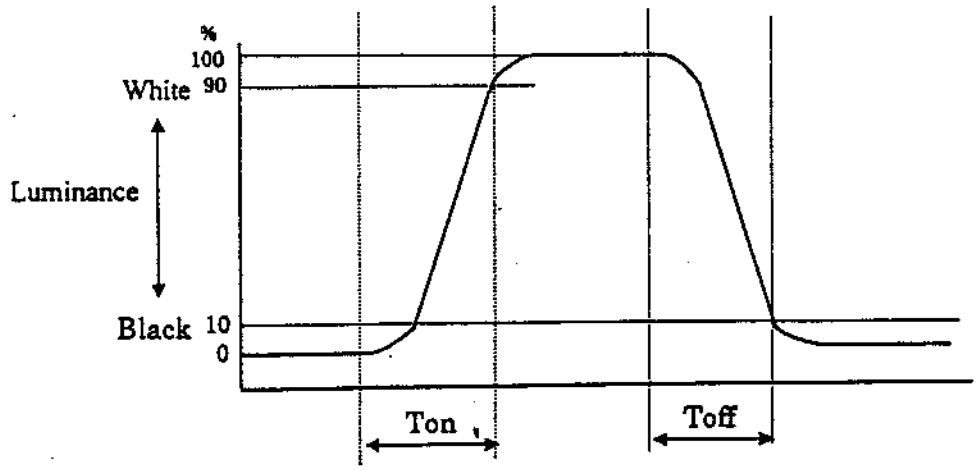


note 4: Definitions of viewing angle are as follows.



note 5: Definitions of response time is as follows.

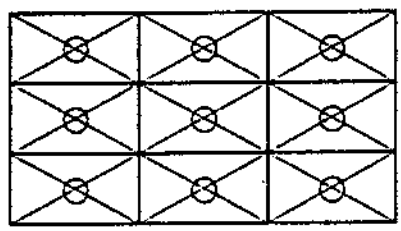
Photo-detector output signal is measured when the luminance changes " black " to " white " and " white " to " black ". Response time are Ton and Toff of the photo-detector output amplitude. Ton is the time between 0% and 90%. Toff is the time between 100% and 10%.



7.12. RELIABILITY TEST

Test item	Test condition	Judgment
High temperature/humidity operation	50±2℃, 85% relative humidity 240 hours, Display data is black.	*1
Heat cycle (operation)	① 0℃±3℃···1 hour 55℃±3℃···1 hour ② 50 cycles , 4 hours/cycle ③ Display data is black.	*1
Thermal shock (non-operation)	① -20℃±3℃···30 minutes 60℃±3℃···30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	*1
Vibration (non-operation)	① 5-100Hz, 2G 1 minute/cycle, X,Y,Z direction ② 50 times each direction	*1, *2
Mechanical shock (non-operation)	① 55G, 11ms X,Y,Z direction ② 3 times each direction	*1, *2
ESD (operation)	150pF, 150Ω, ±10KV 9 places on a panel *3 10 times each place at one-second intervals	*1
Dust . (operation)	15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	*1

*1: Display function is checked by the same condition as LCD module out-going inspection.
*2: Physical damage
*3: Discharge points are shown in the figure.



8.GENERAL CAUTIONS

Because next figures and sentence are very important, please understand these contents as follows.

⚠CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

 CAUTION

Do not touch an inverter --on which is stuck a caution label-- while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module

① Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

②

 As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.

⑧The torque to mounting screw should never exceed 0.392 N·m (4 Kgf·cm) .

(3) Cautions for the atmosphere

①Dew drop atmosphere should be avoided.

②Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

③This module uses cold cathode fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.

④Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

①Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(5) Other cautions

① Do not disassemble and/or reassemble LCD module.

② Do not readjust variable resistor or switch etc.

③ When returning the module for repair or etc., please pack the module not to be broken. We recommend to the original shipping packages.

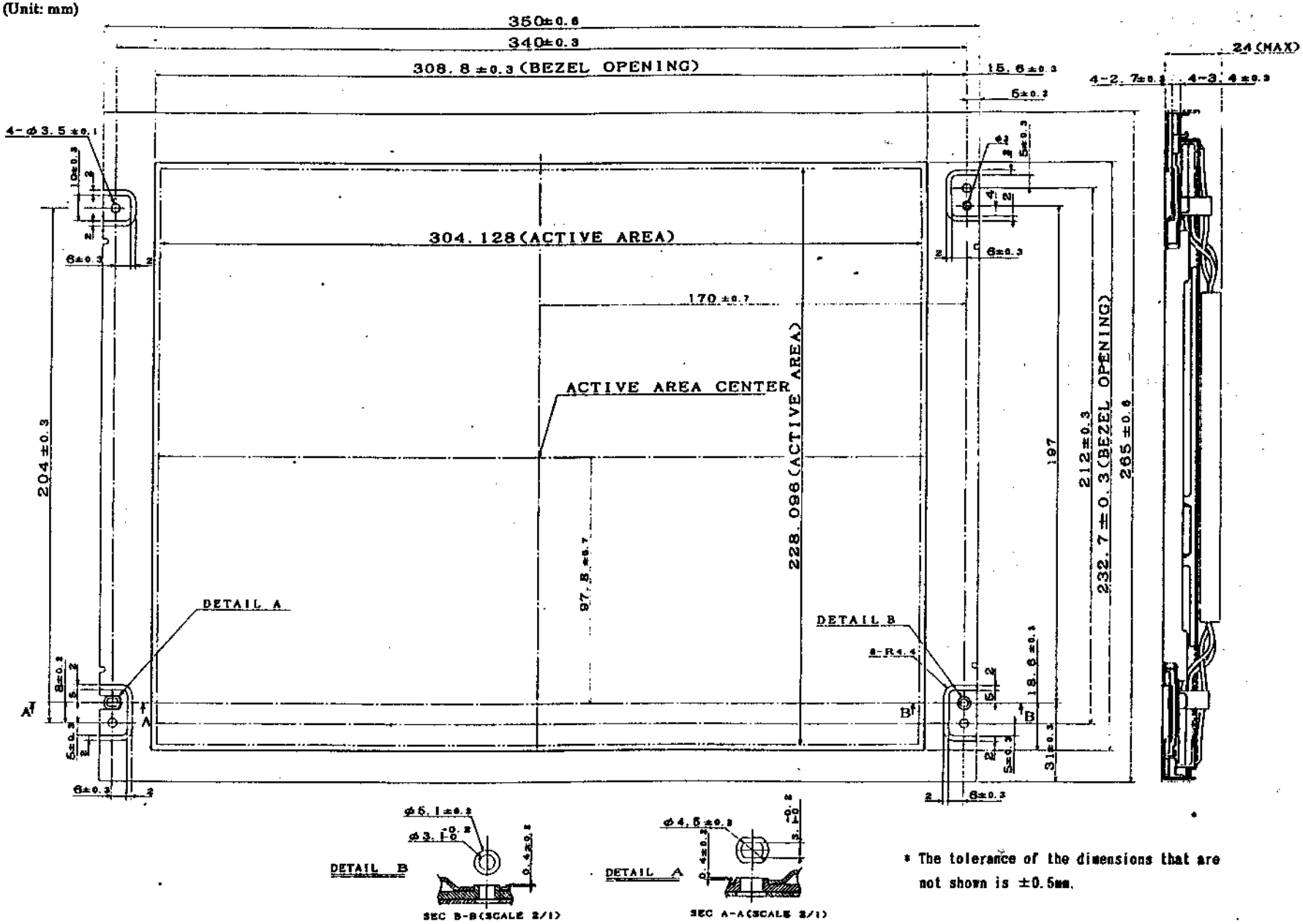
Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

The display condition of LCD module may be affected by the ambient temperature.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

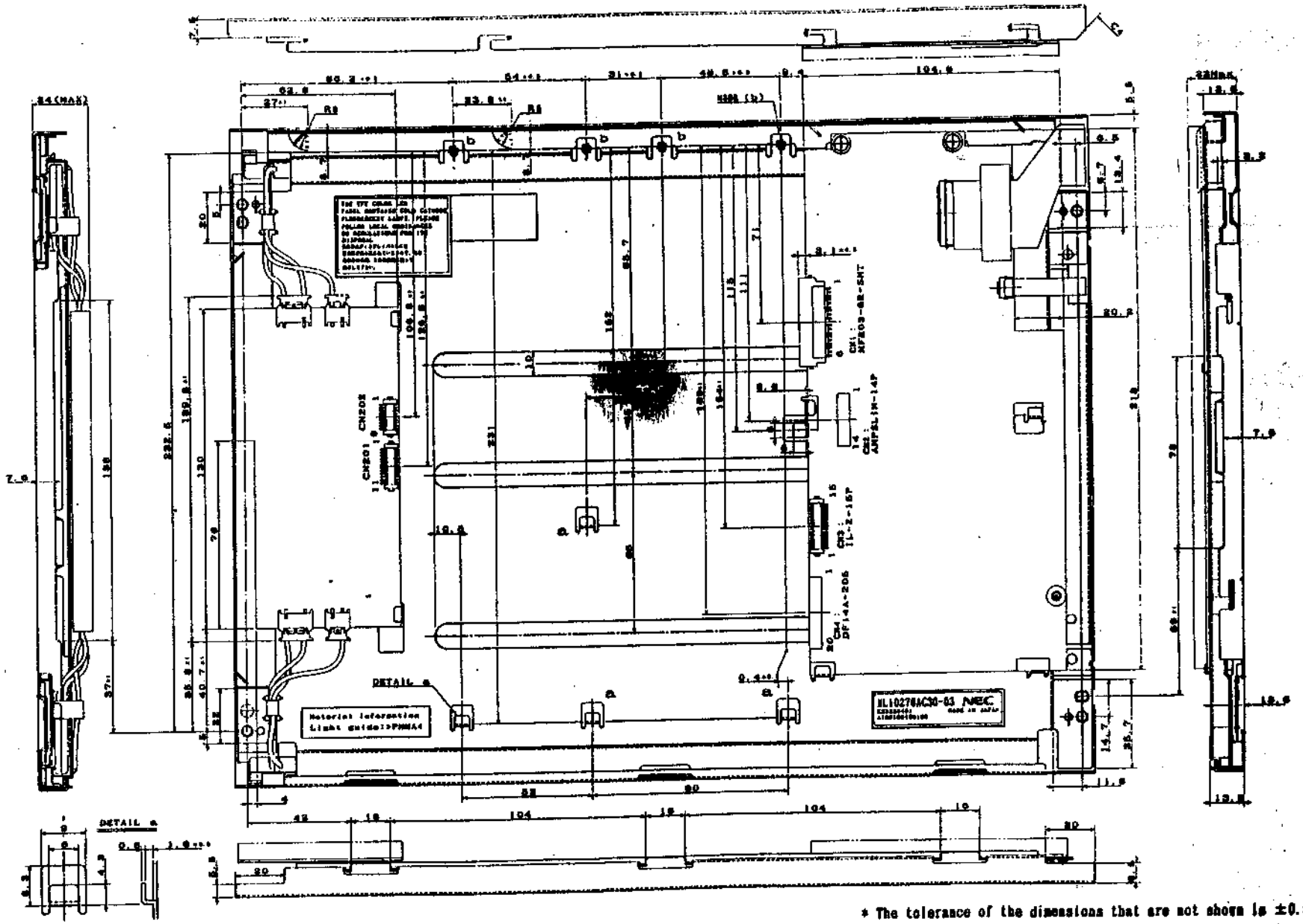
9. OUTLINE DRAWINGS

9.1 Front view (Unit: mm)



* The tolerance of the dimensions that are not shown is ±0.5mm.

9.2 Rear view



* The tolerance of the dimensions that are not shown is ±0.5mm.

Revision History

Rev.	Prepared date	Revision contents	Approved	Checked	Prepared	Issued date
1	Jun. 10, 1998	DOD-H6466			T. Kusanagi M. Yoshida	