NEC

TFT COLOR LCD MODULE

Type: NL10276BC28-21F
36cm (14.1 Type), XGA
LVDS interface (1 port)

SPECIFICATIONS

(First Edition)

PRELIMINARY

This document is preliminary. All information in this document is subject to change without prior notice.

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CONTENTS

1. DESCRIPTION

NL10276BC28-21F is a TFT (thin film transistor) active matrix color liquid crystal display(LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276BC28-21F has a built-in backlight.
The 36cm(14.1 Type) diagonal display area contains 1024×768 pixels and can display 262,144 colors simultaneously.

2. FEATURES

- Mounting structure of rear screw type
- Module thickness: 5.4mm (Typ.)
- High luminance (160 cd/m^2 at IL= 6mArms)
- Expanded screen size without increasing the frame area
- LVDS interface (adapted THC63LVDF64A, THine Electronics, Inc. as a receiver core with timing controller)
- Supply voltage: 3.3V
- Incorporated edge type backlight (One lamp, Inverter-less)

3. APPLICATIONS

- Note PC

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.
RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.
Acting as an Electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	285.696 (H) × 214.272 (V) mm
Drive system	a-Si TFT active matrix
Display colors	262,144 colors
Number of pixels	1024 × 768
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.279 (H) × 0.279 (V) mm
Module size	298.0 (H) × 225.5 (V) × 5.4 (D) Typ. mm
Weight	530 g (Typ.)
Contrast ratio	150:1 (Typ.)

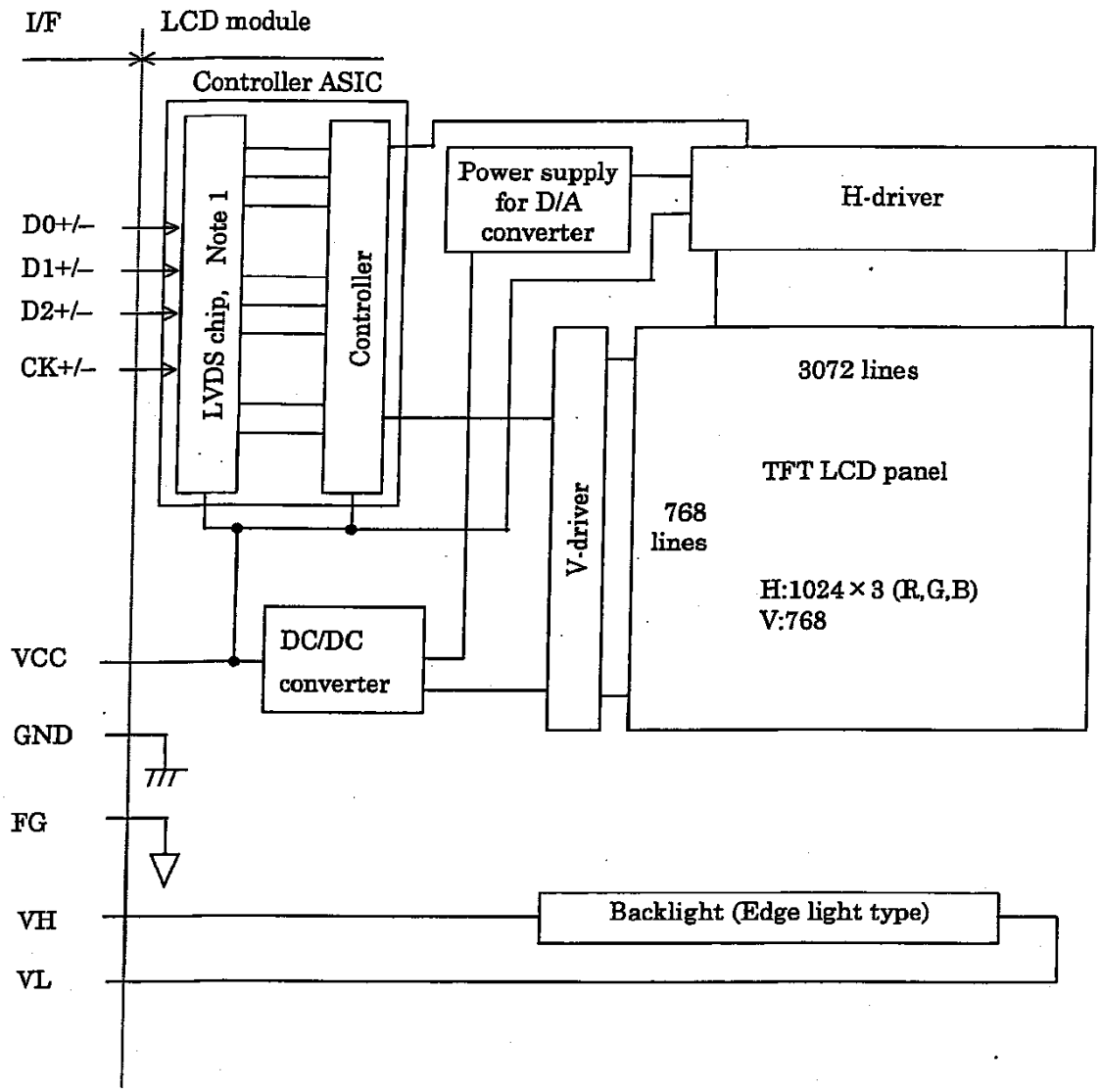
Viewing angle (more than the contrast ratio of 10:1)
- Horizontal: 50 ° (Typ. , left side, right side)
- Vertical: 20 ° (Typ. , up side), 40 ° (Typ., down side)

Designed viewing direction

· Wider viewing angle without image reversal:	up side (12 o'clock)
· Best contrast angle:	5 ° (down side, 6 o'clock)
· Optimum grayscale (γ =2.2):	Perpendicular

Pencil hardness	3 H (Min. JIS K5400)
Color gamut	40 % (Typ. At center, To NTSC)
Response time	15 ms (Typ.), "white" to "black"
Luminance	160cd/m^2 (Typ. at IL= 6.0mArms)
Signal system	LVDS interface (Receiver:THC63LVDF64A core, THine Electronics, Inc.) RGB 6-bit signals, Synchronous signals (Hsync, Vsync), Data enable signal(DE) and dot clock(CLK) encoded with THC63LVDF63A (THine Electronics, Inc.) are preferable.
Supply voltage	3.3 V for Logic and LCD driving
Backlight	Edge light type: One cold cathode fluorescent lamp in a holder, Inverter-less
Power consumption	5.0 W (Typ. at 160 cd/m^2)

6. BLOCK DIAGRAM



Note 1: THC63LVDF64A core (THine)
Note 2: GND is not connected to FG(Frame Ground) in the module.
These grounds should be connected in customer equipment.

7. GENERAL SPECIFICATIONS

Items	Specifications	Unit
Module size	298.0±0.5 (H) × 225.5±0.5 (V) × 5.7 Max.(D) Note 1	mm
Display area	285.696 (H) × 214.272 (V) 【 Diagonal display area: 36cm (Type: 14.1) 】	mm
Number of pixels	1024 (H) × 768 (V)	pixel
Dot pitch	0.093 (H) × 0.279 (V)	mm
Pixel pitch	0.279 (H) × 0.279 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	262,144 (RGB 6-bit each)	color
Weight	530 (Typ.) , 560 (Max.)	g

Note 1: Lamp cable and sealing tape are excepted.

8. ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Ratings	Unit	Remarks
Supply voltage	VCC	-0.3 to +4.0	V	Ta = 25℃
Logic input voltage	VI	-0.3 to VCC+0.3	V	
Lamp voltage	VL	2000	Vrms	
Storage temperature	Tst	-20 to +60	℃	–
Operating temperature	Top	0 to +50	℃	Module surface Note 1
Relative humidity (RH) Note 2		≤ 95	%	Ta≤40℃
		≤ 85	%	40℃ < Ta≤50℃
Absolute humidity Note 2		Absolute humidity shall not exceed Ta=50℃, RH= 85%	g/m³	Ta > 50℃

Note 1: Measured at the display area (including self heat)
Note 2: No condensation

9. ELECTRICAL CHARACTERISTICS

(1) Logic/ LCD driving

Ta = 25℃

Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VCC	3.0	3.3	3.6	V	–
Ripple voltage	Vrp	–	–	100	mV	for VCC
LVDS signal input "L" voltage	ViL	-100	–	–	mV	VCM=1.2V VCM: Common mode voltage in LVDS driver
LVDS signal input "H" voltage	ViH	–	–	+100	mV	
Terminating resistor	Rt	–	100	–	Ω	–
Supply current	ICC	–	320 Note 1	650 Note 2	mA	VCC=3.3V

Note 1: Checker flag pattern (in EIAJ ED-2522)
Note 2: Theoretical maximum current pattern

(2) Backlight

Ta = 25℃

Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
Lamp current	IL	2.0	—	6.0	mArms	IL=6.0 mArms: 150 cd/cm^2 Note 2
Lamp voltage	VL	—	675	—	Vrms	IL= 6.0 mArms
Lamp turn on voltage	VS	1300	—	—	Vrms	Ta=0℃ Note 2
		900	—	—		Ta=25℃ Note 2
Oscillator frequency	Ft	50	60	—	kHz	Note 1

Note 1: Recommended value of "Ft"

- Ft is within the specification.
- $Ft = \frac{1}{4th} \times (2n-1)$

th: Hsync period
n: a natural number (1,2,3,・・・・)

If Ft is out of the recommended value, interference between Ft frequency and Hsync frequency may cause beat on the display.

Note 2:When VS and IL are less than Min. value, the lamp might be not turned on it.

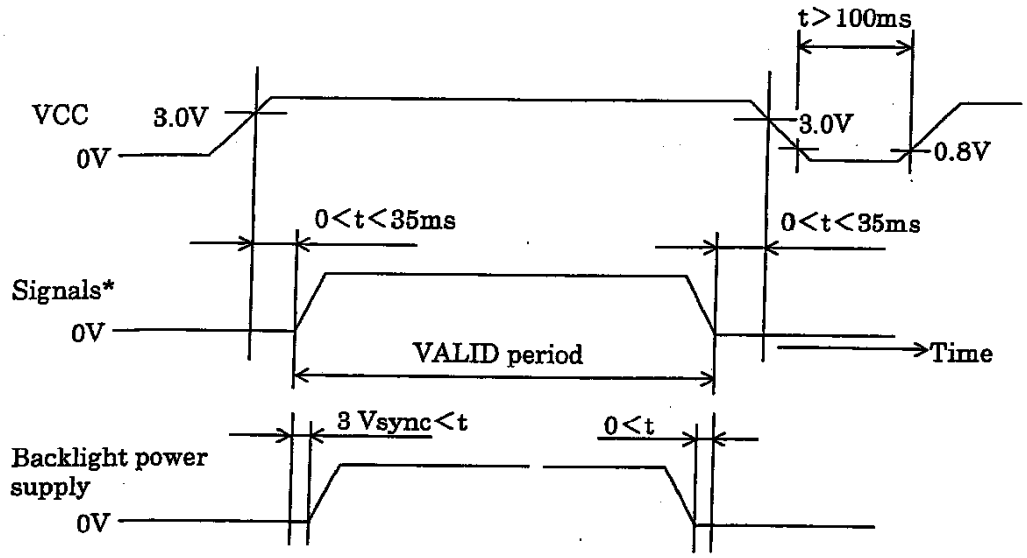
(3)Fuse

This LCD module uses a fuse as follows.

Supply voltage	Part No.	Supplier	Ratings	Remarks
VCC	KAB2402132	MATSUO ELECTRIC Co., Ltd	1.3A	—

Note 1: Before the power is designed, the fuse should be considered. The power capacity should be used more than 2.0 times of the fuse rating.
In case of small power capacity calculated above, the module must be evaluated enough from safety point of view.

10. POWER SUPPLY SEQUENCE



*Signals: Hsync, Vsync, CLK, DE, R0-R5, G0-G5, B0-B5

Note 1: The supply voltage for input signals should be the same as VCC.
Note 2: Turn on the backlight within the LCD operation period. When the backlight turns on before LCD operation or the LCD operation turns off before the backlight turns off, the display may momentarily become white.
Note 3: When the power is off, keep whole signals (Hsync, Vsync, CLK, DE, R0-R5, G0-G5, B0-B5) low level or high impedance.
Note 4: Wrong power sequence may damage the module.
Note 5: The signal should not be down during operation. Even if the signal could recover, LCD module can not be operated correctly, the display may be un-uniformity. In case signal is down, VCC should be turned off, and then turn VCC and signal on as above sequence.

11. INTERFACE PIN CONNECTIONS

(1) Interface connector for signals and power

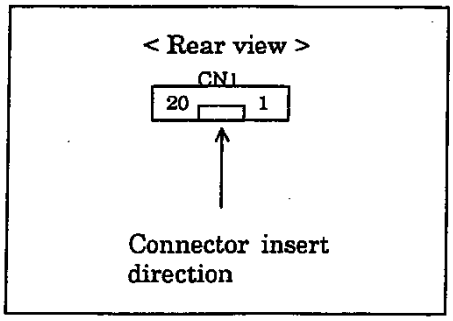
Part No. : FI-AB20S-HF
Adaptable socket : FI-A20M or FI-A20H
Supplier : Japan Aviation Electronics Industry Limited (JAE)

CN1

Pin No.	Symbols	Signal type	Function
1	VCC	Power supply	Supply +3.3V
2	VCC		
3	GND	Ground	Note 1
4	GND		
5	D0-	Pixel data etc.	LVDS differential data input Note 2
6	D0+		
7	GND	Ground	Note 1
8	D1-	Pixel data etc.	LVDS differential data input Note 2
9	D1+		
10	GND	Ground	Note 1
11	D2-	Pixel data etc.	LVDS differential data input Note 2
12	D2+		
13	GND	Ground	Note 1
14	CK-	Pixel clock	CLK for pixel data f=65MHz (Typ.) (LVDS level) Note 2
15	CK+		
16	GND	Ground	Note 1
17	N.C.	Non-connection	–
18	N.C.		
19	GND	Ground	Note 1
20	GND		

Note 1: GND is signal ground for logic and LCD driving. GND is not connected to FG(Frame Ground) in the module. These grounds should be connected in customer equipment.
Note 2: Use 100Ω twist pair wires for the cable.
Remark: Do not keep pins free (except 17 and 18) to avoid noise issue.

CN1: Figure from socket view



(2) Connector for backlight unit

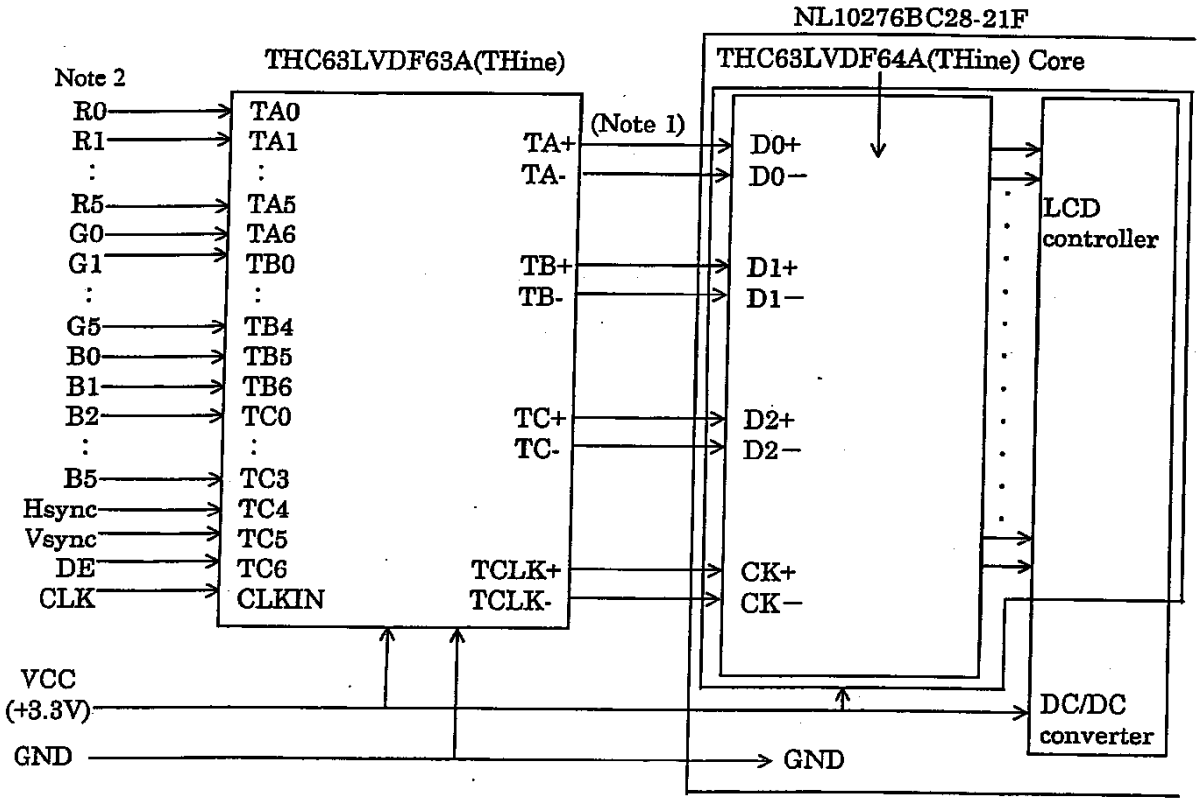
Part No. : BHSR-02VS-1
Adaptable socket : SM02B-BHSS-1
Supplier : J.S.T. TRADING COMPANY, LTD.

CN2

Pin No.	Symbols	Function
1	VH	High voltage terminal (The cable color is white)
2	VL	Low voltage terminal

Note 1: VH and VL must be connected correctly. If you connect wrongly, you will get hurt and the module will be broken.

12. METHOD OF CONNECTION FOR LVDS chip



Note 1: 100Ω twist pair
Note 2: These signals should be kept in the specified range of **14. INPUT SIGNAL TIMINGS.**

13. DISPLAY COLORS vs INPUT DATA SIGNALS

Display colors		Data signal(0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note 1: Colors are developed in combination with 6-bit signals (64 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 262,144 (64 × 64 × 64) colors.

14. INPUT SIGNAL TIMINGS

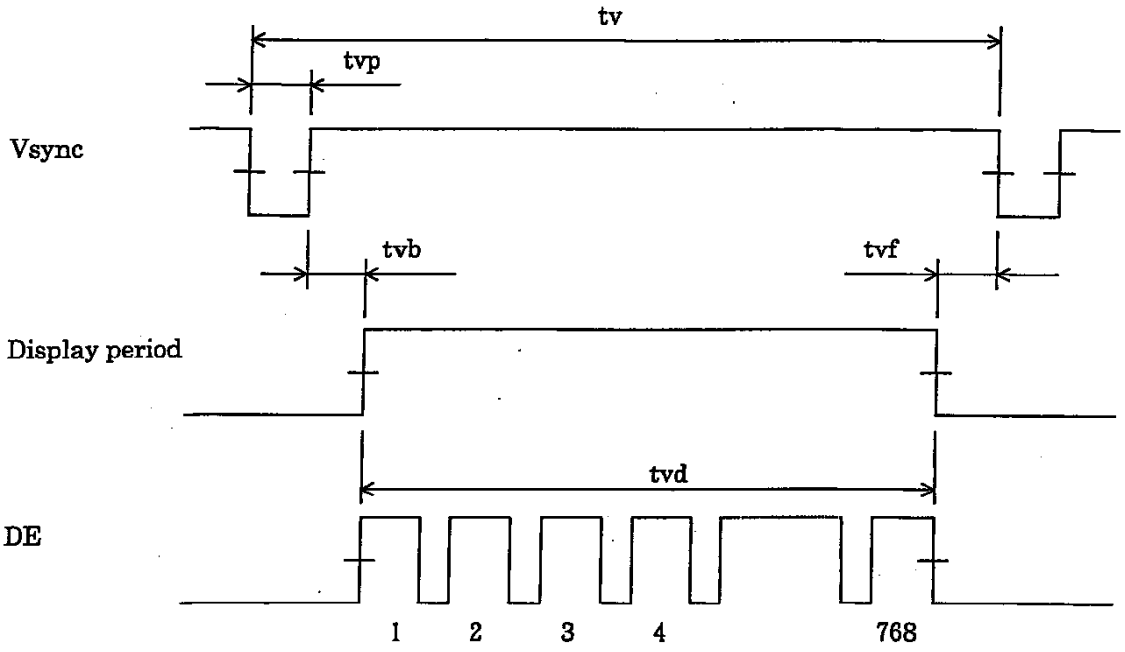
(1) Input signal specification for LCD controller

	Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/tc	60.0	65.0	67.0	MHz	15.384ns (Typ.)
	Duty	tch/tc	Note 1			—	—
	Rise, fall	tcrf				ns	
Hsync	Period	th	—	20.676	—	μs	48.363kHz (Typ.)
				1344		CLK	
	Display period	thd	1024			CLK	—
	Front-porch	thf *	1	40	—	CLK	—
	Pulse width	thp *	2	208	—	CLK	—
	Back-porch	thb *	1	72	—	CLK	—
	* thf + thp + thb		81	320	1023	CLK	—
	Hsync-CLK timing	ths	Note 1			ns	—
	CLK-Hsync timing	thh				ns	
	Rise, fall	thrf				ns	
Vsync	Period	tv	—	16.666	—	ms	60.00Hz (Typ.)
				806		H	
	Display period	tvd	768			H	—
	Front-porch	tvf *	1	3	—	H	—
	Pulse width	tvp *	1	—	—	H	—
	Back-porch	tvb *	1	33	—	H	—
	* tvf + tvp + tvb		4	38	—	H	—
	Vsync-Hsync timing	tvs	Note 1			ns	—
	Hsync-Vsync timing	tvh				CLK	
	Rise, fall	tvrf				ns	
DATA	DATA-CLK (Set up)	tds	Note 1			ns	—
	CLK-DATA (Hold)	tdh				ns	
DE	DE-CLK timing	tes				ns	
	CLK-DE timing	teh				ns	
	Rise, fall	terf				ns	

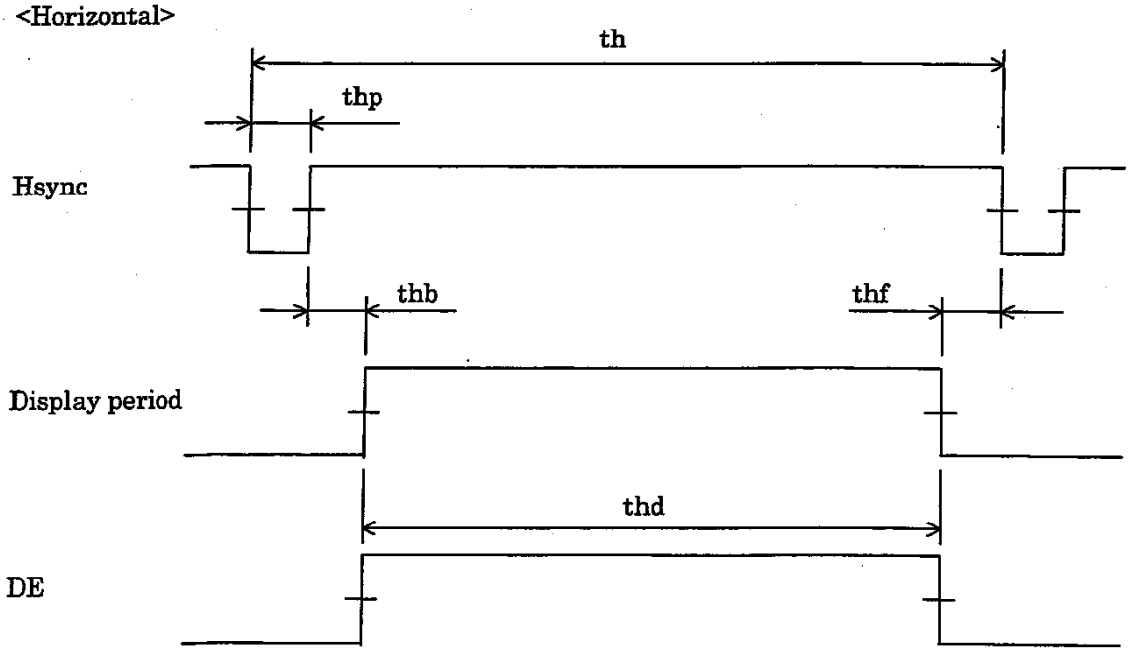
Note: These values are specified at the inputs of THC63LVDF63A.
(Refer to **12. METHOD OF CONNECTION FOR LVDS chip**)

(2) Definition of input signal timing for LCD controller

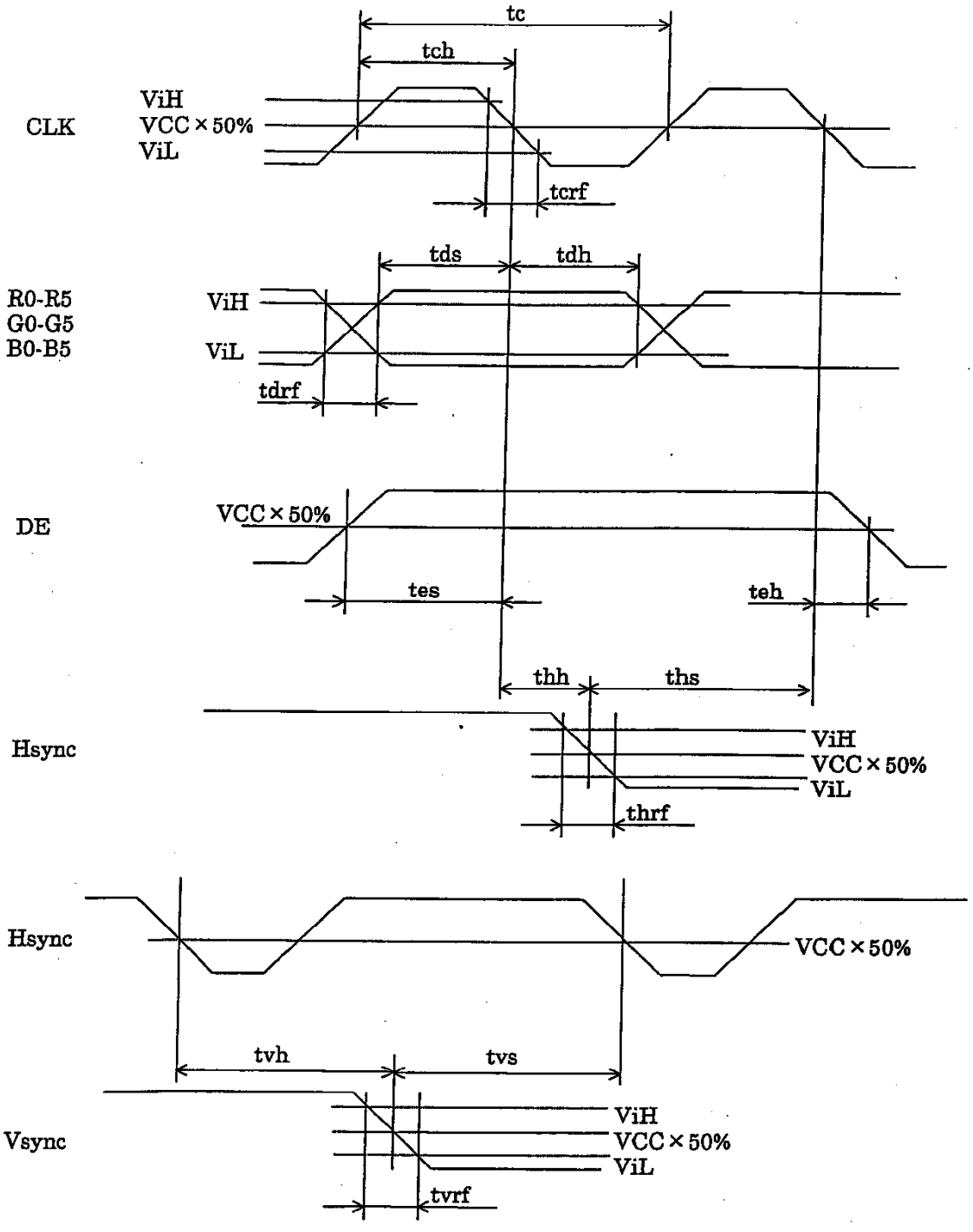
<Vertical>



<Horizontal>

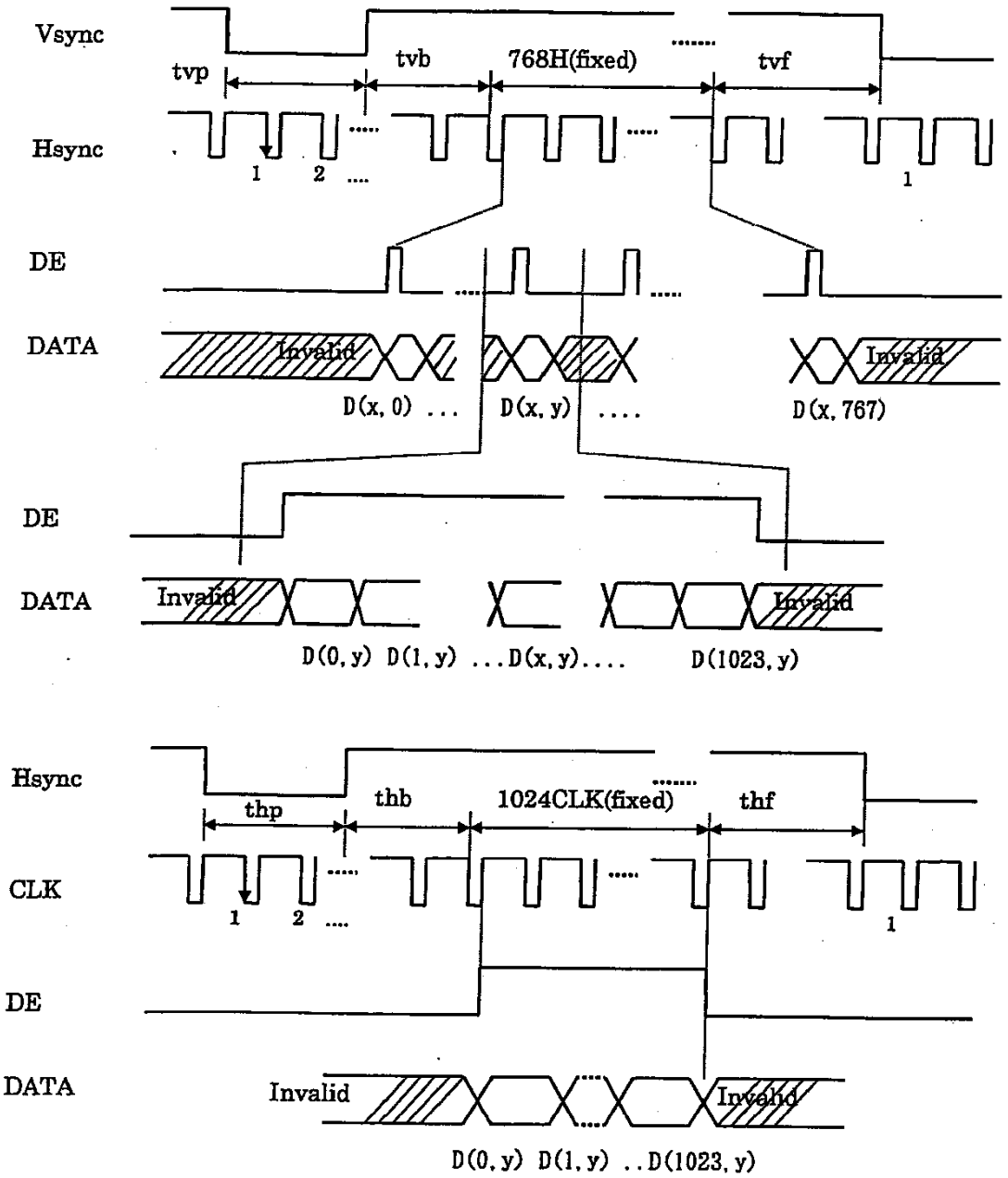


Note 1: "Display period" do not exist as signals.
Note 2: These values are specified at the inputs of THC63LVDF63A.
(Refer to **12. METHOD OF CONNECTION FOR LVDS chip**)



ViH = VCC × 0.7(Min.)
ViL = VCC × 0.3(Max.)

(3) Input signal timing chart for LCD



Note 1: These values are specified at the inputs of THC63LVDF63A.
(Refer to **12. METHOD OF CONNECTION FOR LVDS chip**).

(4) Display positions of input data

D(0, 0)	D(1, 0)	•••	D(X, 0)	•••	D(1023, 0)
D(1, 0)	D(1, 1)	•••	D(X, 1)	•••	D(1023, 1)
⋮	⋮	⋮	⋮	⋮	⋮
D(0, Y)	D(1, Y)	•••	D(X, Y)	•••	D(1023, Y)
⋮	⋮	⋮	⋮	⋮	⋮
D(0,767)	D(1,767)	•••	D(X,767)	•••	D(1023,767)

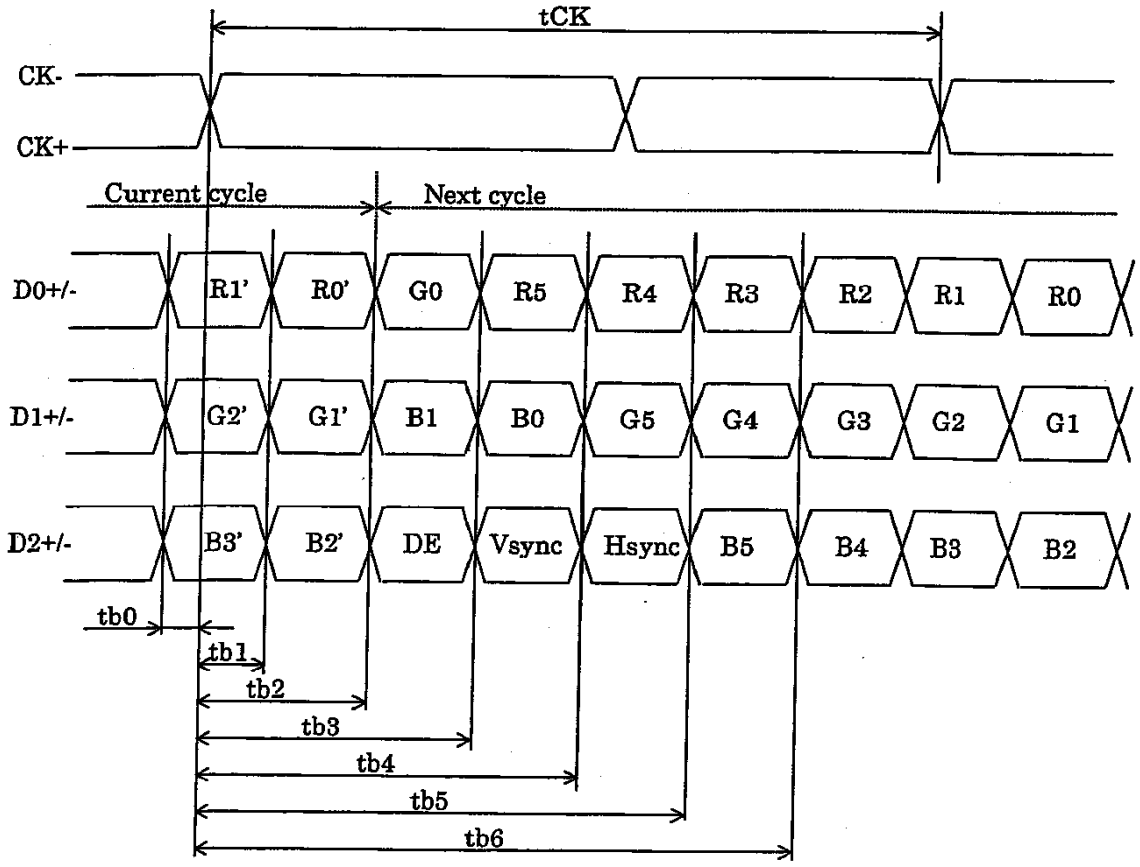
15. FOR LVDS RECEIVER

(1) Input signal specifications

Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
CLK Frequency	tCK	14.71	15.38	16.66	ns	—
Bit0 position	tb0	-0.5	0	0.5	ns	tck=15.38ns
Bit1 position	tb1	1/7tck-0.5	1/7tck	1/7tck+0.5	ns	tck=15.38ns
Bit2 position	tb2	2/7tck-0.5	2/7tck	2/7tck+0.5	ns	tck=15.38ns
Bit3 position	tb3	3/7tck-0.5	3/7tck	3/7tck+0.5	ns	tck=15.38ns
Bit4 position	tb4	4/7tck-0.5	4/7tck	4/7tck+0.5	ns	tck=15.38ns
Bit5 position	tb5	5/7tck-0.5	5/7tck	5/7tck+0.5	ns	tck=15.38ns
Bit6 position	tb6	6/7tck-0.5	6/7tck	6/7tck+0.5	ns	tck=15.38ns
—	SKRM	490	—	—	ps	—

Note 1: See the specifications of LVDS manufactures for detailed design.
In case that CLK jitter value between current cycle and next cycle is big, skew time of the next cycle decreases with the value of the jitter.
CLK jitter+LVDS output skew + cable skew ≦ 500ps
e. q. LVDS output skew: ±200ps
Cable skew: ±100ps
} acceptable CLK jitter ±200ps (500-(200+100) = 200ps)

(2) Input signal timing chart



16. OPTICAL CHARACTERISTICS

(Ta = 25℃, VCC = 3.3V,IL = 6.0 mArms)

Items	Symbols	Condition		Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	θx±=0°, θy±=0°, White/Black, at center		80	150	—	—	Note 1
Luminance	Lvmax	White, at center (IL=6.0 mArms)		135	160	—	cd/m²	Note 2 Note 3
Luminance uniformity	—	White		—	—	1.40	—	Note 2 Note 3
Chromaticity coordinate	—	White (x,y), at center	x	0.310	0.340	0.370	—	Note 2
			y	0.320	0.350	0.380		

Reference data

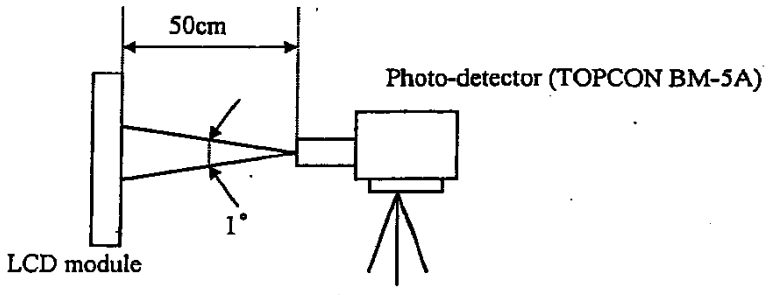
(Ta = 25℃, VCC = 3.3V, IL = 6.0 mArms)

Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	Best contrast angle, θx+=0°, θx-=0°, θy-=5°, White/Black, at center	—	300	—	—	—
Viewing angle range (CR>10)	θ x+	CR > 10, θy+=0°, θy-=0° White/Black, at center	30	50	—	deg.	Note 4
	θ x-		30	50	—	deg.	
	θ y+	CR > 10, θx+=0°, θx-=0° White/Black, at center	10	20	—	deg.	
	θ y-		30	40	—	deg.	
Color gamut	C	θx±=0°, θy±=0°, at center, to NTSC	35	40	—	%	—
Response time	Ton	White to Black	—	15	40	ms	Note 5
	Toff	Black to White	—	50	70		

Note 1: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

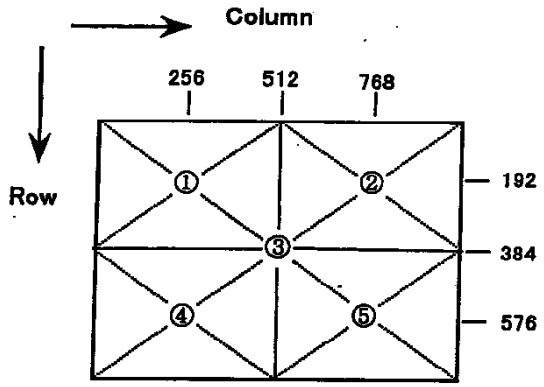
Note 2: The luminance is measured after 20 minutes from the module works, with all pixels in "white". The typical value is measured after luminance saturation, more than one hour after burn-in.



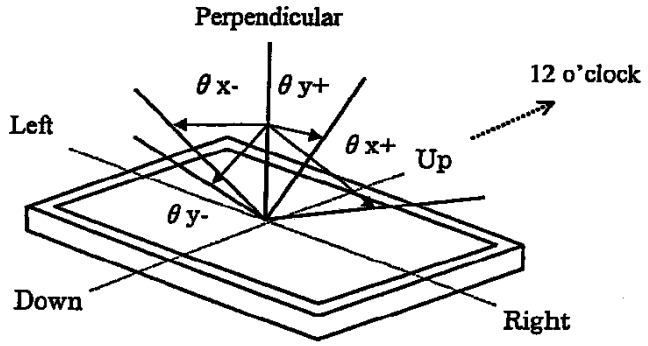
Note 3: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

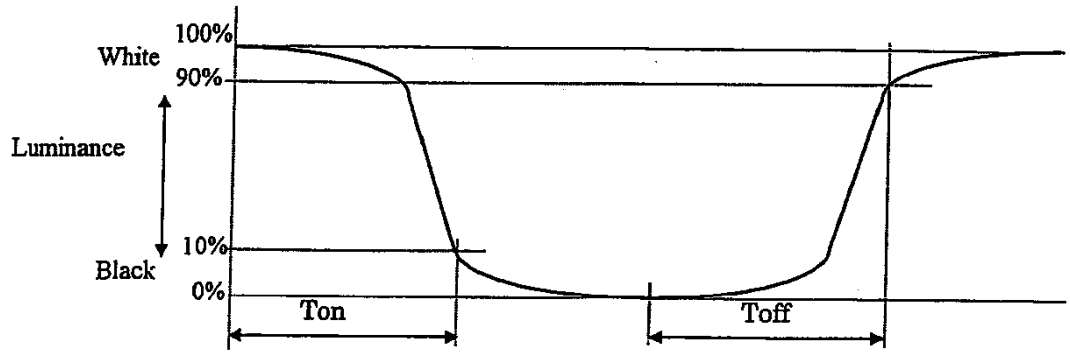
The luminance is measured at near the five points shown below.



Note 4: Definitions of viewing angle are as follows.



Note 5: Definitions of response time are as follows.
Photo-detector output signal is measured when the luminance changes "white" to "black" or "black" to "white".



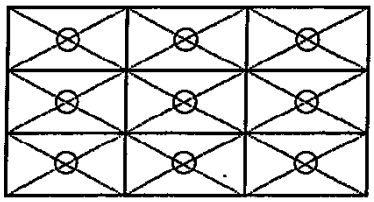
17. RELIABILITY TEST

Test items	Test condition	Judgment
High temperature/humidity operation	50±2℃, RH= 85% 240 hours, Display data is white.	*1
Heat cycle (operation)	① 0℃±3℃···1 hour 55℃±3℃···1 hour ② 50 cycles , 4 hours/cycle ③ Display data is white.	*1
Thermal shock (non-operation)	① -20℃±3℃···30 minutes 60℃±3℃···30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	*1
Vibration (non-operation)	① 5-100Hz, 19.6m/s^2 (2G) 1 minute/cycle, X,Y,Z direction ② 120 times each direction	*1, *2
Mechanical shock (non-operation)	① 490m/s^2 (50G), 11ms X,Y,Z direction ② 5 times each direction	*1, *2
ESD (operation)	150pF, 150Ω, ±10kV 9 places on a panel *3 10 times each place at one-second intervals	*1
Dust (operation)	15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	*1

*1: Display function is checked by the same condition as LCD module out-going inspection.

*2: Physical damage

*3: Discharge points are shown as follow.



18. GENERAL CAUTIONS

Because next figures and sentences are very important, please understand these contents as follows.

⚠ **CAUTION**	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

This figure is a mark that you will get hurt when you make a mistake to operate.

⚠ CAUTIONS

(1) A caution when taking out the module

① Pick a pouch only, when taking out the module from the carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges. Peel protection sheet out from the LCD panel surface as slowly as possible.

② As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

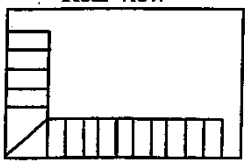
⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one or more of these signals is lost, the LCD panel would be damaged.

⑧ The LCD module should be mounted in strong body such as magnesium alloy. If the press or twist are added to the module, the display may have un-uniformity image. When the module is mounted to customer chassis, please evaluate the display condition carefully.

⑨ Be careful not to touch the sheet at handling because only a thin transparency seat is put on the printed circuit board.

Rear view



← A thin transparency sheet on the printed circuit board.

⑩ Do not push or rub the surface of LCD module.
If you do, the scratches or the marks like rubbing marks may be left on the surface of the module.

⑪ Do not give any stress to the interface connector.

(3) Cautions for the atmosphere

① Dew drop atmosphere must be avoided.

② Do not store and/or operate the LCD module in high temperature and/or high humidity atmosphere. Storage in an Electro-conductive polymer-packing pouch and in relatively low temperature atmosphere is recommended.

③ This module uses cold cathode fluorescent lamp. Therefore, the lifetime of lamp becomes short conspicuously at low temperature.

④ Do not operate the LCD module in high magnetic field.

(4) Caution for the module characteristics

① Do not apply any fixed pattern data signals to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(5) Other cautions

① Do not disassemble and/or reassemble LCD module.

② Do not readjust variable resistors nor switches etc.

③ When returning the module for repair or etc., pack the module not to be broken. We recommend the original shipping packages.

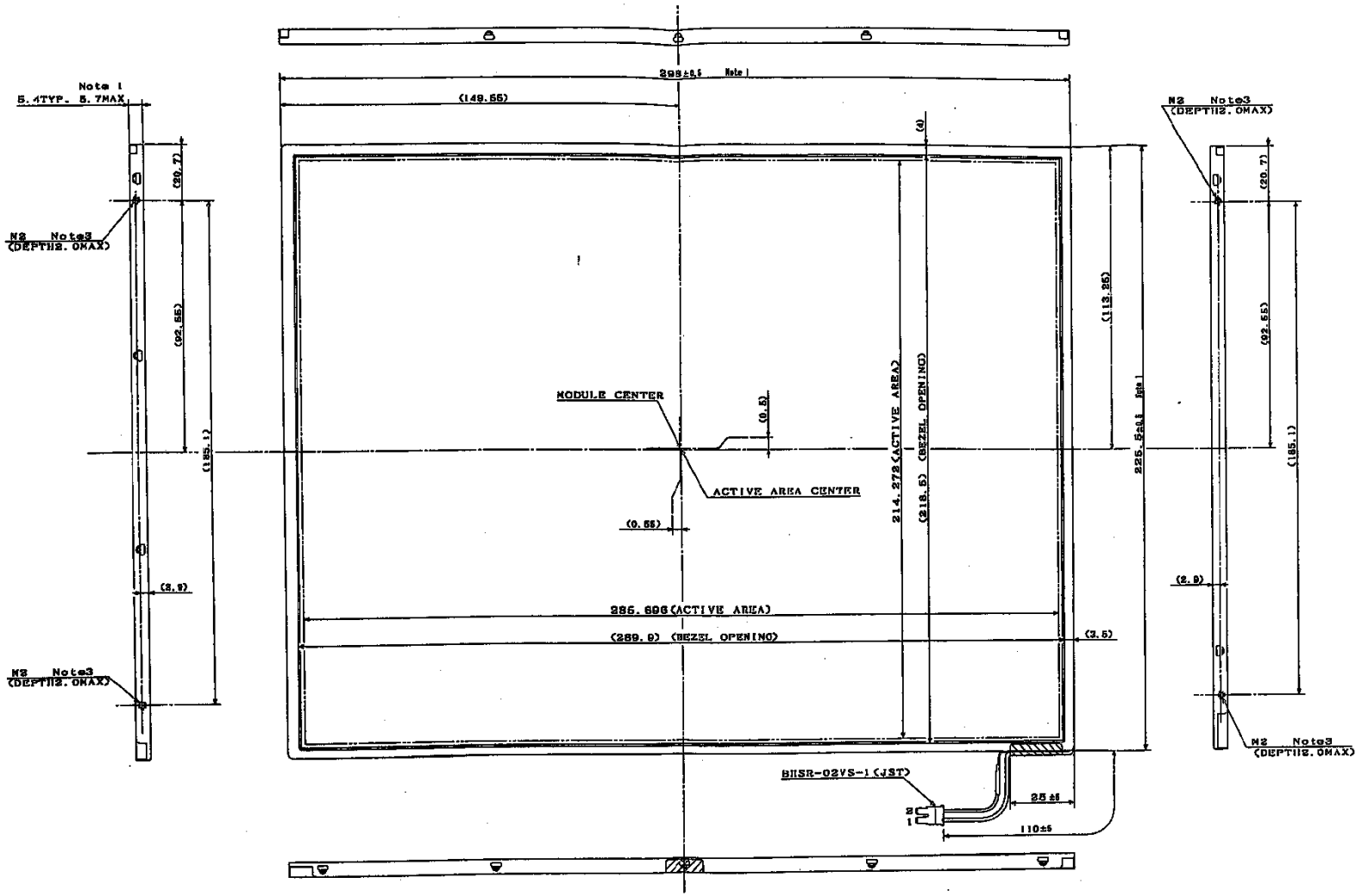
Liquid Crystal Display has the following specific characteristics. These are not defects nor malfunctions.

The ambient temperature may affect the display condition of the LCD module.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

19. OUTLINE DRAWINGS (Unit in mm)

19. 1 FRONT VIEW

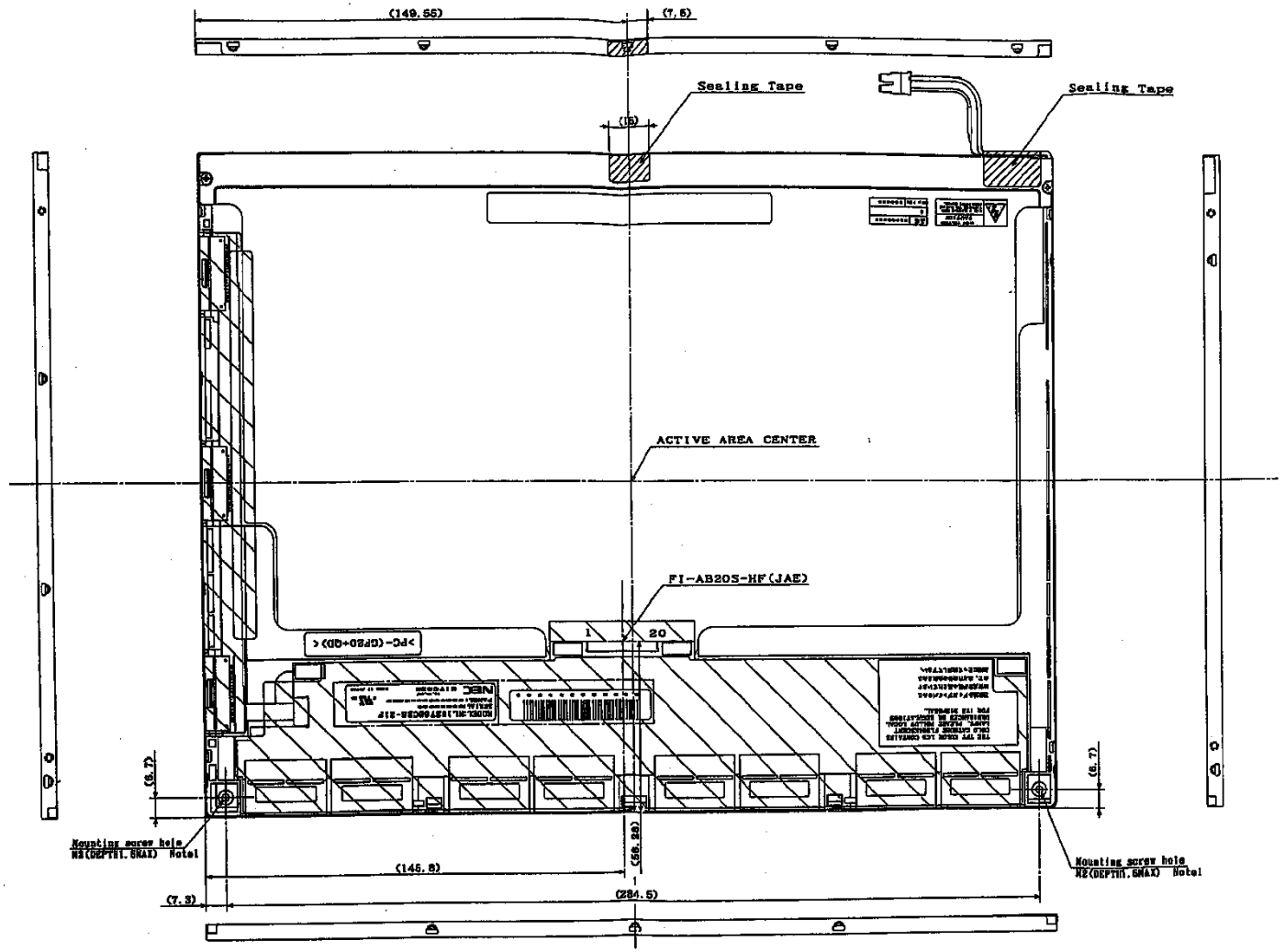


Note 1: Backlight cable and sealing tape are excepted.

Note 2: The values in parentheses are for reference.

Note 3: These holes are not for mounting.

19.2 REAR VIEW



Note 1: The torque for mounting screw should never exceed 0.255N·m.

Note 2: The values in parentheses are for reference.

Revision History

Rev.	prepared date	Revision contents	Approved	Checked	Prepared	Issued date
1	Sep. 18, 2000	DOD-H-8081	E. Nakajima	—	Y. Takeishi	—