Model Name: P650QVN01.0

Issue Date : 2014/8/5

(＊)Preliminary Specifications
( )Final Specifications

Customer Signature	Date	AUO	Date
Approved By _____		Approval By PM Director	
Note		Reviewed By RD Director Reviewed By Project Leader	
		Prepared By PM	

Contents

Record of Revision

Version	Date	Page	Description
0.0	2013/12/20		First release
0.1	2014/1/13	11	4K2K Input Data Format is updated
0.1	2014/1/13	21	Response Time 8=>10
02	2014/1/22	25	5.1 upper=>lower, right=left
03	2014/4/16	6~24	3. Electrical Specification is totally updated
		25	$\delta_{WHITE(9P}$ 1.3=>1.33, Response Time 8=>10
		35	Panel label is modified
04	2014/8/5	4	8 lanes=> 16 lanes
		6	Life time (MTTF): 50000 => 35000, Note 9, 10 was added
		30	Bezel Opening Spec. on drawing IC-DI ≦3.4 => IC-DI ≦2.4
		39~40	9.7 Operation Condition in PID Application was moved to 9.3, content was also modified, original 9.3 was shifted to 9.4, and so on.
		11	PIN 15~23 were modified into N.C.(No connection)
		12	PIN26~33, PIN 35~41 were modified into N.C.(No connection)
		25	Response Time typical 5.5, max is not specified

1. General Description

This specification applies to the 65 inch Color TFT-LCD Module P650QVN01.0. This LCD module has a TFT active matrix type liquid crystal panel 3840x2160 pixels, and diagonal size of 65 inch. This module supports 3840x2160 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

The P650QVN01.0 has been designed to apply the 10-bit 16 Lanes V by one interface method. It is intended to support displays where high brightness, wide viewing angle.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	65	inch	
Display Area	1428.48(H) x 803.52(V)	mm	
Outline Dimension	1445.3 x 823.8 x 11.8(D)	mm	D: front bezel to back bezel
Driver Element	a-Si TFT active matrix		
Bezel Opening	1430.5(H) x 806.6 (V)	mm	
Display Colors	10 bit, 16.7M	Colors	
Number of Pixels	3840x2160	Pixel	
Pixel Pitch	0.372 (H) x 0.372(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-glare, 3H		Haze=11%
Rotate Function	Unachievable		Note 1
Display Orientation	Portrait/Landscape Enabled		Note 2

Note 1: Rotate Function refers to LCD display could be able to rotate. This function does not work in this model.

Note 2: Please refer to 5.1 Placement Suggestions.

2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

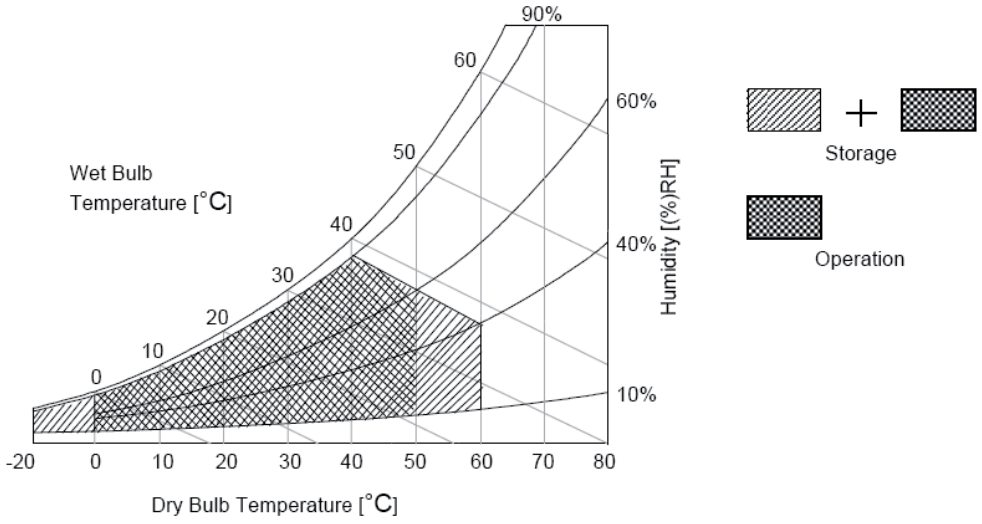
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vcc	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	3.6	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Surface temperature is measured at 50℃ Dry condition



3. Electrical Specification

The P650QVN01.0 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The other is to power Back Light Unit.

3.1 Electrical Characteristics

3.1.1 DC Characteristics (Ta = 25 ± 2 ℃)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V_{DC}	
Power Supply Input Current		I_{DD}	--	1.1	4	A	1
Power Consumption		P_C	--	13.2	48	Watt	1
Inrush Current		I_{RUSH}	--	--	7	A	2
Permissible Ripple of Power Supply Input Voltage		V_{RP}	--	--	V_{DD} * 5%	mV_{pk-pk}	3
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.7	--	3.3	V_{DC}	6
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	6
V-by-one Interface	CML Differential Input High Threshold	V_{RTH}	+50	--	--	mV_{DC}	
	CML Differential Input Low Threshold	V_{RTL}	--	--	-50	mV_{DC}	
	CML Common mode Bias Voltage	V_{RCT}	0.8	0.9	1.0	mV_{DC}	
Backlight Power Consumption		P_{BL}		138	150	Watt	
Life time (MTTF)			35000			Hour	9,10

3.1.2 AC Characteristics (Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
V-by-one Interface	VRXINP/N input each bit Period	T_{RRIP} (UI)	310	--	379	ps	10bit 5
	CDR lock time(CDR training)	T_{RLCK0}	--	--	1.0	ms	5
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -0.5%	--	Fclk +0.5%	MHz	4
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30			KHz	4
	ALN Training	T_{RALN}	--	30720	--	UI	8bit 5
			--	40960	--	UI	10bit
	PDX active to hot plug enable	T_{RHPD0}	--	--	1.0	us	5
	Intra-pair skew	T_{INTRA}	--	--	0.3	UI	6
	Inter-pair skew	T_{INTER}	--	--	5	UI	7
	Eye diagram at receiver	A_X	--	0.25	--	UI	8
		A_Y	--	0	--	mV	
		B_X	--	0.3	--	UI	
		B_Y	--	50	--	mV	
		C_X	--	0.7	--	UI	
		C_Y	--	50	--	mV	
		D_X	--	0.75	--	UI	
		D_Y	--	0	--	mV	
		E_X	--	0.7	--	UI	
		E_Y	--	-50	--	mV	
		F_X	--	0.3	--	UI	
		F_Y	--	-50	--	mV	

3.1.3 Driver Characteristics

Item	Symbol	Min	Max	Unit	condition
Driver Surface Temperature	DST		100	[℃]	Note

Note : Any point on the driver surface must be less than 100℃ under any conditions.

3.1.4 TCON Characteristics

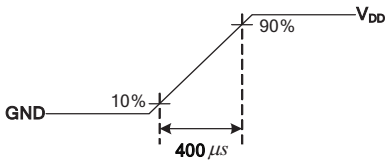
Item	Symbol	Min	Max	Unit	condition
TCON Surface Temperature	TST		85	[℃]	Note

Note: Any point on the TCON surface must be less than 85℃ under any conditions.

Note:

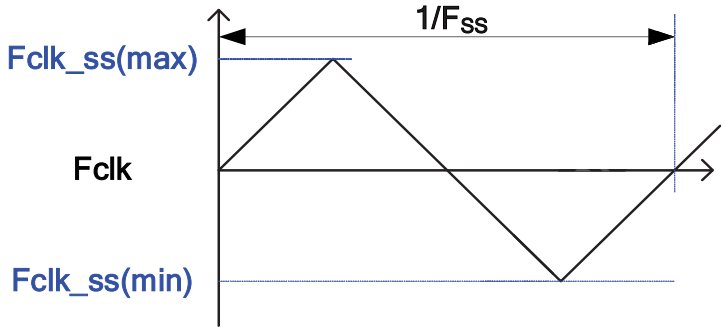
1. Test Condition:
   (1) V_{DD} = 12.0V
   (2) Fv = 120Hz
   (3) Fclk= Max freq.
   (4) Temperature = 25 ℃
   (5) Typ. Input current : White Pattern
   Max. Input current: Heavy loading pattern defined by AUO
   >> refer to "Section:3.3 Signal Timing Specification, Typical timing"

2. Measurement condition : Rising time = 400us

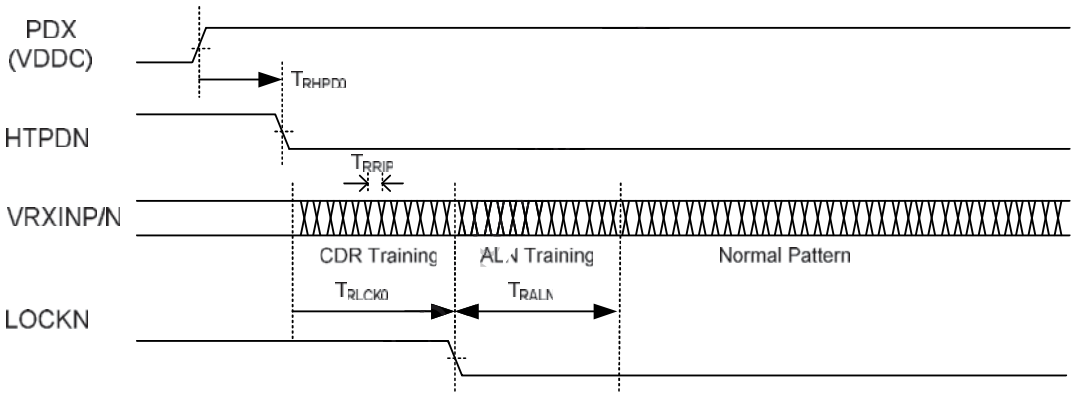


3. Test Condition:
   (1) The measure point of V_{RP} is in LCM side after connecting the System Board and LCM.
   (2) Under Max. Input current spec. condition.

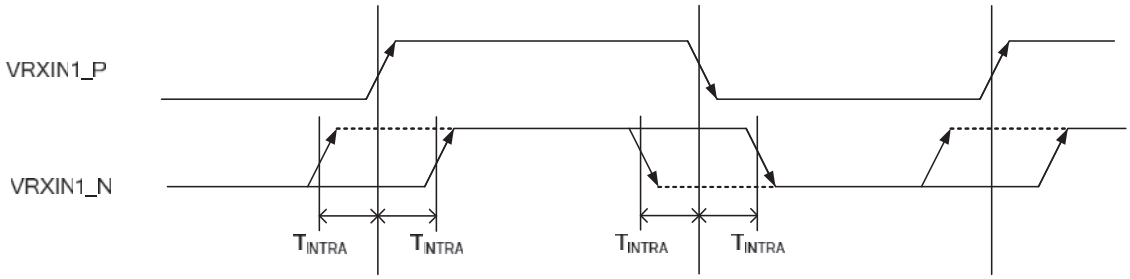
4. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



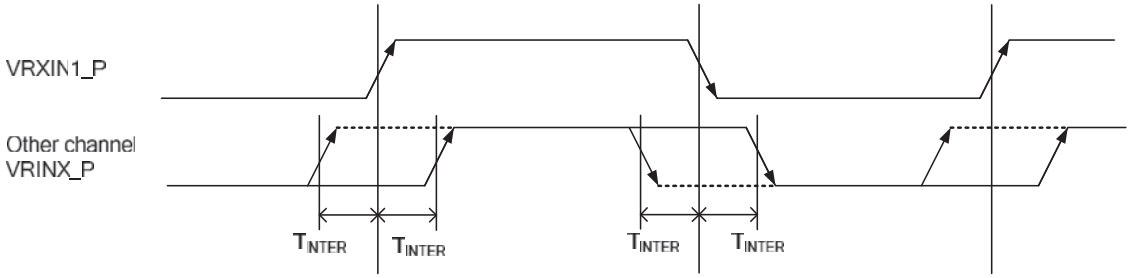
5. V-by-one Receiver start up timing waveform



6. V-by-one Intra-pair Skew

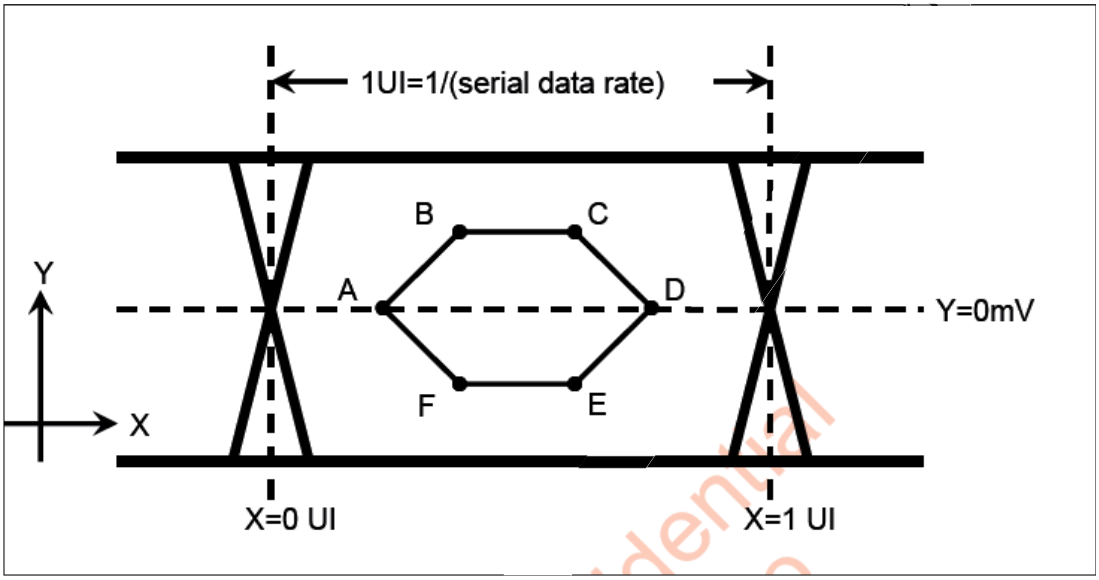


7. V-by-one Inter-pair Skew

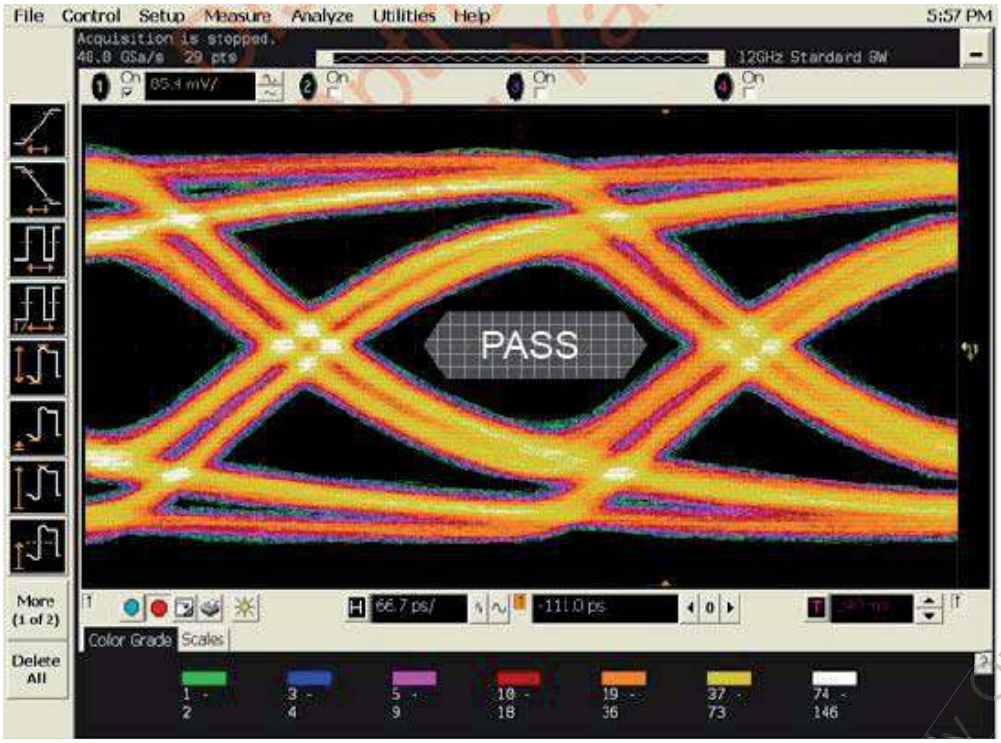


8. Eye diagram at receiver

Eye Mask



Example of Eye diagram



9. The relative humidity must not exceed 80% non-condensing at temperatures of 40 or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃

10. The lifetime (MTTF) is defined as the time which luminance of LED is 50% compared to its original value. [Operating condition: Continuous operating at Ta = 25±2℃, for single lamp/LED only]

3.2 Interface Connections

- LCD connector: FI-RE51S-HF (JAE, V-by-One 51pin connector)；P-Two 187059-5122

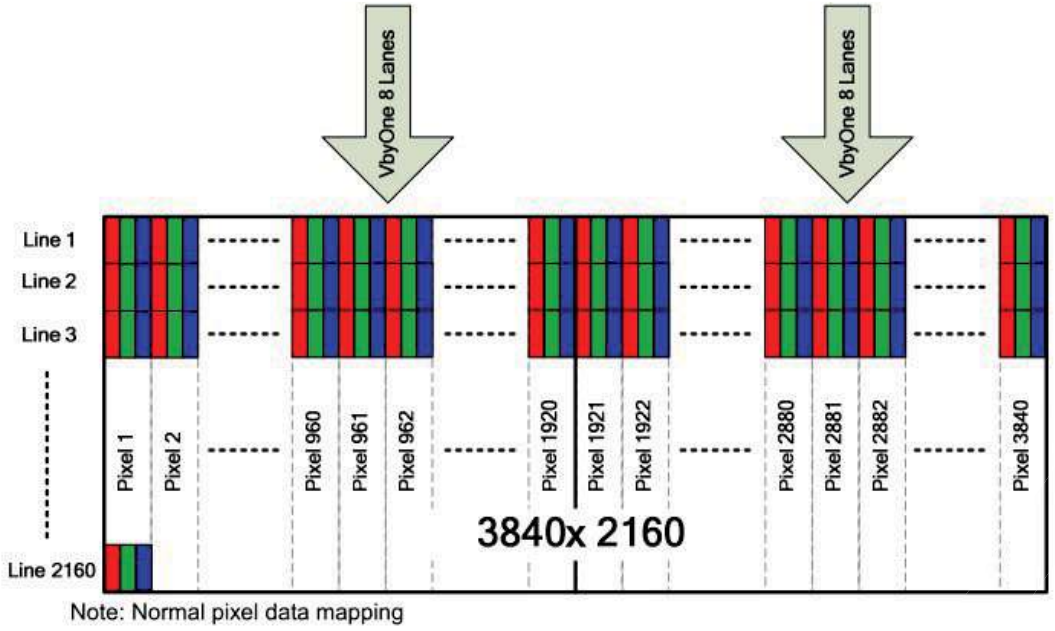
PIN	Symbol	Description	PIN	Symbol	Description
1	VDD	12V_PW	26	LOCKN	Vx1 LOCKN
2	VDD	12V_PW	27	GND	Ground
3	VDD	12V_PW	28	RX0N	Vx1 lane 0
4	VDD	12V_PW	29	RX0P	Vx1 lane 0
5	VDD	12V_PW	30	GND	Ground
6	VDD	12V_PW	31	RX1N	Vx1 lane 1
7	VDD	12V_PW	32	Rx1P	Vx1 lane 1
8	VDD	12V_PW	33	GND	Ground
9	N.C.	No connection	34	RX2N	Vx1 lane 2
10	N.C.	No connection	35	RX2P	Vx1 lane2
11	N.C.	No connection	36	GND	Ground
12	GND	Ground	37	RX3N	Vx1 lane 3
13	GND	Ground	38	RX3P	Vx1 lane 3
14	GND	Ground	39	GND	Ground
15	N.C.	No connection	40	RX4N	Vx1 lane 4
16	N.C.	No connection	41	RX4P	Vx1 lane 4
17	N.C.	No connection	42	GND	Ground
18	N.C.	No connection	43	RX5N	Vx1 lane 5
19	N.C.	No connection	44	RX5P	Vx1 lane 5
20	N.C.	No connection	45	GND	Ground
21	N.C.	No connection	46	RX6N	Vx1 lane 6
22	N.C.	No connection	47	RX6P	Vx1 lane 6
23	N.C.	No connection	48	GND	Ground
24	GND	Ground	49	RX7N	Vx1 lane 7
25	HTPDN	Vx1 HTPDN	50	RX7P	Vx1 lane 7
			51	GND	Ground

- LCD V-by-One connector: FI-RE41S-HF (JAE, V-by-One 41pin connector)；P-Two 187060-4122

PIN	Symbol	Description	PIN	Symbol	Description
1	GND	Ground	21	RX14P	Vx1 lane14
2	RX8N	Vx1 lane8	22	GND	Ground
3	RX8P	Vx1 lane 8	23	RX15N	Vx1 lane15
4	GND	Ground	24	RX15P	Vx1 lane15
5	RX9N	Vx1 lane9	25	GND	Ground
6	RX9P	Vx1 lane9	26	N.C.	No connection
7	GND	Ground	27	N.C.	No connection
8	RX10N	Vx1 lane10	28	N.C.	No connection
9	RX10P	Vx1 lane10	29	N.C.	No connection
10	GND	Ground	30	N.C.	No connection
11	RX11N	Vx1 lane11	31	N.C.	No connection
12	RX11P	Vx1 lane11	32	N.C.	No connection
13	GND	Ground	33	N.C.	No connection
14	RX12N	Vx1 lane12	34	GND	Ground
15	RX12P	Vx1 lane12	35	N.C.	No connection
16	GND	Ground	36	N.C.	No connection
17	RX13N	Vx1 lane13	37	N.C.	No connection
18	RX13P	Vx1 lane13	38	N.C.	No connection
19	GND	Ground	39	N.C.	No connection
20	RX14N	Vx1 lane14	40	N.C.	No connection
			41	N.C.	No connection

- FFC Connector (80 Pin)：196225-80041(P-two) / 106C80-100000-G2-R(CHIEF LAND)

4K2K Input Data Format：



Note: Normal pixel data mapping

Pixel No	Pixel 1			Pixel 2			Pixel 3			~		Pixel 3840		
Line 1	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 2	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 3	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 4	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 5	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 6	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
:	:	:	:	:	:	:	:	:	:	:	~	:	:	:
Line 2158	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 2159	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 2160	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840

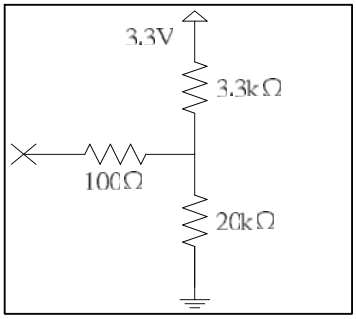
V-by-one Lanes of pixel data

	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8
Blank	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR
Line 1	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8
	Pixel 9	Pixel 10	Pixel 11	Pixel 12	Pixel 13	Pixel 14	Pixel 15	Pixel 16
	.	.	.	.	.	.	.	.
	Pixel 1913	Pixel 1914	Pixel 1915	Pixel 1916	Pixel 1917	Pixel 1918	Pixel 19198	Pixel 1920
Blank	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR
Line2	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8
	Pixel 8	Pixel 10	Pixel 11	Pixel 12	Pixel 13	Pixel 14	Pixel 15	Pixel 16
	.	.	.	.	.	.	.	.
	Pixel 1913	Pixel 1914	Pixel 1915	Pixel 1916	Pixel 1917	Pixel 1918	Pixel 19198	Pixel 1920
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

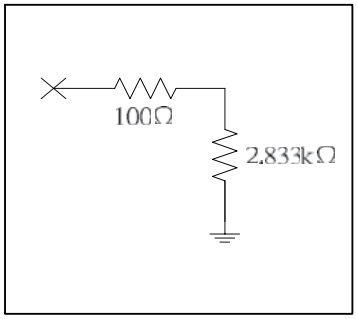
	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15	Lane 16
Blank	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR
Line 1	Pixel 1921	Pixel 1922	Pixel 1923	Pixel 1924	Pixel 1925	Pixel 1926	Pixel 1927	Pixel 1928
	Pixel 1929	Pixel 1930	Pixel 1931	Pixel 1932	Pixel 1933	Pixel 1934	Pixel 1935	Pixel 1936
	.	.	.	.	.	.	.	.
	Pixel 3833	Pixel 3834	Pixel 3835	Pixel 3836	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840
Blank	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR
Line2	Pixel 1921	Pixel 1922	Pixel 1923	Pixel 1924	Pixel 1925	Pixel 1926	Pixel 1927	Pixel 1928
	Pixel 1929	Pixel 1930	Pixel 1931	Pixel 1932	Pixel 1933	Pixel 1934	Pixel 1935	Pixel 1936
	.	.	.	.	.	.	.	.
	Pixel 3833	Pixel 3834	Pixel 3835	Pixel 3836	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3.2.1 LVDS connector control and I2C pin description

Note * : Open/High(3.3V)

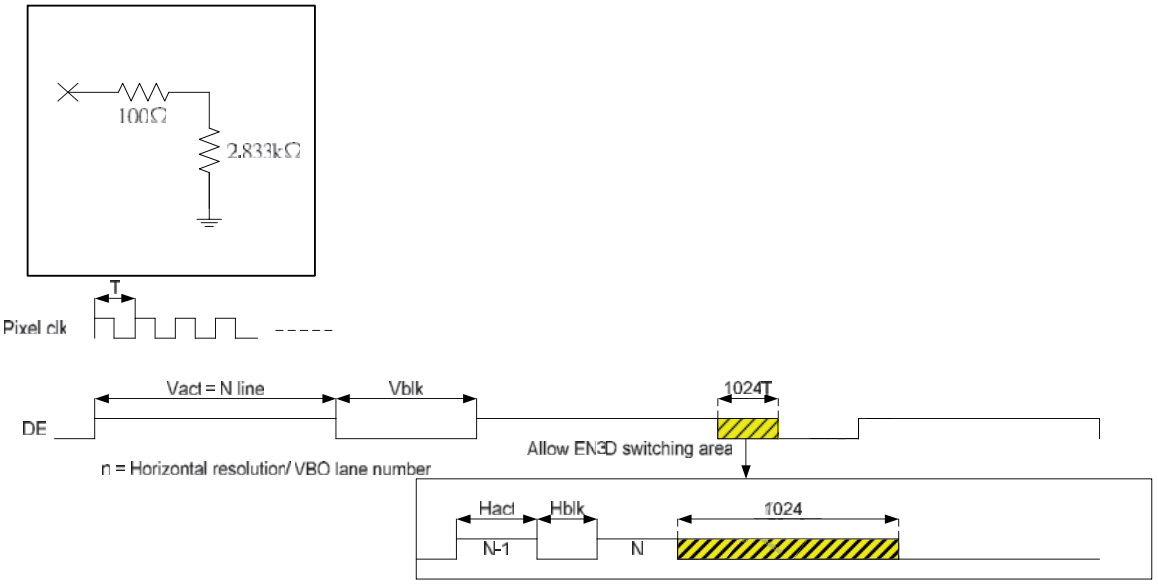


Note ** : Open/Low(GND)

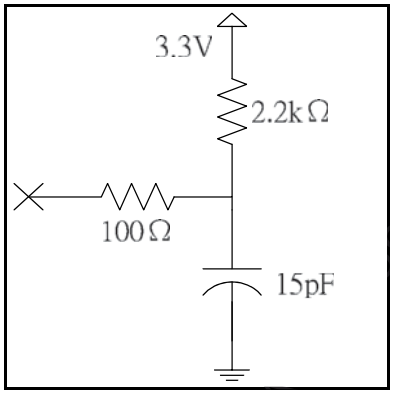


Note * : Open/Low(GND)**

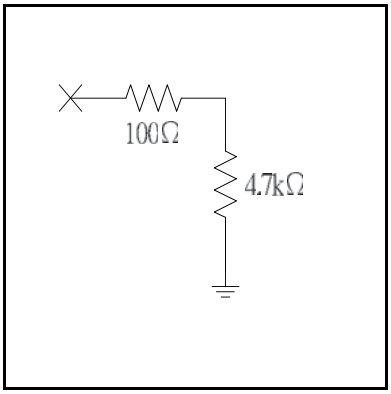
The switch range of 3D_EN control signal is from the last DE falling to 1024T. (T is a pixel clk)



Note ** : SCL/SDA**



Note *** : WP**



3.2.2 V by one color data mapping

Mode		Packer input & Unpacker output		30bpp RGB /YCbCr444 (10bit)	24bpp RGB /YCbCr444 (8bit)
4byte mode	3byte mode	Byte0	D[0]	R/Cr[2]	R/Cr[0]
			D[1]	R/Cr[3]	R/Cr[1]
			D[2]	R/Cr[4]	R/Cr[2]
			D[3]	R/Cr[5]	R/Cr[3]
			D[4]	R/Cr[6]	R/Cr[4]
			D[5]	R/Cr[7]	R/Cr[5]
			D[6]	R/Cr[8]	R/Cr[6]
			D[7]	R/Cr[9]	R/Cr[7]
		Byte1	D[8]	G/Y[2]	G/Y[0]
			D[9]	G/Y[3]	G/Y[1]
			D[10]	G/Y[4]	G/Y[2]
			D[11]	G/Y[5]	G/Y[3]
			D[12]	G/Y[6]	G/Y[4]
			D[13]	G/Y[7]	G/Y[5]
			D[14]	G/Y[8]	G/Y[6]
			D[15]	G/Y[9]	G/Y[7]
		Byte2	D[16]	B/Cb[2]	B/Cb[0]
			D[17]	B/Cb[3]	B/Cb[1]
			D[18]	B/Cb[4]	B/Cb[2]
			D[19]	B/Cb[5]	B/Cb[3]
			D[20]	B/Cb[6]	B/Cb[4]
			D[21]	B/Cb[7]	B/Cb[5]
			D[22]	B/Cb[8]	B/Cb[6]
			D[23]	B/Cb[9]	B/Cb[7]
		Byte3	D[24]	--	
			D[25]	--	
			D[26]	B/Cb[0]	
			D[27]	B/Cb[1]	
			D[28]	G/Y[0]	
			D[29]	G/Y[1]	
			D[30]	R/Cr[0]	
			D[31]	R/Cr[1]	

3.3 Signal Timing Specification

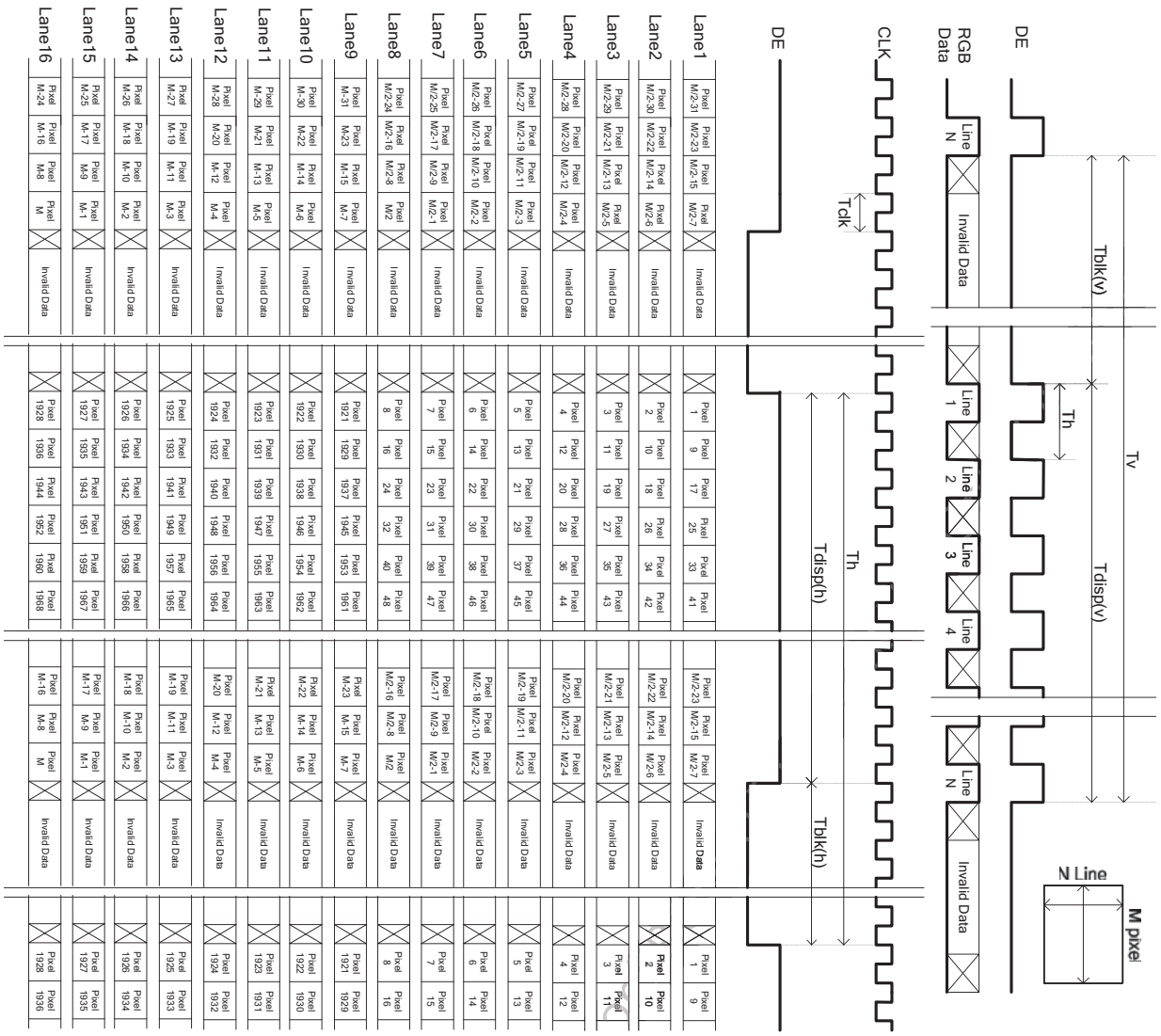
This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	2180	2250	2715	Th
	Active	Tdisp (v)		2160		
	Blanking	Tblk (v)	20	90	555	Th
Horizontal Section	Period	Th	270	275	300	Tclk
	Active	Tdisp (h)		240		
	Blanking	Tblk (h)	30	35	60	Tclk
Clock	Frequency	Fclk=1/Tclk	66	74.25	75	MHz
Vertical Frequency	Frequency	Fv	94	120	122	Hz
Horizontal Frequency	Frequency	Fh	240	270	278.4	KHz

3.4 Signal Timing Waveforms

Two Section Mode (Lane1~16 V-by one data: 1, 2, 3, 4, 5, 6, 7, 8, 1921, 1922, 1923, 1924, 1925, 1926, 1927, 1928)



3.5 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

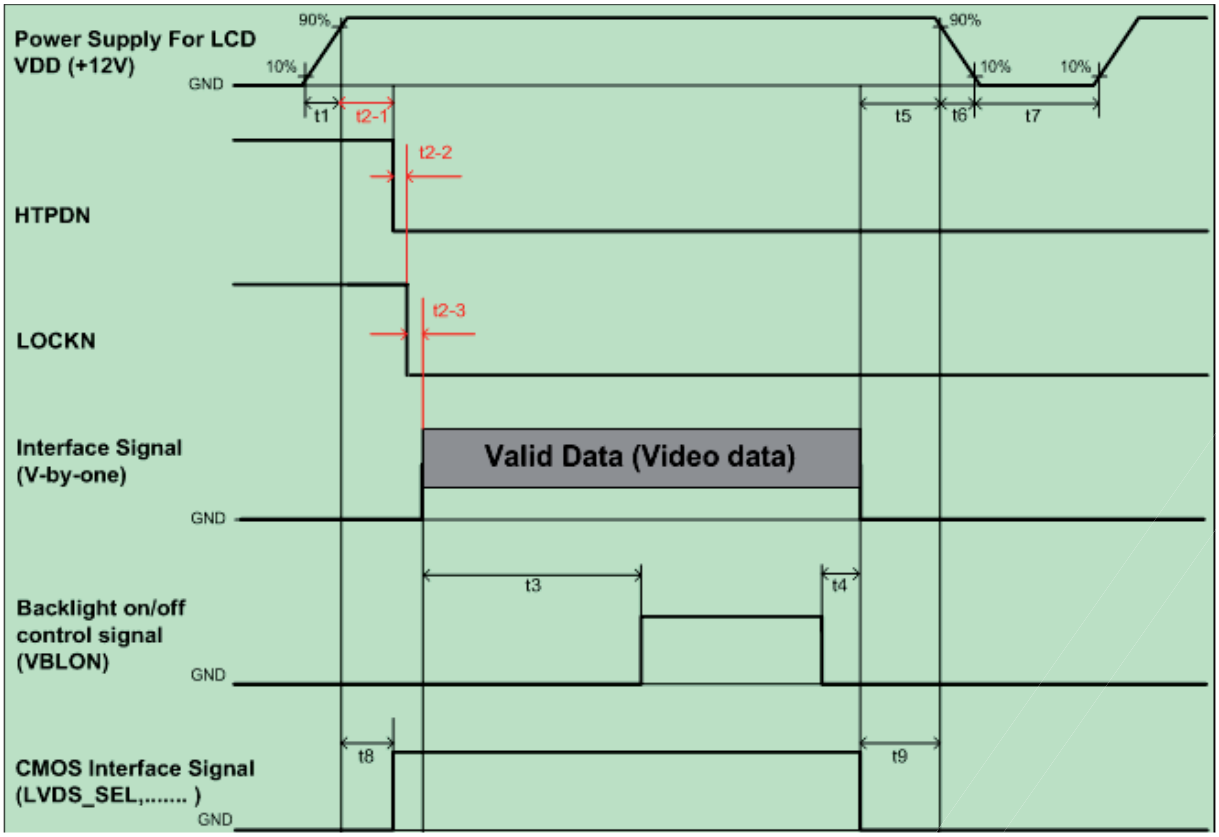
Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3.6 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2-1	10	---	---*1	ms
t2-2	---	---	---*2	ms
t2-3	---	---	1	ms
t3	670	---	---	ms
t4	0*3	---	---	ms
t5	0	---	---	ms
t6	---	---	---*4	ms
t7	500	---	---	ms
t8	10*5	---	50	ms
t9	0	---	---	ms

Note:

(1) t2-1 : The maximum timing of VDD rising(90%) to HTPDN falling edge decided by customer

system.

(2) t2-2 : V by One training time after power-on. The timing of HTPDN falling edge to LOCKN falling edge decided by customer system.

(3) t4=0 : concern for residual pattern before BLU turn off.

(4) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)

(5) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

(6) t2-1: VDD rising(90%) to HTPDN falling edge

t2-2: CDR lock time (CDR training)

t2-3: ALN training

3.7 Backlight Specification

The backlight unit contains 4pcs light bar.

3.7.1 Electrical specification (Ta = 25 ± 2 ℃)

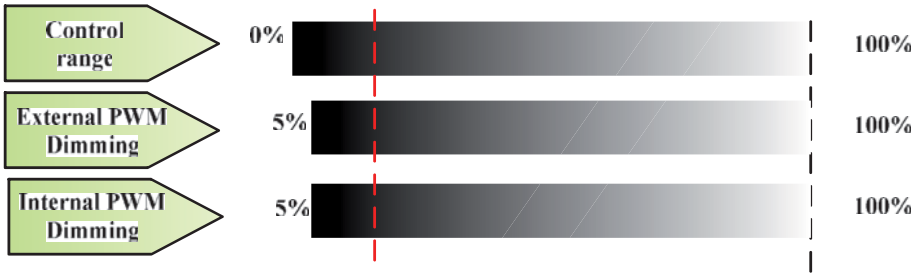
	Item	Symbol		Condition	Spec			Unit	Note
					Min	Typ	Max		
1	Input Voltage	VDDB		-	22.8	24	25.2	VDC	-
2	Input Current	I_{DDB}		VDDB=24V		5.75	6.25	ADC	1
3	Input Power	P_{DDB}		VDDB=24V		138	150	W	1
4	Inrush Current	I_{RUSH}		VDDB=24V			14.7	ADC	2
5	On/Off control voltage	V_{BLON}	ON	VDDB=24V	2	-	5.5	VDC	5
			OFF		0	-	0.8		
6	On/Off control current	I_{BLON}		VDDB=24V	-	-	1.5	mA	-
7	External PWM Control Voltage	V_EPWM	MAX	VDDB=24V	2	-	5.5	VDC	7
			MIN	VDDB=24V	0	-	0.8		
8	External PWM Control Current	I_EPWM		VDDB=24V	-	-	2	mADC	-
9	External PWM Duty ratio	D_EPWM		VDDB=24V	5	-	100	%	4
10	External PWM Frequency	F_EPWM		VDDB=24V	140	180	240	Hz	-
11	DET status signal	DET	HI	VDDB=24V	Open Collector			VDC	5
			Lo		0	-	0.8	VDC	
12	Input Impedance	Rin		VDDB=24V	300			Kohm	-

Note 1 : Dimming ratio= 100% (MAX)（Ta=25±5℃, Turn on for 45minutes）
Note 2: Measurement condition Rising time = 20ms (VDDB : 10%~90%);
Note 3: Less than 5% dimming control is functional well and no backlight shutdown happened
Note 4: Normal : 0~0.8V ; Abnormal : Open collector

3.7.2 Input Pin Assignment

LED driver board connector : Cvilux CI0114M1HR0-NH

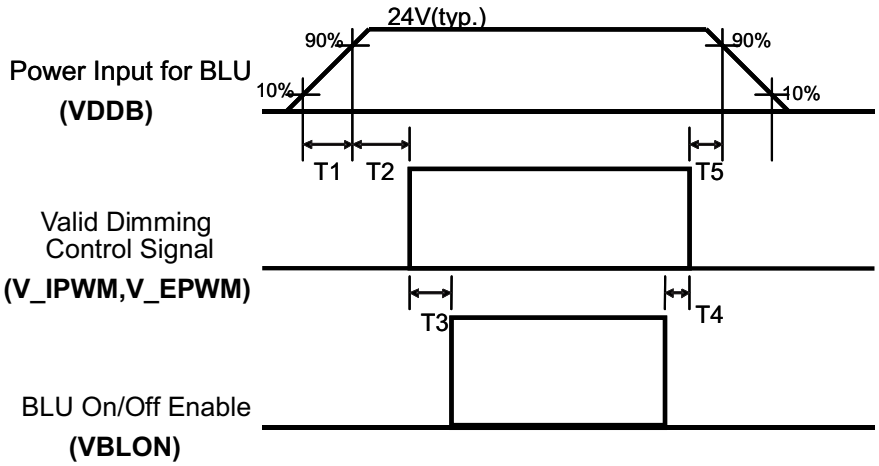
Pin	Symbol	Description
1	VDDB	Operating Voltage Supply, +24V DC regulated
2	VDDB	Operating Voltage Supply, +24V DC regulated
3	VDDB	Operating Voltage Supply, +24V DC regulated
4	VDDB	Operating Voltage Supply, +24V DC regulated
5	VDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	DET	BLU status detection: Normal : 0~0.8V ; Abnormal : Open collector (Recommend Pull high R > 10K, VDD = 3.3V)
12	VBLON	BLU On-Off control: High/Open (2~5.5V) : BL On ; Low (0~0.8V/GND) : BL Off
13	NC	NC
14	PDIM(*)	External PWM (5%~100% Duty, open for 100%)



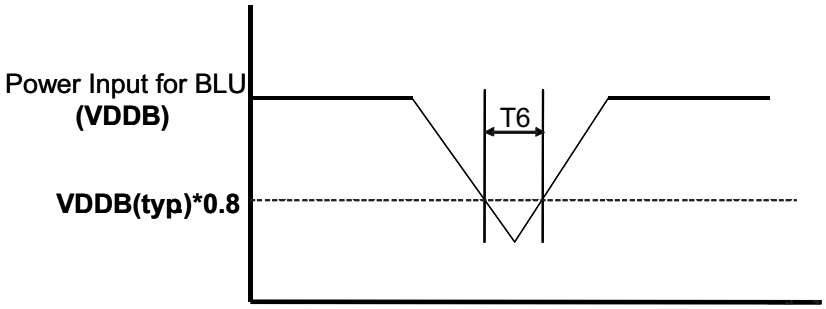
PWM Dimming : include Internal and External PWM Dimming

(Note*) IF External PWM function includes 5% dimming ratio. Judge condition as below:
(1) Backlight module must be lighted ON normally.
(2) All protection function must work normally.
Uniformity and flicker could NOT be guaranteed

3.7.3 Power Sequence for Backlight (CCFL and LED)



Dip condition



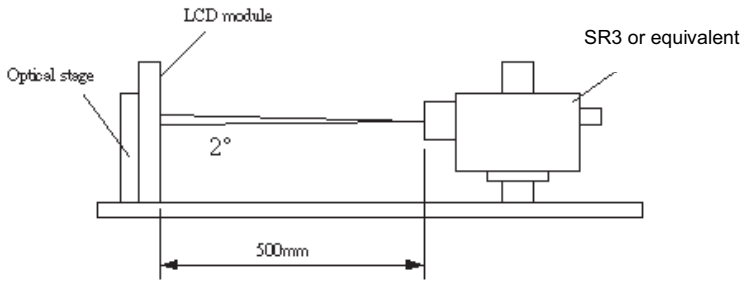
Parameter	Value			Units
	Min	Typ	Max	
T1	20	-	-	ms
T2	250	-	-	ms
T3	200			ms
T4	0	-	-	ms
T5	0	-	-	ms
T6		-	1000	ms*1

Note:1. T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.

4 Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio		CR	3200	4000	--		1
Surface Luminance (White)		L_{WH} (2D)	360	450	--	cd/m^2	2
Luminance Variation		$\delta_{WHITE(9P)}$	--	--	1.33		3
Response Time (G to G)		Tγ	--	5.5	--	ms	4
Color Gamut		NTSC		72		%	
Color Coordinates **(TBD)**							
	Red	R_X	Typ.-0.03	0.640	Typ.+0.03		
		R_Y		0.330			
	Green	G_X		0.300			
		G_Y		0.600			
	Blue	B_X		0.150			
		B_Y		0.050			
	White	W_X		0.280			
		W_Y		0.290			
Viewing Angle							5
	x axis, right(φ=0°)	θ_r	--	89	--	degree	
	x axis, left(φ=180°)	θ_l	--	89	--	degree	
	y axis, up(φ=90°)	θ_u	--	89	--	degree	
	y axis, down (φ=270°)	θ_d	--	89	--	degree	

Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. LED current I_F = typical value (without driver board), LED input VDDB =24V, I_{DDB}. = Typical value (with driver board), L_{WH}=Lon5 where Lon5 is the luminance with all pixels displaying white at center 5 location.
3. The variation in surface luminance, δWHITE is defined (center of Screen) as:

   $\delta_{WHITE(9P)}$= Maximum(L_{on1}, L_{on2},…,L_{on9})/ Minimum(L_{on1}, L_{on2},…L_{on9})
4. Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on F_V=120 Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

The response time is defined as the following figure and shall be measured by switching the input signal for “any level of gray(bright) “ and “any level of gray(dark)”.

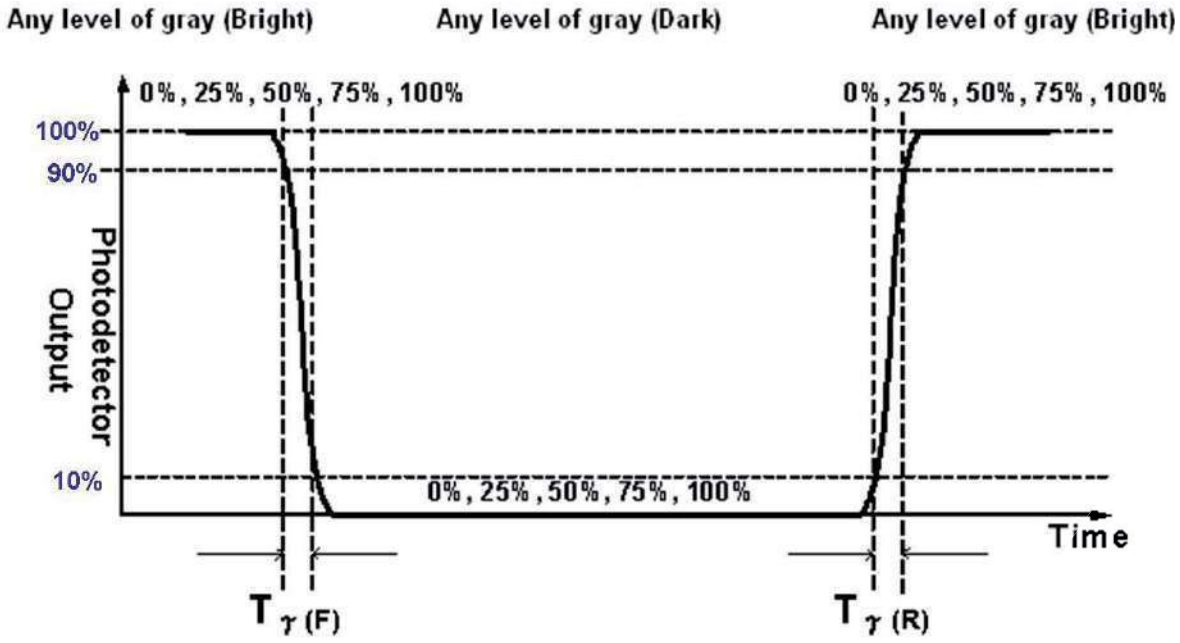
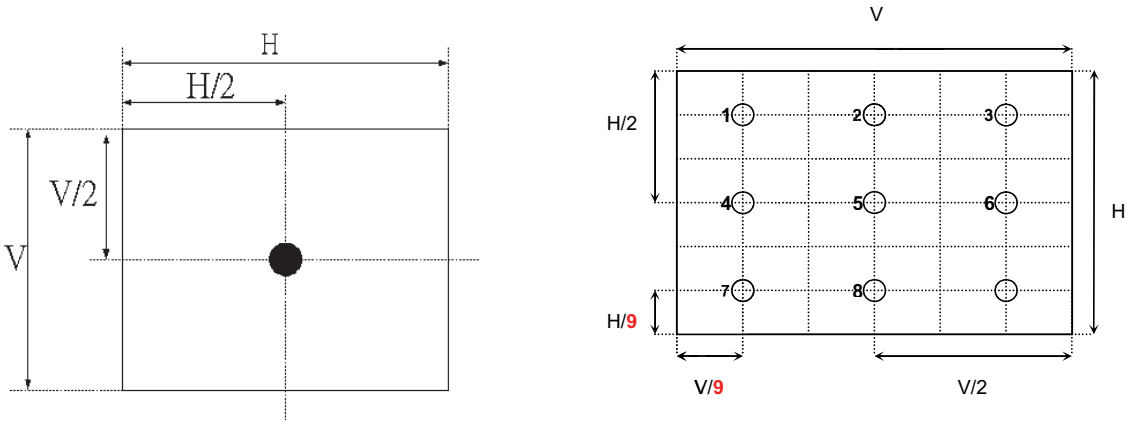
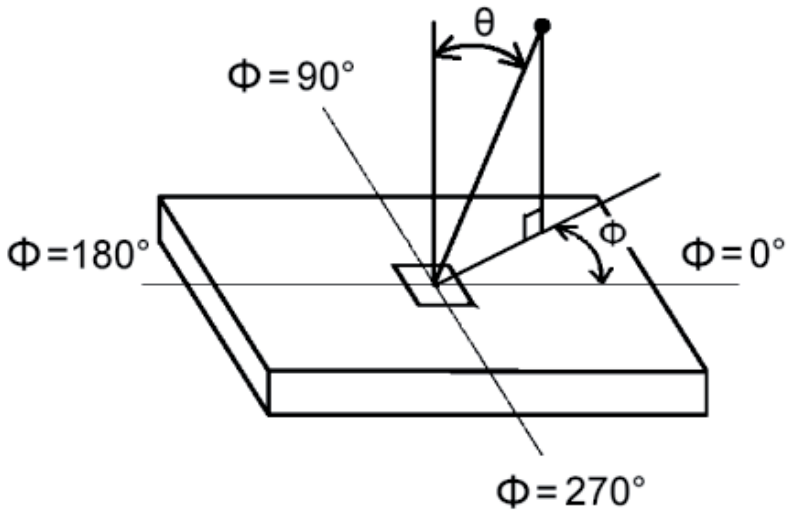


FIG. 2 Luminance



5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG3.

FIG.3 Viewing Angle



5 Mechanical Characteristics

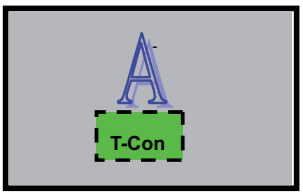
The contents provide general mechanical characteristics for the model P650QVN01.0 In addition the figures in the next page are detailed mechanical drawing of the LCD.

Item		Dimension	Unit	Note
Outline Dimension	Horizontal	1445.3	Mm	
	Vertical	823.8	Mm	
	Depth (Dmin)	11.8	Mm	front bezel to back bezel
	Depth (Dmax)	29.3	Mm	to wall mount
Weight	24600 (TBD)		G	w/ DB

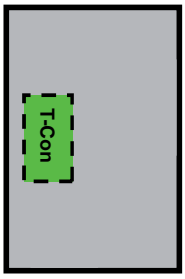
5.7 Placement Suggestions

1. Landscape Mode: The default placement is T-Con Side on the lower side and the image is shown upright via viewing from the front.
2. Portrait Mode: The default placement is that T-Con side has to be placed on the left side via viewing from the front.

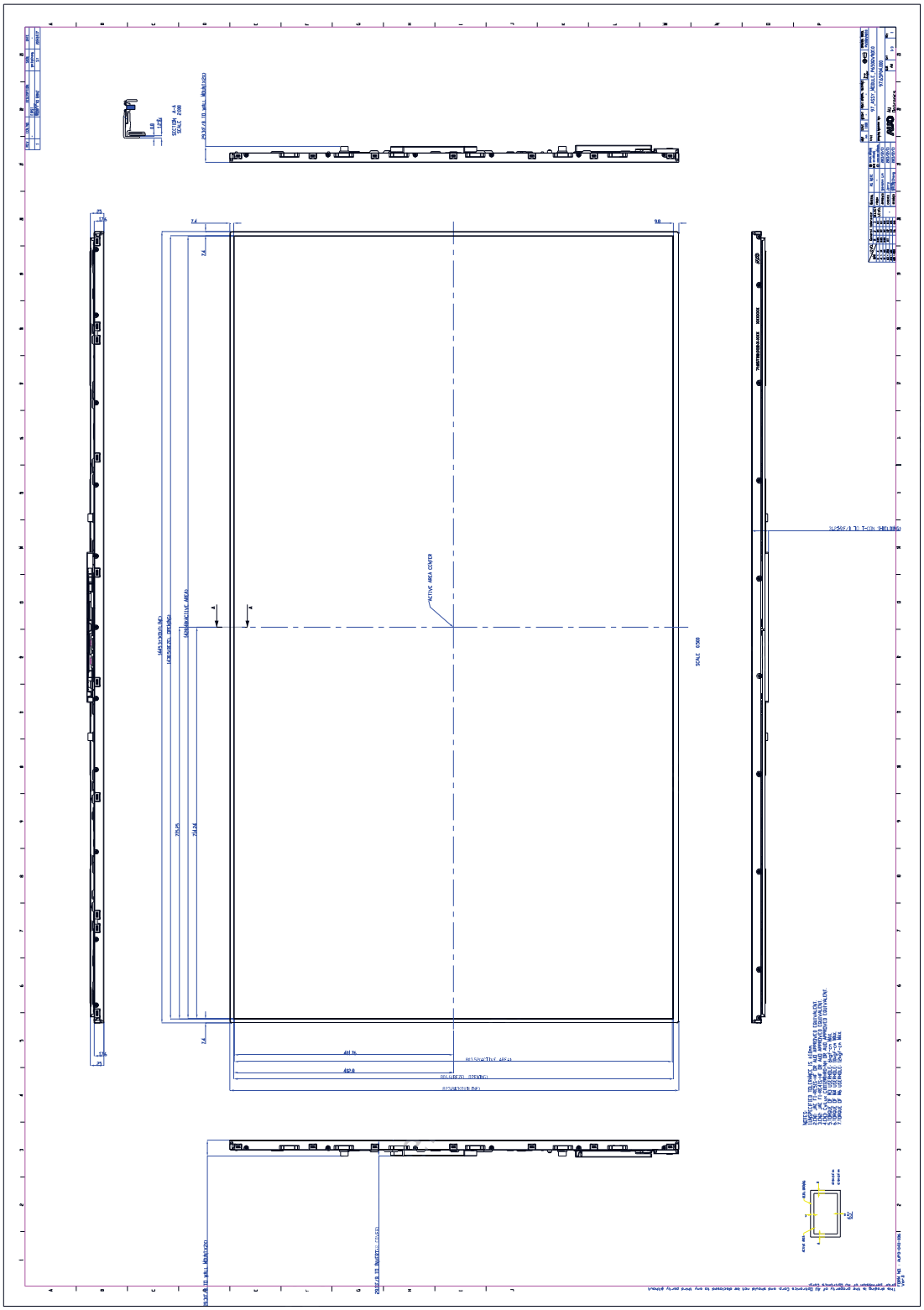
Landscape (**Front view**)



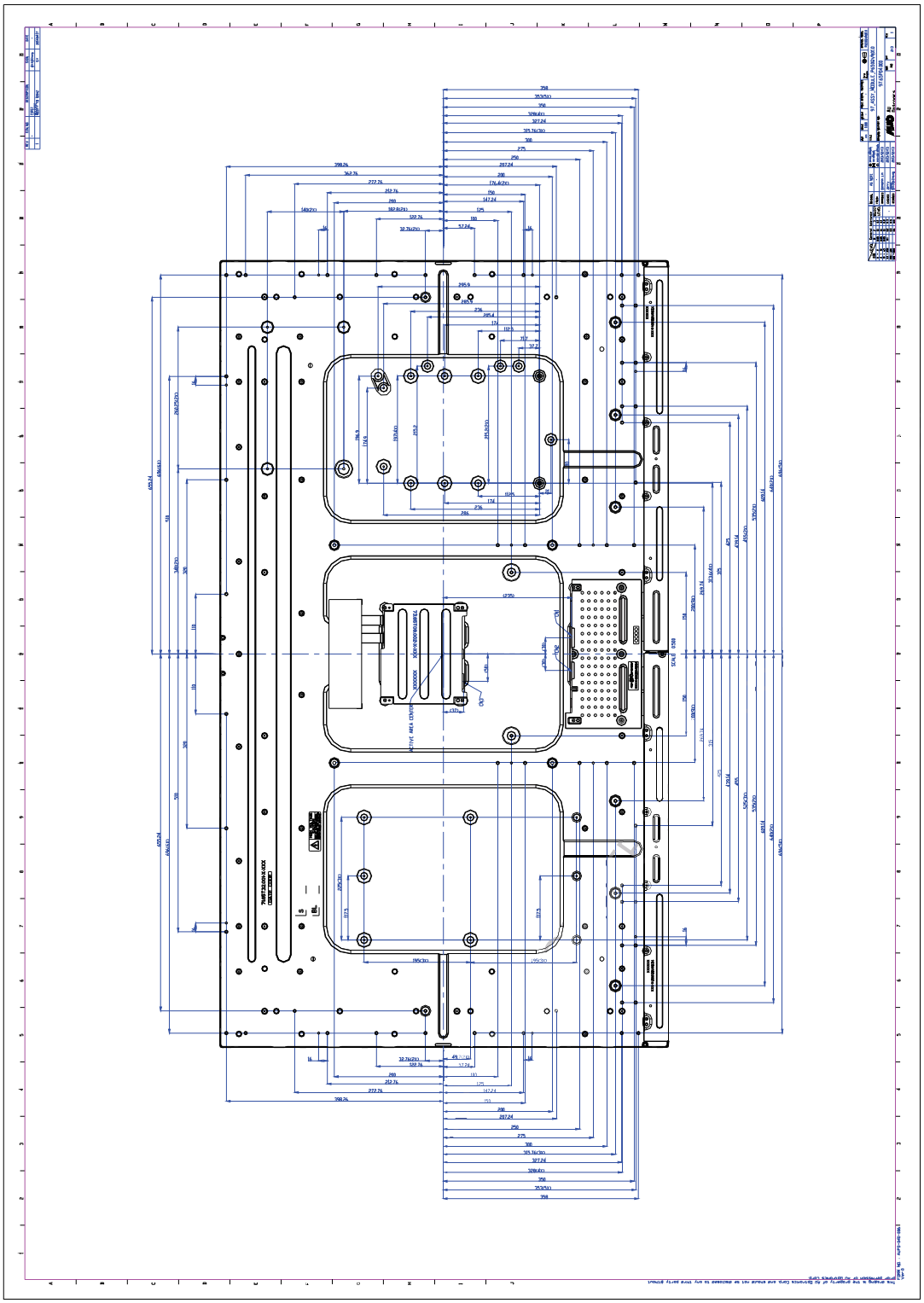
Portrait (**Front view**)

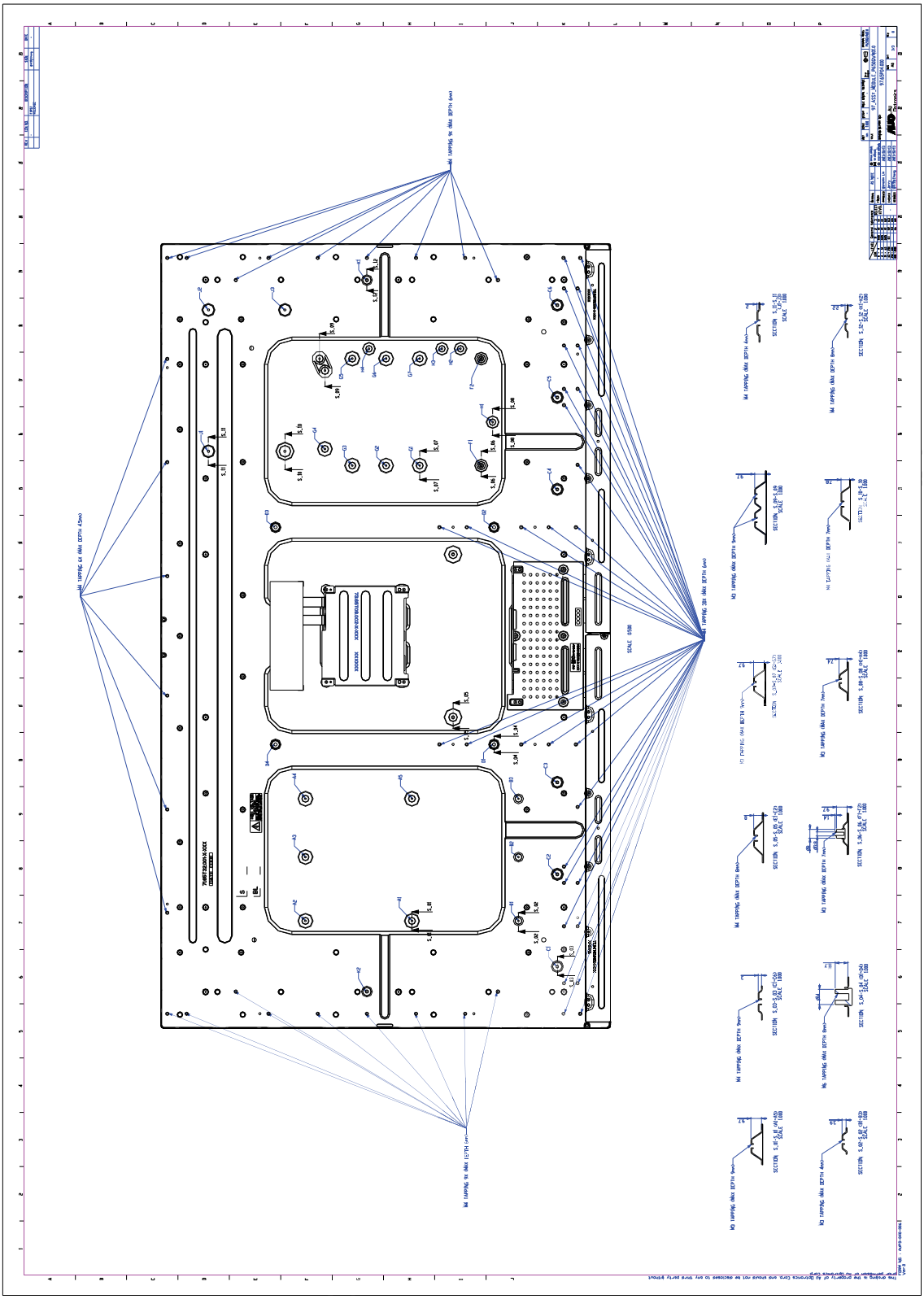


Front View



Back View





6. Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60℃, 500hrs
2	Low temperature storage test	3	-20℃, 500hrs
3	High temperature operation test	3	50℃, 500hrs
4	Low temperature operation test	3	-5℃, 500hrs
5	Vibration test (With carton)	1(PKG)	Random wave (1.04Grms 2~200Hz) Duration : X,Y,Z 20min per axes
6	Drop test (With carton)	1(PKG)	Height: 25.4 cm Direction: Only bottom flat twice (ASTMD4169-I)

7. International Standard

7.1 Safety

(1) UL 60950-1; Standard for Safety of Information Technology Equipment Including electrical Business Equipment.

(2) IEC 60950-1; Standard for Safety of International Electrotechnical Commission

(3) EN 60950-1; European Committee for Electrotechnical Standardization (CENELEC), EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

7.2 EMC

(1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992

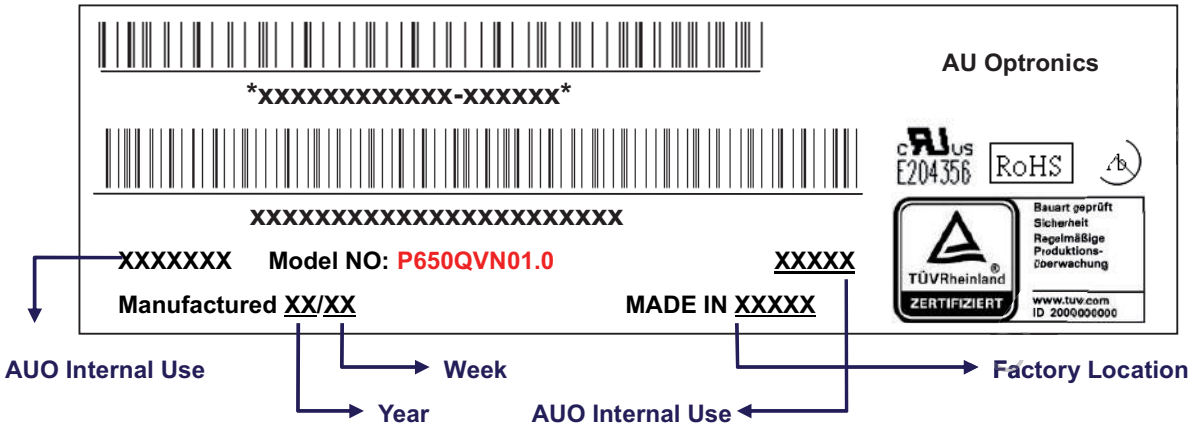
(2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.

(3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electrotechnical Standardization. (CENELEC), 1998

8. Packing

8.1 Definition of Label

A. Panel Label:



Green mark description

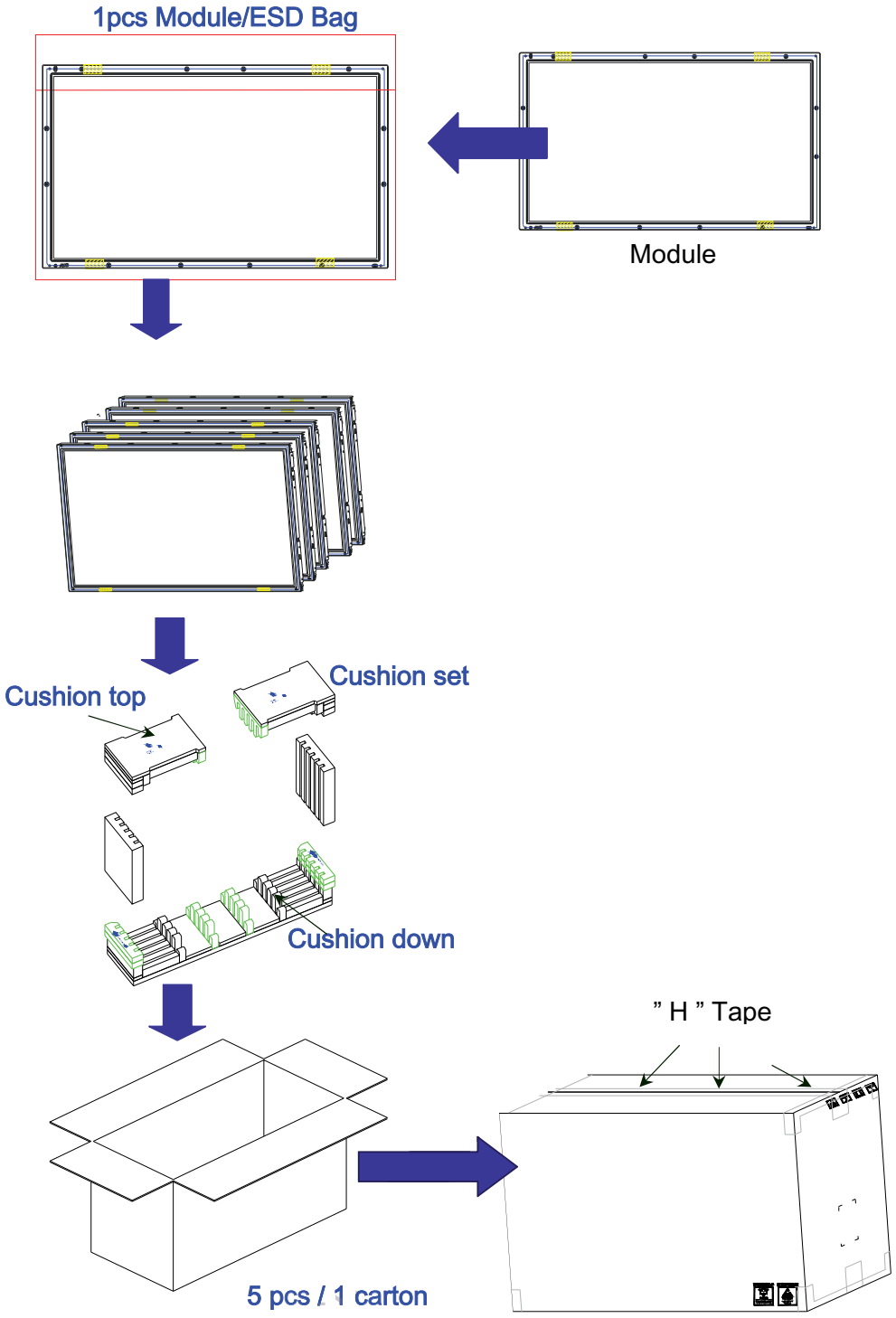
(1) For Pb Free Product, AUO will add for identification.

(2) For RoHs compatible products, AUO will add RoHS for identification.

Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

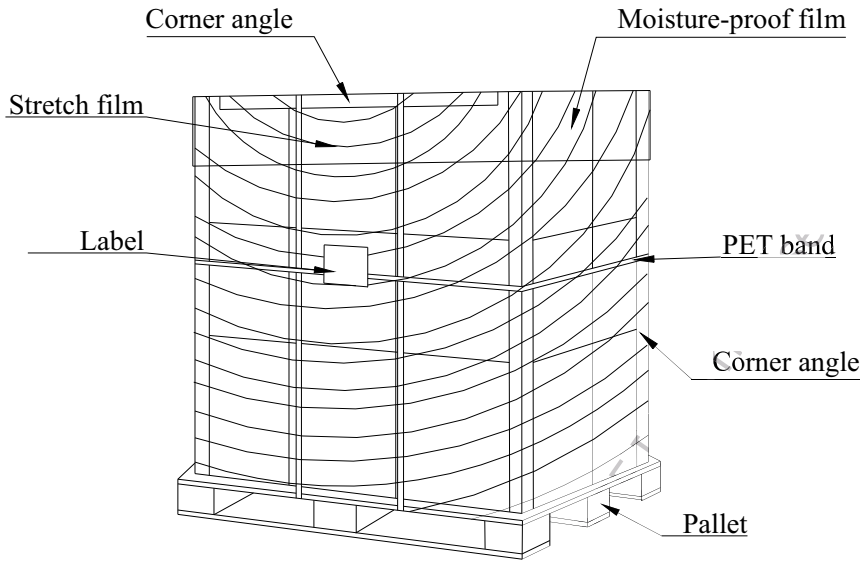
B. Carton Label:

8.2 Packing Methods



8.3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	5 pcs/box	1565(L)mm*380(W)mm*978(H)mm	135	
2	Pallet	1	1660(L)mm*1150(W)mm*144(H)mm	20	
3	Boxes per Pallet	5 boxes/Pallet (By Air) ; 3 Boxes/Pallet (By Sea)			
4	Panels per Pallet	25 pcs/pallet(By Air) ; 15 pcs/Pallet (By Sea)			
5	Pallet after packing	15 (by Air)	1660(L)mm*1150(W)mm*1122(H)mm	425(by Air)	
		30 (by Sea)	1660(L)mm*1150(W)mm*2244(H)mm	850(by Sea)	40ft HQ



9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9.1 Mounting Precautions

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

9.2 Operating Precautions

(1) The device listed in the product specification sheets was designed and manufactured for PID application under normal conditions. Normal condition is defined as below:

A. Temperature 5~40

B. Display pattern: continuously changing pattern (Not stationary).

If product will be used in extreme conditions such as high temperature/humidity, display stationary patterns or long operation time etc.., It is strongly recommended to contact AUO for Field Application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at Airports, Transit Stations, Banks, Stock Market, and Controlling systems.

(2) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(3) Response time depends on the temperature. (In lower temperature, it becomes longer..)

(4) Brightness depends on the temperature. (In lower temperature, it may become lower.) And in

lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(5) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(6) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(7) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

9.3 Operating Condition in PID Application

(1) . Normal operating condition

A. Operating temperature: 5~40℃

B. Operating humidity: 10~90%

C. Display pattern: dynamic pattern (Real display).

Note) Long-term static display would cause image sticking.

(2) Operation usage to protect against abnormal display due to long-term static display.

A. Suitable operating time: under 14 hours a day.

B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.

C. Periodically change background and character (image) color.

D. Avoid combination of background and character with large different luminance.

(3) Periodically adopt one of the following actions after long time display.

A. Running the screen saver (motion picture or black pattern)

B. Power off the system for a while

(4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.

(5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc…, it is strongly recommended to contact AUO for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

9.4 Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

9.5 Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9.6 Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

9.7 Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

