PRIME VIEW

PW080XU1

Version : 4.0

TECHNICAL SPECIFICATION

MODEL NO : PW080XU1

The content of this information is subject to be changed without notice.
Please contact PVI or its agent for further information.

☐Customer's Confirmation

Customer

Date

By

☐PVI's Confirmation

Confirmed By 

Prepared By 

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to 8” color TFT-LCD module, PW080XU1.
The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

2. Features

. Amorphous silicon TFT-LCD panel with Back-Light unit.

. Pixel in stripe configuration

. Compatible with NTSC and PAL system

. Slim and compact

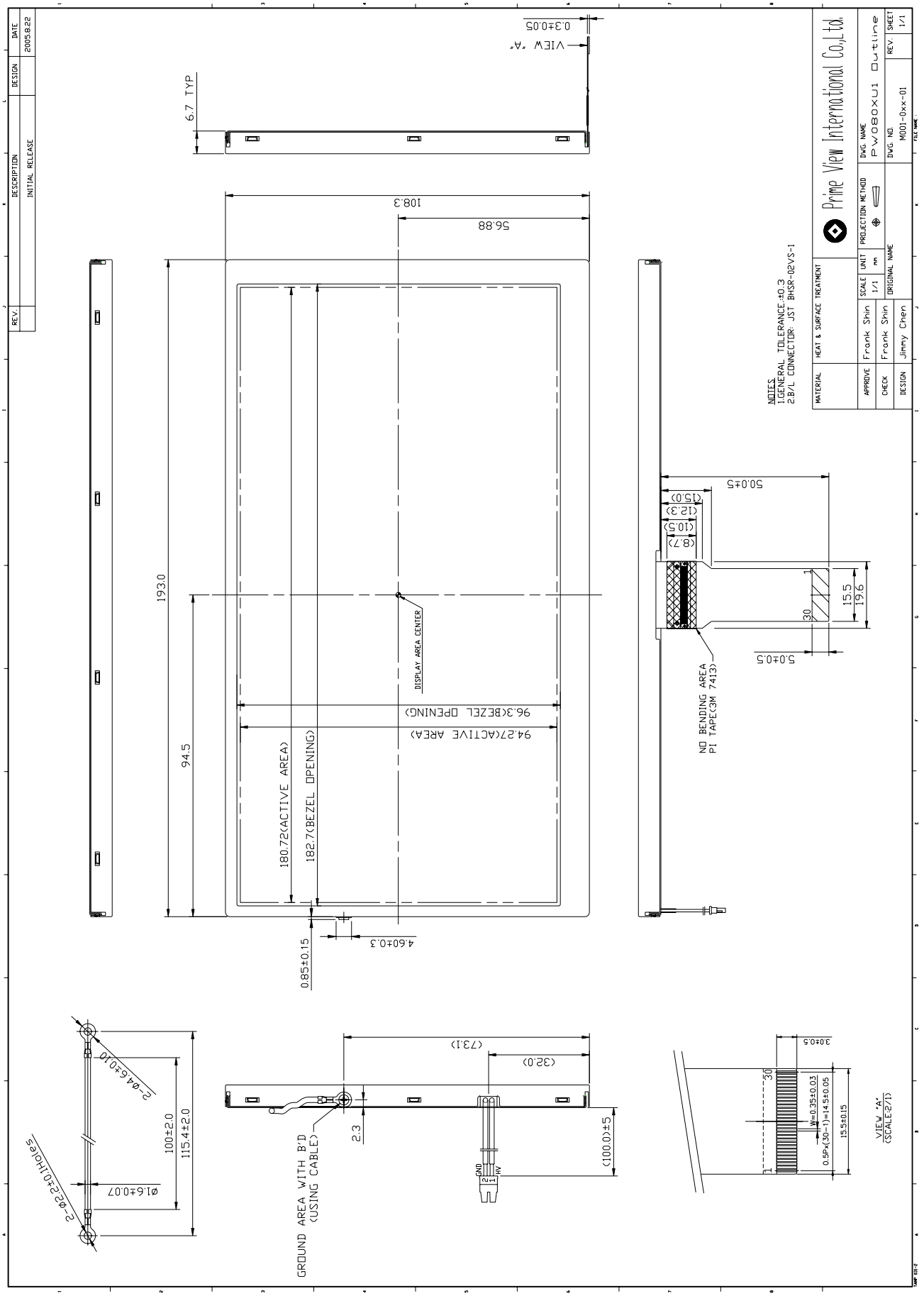
. Up / Down and Left / Right Image Reversion

. Support full , center , wide mode with PVI-1004D
(If customer use PVI-1004D , this panel doesn’t support zoom mode)

3. Mechanical Specifications

arameter	**Specifications**	**Unit**
Screen Size	8.0 (diagonal)	Inch
Display Format	480X(R,G,B)×220	Dot
Active Area	180.72 (H)×94.27 (V)	mm
Pixel Pitch	0.3765 (H)×0.4285 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	193.0 (W)ˣ108.3 (H)ˣ6.7 (D) (typ.)	mm
Weight	198±3	g
Back-light	CCFL,1 tube	
Surface Treatment	Anti-Glare	
Display mode	Normally white	

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

LCD Module Connector
FPC Down Connect , 30 Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V_{CCG}	I	Supply voltage of logic control circuit for gate driver	Note 5-3
3	NC	-	No connection	
4	V_{EE}	I	Negative power for gate driver	Note 5-2
5	NC	-	No connection	
6	V_{GH}	I	Positive power for gate driver	Note 5-4
7	NC	-	No connection	
8	STVD	I/O	Vertical start pulse	Note 5-5
9	STVU	I/O	Vertical start pulse	
10	CLK	I	Shift clock for gate driver	
11	U/D	I	Up / Down Control for gate driver	Note 5-5
12	OE3	I	Output enable for gate driver	
13	OE2	I	Output enable for gate driver	
14	OE1	I	Output enable for gate driver	
15	V_{COM}	I	Common electrode voltage	Note 5-1
16	STH2	I/O	Start pulse for source driver	Note 5-5
17	AGND	-	Ground for analog circuit	
18	V_R	I	Video Input R	
19	V_G	I	Video Input G	
20	V_B	I	Video Input B	
21	GND	-	Ground for digital circuit	
22	AV_{DD}	I	Supply power for analog circuit	Note 5-3
23	CPH1	I	Sampling and shift clock for source driver	
24	CPH2	I	Sampling and shift clock for source driver	
25	CPH3	I	Sampling and shift clock for source driver	
26	V_{CC}	I	Supply power for digital circuit	Note 5-3
27	R/L	I	Left / Right Control for source driver	Note 5-5
28	NC	I	No Connection	
29	OEH	I	Output enable for source driver	
30	STH1	I/O	Start pulse for source driver	Note 5-5

Note 5 – 1 : $V_{COM\ (TYP.)}$ = +6V_{PP}.

Phase of the video signal input and V_{COM}
The relation between these values could refer to 8-1 Operating condition.

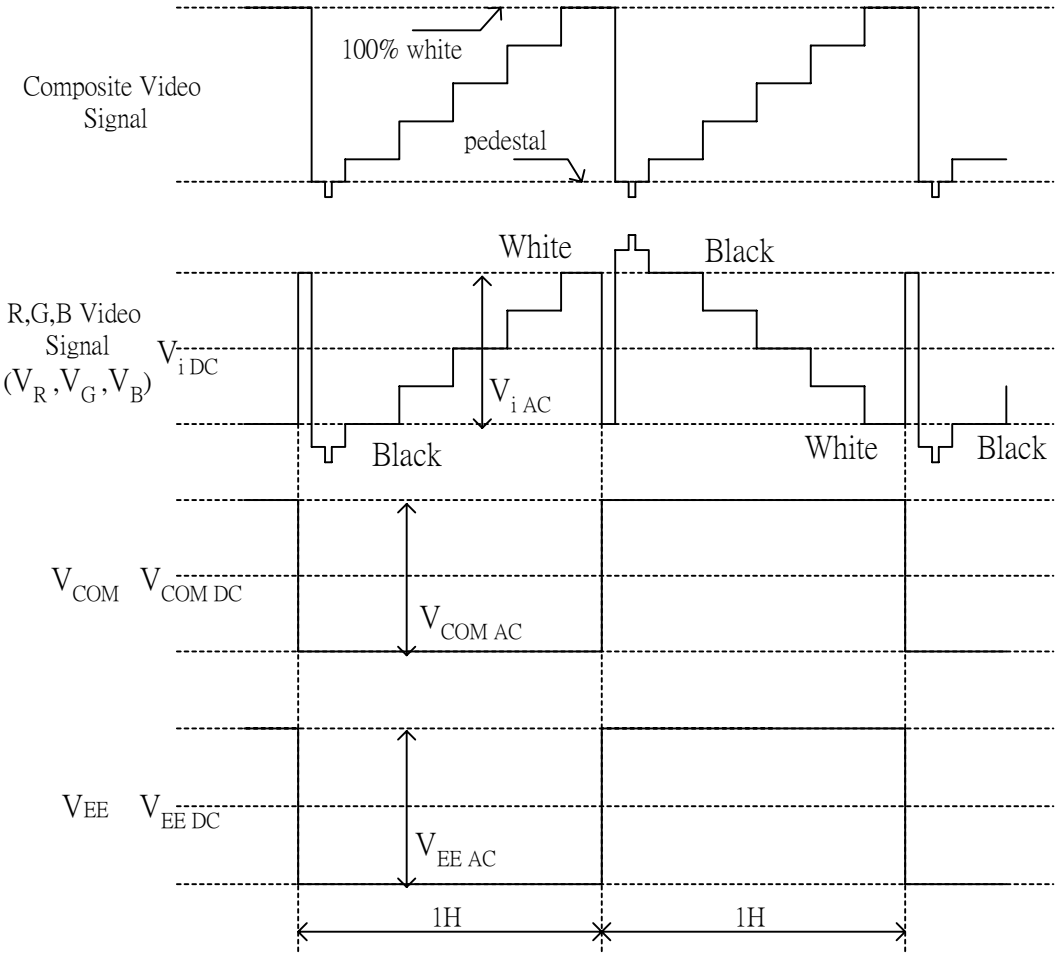


Fig.1

Liquid crystal transmission of the video signal input, V_{COM} and timing

	V_{COM}	
	H Level	L Level
Video Signal Input Maximum	Black	White
Video Signal Input Minimum	White	Black

White : maximum transmission / Black : minimum transmission

Note 5 – 2 : $V_{EE\ (TYP.)}$ = -12V

Note 5 – 3 : V_{CCG}, $V_{CC(TYP.)}$ = +3.3V , $AV_{DD\ (TYP.)}$= +5V

Note 5 – 4 : $V_{GH(TYP.)}$ = +17V

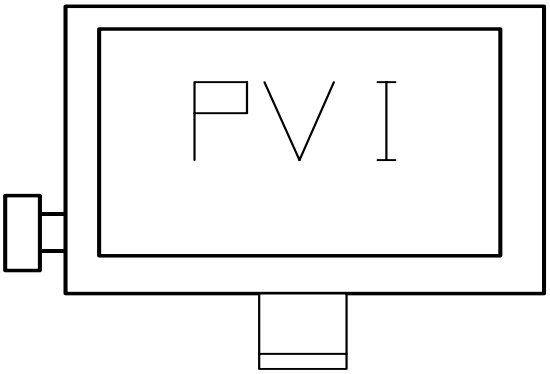
Note 5 – 5 : STH1, STH2 and R/L mode

R/L	STH1	STH2	Remark
High(V_{CC})	Input	Output	Left to Right
GND	Output	Input	Right to Left

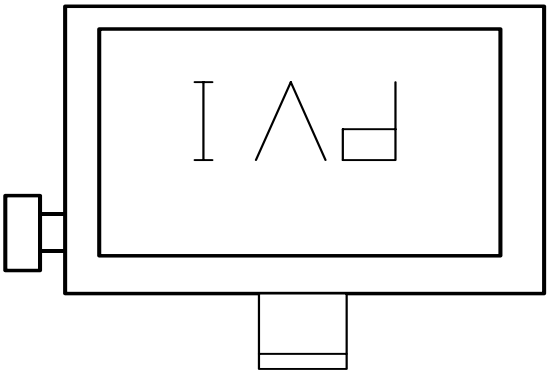
STVD, STVU and U/D mode

U/D	STVD	STVU	Remark
High(V_{CCG})	Input	Output	Down to Up
GND	Output	Input	Up to Down

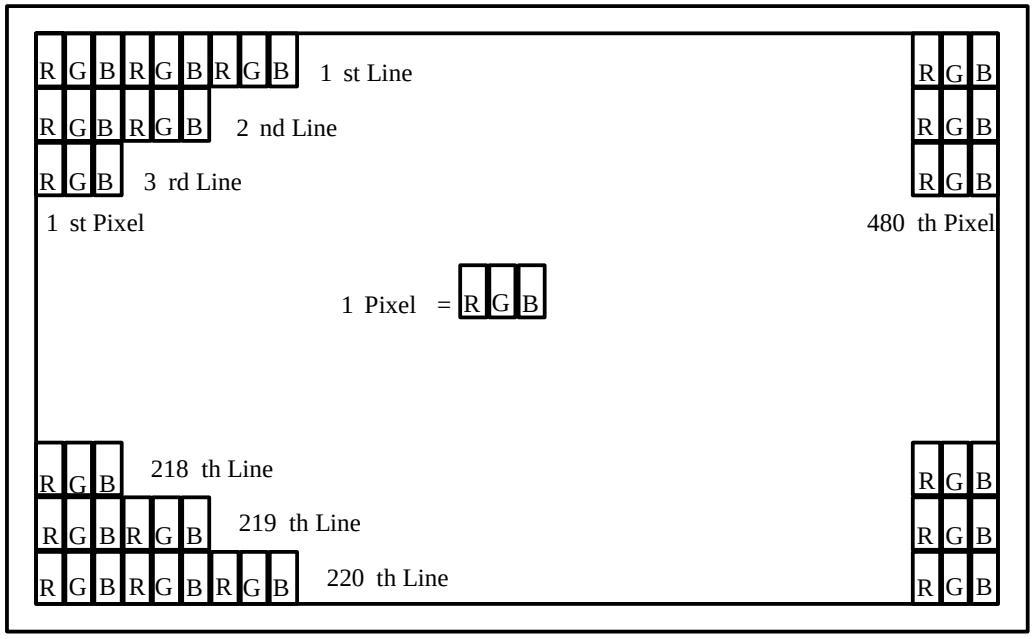
U/D(PIN 11)=Low R/L(PIN 27)=High



U/D(PIN 11)=High R/L(PIN 27)=Low



6. Pixel Arrangement



7. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

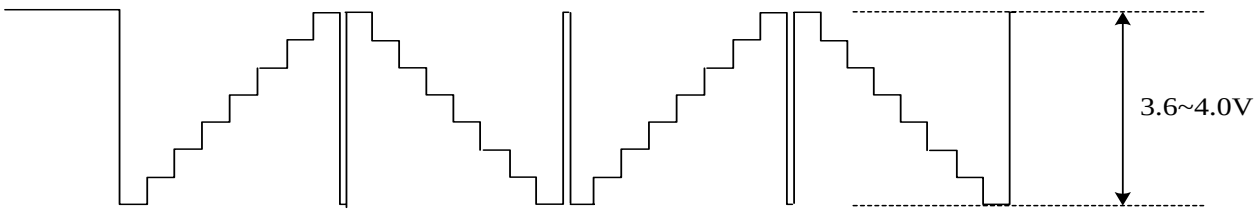
Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver		AV_{DD}	-0.3	+5.8	V	
		V_{CC}	-0.3	+7.0	V	
Supply Voltage for Gate Driver		V_{CCG}	-0.3	+7.0	V	
		V_{GH}-V_{EE}	-0.3	+40.0	V	
	H Level	V_{GH}	-0.3	+32.0	V	
	L Level	V_{EE}	-22.0	+0.3	V	

8. Electrical Characteristics

8-1) Recommended Driving condition for TFT-LCD panel

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage for Source Driver	Analog	AV_{DD}	+4.5	+5.0	+5.5	V	
	Logic	V_{CC}	+3.0	+3.3	+3.6	V	Depend on T/C signal voltage
			+4.5	+5.0	+5.5	V	
Supply Voltage for Gate Driver	V_{GH}		+15	+17	+19	V	
	$V_{EE\text{-}DC}$		-13.0	-12	-11	V	DC Component of
	$V_{EE\text{-}AC}$		-	+6.0	-	$V_{P\text{-}P}$	AC Component of
	Logic	V_{CCG}	+3.0	+3.3	+3.6	V	Depend on T/C signal voltage
			+4.5	+5.0	+5.5	V	
Analog Signal input Level (VR , VG , VB)	V_{IAC}		-	+3.6	+4.0	V	Note8-1
	V_{IDC}		-	+2.5	-	V	
Digital input voltage	H level	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	L level	V_{IL}	-0.3	-	0.3 V_{CC}	V	
Digital output voltage	H level	V_{OH}	0.7 V_{CC}	-	V_{CC}	V	
	L level	V_{OL}	-0.3	-	0.3 V_{CC}	V	
V_{COM} Voltage		V_{COMAC}	-	+6.0	-	$V_{P\text{-}P}$	AC Component of V_{COM}
		V_{COMDC}	-	1.5	-	V	DC Component of V_{COM} Note8-2

Note 8-1 : Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



Note 8-2 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 1.5V±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

8-2) Recommended driving condition for back light

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	513	570	627	Vrms	I_L=6mA
Lamp current	I_L	4	6	8	mA	Note 8-2
Lamp frequency	P_L	30	45	60	KHz	Note 8-3
Starting voltage (25℃) (Reference Voltage)	Vs	-	-	1209	Vrms	Note 8-4
Starting voltage (0℃) (Reference Voltage)	Vs	-	-	1260	Vrms	
Starting voltage (-20℃) (Reference Voltage)	Vs	-	-	1580	Vrms	

Note 8-2 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-3 : The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 8-4 : The "Max of starting voltage" means the minimum voltage of inverter to turn on the CCFL. and it should be applied to the lamp for more than 1 second to start up. Otherwise the lamp may not be turned on.

Back Light driving

Back Light Connector : JST BHSR-02VS-1, Pin No. : 2 , Pitch : 3.5 mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 8-5

Note 8-5 : Low voltage side of back light inverter connects with Ground of inverter circuits.

8-3) Power Consumption

Ta= 25 ℃

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	V_{GH} =+17V	0.87	0.114	mA	
Supply current for Gate Driver (Low level)	I_{EE}	V_{EE} =-12V	0.91	1.23	mA	V_{EE} center voltage
Supply current for Source Driver(Digital)	I_{CC}	V_{CC}=+3.3V	1.10	1.35	mA	
Supply current for Source Driver(Analog)	AV_{DD}	AV_{DD}=+5V	14.0	18.5	mA	
Supply current for Gate Driver (Digital)	I_{CCG}	V_{CCG}=+3.3V	0.014	0.018	mA	
LCD Panel Power Consumption	-	-	41.27	68.52	mW	Note 8-6
Back Light Lamp Power Consumption	-	-	3.30	-	W	Note 8-7

Note 8-6 : The power consumption for back light is not included.

Note 8-7 : Back light lamp power consumption is calculated by $I_L \times V_L$.

8-4) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t_r	-	-	10	ns	
Falling time	t_f	-	-	10	ns	
High and low level pulse width	t_{CPH}	9.2	9.6	10.0	MH_Z	CPH1~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STH1,STH2
STH hold time	t_{HDH}	20	-	-	ns	STH1,STH2
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STH1,STH2
STH period	t_H	61.5	63.5	65.5	μs	STH1,STH2
OEH pulse width	t_{OEH}	-	1.40	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	7.43	-	μs	
OEV pulse width	t_{OEV}	-	18	-	μs	OE1,2,3
CLK pulse width	t_{CKV}	-	31.75	-	μs	CLK
Clean enable time	t_{DIS2}	-	9.0	-	μs	
Horizontal display timing range	t_{DH}	-	480	-	t_{CPH}	
STV setup time	t_{SUV}	400	-	-	ns	STVU,STVD
STV hold time	t_{HDV}	400	-	-	ns	STVU,STVD
STV pulse width	t_{STV}	-	-	1	t_H	STVU,STVD
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}	-	10	-	t_H	
Vertical display timing range	t_{DV}	-	220	-	t_H	
VCOM rising time	t_{rCOM}	-	-	5	μs	
VCOM falling time	t_{fCOM}	-	-	5	μs	
VCOM delay time	t_{DCOM}	-	-	3	μs	
RGB delay time	t_{DRGB}	-	-	1	μs	

8-5) Signal Timing Waveforms

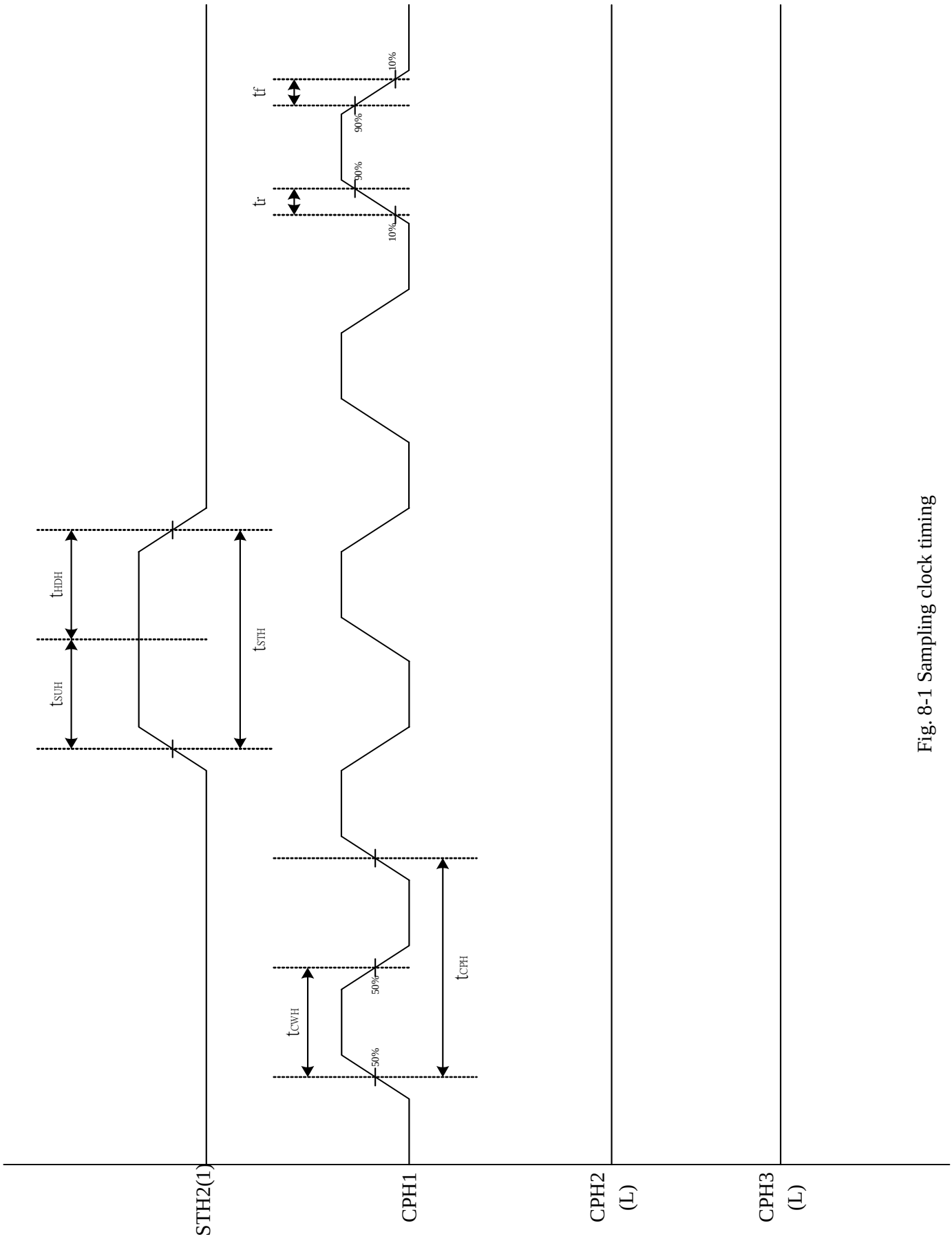


Fig. 8-1 Sampling clock timing

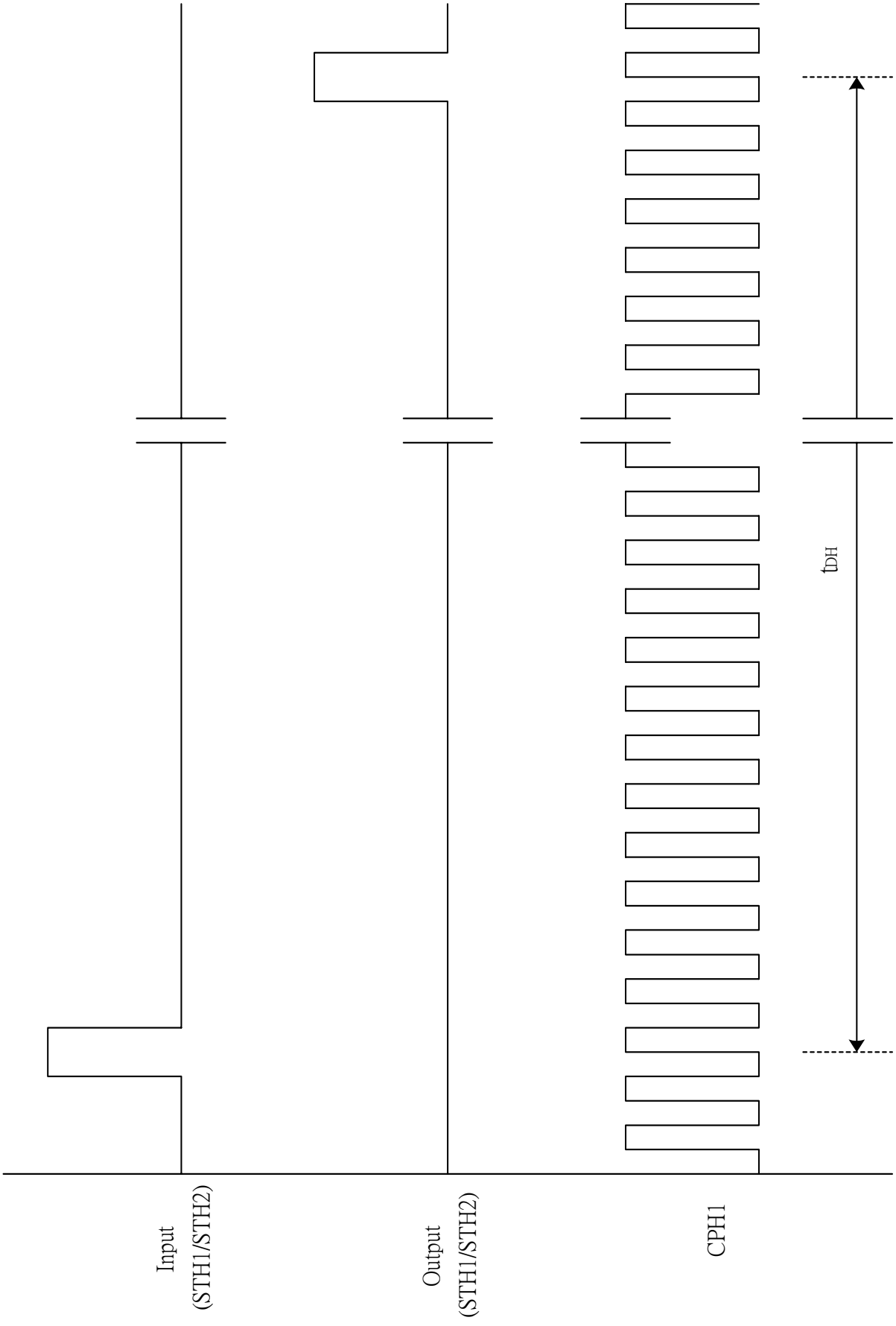


Fig. 8-2 Horizontal display timing range

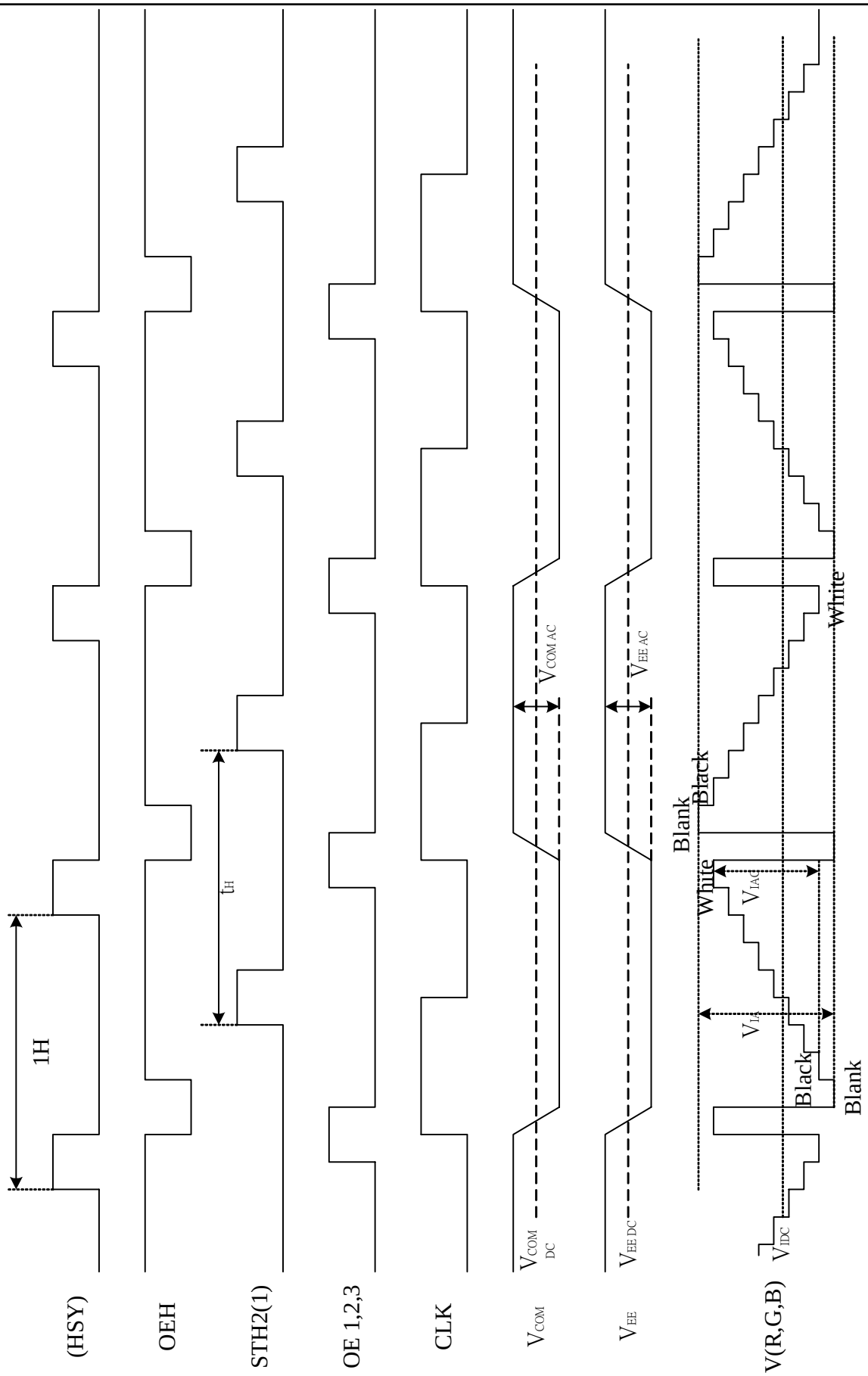
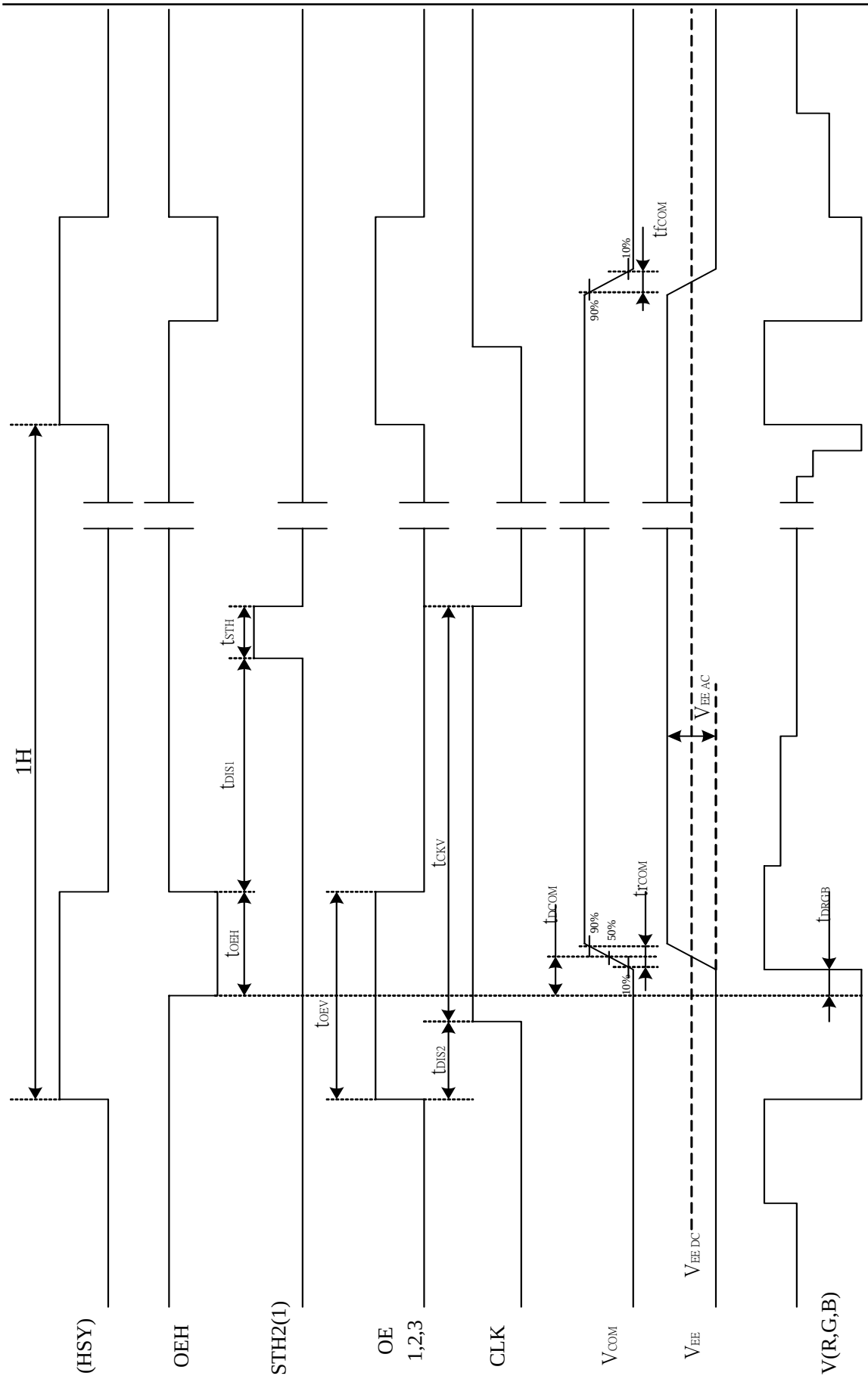


Fig. 8-3 (a) Horizontal timing



Note : The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

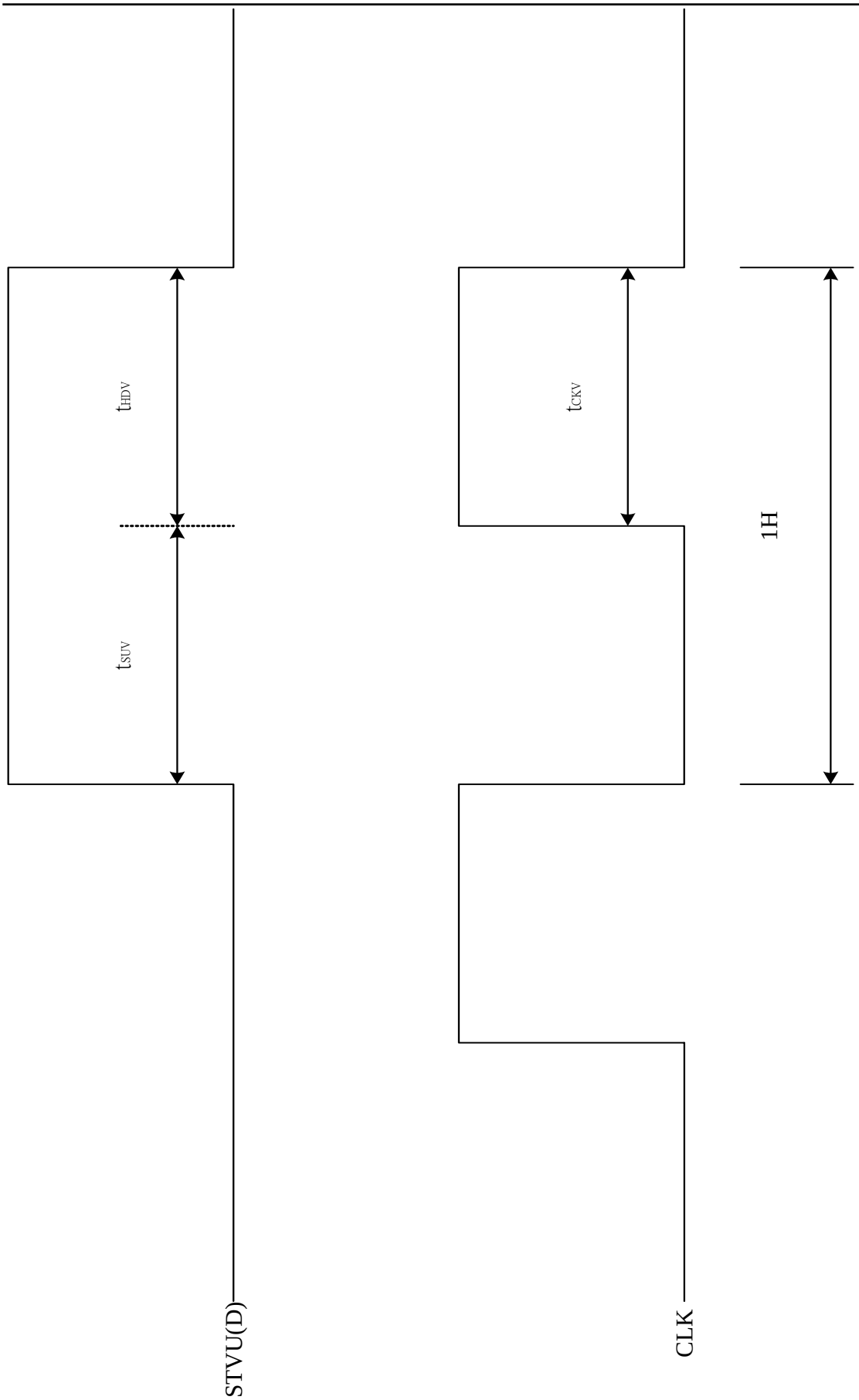


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

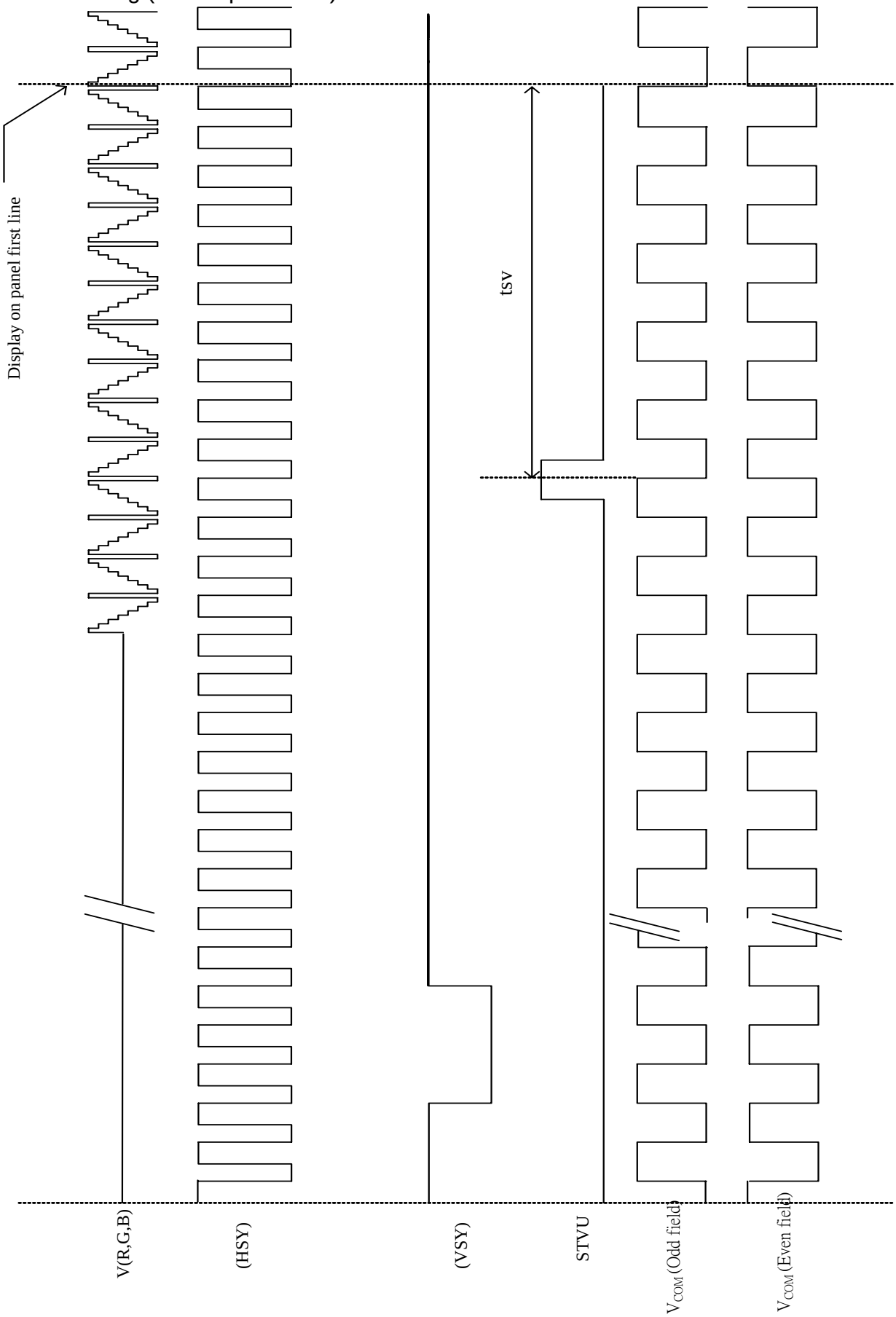


Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

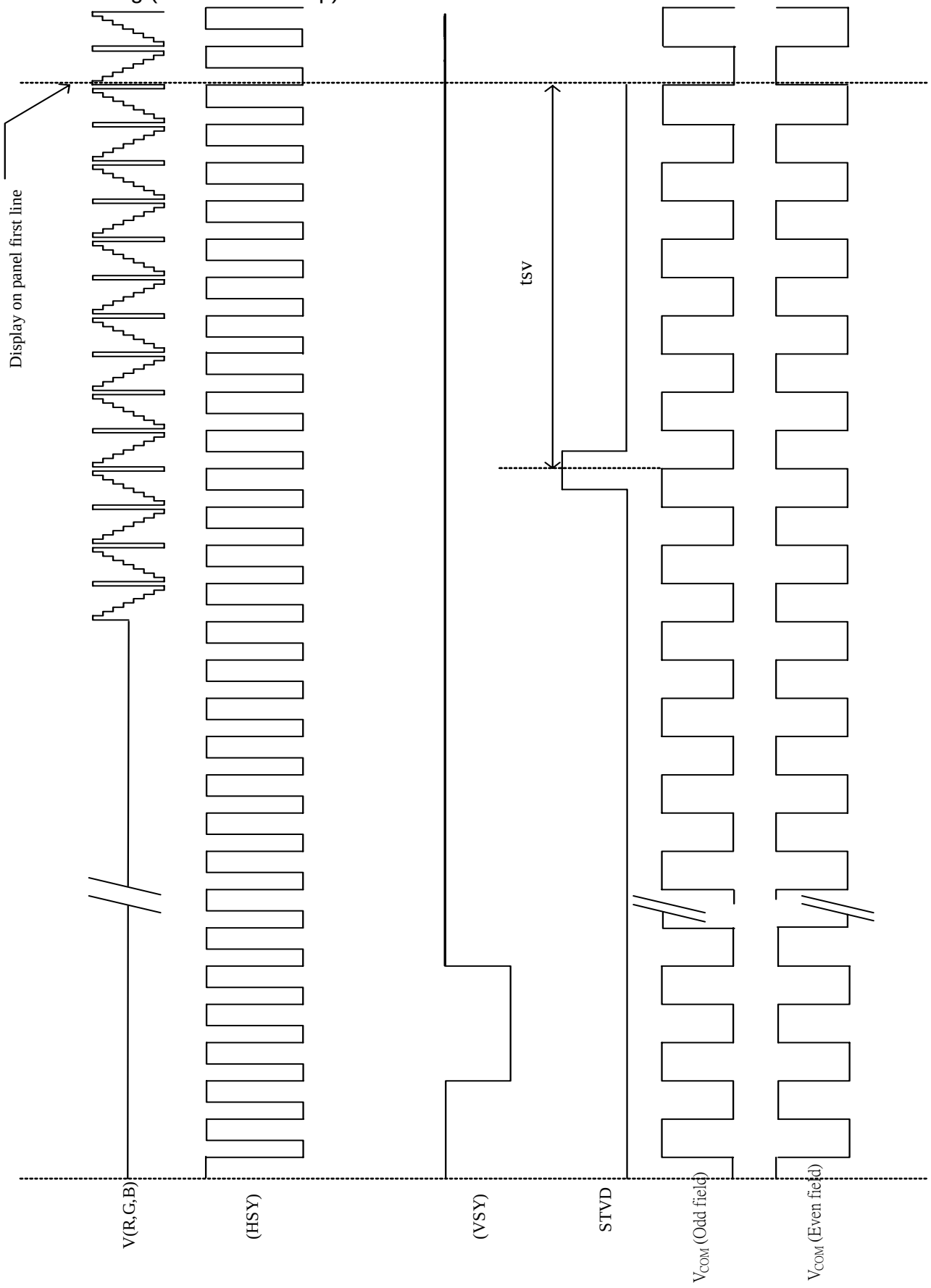
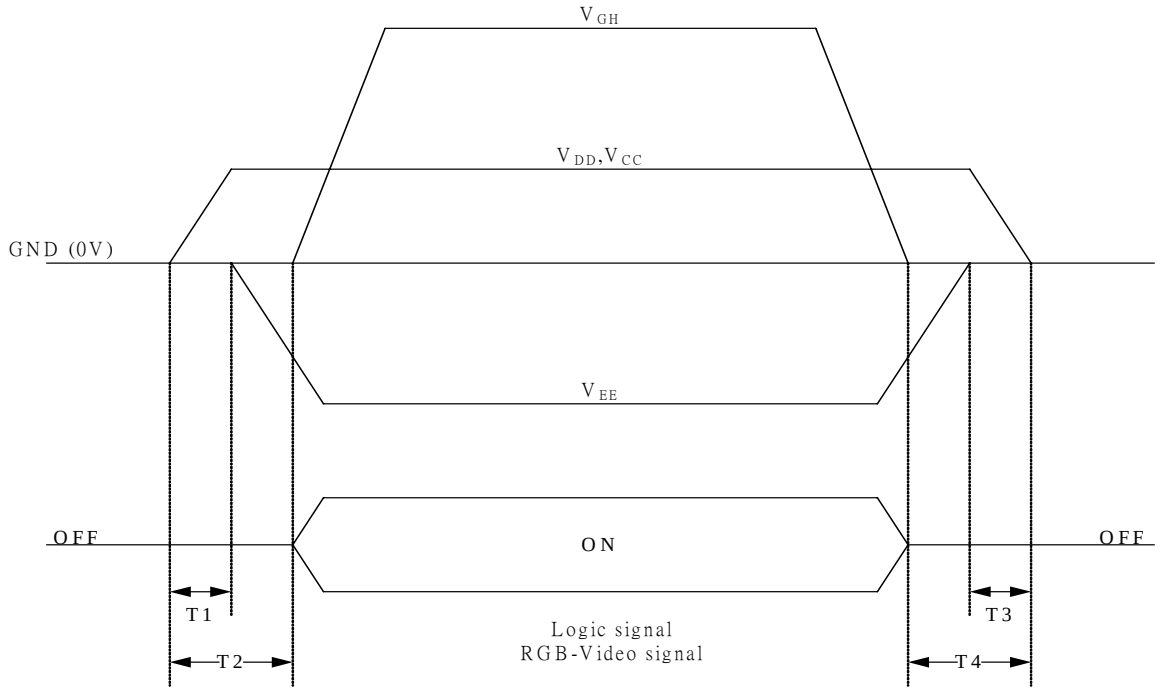


Fig. 8-5 (b) Vertical timing (From Dwon to Up)

9. Power on Sequence

The Power on Sequence only effect by V_{CC},GND,V_{DD},V_{EE} and $V_{GH,}$ the others do not care.



1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

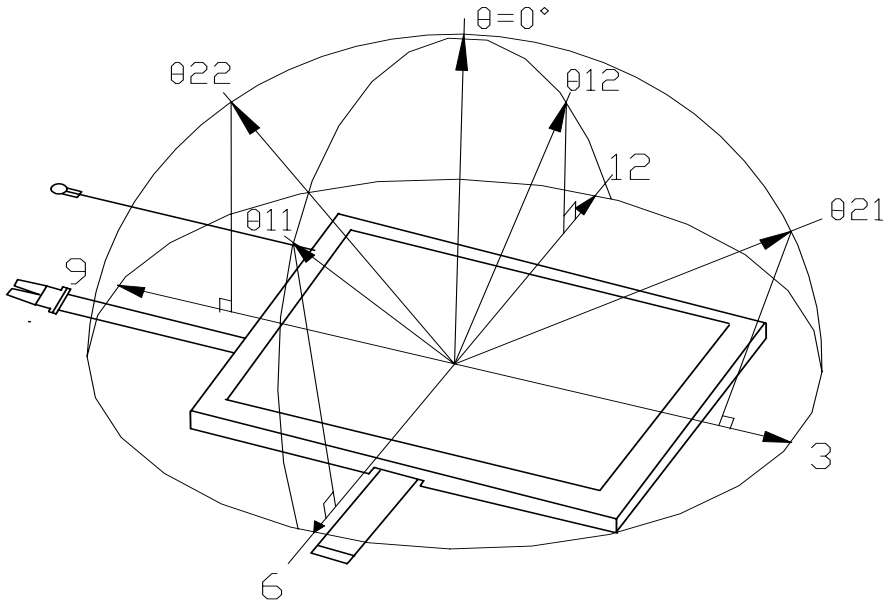
10. Optical Characteristics

10-1) Specification Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ 21, θ 22	CR≧10	45	50	-	deg	Note 10-1
	Vertical	θ 12		10	15	-	deg	
		θ 11		30	35	-	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350	-	-	Note 10-2
Response time	Rise	Tr	θ =0°	-	15	30	ms	Note 10-4
	Fall	Tf		-	25	50	ms	
Brightness		L	θ =0°	300	350	-	cd/㎡	Note 10-3
White Chromaticity		x	θ =0°	0.28	0.31	0.34	-	
		y		0.30	0.33	0.36	-	
Uniformity		U		70	75	-	%	Note 10-5
Lamp Life Time			+25℃	20000	30000	-	hr	

10-2)Testing configuration

Note 10-1 : The definitions of viewing angles



Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 8-2)

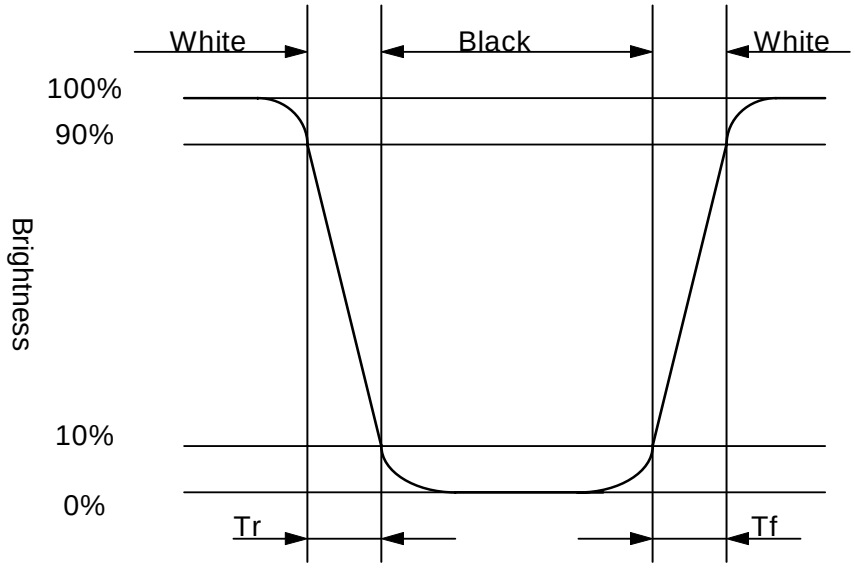
Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : 1.Topcon BM-7(fast) luminance meter 1°field of view is used in the testing (after 20~30 minutes operation).

2.Lamp current : 6 mA

3.Inverter model : TDK-347.

Note 10-4 : The definition of response time:

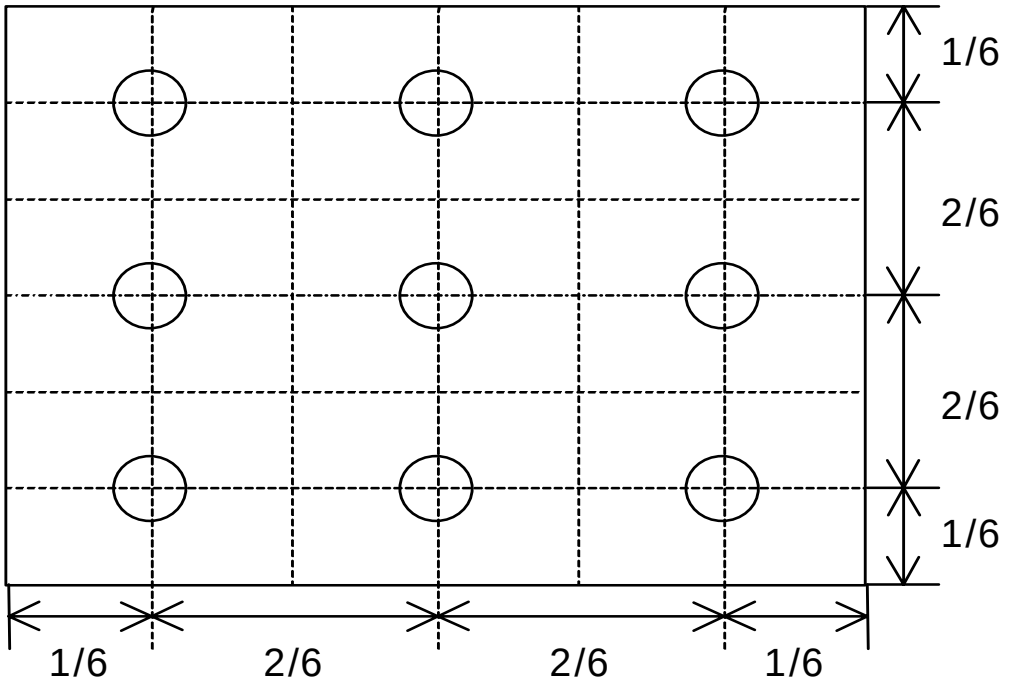


Note 10-5 : The uniformity of LCD is defined as

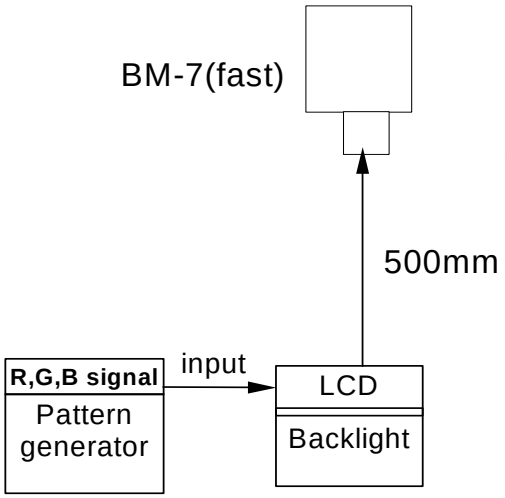
$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-5A or BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

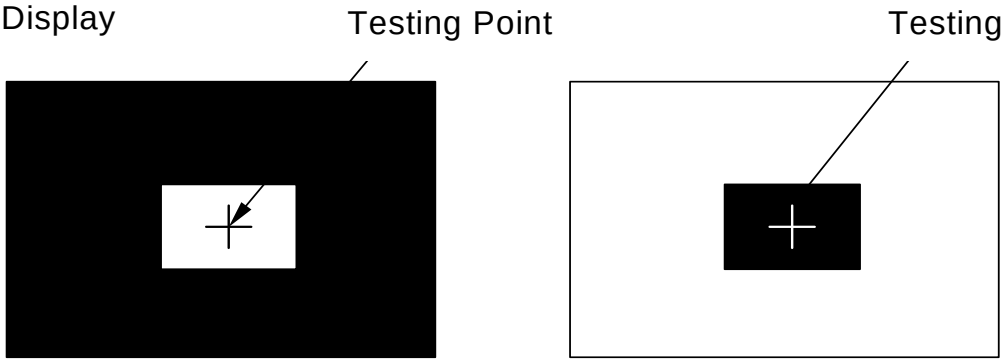


10-2) Testing configuration



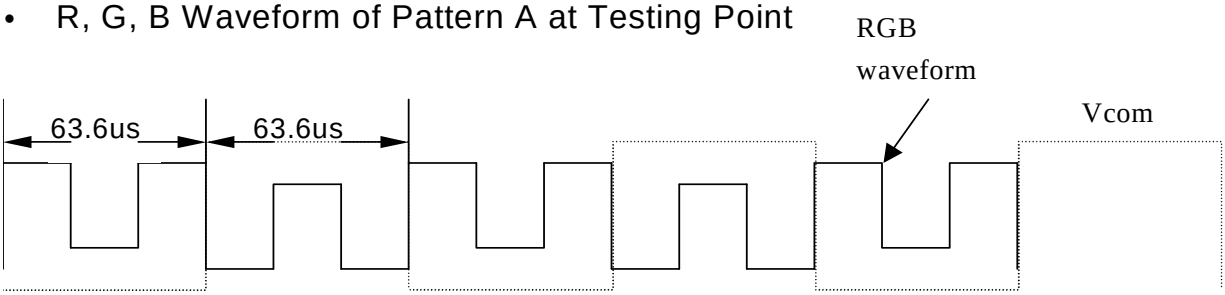
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display

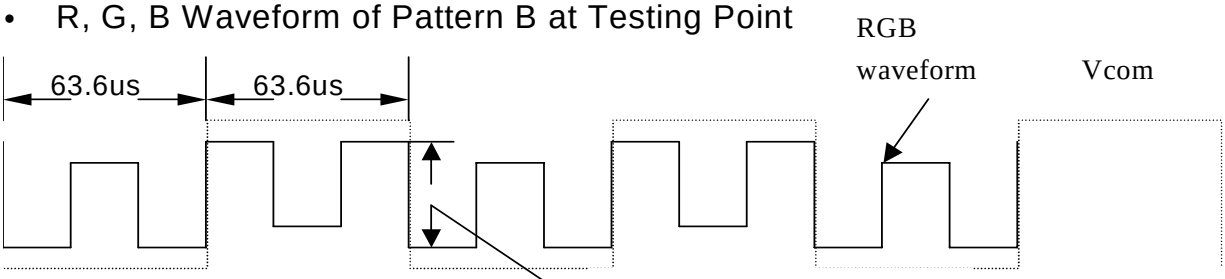


Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



11. Handling Cautions

11-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1.The noise from the backlight unit will increase.

2.The output from inverter circuit will be unstable.

3.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

12. Reliability Test

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70℃, 240 hrs
2	Low Temperature Storage Test	Ta = -20℃, 240 hrs
3	HighTemperature Operation Test	Ta = +60℃, 240 hrs
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH , 240 hrs
6	Thermal Cycling Test (non-operating)	-20℃ ⟷ +70℃, 200Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 H_Z Amplitude : 1 mm Sweep time : 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G , 6ms Direction : ±X , ±Y , ±Z Cycle : 3 times
9	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

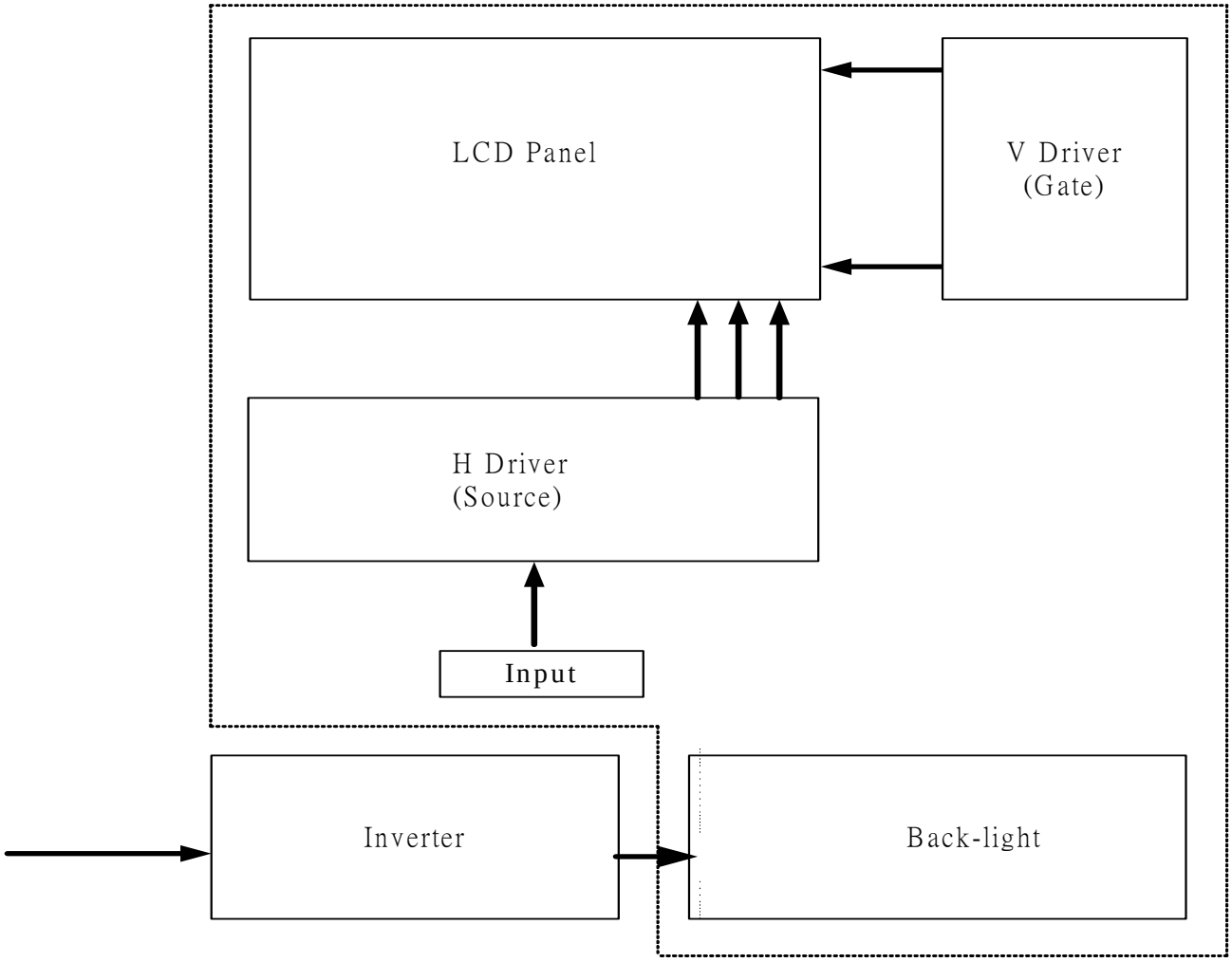
Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

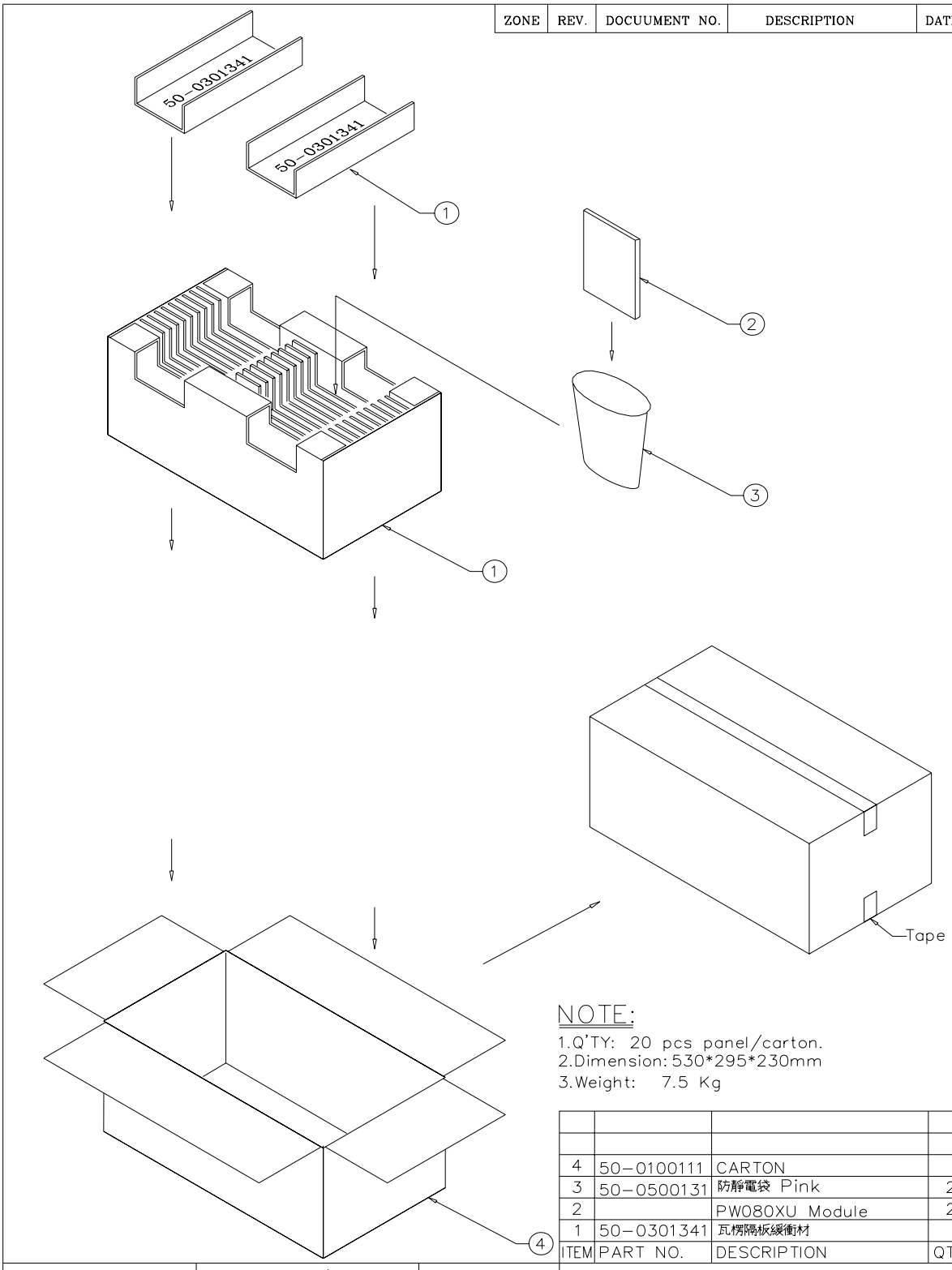
In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

13. Block Diagram



14. Packing

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:

1.Q'TY: 20 pcs panel/carton.
2.Dimension: 530*295*230mm
3.Weight: 7.5 Kg

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
4	50-0100111	CARTON	1	
3	50-0500131	防靜電袋 Pink	20	抗靜電
2		PW080XU Module	20	
1	50-0301341	瓦楞隔板緩衝材	1	上蓋+ 底座

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK

元太科技工業股份有限公司
Prime View International Co., Ltd.

APPROVE	Franks	'05.08.22	SCALE	UNIT	SHEET 1 OF 1
CHECK	Franks	'05.08.22			
DRAWN	Jimmyc	'05.04.28			

DWG.TITLE: PW080XU Module Packing Draw

MTL.NO. | DWG FILE: | REV. 01 | A4 SIZE

Revision History

Rev.	Eng.	Issued Date	Revised Contents
0.1		Apr, 14 . 2005	Preliminary
1.0	蔡弘毅	Aug, 25 . 2005	Release Verson
2.0	黃秀晶	Sep. 07 , 2005	Modify Page 3 2.Features . Support Multi Video Display Mode (With PVI timing controller : PVI-1004D) 變更爲 . Support full , center , wide mode with PVI-1004D (If customer use PVI-1004D , this panel doesn't support zoom mode)
3.0	黃秀晶	Oct . 03 . 2005	Modify Page 3 4. Mechanical Drawing of TFT-LCD Module
4.0	黃秀晶	Nov 07, 2006	Modify Page 23 12. Reliability Test LTOT from 0℃ to -20℃