TFT LCD Approval Specification

MODEL NO.: R208R1-L01 (IDT ITQX21J)

Customer: _____

Approved by: _____

Note:

時間	核准部門	審核	角色	投票
2010-05-10 14:27:12	APPL 產品管理處	張喻翔 (yhchang)	Director	Accept

REVISION HISTORY

Version	Date	Section	Description
Ver 2.0	Nov. 23, 06'	All	Index to IDT OEM I-921J-02
Ver 2.1	Dec. 08, 09'		Index to IDT OEM I-921J-03
		4.2	4.2 Image Retention spec delete
		4.0	4.0 Optical Characteristics Optical measurement warm up time update (from 30 minutes to 60 minutes)
		16.0	Add Section 16 Sea/Air Transportation Packing
Ver 2.2	Apr. 30, 10'		Index to IDT OEM I-921J-04
		2.2	Revise "Functional block diagram"- LVDS connector manufacturer
		5.1	Change LVDS J1/J2 connector manufacturer
		5.2	change J1(master)-Pin 1,2,3,4,5,7,8 Note(2): Change DAC IC manufacturer Add note(3) Change J2(slave)- Pin 4,5,7,8 Add Note(1),(2),(3),(4) RxEIN2+/RxEIN2- : DSP change to DE; V-S, H-S change to NA RxOIN2+/RxOIN2- : first NA change to DE
		5.3	"Electrical Characteristics", Vcm change to 1.25V "LVDS timing", change the symbal "Inverter Input Signal Electrical Characteristics", delete Vcont-IN, Note1 and Note2; add new Note(1)
		7.1	Revise timing characteristics, timing diagram and add Note(1) and Note(2)
		8.0	Add rush current(I_{rush}) spec Revise I_{in} spec Revise P_{in} spec Revise V_{in} rp spec Revise V_{in} ns spec Add note(1), (2), (3), (4)
		9.0	Revise power On/Off sequence diagram Add note(1),(2),(3),(4),(5),(6),(7)
		10.1	Insert new description of I2C
		10.4	I2C pulled-up resistor value change from 5.1Kohm to 4.7Kohm Note(3) I2C pulled-up resistor value change from 5.1Kohm to 4.7Kohm

Approval Specification

Type 20.8 QXGA Monochrome TFT/LCD Module
Model Name:ITQX21J

Document Control Number : OEM I-921J-04

i Contents

ii Record of Revision

Date	Document Revision	Page	Summary
Nov 21, 2005	OEM I-921J-01	All	First Edition for customer.
Feb 01, 2007	OEM I-921J-02	14	4.0 Optical Characteristics Update Optical equipment.
		15	4.2 Add Image Retention spec
		16	5.1 Connectors IF connector change to RoHs type Inverter connector change to RoHs type DC/DC card connector change to RoHs type
		38	14.0 Backlight Life spec add.
		39	15.0 Packaging Requirement add
		40,41,42	16.0 Label spec add
Dec 08, 2009	OEM I-921J-03	4	I Content (2007/11/23 OQC meeting minute, change Image Retention spec to IIS) Delete section 4.2 Image Retention
		15	4.2 Image Retention spec delete
		14	4.0 Optical Characteristics Optical measurement warm up time update (from 30 minutes to 60 minutes)
		42,43	Add Section 16 Sea/Air Transportation Packing
Apr 30, 2010	OEM I-921J-04	9	2.2 Revise “Functional block diagram”- LVDS connector manufacturer
		15	5.1 Change LVDS J1/J2 connector manufacturer
		16	5.2 change J1(master)-Pin 1,2,3,4,5,7,8 Note(2): Change DAC IC manufacturer Add note(3)
		17	Change J2(slave)- Pin 4,5,7,8 Add Note(1),(2),(3),(4)
		18	RxEIN2+/RxEIN2- : DSP change to DE; V-S, H-S change to NA RxOIN2+/RxOIN2- : first NA change to DE
		19	5.3 “Electrical Characteristics”, Vcm change to 1.25V “LVDS timing”, change the symbal
		20	“Inverter Input Signal Electrical Characteristics”, delete Vcont-IN, Note1 and Note2; add new Note(1)
		24	7.1 Revise timing characteristics, timing diagram and add Note(1) and Note(2)
		26	8.0 Add rush current(I_{rush}) spec Revise I_{in} spec Revise P_{in} spec Revise V_{in} rp spec Revise V_{in} ns spec
		26~28	Add note(1), (2), (3), (4)
		29	9.0 Revise power On/Off sequence diagram Add note(1),(2),(3),(4),(5),(6),(7)
		30	10.1 Insert new description of I2C
		30	10.4 I2C pulled-up resistor value change from 5.1Kohm to 4.7Kohm
		31	10.4 Note(3) I2C pulled-up resistor value change from 5.1Kohm to 4.7Kohm

1.0 Handling Precautions

- Damage to the panel or the panel electronics may result from any deviation from the recommended power on/off sequencing. The panel should not be hot plugged. Refer to the Power On/Off Sequence section in this Specification.
- Handle the panel with care. The LCD panel and CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may crack or break if dropped or subjected to excessive force.
- The CCFLs contain a small amount of Mercury so should not be disposed of to landfill. Dispose of as required by local ordinances or regulations.
- The LCD module contains small amounts of material having no flammability grade. The exemption conditions of the flammability requirements (4.4.3.3, IEC60950 or UL1950) should be applied.
- The panel may be damaged by the application of twisting or bending forces to the module assembly.Care should be taken in the design of the monitor housing and the assembly procedure to prevent stress damage to the panel especially the lamp cable and the lamp connector..
- Use standard earthing/grounding procedures to prevent damage to the CMOS LSI while handling the module.
- Use earthing/grounding procedures, an ionic shower, or similar to prevent static damage while removing the protective front sheet.
- The front polarizer can be easily damaged. Take care not to scratch the front surface with any hard or abrasive material. Dust, finger marks, grease etc. can be removed with a soft damp cloth (a small amount of mild detergent can be used on the damp cloth). Do not apply water or datergent directly to the front surface as this may cause staining or damage the electronic components.
- Never use any solvent on the front polarizer or module as this may cause permanent damage.
- Do not open or modify the module assembly.
- Continuous operation of the panel with the same screen content may result in some image sticking. Over 10 hours operation with the same content is not recommended.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by International Display Technology for any infringements of patents or other right of the third partied which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of International Display Technology or others.

2.0 General Description

This specification applies to the Type 20.8 Monochrome TFT/LCD Module 'ITQX21J'.

This module is designed for a LCD monitor style display unit. This module includes an inverter card for backlight.

The screen format and electrical interface are intended to support the QXGA (2048(H) x 1536(V)) screen.

Supported gray scale is 8-bit per 1(one) sub-pixel.

All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.

This model is the brightness enhancement version of the ITQX21A/H series and also meets RoHS requirements.

This model is intended for the migration version and therefore plug compatible to the previous models. Main changes were applied to the inverter and sourcing was changed to meet the requirements.

2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	528
Pixels H x V	2048(x3) x 1536
Active Area [mm]	423.9(H) x 318.0(V)
Pixel Pitch [mm]	0.207 x 0.207
Pixel Arrangement	Sub-pixel Vertical Stripe
Weight [grams]	2,300 Typ.
Physical Size [mm]	457.0(W) x 350.0(H) x 45.0(D) Typ.(w/inverter)
Display Surface Treatment	Anti Glare
Polarizer Pencil Hardness	3H Min.
Display Mode	Normally Black
Support Grayscale	8-bit per 1(one) sub-pixel
White Luminance [cd/m^2]	1,000 Typ.
Contrast Ratio	900 : 1 Typ. (In the dark room)
Optical Rise Time/Fall Time [msec]	50 Typ.
Input Voltage [V]	+12 +/- 5%
Power Consumption [W]	60 Typ
Electrical Interface	LVDS (5 Pairs) x 4 (Right x 2, Left x 2)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 **(Note1)** -20 to +60
Atmospheric Pressure	Maximum Pressure 104.0 [kPa] Minimum Pressure 67.4 [kPa] **(Note2)**

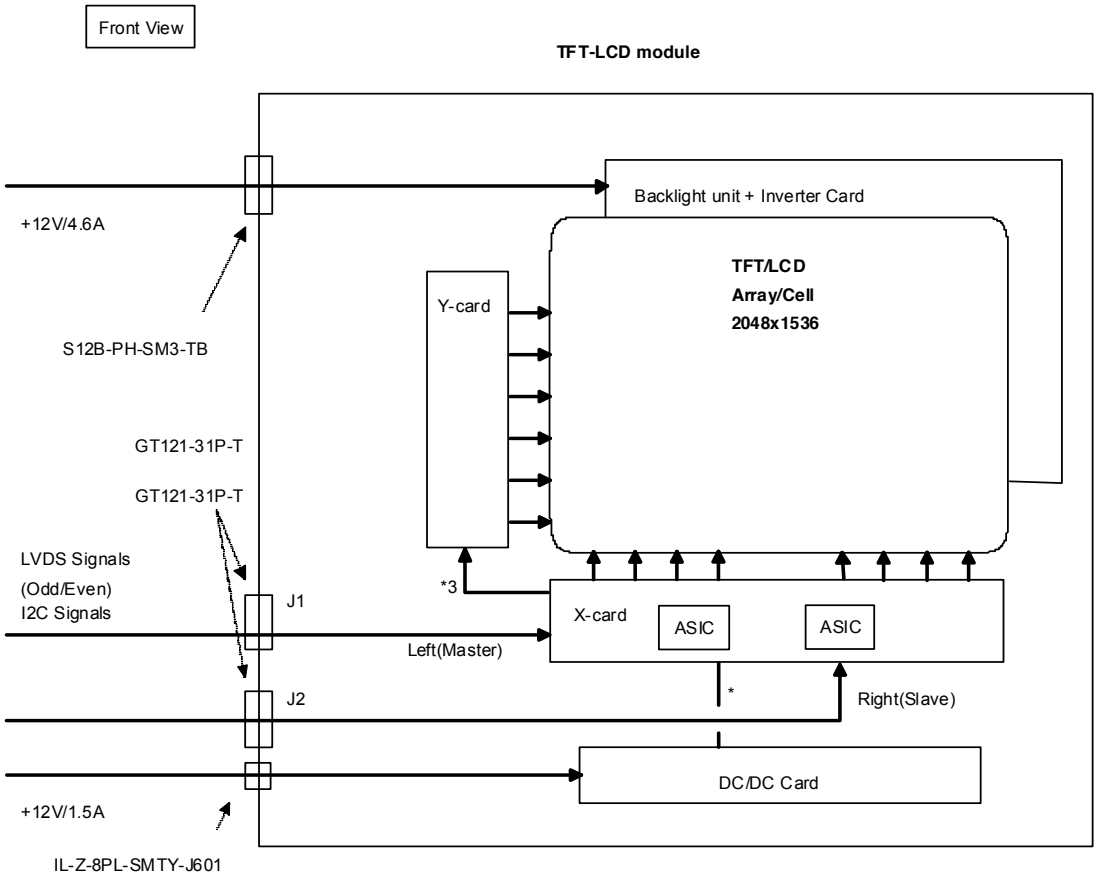
Note1 : Max. Operating Temperature 50 degree C in the Spec means the temperature measured for the point of the front surface of the LCD glass cell.

Note2 : The display system assembly is capable of being operated without affecting its operations over the pressure range as specified.

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 20.8 Monochrome TFT/LCD Module.

Type 20.8 Monochrome TFT-LCD Module Functional Block Diagram



*15.6V 450mA
3.3V 500mA
23.2V 20mA (for Y-card)
-5.5V 100mA (for Y-card)
3.3V 10mA (for Y-card)

2.2.1 Interface Summary

- 4 sets of LVDS interface for Video input (65MHz Typ per set, R/G/B 24 bits total)
- Voltage control or I2C interface (3.3V) control for Brightness and Contrast Control
- Power (+12V) for Logic
- Power (+12V) for Backlight

ITQX21J TFT-LCD module does not have any frame buffer. Image expansion (Scaling) should be managed by a device driving this module and the device should supply constant timings with the frame locked to this module.

ITQX21J has 4 sets of LVDS interface and they are bundled to two channels. The screen is divided into two half-size screens (Left and Right) and each channel controls one of the half-size screens.

Each LVDS interface is named as :

- LVDS-LE (Left screen, even dot) : Left channel
- LVDS-LO (Left screen, odd dot) : Left channel
- LVDS-RE (Right screen, even dot) : Right channel
- LVDS-RO (Right screen, odd dot) : Right channel

The Left channel consists of LVDS-LE and LVDS-LO and the Right channel consists of LVDS-RE and LVDS-RO.

Each channel has the following signals.

- 4 pairs of Video and timing signals for Even dots (8 bits per pixel)
- 4 pairs of Video signals for Odd dots (8 bits per pixel)
- 1 pair of Dot Clock for Even dots
- 1 pair of Dot Clock for Odd dots

3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+13.2	V	
Backlight Voltage	VBL	-0.3	+13.2	V	
Brightness control	VDIM	-0.3	+5.3	V	
Backlight on signal	BLON	-1.0	+5.3	V	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Humidity	HOP	8	80	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	**(Note 2)**
Shock			50 11	G ms	**(Note 2)** Half sine wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.
Max. Operating Temperature 50 degree C in the Spec means the temperature measured for the point of the front surface of the LCD glass cell.

Note 2 : Vibration Specification
- Sign Vibration:10-200-10Hz, 1.5G, 30 min, X, Y, Z Axis, Each One Time.
  Shock Specification
- Half sine wave:50G 11msec. -X+/-, -Y+/-, -Z+/- (Total 6 directions), Each one time Shock.

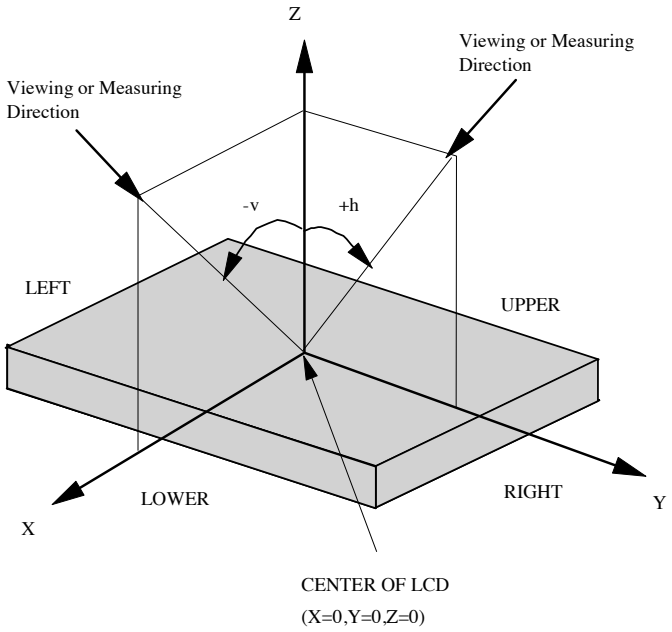
4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

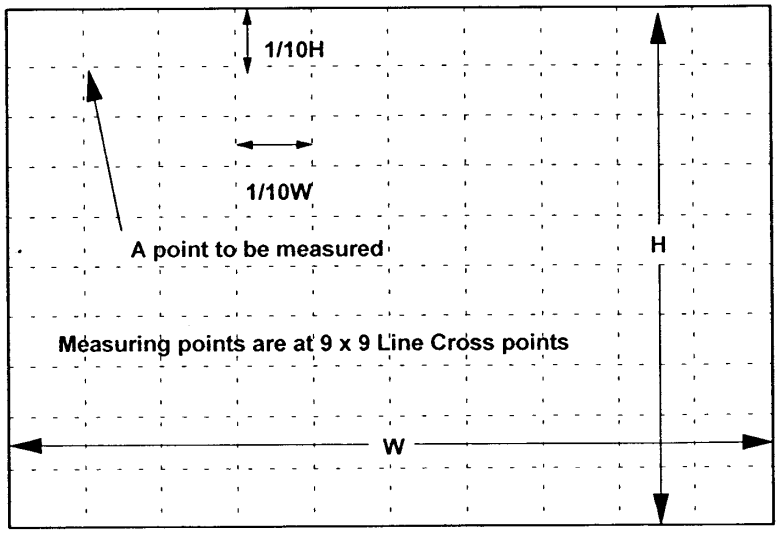
Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K∞10 (Left) Vertical (Upper) K∞10 (Lower)	85 85 85 85	- - - -
Contrast ratio		900	600 min
Response Time (ms)	Rising	25	-
	Falling	25	-
White Point	White x	0.294	±0.030
	White y	0.309	±0.030
Maximum White Luminance (cd/m^2)	VDIM-IN = 0V **(*1)**	1,000	860 min
Minimum White Luminance (%)	VDIM-IN = 3.0V	10	20 max.

(*1) Measure center of the screen.

The following is the note for the Optical Characteristics:



There is the Uniformity Measurement below:
'Lbright' represents the Luminance of the point that is brighter than the other point to be compared.
'Ldark' represents the Luminance of the point that is darker than the other point to be compared.Measuring points are shown in the following Fig.



Chromaticity and White Balance are defined as the C.I.E. 1931 x,y coordinates at the center of LCD.
The Standard Equipments are as shown below table.

Item	Standard Equipment
Viewing Angle	BM5A by Topcon Optical
Contrast	USB 2000 Ocean Optics
Response Time	6030 Lecory
White Luminance	USB 2000 Ocean Optics
Luminance Uniformity	USB 2000 Ocean Optics
Chromaticity	CS1000T by Konica Minolta
White Balance	USB 2000 Ocean Optics

The measurement is to be done after 60 minutes of Power-on of BackLight.
Unless otherwise specified, the ambient conditions are as following.

Ambient Temperature	:	25	+	2	(degreeC)
Ambient Humidity	:	25	-	85	(%)
Atmospheric Pressure	:	86.0	-	104.0	(kPa)

4.1 Luminance Uniformity

When the backlight is on with all the pixels in the unselected state (white), the luminance uniformity is defined as follows;

Where:
L_{bright} : The luminance of the brightest part of the area
L_{dark} : The luminance of the darkest part of the area

Adjacent Area

$$\text{Luminance Uniformity} = \frac{L_{dar\,k}}{L_{bright}} >= 0.80$$

over a circular area of 10 mm diameter placed anywhere on the screen.

2. Screen Total

$$\text{Luminance Uniformity} = \frac{L_{dar\,k}}{L_{bright}} >= 0.75$$

over the entire screen.

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

J1/J2 Connector (On X-cards)

J1/J2 Connector

Connector Name / Designation	Signal Connector
Manufacturer	LG
Type / Part Number	GT121-31P-TD-A
Mating connector	ZIF-31-0.625

Note : For pin assignment, please refer to '5.1.2 LCD Drive Connector Description'.

Inverter Connector (CN-1 on Inverter Card)

Connector Name / Designation	Signal Connector
Manufacturer	JST
Type / Part Number	S12B-PH-SM4-TB(LF)(SN)
Mating connector	PHR-12

DC/DC Connector Type (J601 on DC/DC Card)

Connector Name / Designation	Signal Connector
Manufacturer	JAE
Type / Part Number	IL-Z-8PL-SMTYE<R1500>
Mating connector	IL-Z-8S-S125C3

5.2 Interface Signal Description

The module uses a pair of LVDS receiver macro which is equivalent to THC63LVDF84A/R84A(THine Electronics, Inc.). LVDS is a differential signal transfer technology for LCD interface and high speed data transfer device. Transmitter shall be THC63LVDF83A/M83A(THine Electronics, Inc.) or equivalent.

J1 (Master) : Left side (Front View)

Signal Description (J1)

PIN #	SIGNAL NAME	Description
1	NC	Not connection should keep open.
2	NC	Not connection should keep open.
3	NC	Not connection should keep open.
4	NC	Not connection should keep open.
5	NC	Not connection should keep open.
6	DGND	Digital Ground
7	SDA	I2C data for brightness adjustment.
8	SCL	I2C clock for brightness.
9	DGND	Digital Ground
10	LGND	LVDS Ground
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXO3-	Negative LVDS differential data input. Channel O3 (odd)
13	RXOC+	Positive LVDS differential clock input. (odd)
14	RXOC-	Negative LVDS differential clock input. (odd)
15	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
16	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
17	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
18	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
20	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
21	RXE3+	Positive LVDS differential data input. Channel E3 (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXEC+	Positive LVDS differential clock input. (even)
24	RXEC-	Negative LVDS differential clock input. (even)
25	RXE2+	Positive LVDS differential data input. Channel E2 (even)
26	RXE2-	Negative LVDS differential data input. Channel E2 (even)
27	RXE1+	Positive LVDS differential data input. Channel E1 (even)
28	RXE1-	Negative LVDS differential data input. Channel E1 (even)
29	RXE0+	Positive LVDS differential data input. Channel E0 (even)
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)
31	LGND	LVDS Ground

Note:

(1) I2C address for Brightness and Contrast is '0101101'b.

(2) DAC for brightness adjustment is MAXIM DS1805 or equivalent.

(3) The method of SCL/SDA can refer to the section 10.0

J2 (Slave) : Right side (Front View)

Signal Description (J2)

PIN #	SIGNAL NAME	Description
1	BLON	Backlight on/off signal
2	VDIM_IN	Brightness Dimming Control Voltage
3	VDIM_OUT	Brightness Dimming Control Voltage Output Generated by I2C command
4	GMA_SEL	Gamma curve selection for customs(0 V: G2.2 3.3V: DICOM)
5	NC	Not connection should keep open.
6	DGND	Digital Ground
7	NC	Not connection should keep open.
8	NC	Not connection should keep open.
9	DGND	Digital Ground
10	LGND	LVDS Ground
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXO3-	Negative LVDS differential data input. Channel O3 (odd)
13	RXOC+	Positive LVDS differential clock input. (odd)
14	RXOC-	Negative LVDS differential clock input. (odd)
15	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
16	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
17	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
18	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
20	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
21	RXE3+	Positive LVDS differential data input. Channel E3 (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXEC+	Positive LVDS differential clock input. (even)
24	RXEC-	Negative LVDS differential clock input. (even)
25	RXE2+	Positive LVDS differential data input. Channel E2 (even)
26	RXE2-	Negative LVDS differential data input. Channel E2 (even)
27	RXE1+	Positive LVDS differential data input. Channel E1 (even)
28	RXE1-	Negative LVDS differential data input. Channel E1 (even)
29	RXE0+	Positive LVDS differential data input. Channel E0 (even)
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)
31	LGND	LVDS Ground

Note:

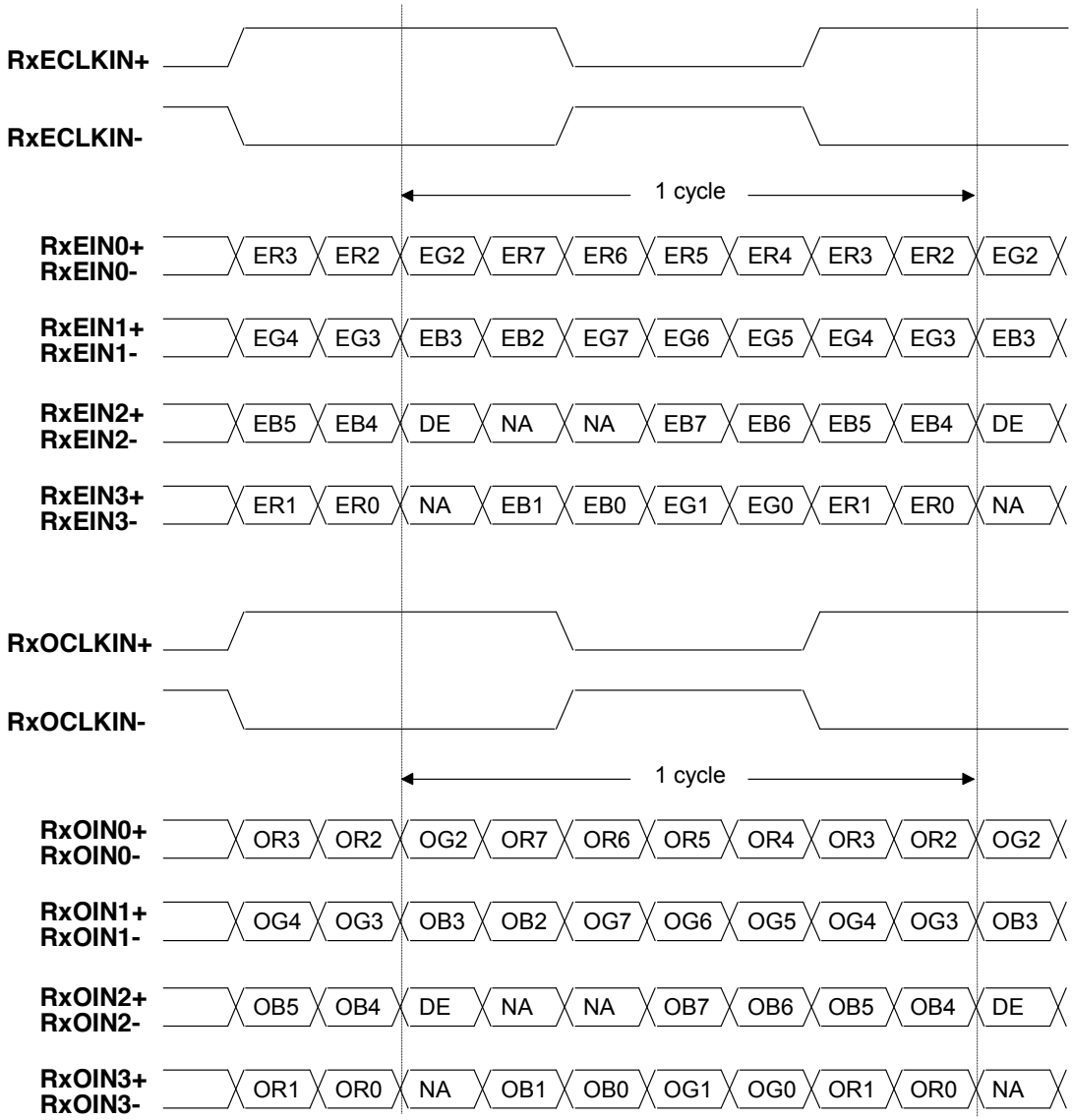
(1) Adjusting brightness is by I2C function of J1.

(2) If you don't use I2C to adjust brightness by J1, you should make the pin7, pin8 of J1 open.

(3) The module uses a 100-ohm resistor between positive and negative data lines of each receiver input.

(4) The method of operating VDIM can refer to the section 10.1

The following is LVDS Data Order :



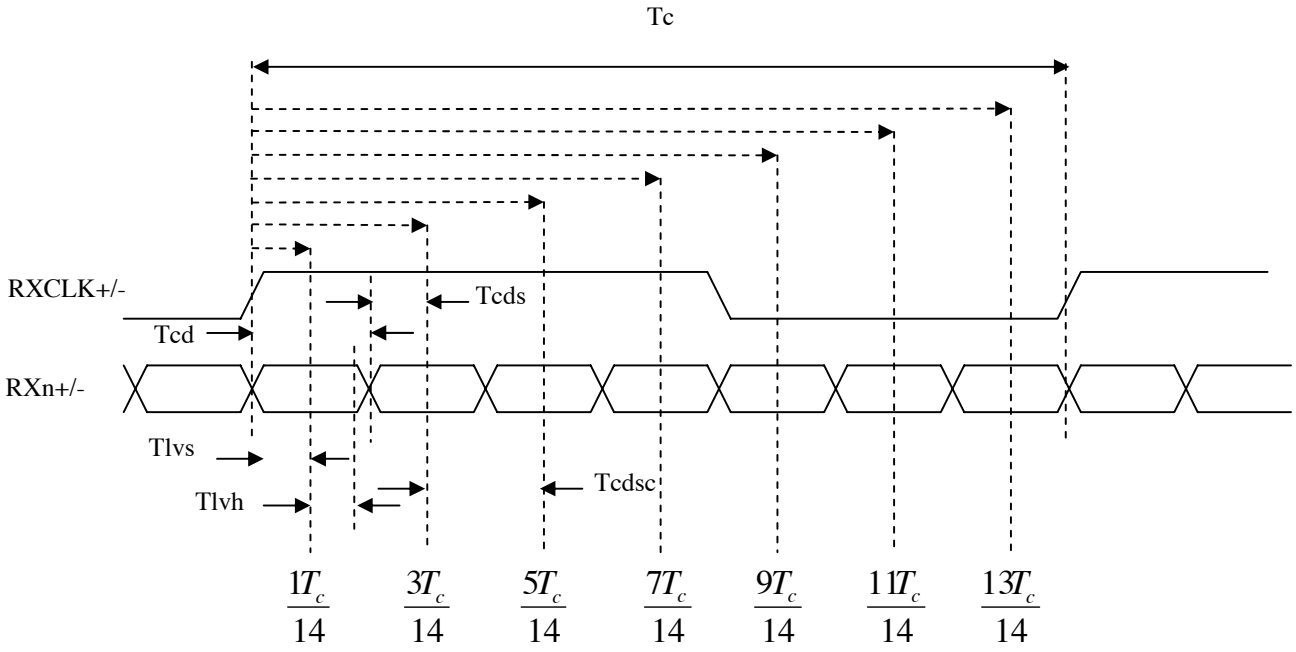
5.3 Interface Signal Electrical Characteristics

Each signal characteristics are as follows;

Electrical Characteristics

Parameter	Condition	Min	Max	unit
Vth	Differential Input High Voltage (Vcm=+1.25V)		100	mV
Vtl	Differential Input High Voltage (Vcm=+1.25V)	-100		mV

LVDS Timing



LVDS Macro AC characteristics.

Parameter	Symbol	Min	Typ	Max	Unit
LVDS Clock Cycle	Tc	15.15	15.38	16.66	[ns]
LVDS Data Cycle	Tcd		Tc/7		[ns]
Sample Data Setup Time (Tc=Typ.)	Tlvs	600			[ps]
Sample Data Hold Time (Tc=Typ.)	Tlvh	600			[ps]
Data Sample Time	Tcds		Tc/14		[ns]
Data Sample Cycle	Tcdsc		Tc/7		[ns]

Inverter Input Signal Electrical Characteristics

NAME	Description	Min	Typ	Max	Unit	Note
BLON	High voltage	2.0	3.3	5.25	V	
	Low voltage	-0.1	0.0	0.8	V	
	Current	-1.0	-	1.0	mA	
VDIM-IN	Input Voltage range	0.0	-	3.0	V	0V:Brightness Max 3V:Brightness Min
	Current	-1.0	-	1.0	mA	

Note
(1)The method of operating VDIM can refer to the section 10.1

5.4 Inverter Connector Signal Description

Inverter Connector Signal Description

PIN #	SIGNAL NAME	Description
1-5	VBL	+12.0V Power Source for backlight
6-10	RTN	Ground for VBL line
11	(RESERVED)	
12	(RESERVED)	

Inverter Input Signal Electrical Characteristics

NAME	Description	Min	Typ	Max	Unit	Note
VBL	B/L Unit Drive Voltage	11.4	12	12.6	V	

5.5 DC/DC Connector Singal Description

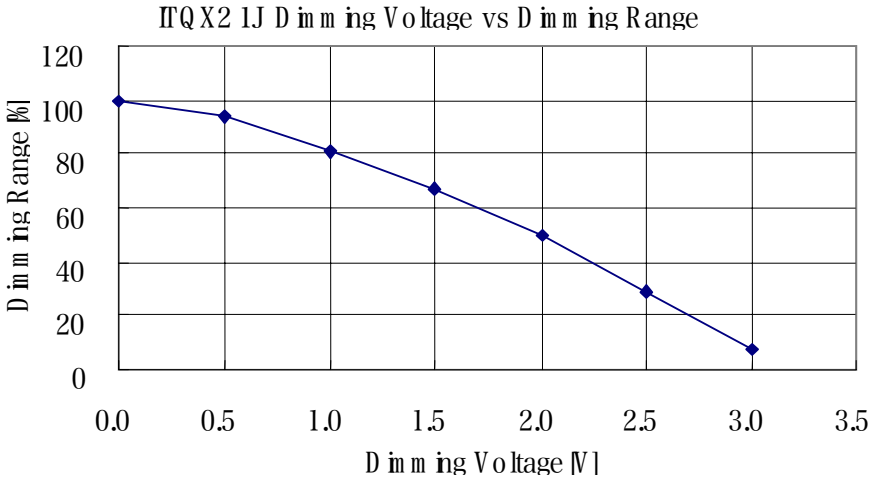
DC/DC Connector Signal Description

PIN #	SIGNAL NAME	Description
1-4	RTN	Ground for Vin line
5-8	Vin	+12.0V Power Supply for LCD Driver Cards (Except Inverter and Backlight)

DC/DC Input Signal Electrical Characteristics

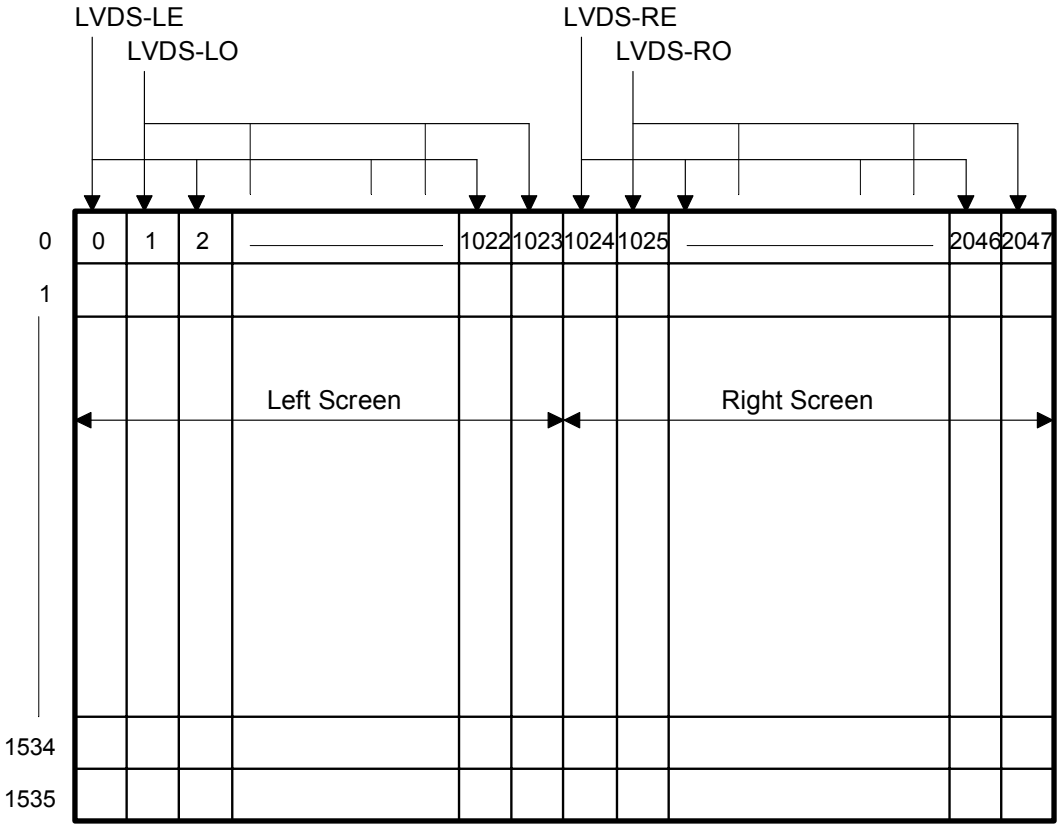
NAME	Description	Min	Typ	Max	Unit	Note
Vin	Logic/LCD Drive Voltage	11.4	12	12.6	V	

The following chart is the VDIM vs Dimming Range for your reference.



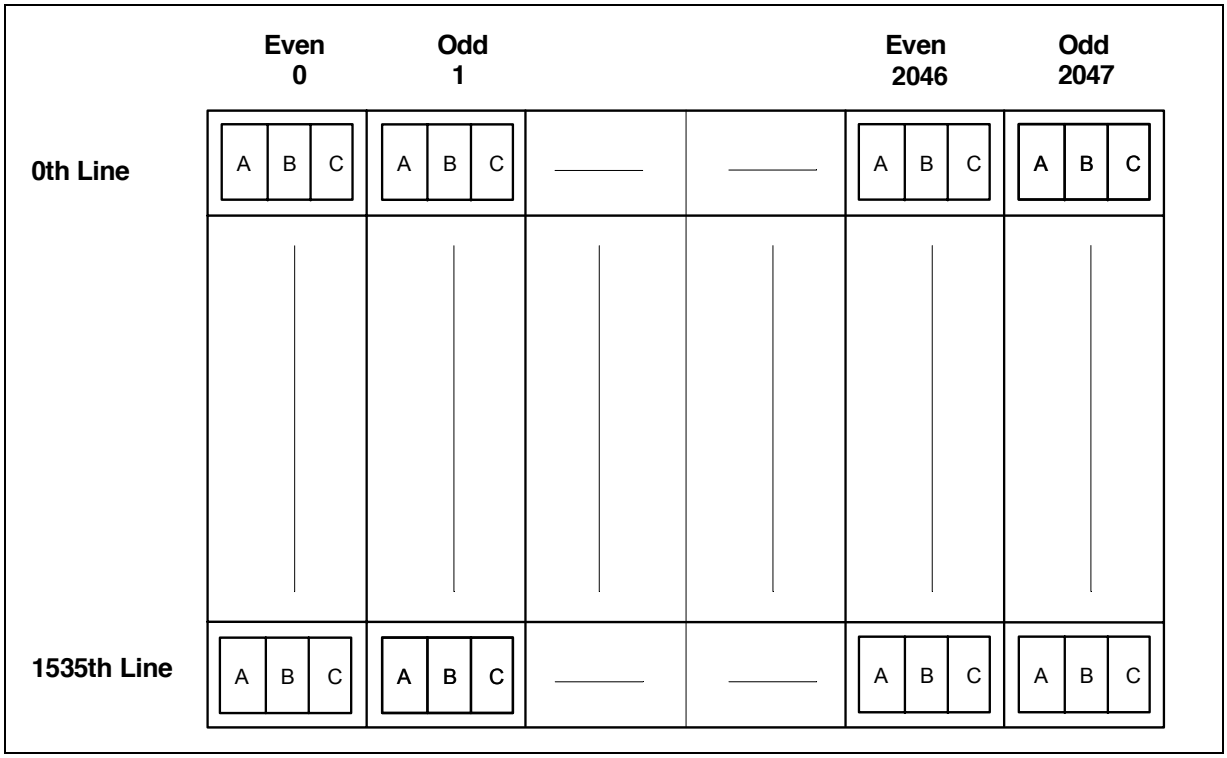
6.0 Pixel format image

Screen Format



Following figure shows the relationship between the input signals and the LCD pixel format image. Each sub-pixel data(A,B,C) of an Even and the right adjacent Odd pixel unit are sampled at the same time.

Pixel Arrangement



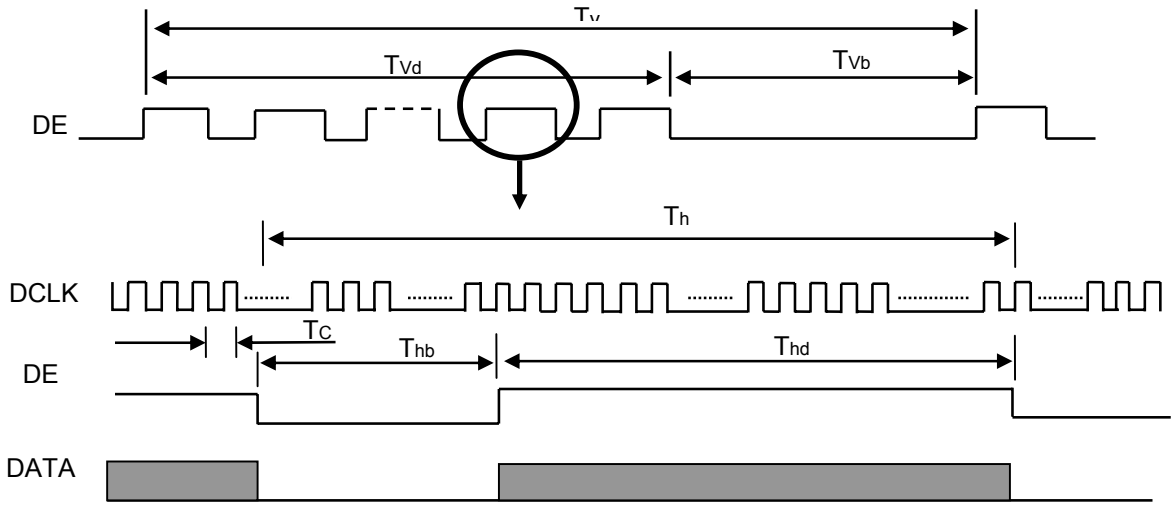
7.0 Interface Timings

Following is the Video timing diagrams per channel (a half screen refresh) to be converted to/from the LVDS interface signals.

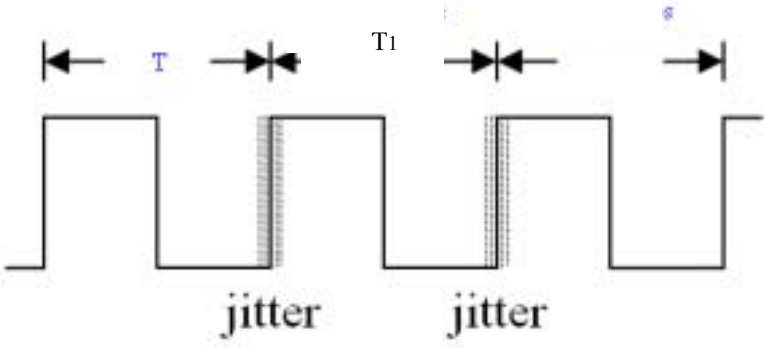
7.1 Timing Characteristics

Timing Characteristics

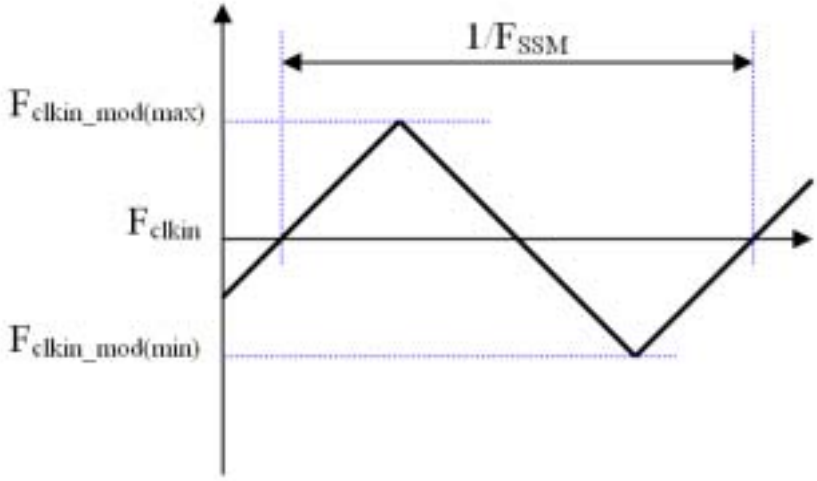
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS clock	Frequency	Fc	60	65	66	MHz	
	Period	Tc	15.15	15.4	16.66	ns	
	Input cycle to cycle jitter	T_{rcl}	---	---	250	ps	(1)
	Spread spectrum modulation range	F_{clkin_mod}	---	---	1.02*Fc	MHz	(2)
	Spread spectrum modulation frequency	F_{SSM}	---	---	200	KHz	
	High Time	Tch	-	4/7	-	Tc	-
	Low Time	Tcl	-	3/7	-	Tc	-
Vertical Active Display Term	Frame Rate	Fr	-	60	-	Hz	Tv=Tvd+Tvb
	Total	Tv	1546	1612	1628	Th	-
	Display	Tvd	1536	1536	1536	Th	-
	Blank	Tvb	Tv-Tvd	76	Tv-Tvd	Th	-
Horizontal Active Display Term	Total	Th	640	672	700	Tc	Th=Thd+Thb
	Display	Thd	512	512	512	Tc	-
	Blank	Thb	Th-Thd	160	Th-Thd	Tc	-



Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



Note (2) The SSCG (Spread spectrum clock generator) is defined as below figures.



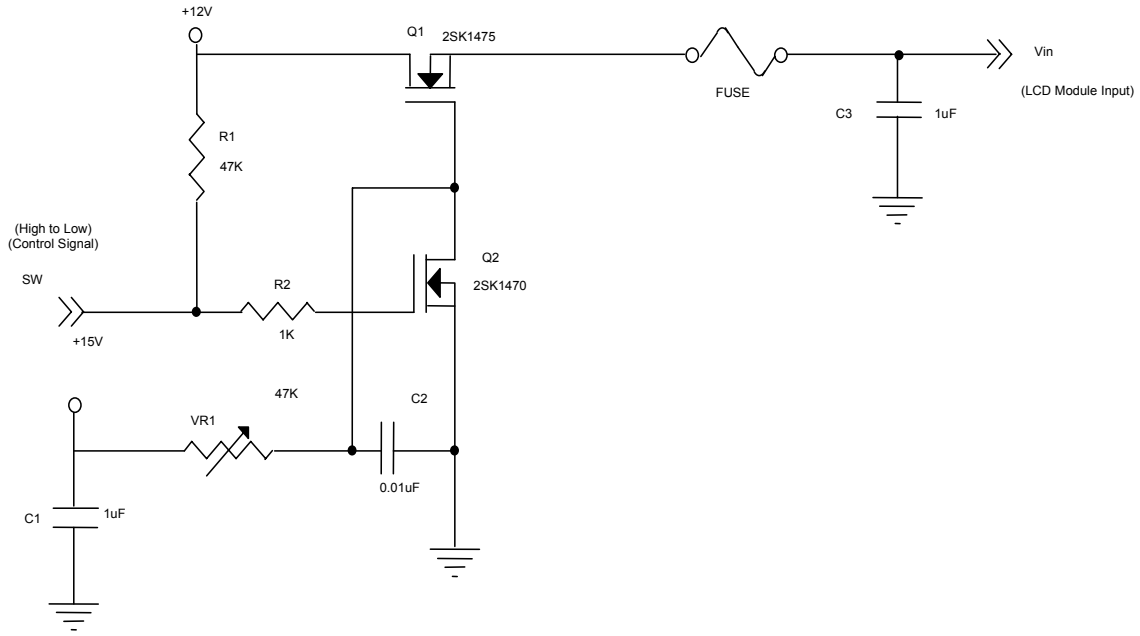
8.0 Power Consumption

Input power specifications are as follows;

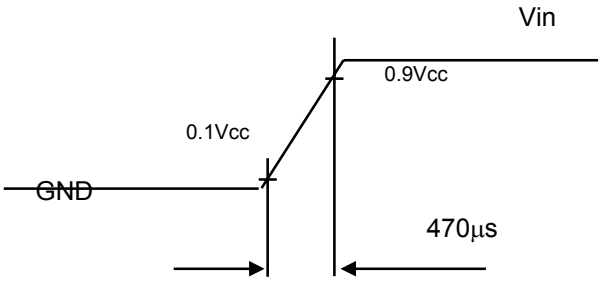
SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
Vin	Logic/LCD Drive Voltage	11.4	12	12.6	V	
Irush	Rush Current			3.8	A	(2)
Iin	White		0.73	0.92	A	(3)a
	Black		0.43	0.54	A	(3)b
	Vertical Stripe		0.68	0.85	A	(3)c
Pin	Vin Power		8.76	10.2	W	(4)
Vin rp	Allowable Logic/LCD Drive Ripple Voltage			300	mVp-p	
Vin ns	Allowable Logic/LCD Drive Ripple Noise			300	mVp-p	
VBL	Backlight power Voltage	11.4	12	12.6	V	
PBL	Backlight Power consumption		51	56	W	Brightness=max

Note (1)The module is recommended to operate within specification ranges listed above for normal function.

Note (2)Measurement Conditions:

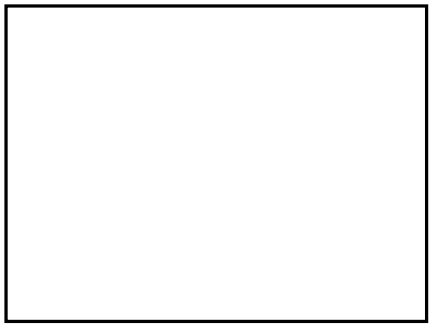


Vcc rising time is 470μs



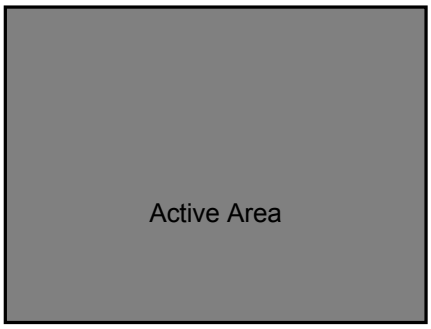
Note (3)The specified power supply current is under the conditions at Vin = 12.0 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

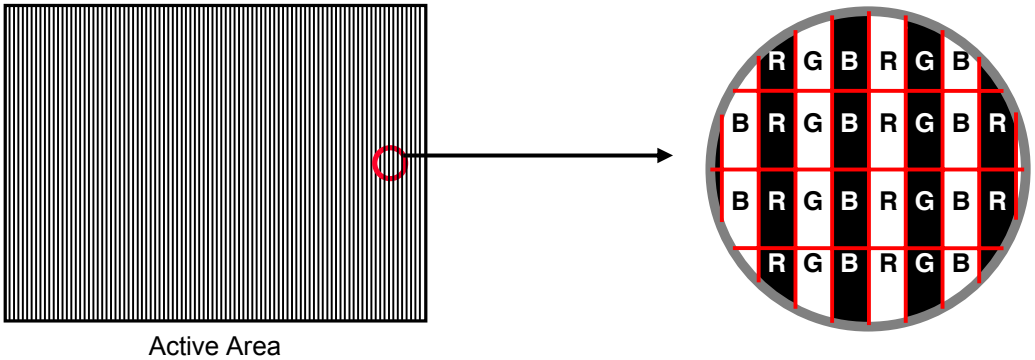


Active Area

b. Black Pattern



c. Vertical Stripe Pattern

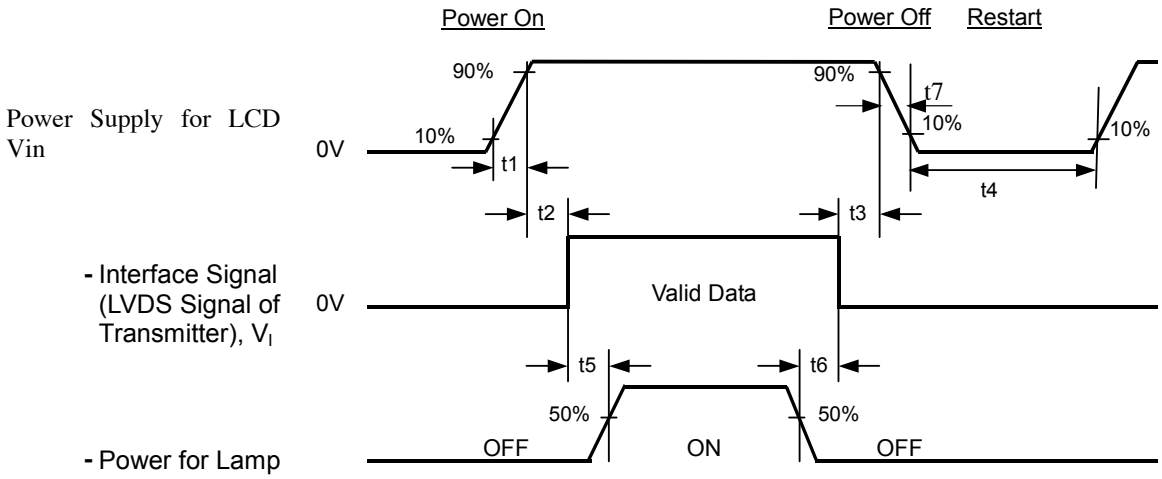


Active Area

Note(4) The power consumption is specified at Vin =12V, and the pattern with the maximum current.

9.0 Power ON/OFF Sequence

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Timing Specifications:

0.5< t1 ≦ 10 msec
0 < t2 ≦ 50 msec
0 < t3 ≦ 50 msec
t4 ≧ 500 msec
t5 ≧ 450 msec
t6 ≧ 90 msec
5 ≦ t7 ≦ 100 msec

Note.
(1)The supply voltage of the external system for the module input should be the same as the definition of V.
(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.
(3) In case of V_{in}=off level, please keep the level of input signals on the low or keep a high impedance.
(4) t4 should be measured after the module has been fully discharged between power of and on period.
(5) Interface signal shall not be kept at high impedance when the power is on.
(6) It is not guaranteed that products are damaged which is caused by not following the Power Sequence.
(7) It is suggested that Vin falling time follows t7 specification; else slight noise is likely to occur when LCD is turned off (even backlight is already off).

10.0 I2C Specification

10.1 Backlight on/off (BLON) and brightness adjustment (VDIM_IN / VDIM_OUT)

The backlight unit can be controlled to turn on or turn off by BLON signal that is in the pin 1 of J2. The input voltage specification of BLON signal is described in section 5.3. If the input voltage level is low, the backlight unit will be turned off. If high, it will be turned on.

The backlight unit also can be controlled to adjust brightness by VDIM_IN signal that is in pin 2 of J2. The input voltage range is from 0V to 3V. The maximum brightness is acquirement when the input voltage is 0V. If the input voltage is 3V, the backlight unit will present the minimum brightness.

You can use I2C interface protocol to program DS1805 (DAC, Digital-to-Analog Converter) by pin7, 8 of J1. The port-1 of DS1805 will generate one voltage that you want. Then, the voltage is sent to VDIM_OUT signal that is in pin 3 of J2. The systems can feedback this signal to VDIM_IN signal to control the BLU brightness. Please refer to I2C interface protocol in MAXIM DS1805 datasheet for brightness adjustment.

10.2 I2C Specification

Following describes the I2C specifications equipped in the LCD module. Since the DAC (DALLAS DS1805) is used for Brightness, please refer to its own specifications in detail. 2 signals (SCL and SDA) in the LCD module interface are used for the DAC. The address for DAC is '0101101'b. Its port-1 is for Brightness. Reserved addresses are from '0010000'b to '0011111'b and from '0110000'b to '0111111'b.

10.3 I2C Feature Summary

- Standard mode (100KHz max) support
- 3.3V interface
- Slave mode operation only

10.4 Electrical Specification

2 signals (SCL and SDA) are equipped at the LCD module interface. SCL is the clock input and SDA is the data input/output. These signals should be driven by Open-Drain or Open-Collector without any pull-up resister. Both signals are pulled up by 4.7K ohm resisters to 3.3V typ respectively in the LCD module.

Electrical Specification

	Symbol	Min	Max	Unit
Input Low voltage (*1)	Vil	-0.5	0.5	V
Input High voltage (*2)	Vih	2.3	3.6	V
Input Hysteresis voltage	Vhys	0.4	-	V
Input leakage current @ Vil-Min or Vih-Max (*3)	Ii	-30	30	uA
Output Low voltage	Vol	-	0.5	V
Output High impedance leakage current (*3)	Ioh	-30	30	uA
Input capacitance	Ci	-	35	pF

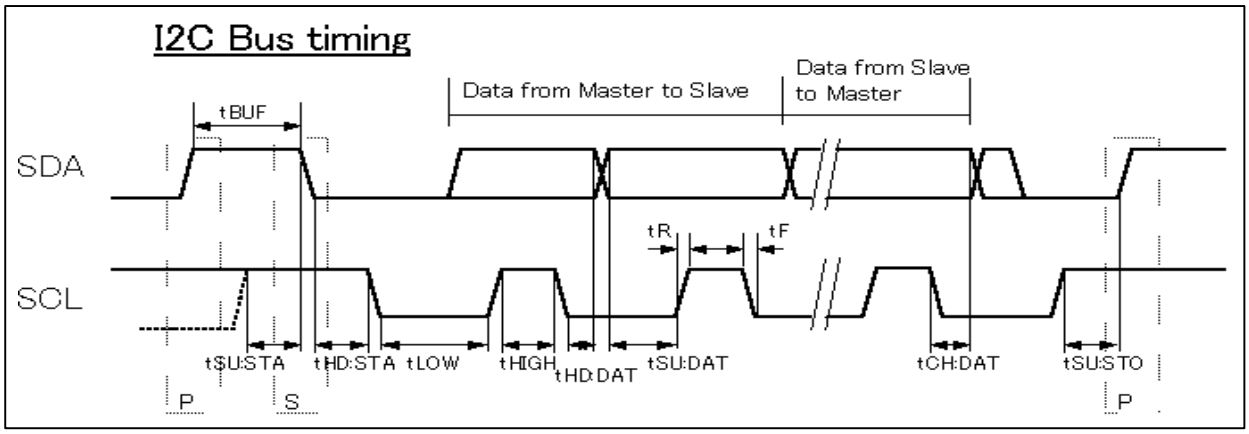
NOTE:

*1: Vil (typ) = 0.9V
*2: Vih (typ) = 1.8V
*3: without pull up resisters (4.7K ohm)

10.5 Timing Specification

In the following figure and table, Slave is the control ASICs in the LCD module and Master is the controller to drive the LCD module. "S" is the START condition and "P" is the STOP condition.

I2C Bus timing



Timing Specification

	Symbol	Min	Max	Unit
Frequency of SCL	fSCL	0	100	KHz
Bus Free Time from STOP to START	tBUF	4.7	-	us
Setup time of START	tSU:STA	4.7	-	us
Hold time of START	tHD:STA	4.0	-	us
Low time of SCL	tLOW	4.7	-	us
High time of SCL	tHIGH	4.0	-	us
Data hold time for Slave	tHD:DAT	0	-	us
Data setup time for Slave	tSU:DAT	250	-	ns
Data change from SCL falling edge (to Master)	tCH:DAT	300	900	ns
Rise time Vil-Max --> Vih-Min	tR	-	1000	ns
Fall time Vil-Max <-- Vih-Min	tF	-	300	ns
Setup time of STOP	tSU:STO	4.0	-	us
Spike suppression	tSP	-	50	ns

11.0 National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

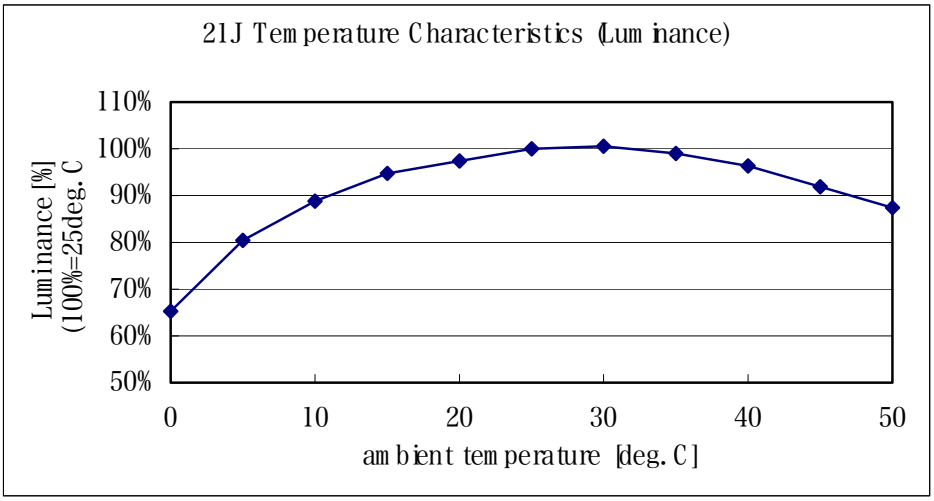
- This component has been judged on the basis of the required spacings in the Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment, CAN/CSA C22.2 No.950-95 *UL 1950, Third Edition, including revisions through revision date March 1,1998, which are based on the Fourth Amendment to IEC 950, Second Edition, which would cover the component itself if submitted for Listing.
- The inverter output circuit supplied with this model is a limited Current Circuit.
- The units are intended to be supplied by SELV.
- The terminals and connectors are suitable for factory wiring only.
- The terminals and connectors have not been evaluated for field wiring.
- A suitable Electrical and Fire enclosure shall be provided.

12.0 Application Note

This section describes some outstanding characteristics of ITQX21J module and also describes some design recommendations.

12.1 Luminance vs. Temperature

The following chart shows the initial luminace transition coming along with the module temperature.



12.2 Design Recommendation

This chapter describes the recommendation when monitor frame is designed.

12.2.1 Recommendations for cooling

The ITQX21J is a high luminance and high resolution panel and produces some heat. Inadequate cooling can result in damage to the module or the monitor unit.

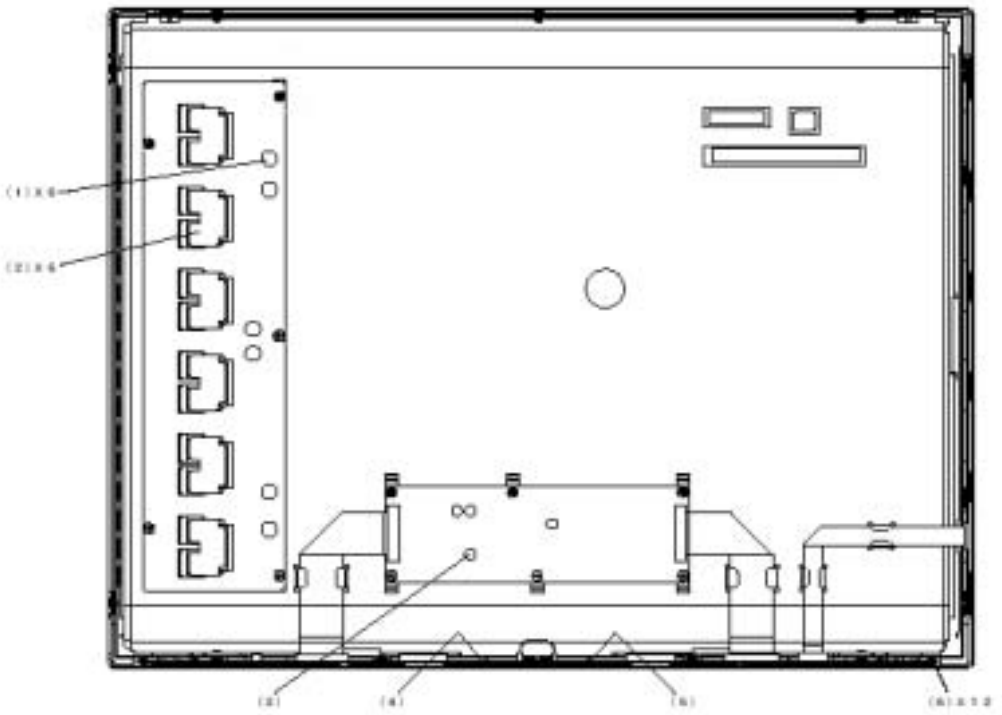
COOLING FANS ARE STRONGLY RECOMMENDED TO ENSURE CORRECT TEMPERATURE OPERATION.

Because of the large panel size the use of 2 fans is recommended.

The recommended position of the fans is to supplement the normal convective flow. The optimum configuration would be to input cool air at the base of the panel and exhaust hot air at the top. The exact size, position, and flow rates are a function of the monitor enclosure design. Please refer to the maximum operating temperatures of the various components to verify the design.

*** Reference ***

See the rear side of module below;



- ABSOLUTELY NECESSARY POINTS are next two components.
(6) X-DRIVER (Will get very hot.)
and
(1) Choke Coil
- Backlight Inverter
(2) Transformer
- DC/DC Card
(3) Choke Coil
- PCB-X
(4), (5) Gate Array

The table below shows the maximum component temperature Spec.

Component	Max. Temperature Spec. (degree C)
Gate Array	100
X-Driver	85
Choke Coil(Inverter)	105
Transformer(Inverter)	100
Choke Coil(DC/DC)	105
Polarizer(Cell)	60

12.2.2 Mechanical recommendation for monitor enclosure design.

This TFT module uses IPS technology to enhance viewing angle, this technology is weak against twisting and bending forces.
These forces cause bad FOS quality, such a un uniformity.
In order to keep original FOS quality, please following instruction at manufacturing and designing.

1. After installation of the TFT Module into an enclosure, do not twist nor bent the TFT Module even momentary.

2. At designing the enclosure, it should be taken into below consideration. otherwise the TFT Module occur uniformity problem.

2-1. Material of chassis or bracket to mounting TFT module should be hard material, stainless or SECC or SPCC. Material thickness should be exceeded 1mm.

2-2. No bending/ twisting forces are applied to the TFT Module from out side.

2-3. No pushing force for EMI grounding using metal fingers or gasket TFT metal bezel, to push glass surface by TFT metal bezel opening edge, is applied to TFT module metal bezel wall.

2-4. At designing system front plastic bezel, do not touch and push glass surface to avoid un uniformity.

12.2.3 Recommendation of designing monitor which uses ITQX21J for EMC Compliance

A. Chassis and Frame Ground of Monitor

1. LCD Module should be covered by metal chasis over all except front side. the chasis of the monitor's interface card should be designed as separate parts with the chasis of the LCD module.
   Holes on the partition wall between the two chasis should be as small as possible to pass through the cable
   The two chassis should be contacted each other with low impedance.

2. Monitor's chasis(equal chasis of LCD module)should have the contact with the frame ground of voltage source(Power FG) with low impedance.

3. The chasis of LCD module should have the contact with the surrounding of front bezel by finger or something at intervals of less than 1 inch.

4. The ground of the monitor's interface card should be contacted with its chasis with low impedance.

5. The holes for thermal radiation, on chasis of LCD module or monitor's interface card, should be less than 1 inch in diameter, at intervals of less than 1 inch. We recommend the holes are about 5mm in diameter, at intervals of about 10mm to 15mm.

B. LVDS cable (assumption as wire type, not FPC or FFC)

1. Signal pairs of the differential signals should be twisted each other with more than a turn per a centimeter.

2. The ground line would wind around the set of LVDS cables(1 channel).

3. The set of LVDS cables would be covered by shield mesh.
   To make the shield mesh contacted with the signal ground, it is possible to strip the cover of ground line wound around LVDS signals.

4. Ferrite Core would be added to LVDS cables at the point near signal source.
   We recommend the above works at that priority(1. is the highest).

C. A ferrite core would be added to the power cable which supply +12volt to LCD module.

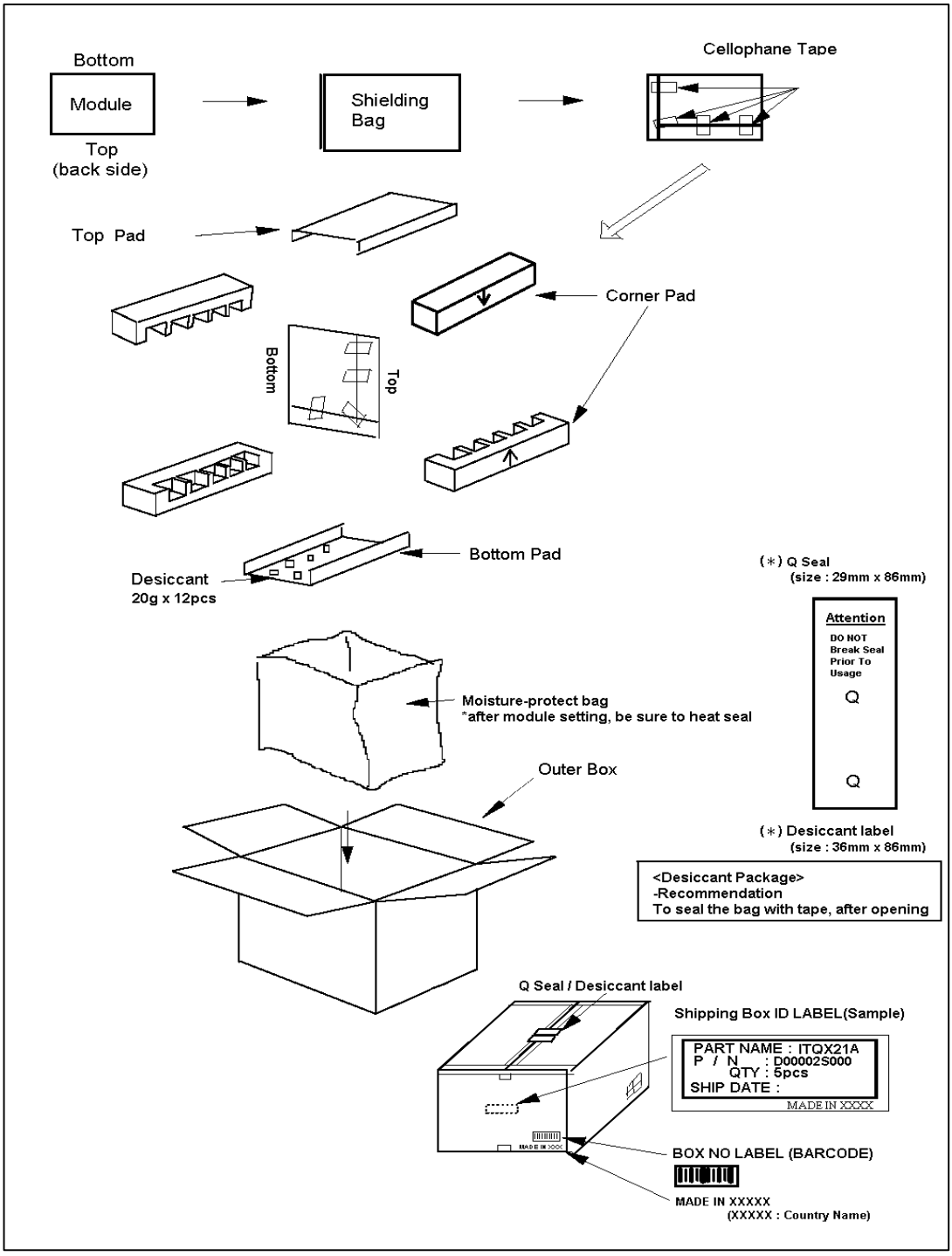
13.0 Backlight Life

Backlight Life Time	30,000 Hours	condition 25 degree C

The assumed Backlight Life will be until the luminance becomes 430 cd/m^2 or more at maximum white luminance.

14.0 Packaging Requirement

The packaging of the LCD meets 75 cm drop test. (Note: 1 corner, 3 edges, 6 faces)
The following is the drawing of the package:

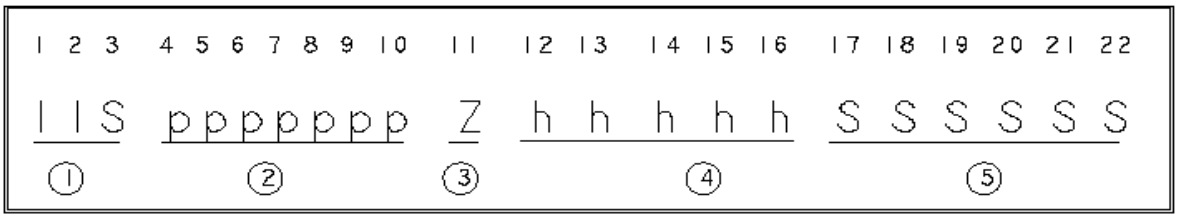


15.0 Label

There are labels on the rear side of the Module.

Serial Number Label

BARCODE CHARACTER AREA



① 1 1 S = FIXED
STARTING IDENTIFIER WHICH IS COMMON TO COMPONENT LEVEL SERIAL NUMBERS

② SEVEN DIGIT IDT PART NUMBER ASSIGNED BY THE IDT DEVELOPMENT RELEASING THE PART

③ Z = FIXED
AUTOMATICALLY GIVEN WHEN USING THE 1 1 S-Z FORMAT

④ hhhhh=HEADER CODE(EC LEVEL)

⑤ SSSSS=SEQUENCE

Date Label

YY and WW of the Week Code stand for the Year and the Week of the Year of manufacturing of the Module respectively.

Backlight Label

ASM P/N	
BL P/N	.
BL EC	.
BL LOT No	
CFL LOT No	
BL No.	

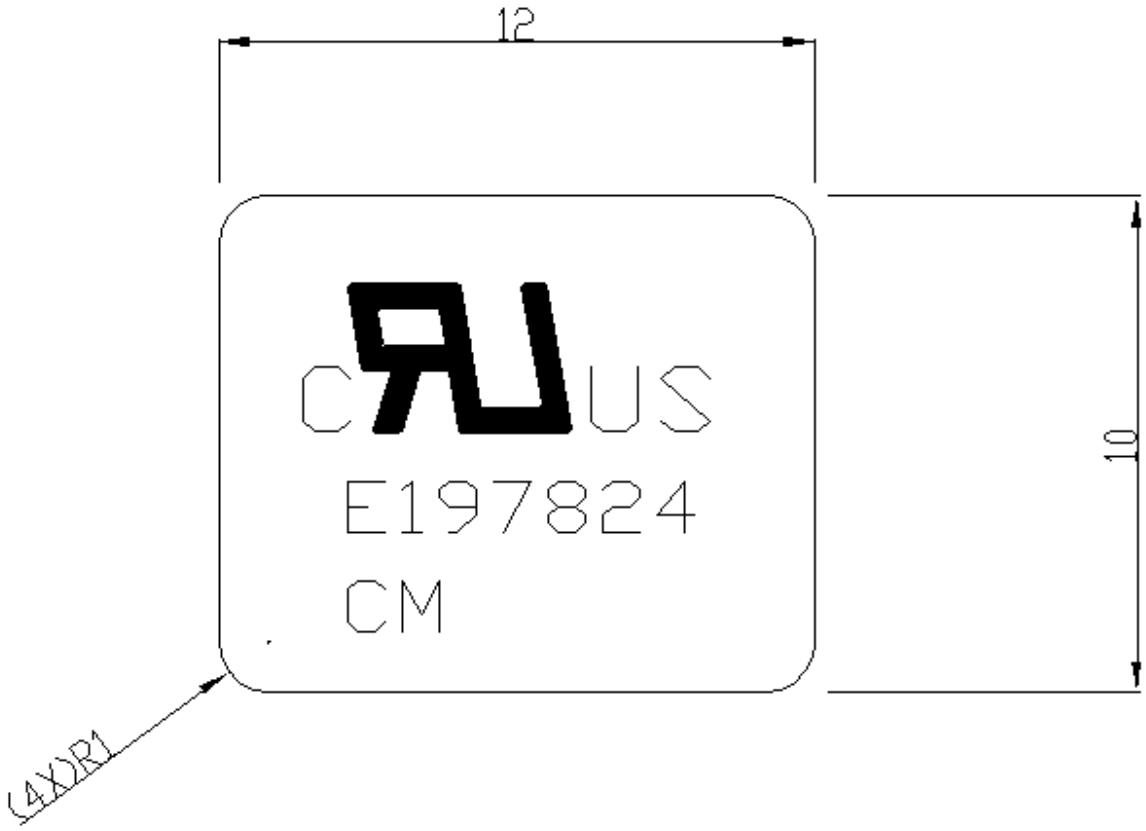
THE FLUORESCENT LAMP IN THE LIQUID CRYSTAL DISPLAY(LCD) CONTAINS MERCURY. DO NOT PUT IT IN TRASH THAT IS DISPOSED OF IN LANDFILLS. DISPOSE OF IT AS REQUIRED BY LOCAL ORDINANCES OR REGULATIONS.

Material Label

Label to indicate the material of light guide used in backlight system.

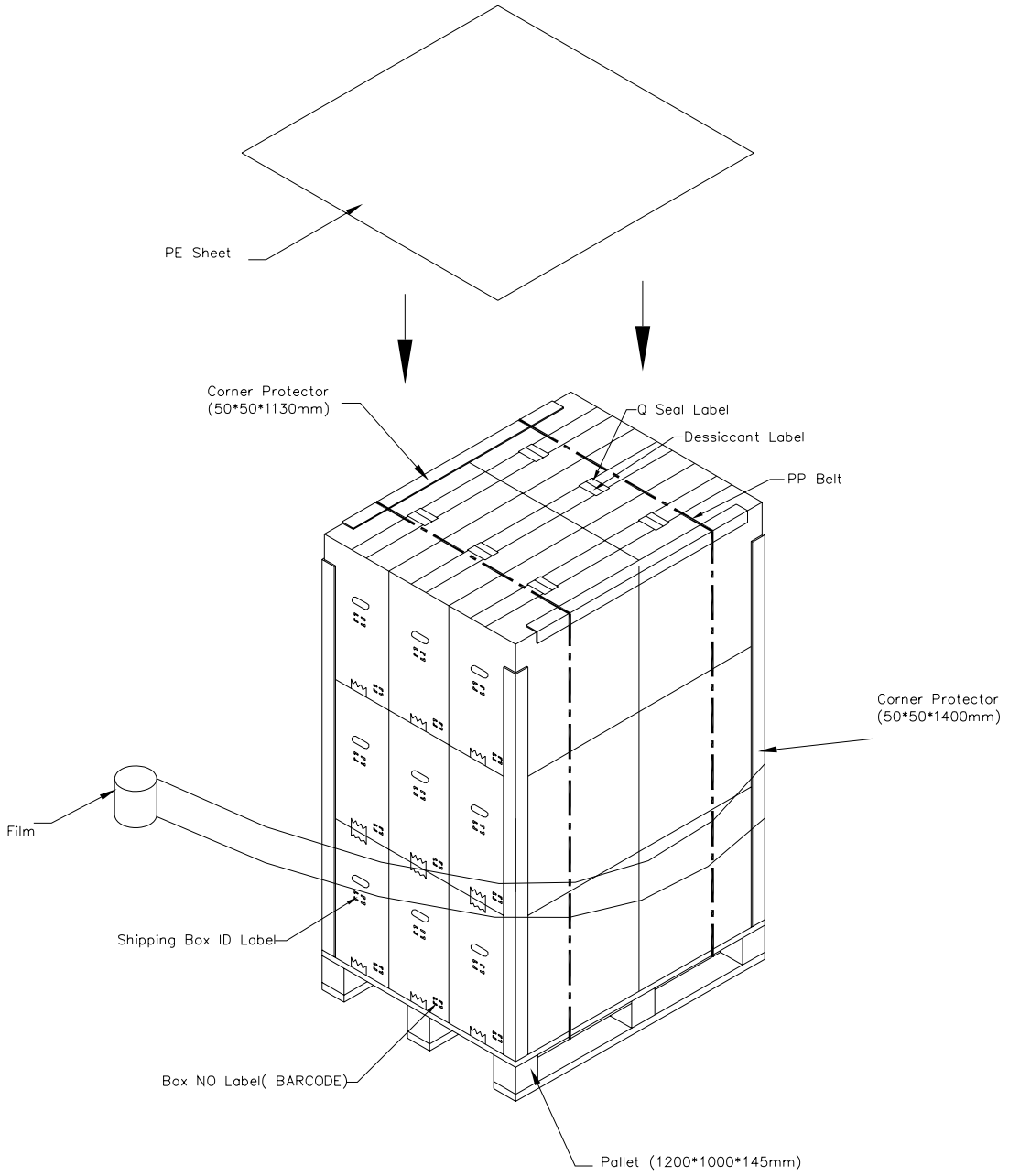
Material Information
Diffuser
>PC<
Diffusing Sheet
>PET<
Reflection Sheet
>PP<

UL Label

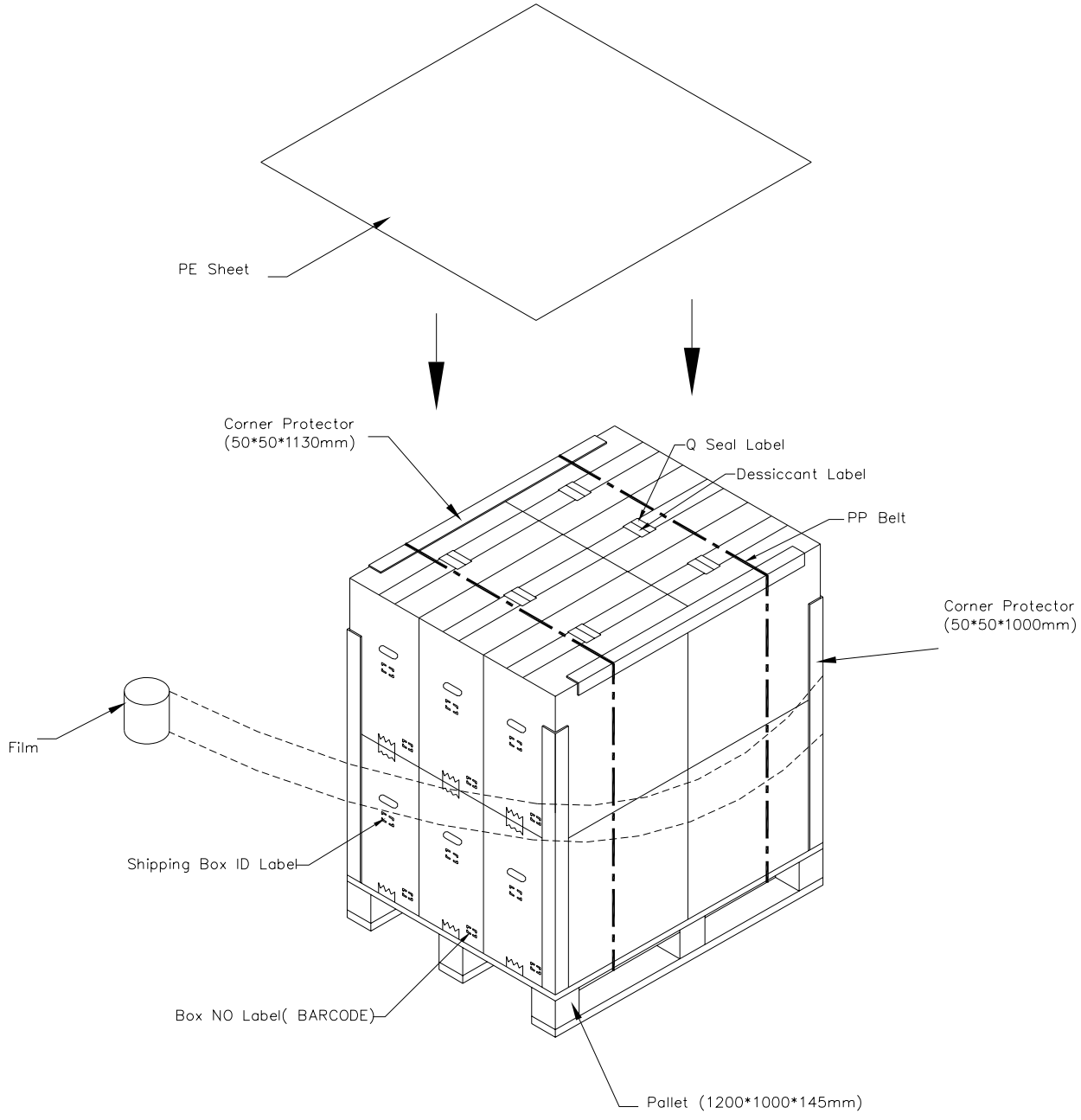


16.0 Sea/Air Transportation Packing

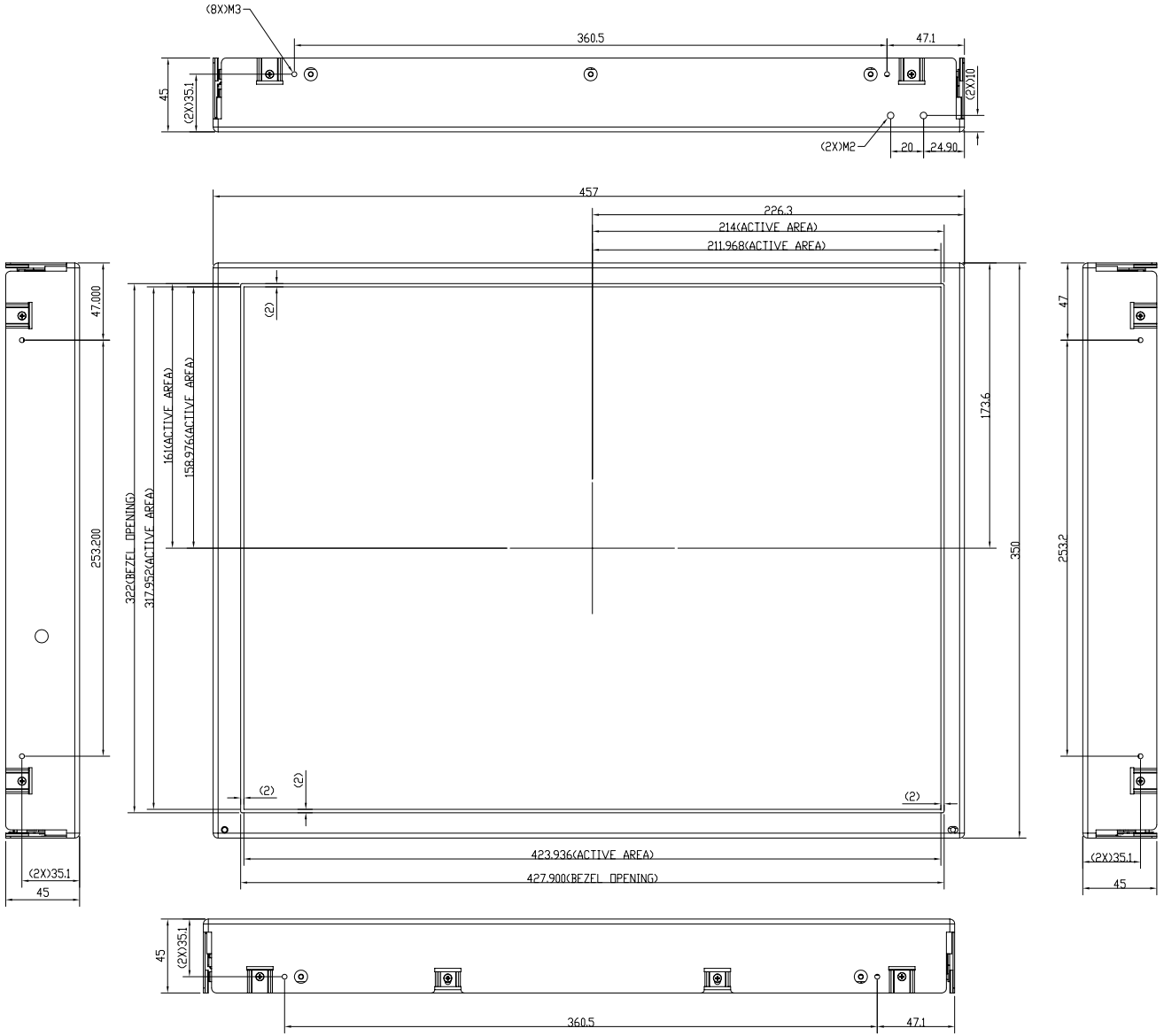
Sea transportation



Air transportation



17.0 Mechanical Characteristics



NOTES:

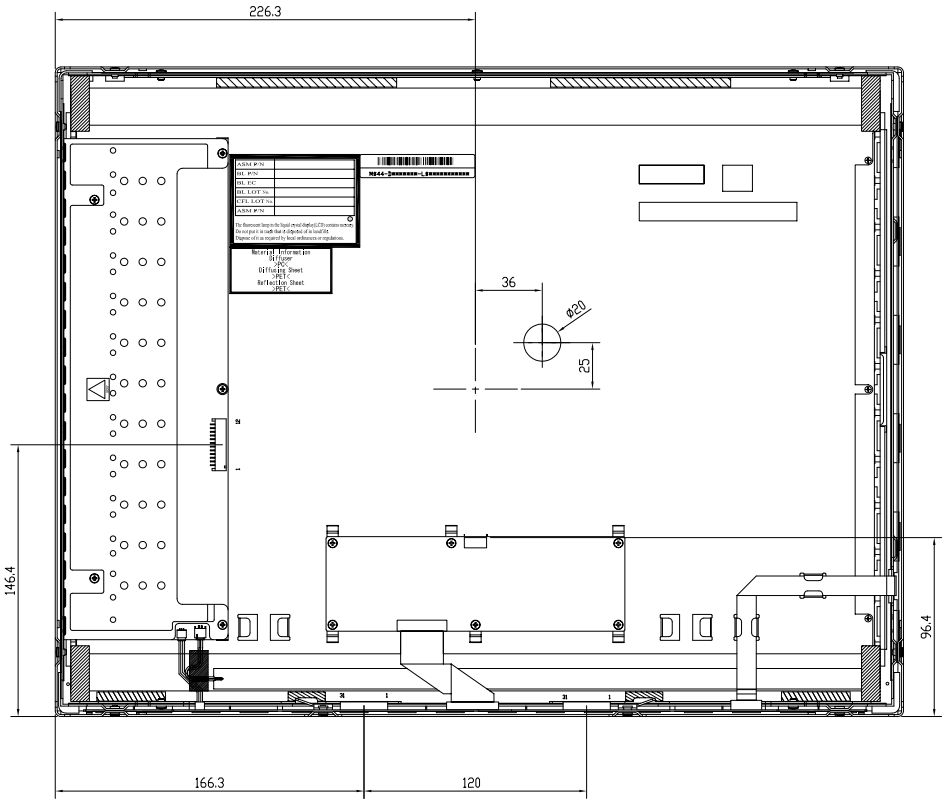
1 TO BE USED FOR PANEL FIXING.
2 IF CONNECTOR TO BE LS CABLE(JOYTECH)
  THEIR P/N GT121-31P-TD-A
3 DC/DC CONNECTOR TO BE JAE CO., LTD
  THEIR P/N IL-Z-8PL-SMTY
4 INVERTER CONNECTOR TO BE CviLux
  THEIR P/N CI0112M1HR0-LF
5 TO EXCLUDE DEFORMATION
6 UNSPECIFIED TOLERANCE TO BE ±0.8mm
7 SCREW TOQUE FOR MOUNTING SHALL NOT
  EXCEED 0.294N-m (3kgf-cm)
8 GAP BETWEEN BEZEL & PANEL IS
  0.2mm MIN. AND 1.2mm MAX.

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
A	Add Notes No.8	2010/03/09	MLHsieh	CKHung	EA	

General Tolerance Unless Specified					
0~3	±0.05	30~120	±0.15	1000~2000	±0.5
3~6	±0.05	120~400	±0.2	2000~4000	–
6~30	±0.1	400~1000	±0.3	VERTICAL ANGLE / SEND ANGLE	45° / 45.5°

TITLE	ASSY_MODULE_R208R1/R2-L0X		2D REV. A 3D REV.
Approved	CK_HUNG	Drawing No.	(M208141028)
Checked	CHANEY	Part No.	NA
Drawer	MLHsieh	Material	NA
Designer	ANDYLEE	Date	2010/04/07
		Scale	1/1
		Sheet	1 / 2
		Unit	mm

CHI MEI OPTOELECTRONICS CORP.



NOTES:

1 TO BE USED FOR PANEL FIXING.
2 IF CONNECTOR TO BE LS CABLE(JOYTECH)
THEIR P/N GT121-31P-TD-A
3 DC/DC CONNECTOR TO BE JAE CO., LTD
THEIR P/N IL-Z-8PL-SMTY
4 INVERTER CONNECTOR TO BE CviLux
THEIR P/N CI0112M1HR0-LF
5 TO EXCLUDE DEFORMATION
6 UNSPECIFIED TOLERANCE TO BE ±0.8mm
7 SCREW TOQUE FOR MOUNTING SHALL NOT
EXCEED 0.294N-m (3kgf-cm)
8 GAP BETWEEN BEZEL & PANEL IS
0.2mm MIN. AND 1.2mm MAX.

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

General Tolerance Unless Specified					
0~3	±0.05	30~120	±0.15	1000~2000	±0.5
3~6	±0.05	120~400	±0.2	2000~4000	--
6~30	±0.1	400~1000	±0.3	VERTICAL ANGLE	45'
				BEND ANGLE	45'

TITLE	ASSY_MODULE_R208R1/R2-LOX	2D REV.	A
		3D REV.	
Approved	CK_HUNG	Drawing No.	(M208141028)
Checked	Tangit_Yang	Part No.	NA
Drawer	MLHsieh	Material	NA
Designer	ANDYLEE	Date	2010/04/07
Scale	1/1	Unit	mm
Sheet	2 / 2		

CHI MEI OPTOELECTRONICS CORP.