Customer Name	Date of Issue	November. ** .2013
	Issued No.	Rev.00

PRODUCT INFORMATION	
Product Name	8.9”WQXGA LCD (LCD Module)
	-

【FUNCTION】8.9inch Transmissive WQXGA Color LCD Module

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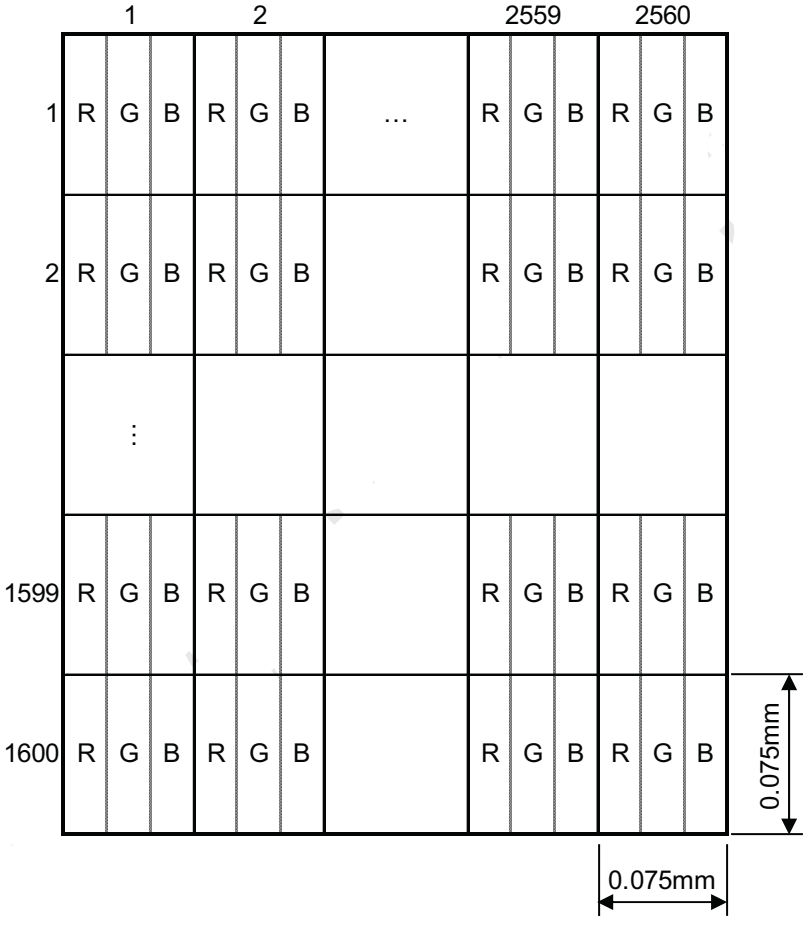
1. Scope of Application

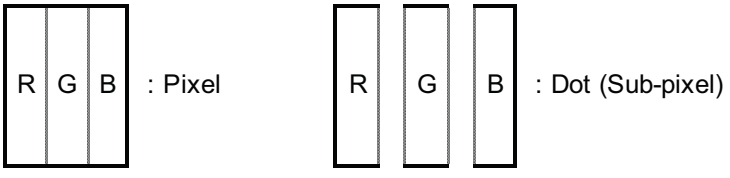
This specification shall be applicable to TFT-LCD Cell TFTMD089030, designed for Tablet Devices

2. General Data

Item	Specifications	Remark
Display Mode	Transmissive Type, Normally Black Mode, In-Plane Switching Mode 16,777,216 Colors	
Driving Method	TFT active matrix, Low-temperature poly-silicon	
Input Signals	MIPI-DSI,Command/Video mode (4Lane x 2Port)	
Outside Dimensions	197.60(W) x 129.60(H) (typ.)	
Active area	192.0(W) x 120.0(H) (mm)	
Number of Pixels	2560(W) x 1600(H)	
Pixel Pitch	0.075 (W) x 0.075 (H) (mm)	
Pixel arrangement	RGB Vertical stripe	
Required LCD Driver IC	2 chip IC : Renesas R69429	

Note 1) Refer to the below.

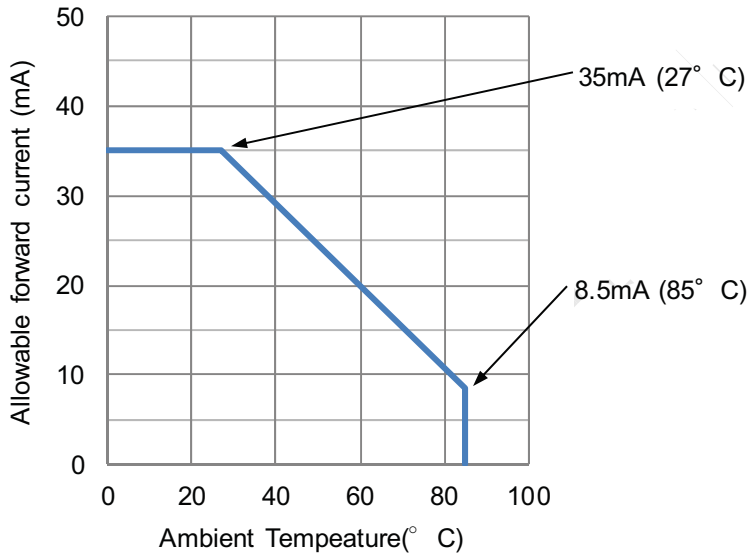




3. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Note
Power Supply for I/O Interface	IOVCC	-0.3	4.6	V	(1)
Power Supply for MIPI DSI DPHY	DPHYVCC	-0.3	4.6	V	(1)
Power Supply for Analog	VSP	-0.3	6.5	V	(1)
Power Supply for Analog	VSN	-6.5	+0.3	V	(1)
Input Voltage	Vi	-0.3	IOVCC+0.3	V	(2)
LED Reverse Voltage	V_R	-	5	V	
LED Forward Current	I_{LED}	-	Note (3)	mA	per LED
Static Electricity	-	-	±2	kV	(4)

Notes (1) Keep all Voltages no lower than GND.
(2) Applies to the RESET pin.
(3) Ambient Temperatures vs. Allow able Forward

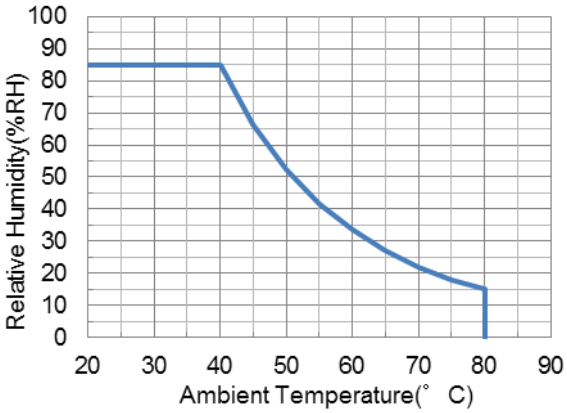


(4) 100 pF - 1.5 kohm, 25°C-70%RH
Static electricity discharge is to be aimed at the center of the active area.

4. Environmental Absolute Maximum Ratings

Item	Operating		Non-Operating Note(3)		Remarks
	Min	Max	Min	Max	
Ambient Temperature	-20°C	60°C	-20°C	65°C	Note (2)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Ta < 40°C 85%RH max.
Ta > 40°C Absolute humidity must be lower than the humidity of 85%RH at 40°C.
No dew condensation is allowed.



(2) Background color slightly changes depending on ambient temperature and viewing angle.
The temperature for operating in the table above apply to operation only.
Visual qualities, such as contrast ratio and response time, to be evaluated at Ta = 25°C Operating.

(3) This is not for storing condition.
The following precautions are necessary in long-term storage for the LCD modules.
(1) Store the LCD modules in a dark place; do not expose them to Keep the temperature between 10 and 30°C, and the humidity between 55% and 75%RH.

5. Electrical Characteristics

GND=0V,Ta=25°C

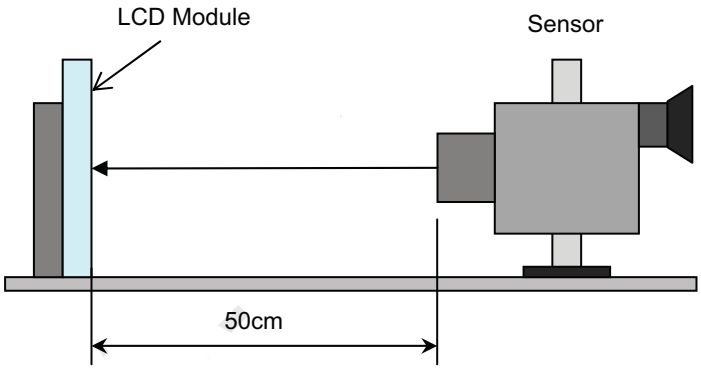
Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Supply Voltage for Logic and Analog	VBAT		3.0	3.3	4.5	V	-
Power Supply for I/O Interface	VDDIO		1.7	1.8	1.9	V	-
Input Voltage for Logic Circuits	Vi	"H" level	0.70×VDDIO	-	VDDIO	V	(1),(2)
		"L" level	0	-	0.30×VDDIO		
Input Voltage for EN	Vi	"H" level	0.90×VDDIO	-	VDDIO	V	(1)
		"L" level	0	-	0.10×VDDIO		
Output Voltage for Logic Circuits	Vo	"H" level	0.80×VDDIO	-	-	V	(1),(2)
		"L" level	-	-	0.20×VDDIO		
Input/Output Leak Current	ILi	-	-10	-	10	μA	(3)
Power Consumption	POWER	All White	-	230	300	mW	(4),(5)

Notes (1) VDDIO = 1.7V to 1.9V
(2) Input : RESET, DBIST, Output : PWM, TE
(3) Except the current of out driving MOS.
(4) IOVCC= 1.7V～1.9V, VBAT=3V～4.5V, Column inversion mode.
Display image : ALL White.
(5) Operation Mode : MIPI-DSI Command mode LCM Display frame rate = 60.37～66.72fps
MIPI-DSI Data and Clock lane = LP11

6. Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Brightness		B	φ=0°, θ=0°	380	(500)	-	Cd/m2	(1),(2)
Viewing Angle on axis	φ=0	θ	CR>10	-	(80)	-	degree	(3),(4)
	φ=90							
	φ=180							
	φ=270							
Contrast Ratio		CR	φ=0°, θ=0°	-	(1200)	-	-	(5)
Color Gamut CIE 1931 (Primary Color)	Red	x	φ=0°, θ=0°	-	(0.646)	-	-	-
		y		-	(0.330)	-		
	Green	x		-	(0.302)	-		
		y		-	(0.610)	-		
	Blue	x		-	(0.155)	-		
		y		-	(0.062)	-		
	White	x		-	(0.31)	-		
		y		-	(0.33)	-		
NTSC Ratio (CIE1931)		-	φ=0°, θ=0°	-	(72)	-	%	-
Gamma Curve		-	φ=0°, θ=0°	-	(2.2)	-	-	
Cross Talk		CT	-	-	-	(4)	%	(6)

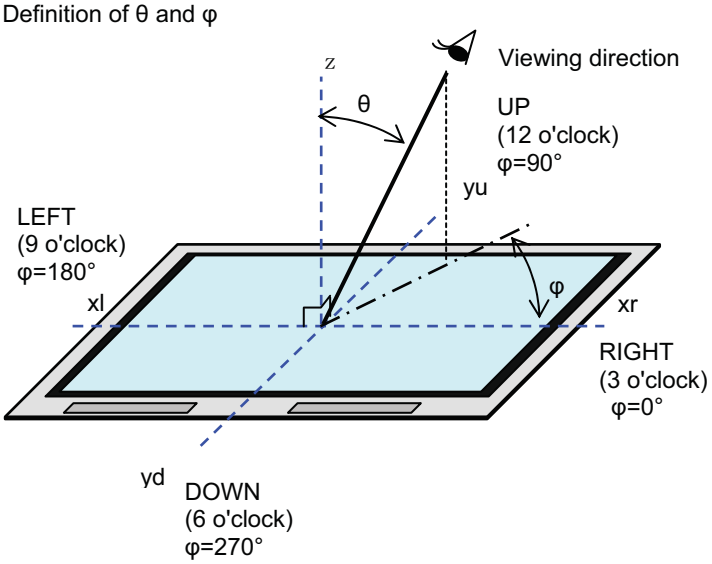
Notes (1) Definition of Brightness "B". At the Center of Active Area.



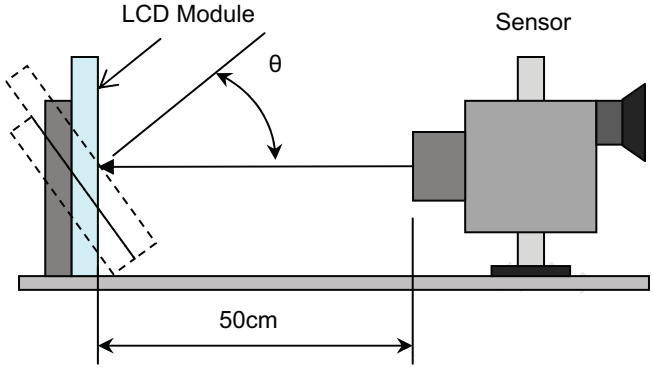
Sensor : KONICA MINOLTA CS-1000 or equivalent

(2) Display image for measurement : All White

(3) Definition of θ and φ



(4) Definition of Viewing Angle θ



Sensor : TOPCON's BM-5A or equivalent

(5) Definition of Contrast "CR"

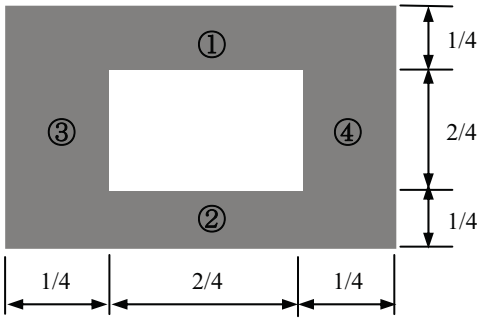
CR = (Brightness when displaying White raster) / (Brightness when displaying Black raster)

(6) Definition of Cross Talk "CT"

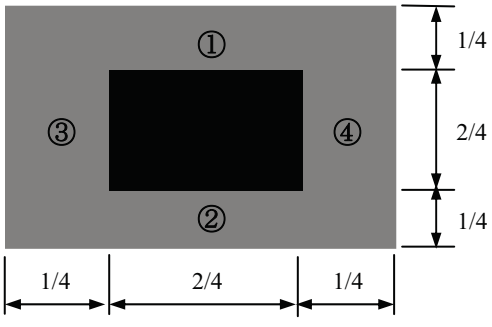
CT = {(Brightness [Cross-talk pattern]) – (Brightness [127Gray])} / (Brightness [127Gray]) x 100(%)

Measurement pattern :
- Cross talk pattern 1 : White box
- Cross talk pattern 2 : Black box

Measurement Point :
- Vertical Crosstalk : ① and ②
- Horizontal Crosstalk : ③ and ④

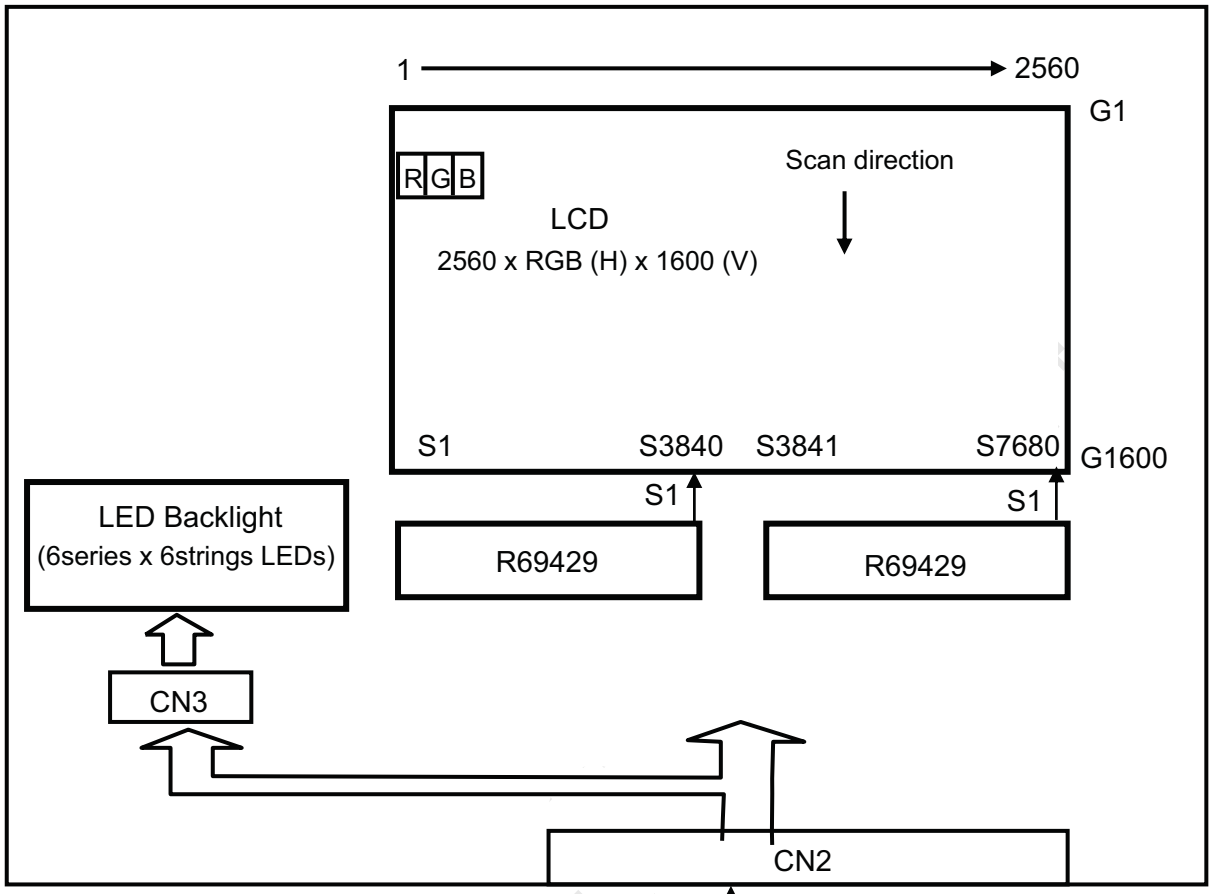


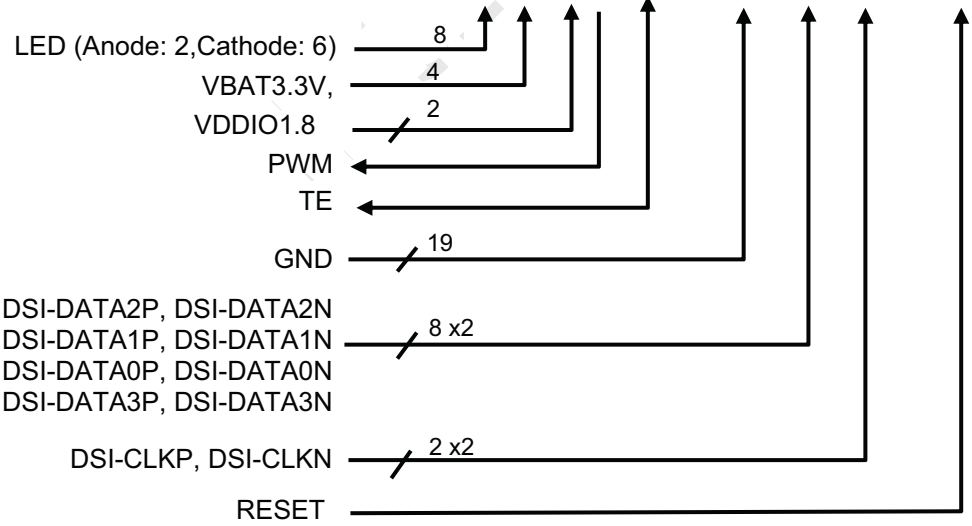
Cross talk pattern 1 : White box

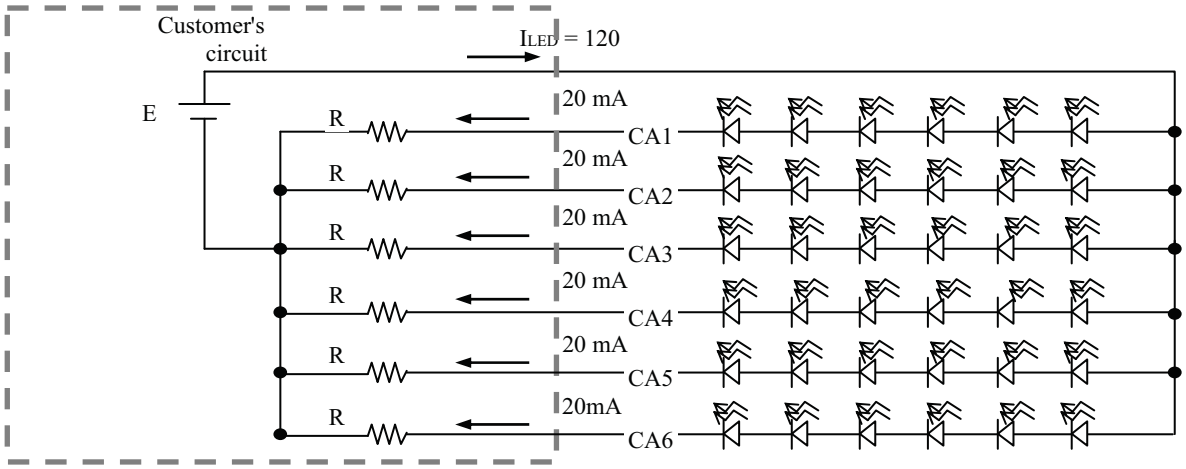


Cross talk pattern 2 : Black box

7. Block Diagram / Interface Pins







PIN	SYMBOL	FUNCTION	I/O	REMARKS
1	GND	GND	-	-
2	GND	GND	-	-
3	GND	GND	-	-
4	V_LED_C6	GND for LED	-	-
5	V_LED_C5	GND for LED	-	-
6	V_LED_C4	GND for LED	-	-
7	V_LED_C3	GND for LED	-	-
8	V_LED_C2	GND for LED	-	-
9	V_LED_C1	GND for LED	-	-
10	V_LED_A	Power Supply for LED	-	-
11	V_LED_A	Power Supply for LED	-	-
12	N.C	Non connect	-	-
13	GND	GND	-	-
14	PWM	Control Signal for LED Brightness	O	LEDPWM
15	TE	Tearing Effect Output	O	TE
16	GND	GND	-	-
17	DSI_R-DATA-2P	Positive MIPI Data2 Input	I	DATA2P
18	DSI_R-DATA-2N	Negative MIPI Data2 Input	I	DATA2N
19	GND	GND	-	-
20	DSI_R-DATA-1P	Positive MIPI Data1 Input	I	DATA1P
21	DSI_R-DATA-1N	Negative MIPI Data1 Input	I	DATA1N
22	GND	GND	-	-
23	DSI-CLKP	Positive MIPI Clock Input	I	CLKP
24	DSI-CLKN	Negative MIPI Clock Input	I	CLKN
25	GND	GND	-	-
26	DSI_R-DATA-0P	Positive MIPI Data0 Input/Output	I/O	DATA0P
27	DSI_R-DATA-0N	Negative MIPI Data0 Input/Output	I/O	DATA0N
28	GND	GND	-	-
29	DSI_R-DATA-3P	Positive MIPI Data3 Input	I	DATA3P
30	DSI_R-DATA-3N	Negative MIPI Data3 Input	I	DATA3N
31	GND	GND	-	-
32	EN	Enable Pin to Operate DC/DC	I	-
33	N.C	Non connect	-	-
34	VBAT	Power Supply for DC/DC converter	-	-
35	VBAT	Power Supply for DC/DC converter	-	-
36	VBAT	Power Supply for DC/DC converter	-	-
37	VBAT	Power Supply for DC/DC converter	-	-
38	N.C	Non connect	-	-
39	VDDIO	Power Supply for I/O Interface and	-	-
40	VDDIO	Power Supply for I/O Interface and	-	-

Note) I : Input O : Output I/O : Input/Output

Continue to next page

PIN	SYMBOL	FUNCTION	I/O	REMARKS
41	GND	GND	-	-
42	DBIST(GND)	GND	I	DBIST
43	TE_S	Non connect	O	-
44	GND	GND	-	-
45	RESET	Reset Signal	I	RESX
46	GND	GND	-	-
47	DSI_L-DATA-2P	Positive MIPI Data2 Input	I	DATA2P
48	DSI_L-DATA-2N	Negative MIPI Data2 Input	I	DATA2N
49	GND	GND	-	-
50	DSI_L-DATA-1P	Positive MIPI Data1 Input	I	DATA1P
51	DSI_L-DATA-1N	Negative MIPI Data1 Input	I	DATA1N
52	GND	GND	-	-
53	DSI-CLKP	Positive MIPI Clock Input	I	CLKP
54	DSI-CLKN	Negative MIPI Clock Input	I	CLKN
55	GND	GND	-	-
56	DSI_L-DATA-0P	Positive MIPI Data0 Input/Output	I/O	DATA0P
57	DSI_L-DATA-0N	Negative MIPI Data0 Input/Output	I/O	DATA0N
58	GND	GND	-	-
59	DSI_L-DATA-3P	Positive MIPI Data3 Input	I	DATA3P
60	DSI_L-DATA-3N	Negative MIPI Data3 Input	I	DATA3N
61	GND	GND	-	-

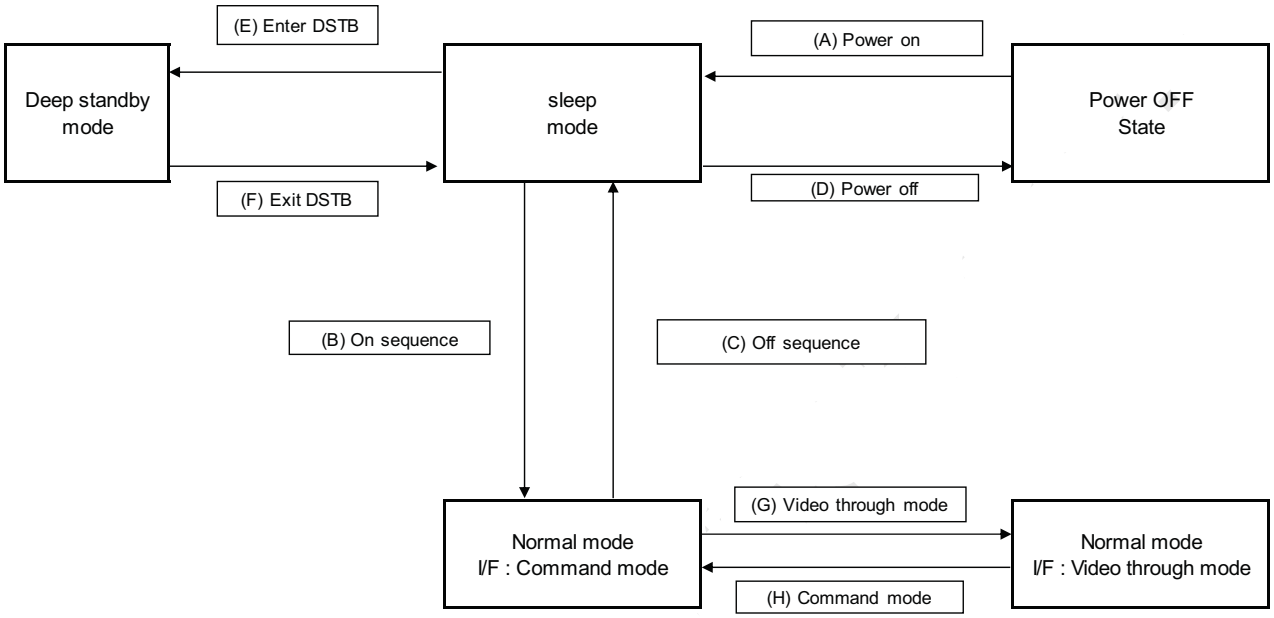
Note) P : Power supply U : User define
CN002 : FH36W-61S-0.3SHW(50) (HIROSE)

8. FUNCTION

The use of 8.9”WQXGA LCD basically conforms to specifications of LCD driver IC: R69429(Renesas SP drivers INC.).
It explains typical function in this manual.

8.1 OVERVIEW

The basic operation mode of 8.9”WQXGA LCD Module is illustrated below. When changing from one mode to another, make sure to follow the sequence indicated in the figure.



8.2 INTERFACE

・MIPI DSI Command mode and Video mode 4 Data Lanes x 2port
・HS(High Speed) Transmission (Unidirectional)
・LP(Low Power) Transmission (Bidirectional)
・Diagnostic function – checksum and ECC error monitoring
・Functionality supported by Escape mode
・Clock Lane supports ULPS
・Packet-Based Protocol
・Maximum MIPI transfer rate : 1000Mbps

The DSI incorporated in the LCD driver complies with the following standards.
・MIPI DSI: Version 1.01.00r11
・MIPI D-PHY: Version 1.00.00
・MIPI DCS: Version 1.01.00

8.2.1 MIPI-DSI

The module DSI interface employs 2port of clock and 4 data lanes.
-DSI-D0+D0-is bi-directional with Low-Power Reverse Escape Mode supporting Low Power Data Transmission.
-DSI-D1+D1-D2+D2-D3+D3- is unidirectional without Turnaround or any kind of Reverse communication functionality.

The DSI interface can communicate in 2 modes, Low Power Data Transmission Mode (LP-Mode) and High Speed Mode (HS-Mode).

In LP-Mode, the differential pair lines are operating in Single End Mode, the differential receiver is disabled and the termination resistor is disconnected from the differential pair lines.

In HS-Mode, the termination resistor is connected and the differential pairs are no longer working in Single End mode.

The lane states are determined by the active Transmitter (Tx). In Normal operation, the lanes are being driven by either a High Speed Transmitter (HS-Tx) or a Low Speed Transmitter (LP-Tx). In HS mode, there are 2 possible lane states and in Low Speed mode, there are 4 possible lanes states defined by the table below:-

State Code	Line Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dx+ line	Dx- line	Burst Mode	Control Mode	Escape Mode
HS-0	HS-Low	HS-High	Differential – 0	Note 1	Note 1
HS-1	HS-High	HS-Low	Differential – 1	Note 1	Note 1
LP-00	LP-Low	LP-Low	N/A	Bridge	Space
LP-01	LP-Low	LP-High	N/A	HS-Request	Mark-0
LP-10	LP-High	LP-Low	N/A	LP-Request	Mark-1
LP-11	LP-High	LP-High	N/A	Stop	Note 2

Notes:-
1. During High Speed Transmission, the Low-Power Receivers constantly check for LP-00 state code.
2. If LP-11 occurs during Escape mode, the Lane will return to Stop State (Control Mode LP-11)

8.2.2 MIPI-DSI Clock Lanes

The DSI Clock Lanes can operate in different power modes, controlled by the Transmitter (Tx):-

- High Speed Clock Mode (HSCM)
  It is only possible to enter High Speed Clock Mode (HSCM) from Low Power Mode (LPM) by the sequence LPM → LP-01 → LP-00 → HS-0 → HS-0/1 (HSCM).

- Low Power Mode (LPM)
  There are 3 possible methods to enter Low Power mode (LPM).
  1. Power On, Software Reset or Hardware Reset → LPM.
  2. From Ultra Low Power Mode (ULPM) by the sequence ULPM → LP-10 → LP-11 (LPM).
  3. From High Speed Clock Mode (HSCM) by the sequence HSCM → HS-0 → LP-11 (LPM)

- Ultra Low Power Mode. (ULPM)
  It is only possible to enter Ultra Low Power Mode (ULPM) from Low Power Mode (LPM) by the sequence LPM LP-10 → LP-00 (ULPM).

The protocols for entering/leaving the different power modes can be summarized by the following diagram:

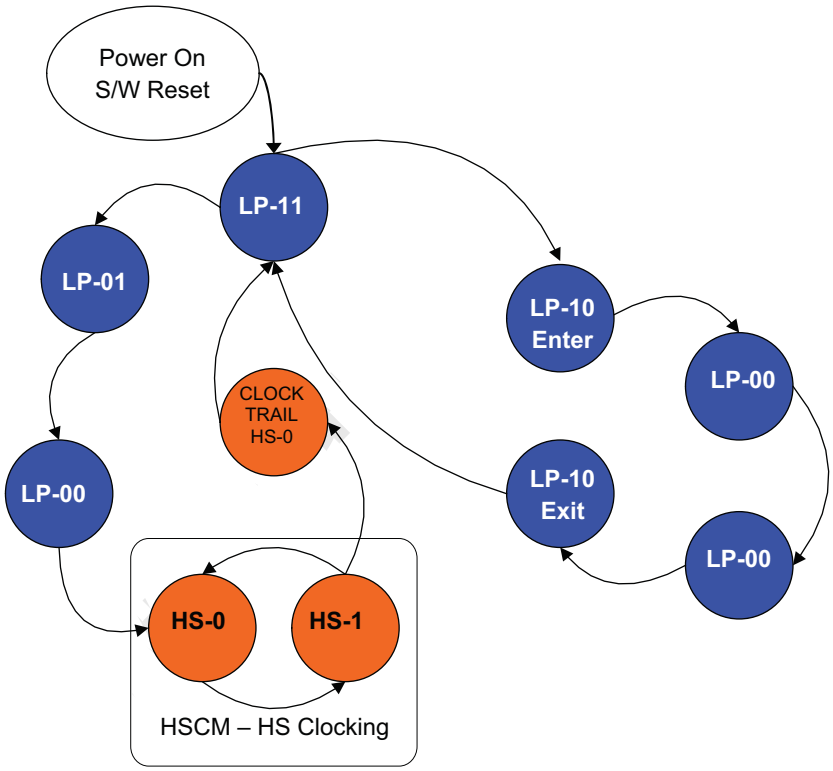


Figure 1 Clock Lane Power Modes.

For a high speed communication, the DSI CLK+/- lines are always started before high speed data is sent on DSI-D0+/- or DSI D1+/- or DSI D2+/- or DSI D3+/-. The clock lines also continue clocking for a defined period after the data transmission has ended as shown in the diagram below.

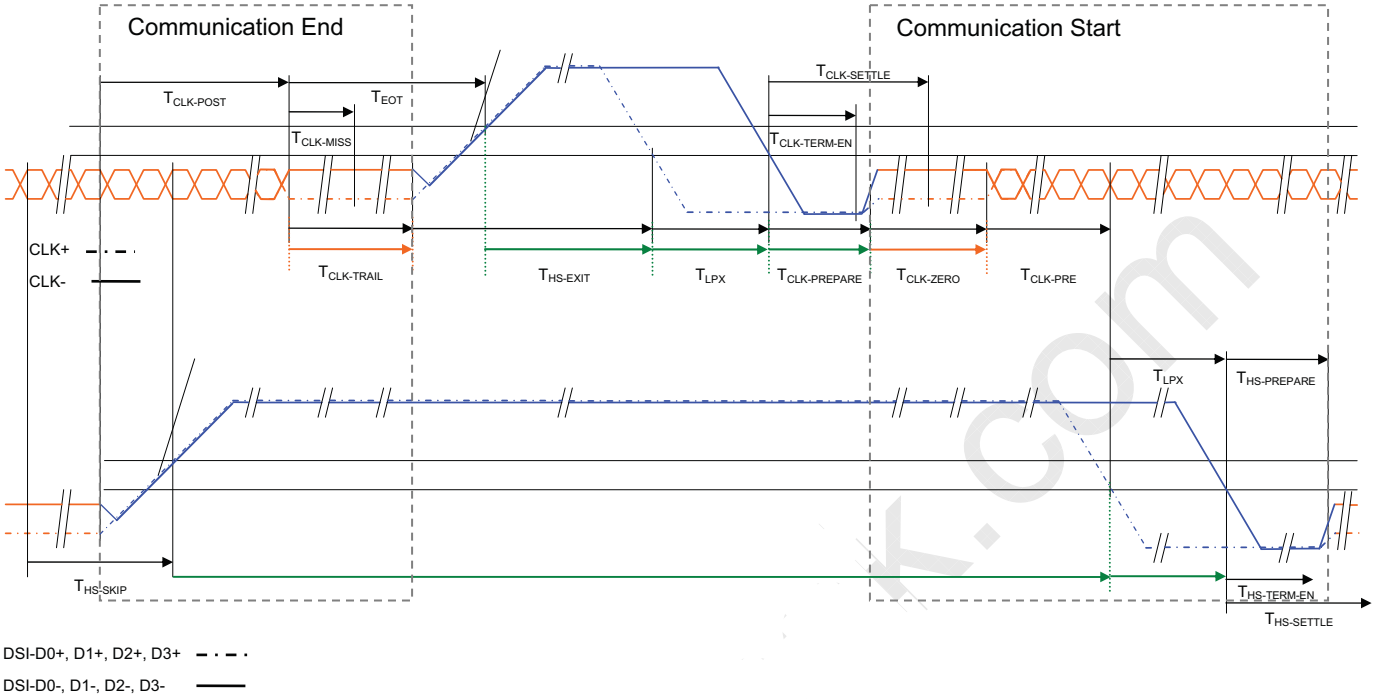


Figure 2 Clock Lane Power Transitions

The High Speed Clock burst always starts and ends with state HS-0 so the burst always contains an even number of clock transitions.

8.2.3 MIPI-DSI Data Lanes

The DSI Data Lanes DSI D0+/-, D1+/-, D2+/- and D3+/- can operate in different modes, controlled by the Transmitter (Tx):-

- High Speed Data Transmission (HSDT) where the display is receiving data from the host.

It is only possible to enter High Speed Data Transmission (HSDT) from Control Mode by the sequence LP-11 → LP-01 → LP-00 → HS-0 → HS-0/1 (HSDT).

- Escape Mode – Applies only to D0+/-.
- Bus Turnaround Mode – Applies only to D0+/-.

It is only possible to enter Bus Turnaround Mode from Control Mode by the sequence LP-11 → LP-10 → LP-00 → LP-10 → LP-00.

Control Mode is defined as the Data Lane Stop State LP-11.

8.2.4 High Speed Data Transmission

All High Speed Data Transmissions start and end with a Stop State (LP-11). The DSI CLK+/- lanes have already entered High Speed Clock Mode before starting High Speed Data Transmission.
A burst of High Speed Data always has an integer number of bytes with a minimum length of one byte.
High Speed Data Transmission can be started and ended independently for any data Lane, however normally the data Lanes will start synchronously but may end at different times if there are an unequal number of transmitted bytes for each Lane.

8.2.4.1 HSDT Start of Transmission

The display module DSI D0+/-, D1+/-, D2+/- and D3+/- enter High Speed High Transmission as follows:-

Step	Host	Display module
1	Drives Stop State LP-11	Monitors the Stop State
2	Drives HS-Request state LP-01 for time T_{LPX}.	Monitors the transition from LP-11 to LP-01
3	Drives LP-00 for time $T_{HS-PREPARE}$.	Monitors the transition from LP-01 to LP-00 and enables the Termination Impedance after time $T_{HS-TERM-EN}$
4	Drives HS-0 for a time $T_{HS-ZERO}$.	Enables HS-RX and timeout $T_{HS-SETTLE}$.
5		Monitoring for Leader-Sequence "011101"
6	Inserts the HS Sync-Sequence "00011101" beginning on a clock rising edge.	
7		Synchronizes after recognizing Leader-Sequence "011101".
8	Transmit High Speed Data	Receive High Speed data.

The sequence for starting High Speed Data Transmission on the DSI bus is shown in the following figure:-

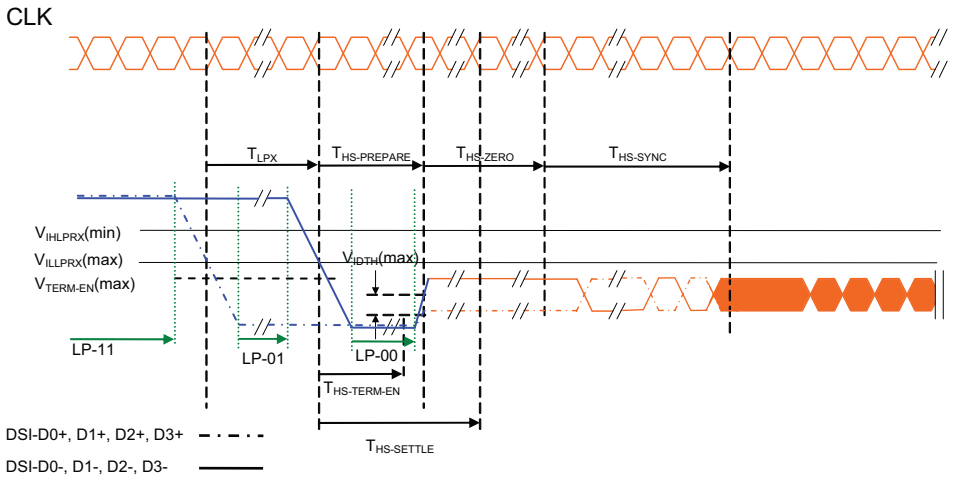


Figure 3 HSDT Start Sequence.

8.2.4.2 HSDT End of Transmission

The display module DSI D0+/-, D1+/-, D2+/- and D3+/- exits High Speed High Transmission as follows:-

Step	Host	Display module
1	End High Speed Data Transmission	Receive the last data
2	Host drives HS-1 for time $T_{HS-TRAIL}$ if the last data bit transmitted was HS-0 Host drives HS-0 for time $T_{HS-TRAIL}$ if the last data bit transmitted was HS-1	
3	Host Drives stop-state LP-11 for a minimum time $T_{HS-EXIT}$.	Monitors the entering stop state LP-11, disables the Termination Impedance and ignores the bits sent during time $T_{HS-SKIP}$.

The sequence for ending High Speed Data Transmission on the DSI bus is shown in the following figure:-

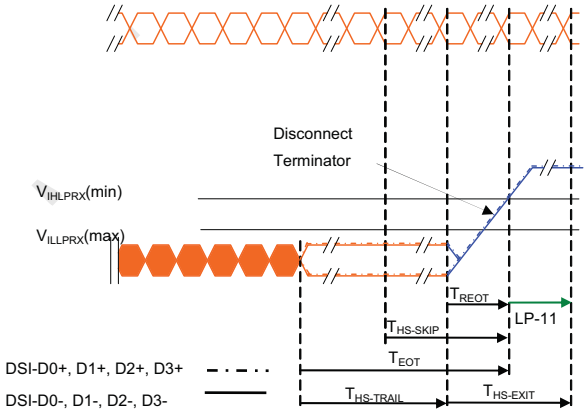


Figure 4 HSDT End Sequence.

8.2.5 Escape Mode

Escape Mode applies only to Data Lane D0+/-. This is a special mode of operation in the Low Power state and is valid in both the forward (Host to Display) and Reverse directions (Display to Host).

The Display module supports the following escape modes:-

Escape Mode Action	Command Type Mode/Trigger	Entry Command Pattern (1^{st} bit to last bit transmitted)	Note
Low Power Data Transmission	Mode	1110 0001 bin	
Ultra Low Power State	Mode	0001 1110 bin	
Remote Application	Trigger	0110 0010 bin	
Acknowledge	Trigger	0010 0001 bin	

It is only possible to enter Escape Mode from Control Mode by the sequence
LP-11 → LP-10 → LP-00 → LP-01 → LP-00.
If LP-11 state is detected before the final bridge state LP-00, then the Escape Mode entry procedure will be aborted and the Display Module will return to the stop state (LP-11).
To exit Escape mode the end sequence LP-10 → LP-00 is applied.

The following example shows the Escape Mode Entry and exit along with Reset-Trigger Escape Command.

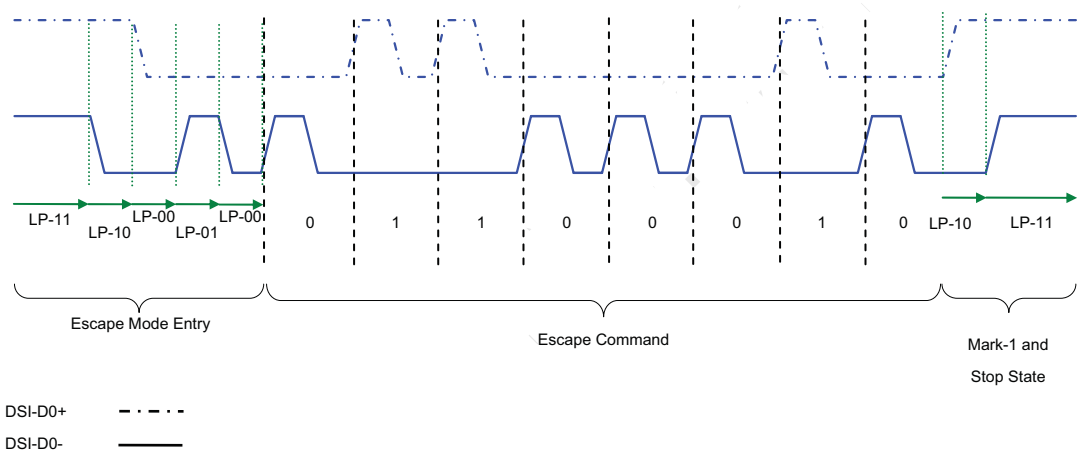


Figure 5 Escape Mode Sequence.

8.2.5.1 Low Power Data Transmission

Data can be written from the Host to the Display in Low Power Data Transmission. Firstly the Escape Mode Entry Procedure is sent followed by the (LPDT) Escape Command 11100001. Data is encoded by the same Spaced One-Hot code used for Entry Commands and it is possible to add a pause between data bytes by holding both DSI D0+/- lines low as shown in the following example.

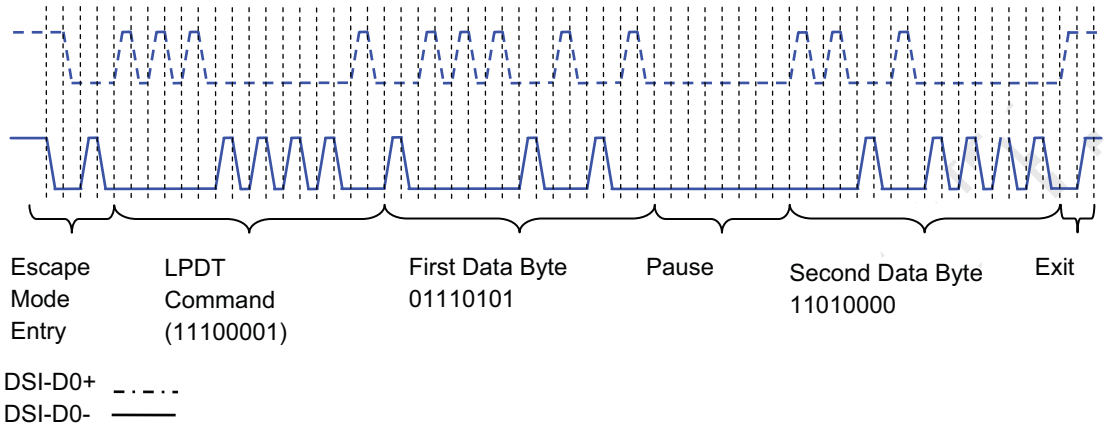


Figure 6 Low Power Data Transmission Example.

8.2.5.2 Ultra Low Power State

The DSI D0+/-, DSI D1+/-, DSI D2+/- and D3+/- data lanes can enter Ultra Low Power State, in this condition both data lines are kept Low by the Host (LP-00)
To enter Ultra Low Power State, the Escape Command 00011110 is sent after the Escape mode Entry Procedure.
To exit Ultra Low Power State, the Mark01 state (LP-10) should be applied for minimum 1msec followed by the stop state (LP-11).

The following diagram explains Ultra Low Power State entry and exit:-

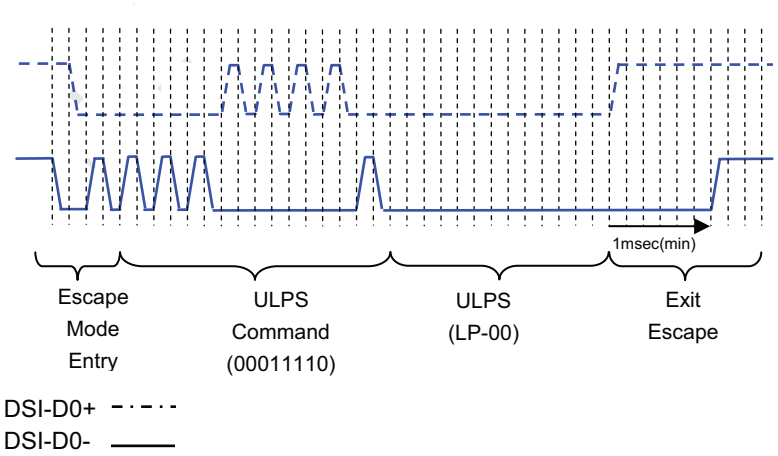


Figure 7 Ultra Low Power State Example.

8.2.5.3 Remote Application Reset

The DSI D0+/-, DSI D1+/- , DSI D2+/- and DSI D3+/- data lanes can enter Remote Application Reset State, in this condition any data bits sent on the data lanes are ignored before the Stop state is received as shown in following example:-

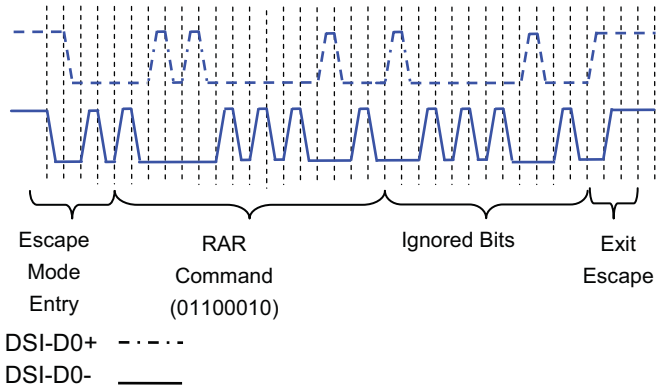


Figure 8 Remote Application Reset Example.

8.2.5.4 Remote Application Reset

The Acknowledge Trigger Escape command is used by the host to request an Acknowledge that the preceding command or data sent from the host was successfully received.
To request an Acknowledge, the host will send the Escape Command 00100001 after the Escape Entry Procedure as shown in the following diagram:-

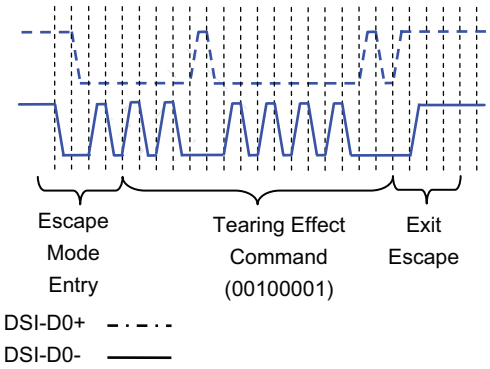


Figure 9 Acknowledge Trigger.

After sending the Acknowledge Request the host will normally send the Bus Turnaround Command and wait for the Display Module to send the Acknowledge response.

8.2.6 Bus Turnaround

The Bus Turnaround procedure can be instigated by either the host or the Display module when they want to receive information from the other device. The same sequence is used regardless of whether the host or the display is performing the turnaround request. The sequence is as follows:-

Step	Initial Tx side => Final Rx Side	Initial Rx side => Final Tx Side
1	Drives Stop State LP-11	Monitors the Stop State
2	Drives LP-Request state LP-10 for time T_{LPX}.	Monitors the transition from LP-11 to LP-10
3	Drives LP-00 for time T_{LPX}.	Monitors the transition from LP-10 to LP-00.
4	Drives LP-10 for a time T_{LPX}.	Monitors the transition from LP-00 to LP-10.
5	Drives LP-00 for a time T_{TA-GO}.	Monitors the transition from LP-10 to LP-00 and waits for a time $T_{TA-SURE}$.
6		Drives LP-00 for a time T_{TA-GET}.
7	Stops driving the DSI Lanes and output drivers become High-Z. Receiver is monitoring for LP-10 state.	
8		Drives LP-10 for a time T_{LPX}.
9	Monitors LP-10 and interprets this as an acknowledgement that the other side has taken over the bus. Waits for Stop state (LP-11) to complete the procedure	
10		Drives LP-11 for a time T
11	Monitors the transition from LP-10 to LP-11 and interprets this as Turnaround complete. Switched to LP Rx mode and waits for next action from the other side.	

The Bus Turnaround Sequence is as follows:-

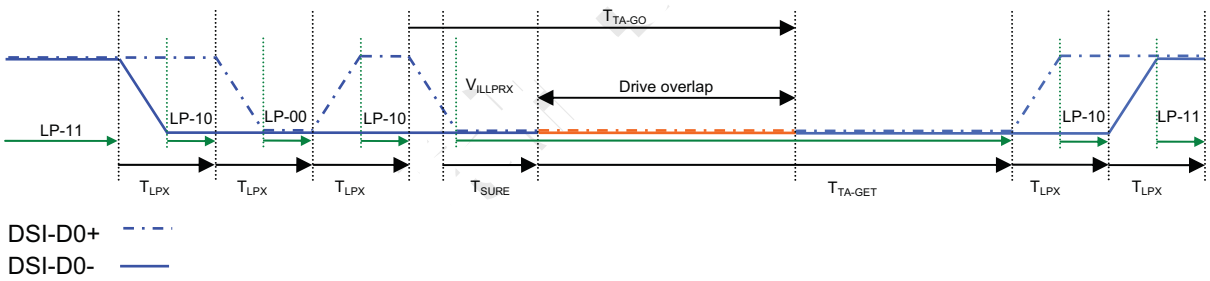


Figure 10 Bus Turnaround Sequence.

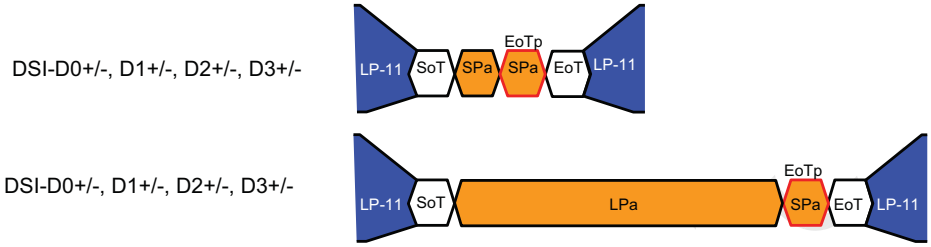
The bus turnaround procedure can be aborted if a Stop state (LP-11) is sent before the bus starts to be driven LP-00 at the beginning of time period TSURE in Fig9. In this event, the lanes will return to the stop state LP-11.
It is not possible to abort the turnaround procedure after LP-00 at the time TSURE has started to be driven.

8.2.7 Packet Level Communication

Data is transferred between host and the display module and vice-versa by means of packet Level communication. Packet communication applies to both Low Power Data Transmission mode (LPDT) and High Speed Data Transmission (HSDT).
A Transmission may consist of both Short Packets (SPa) and Long Packets (LPa), it may contain only one packet or multiple packets. Also multiple packets may consist of both Short (SPa) and Long (LPa) packets.

For High Speed Mode, Each Transmission requires Start of Transmission SoT, End of Transmission Packet (which is the last transmitted packet (SPa)) and End of Transmission (EoT).

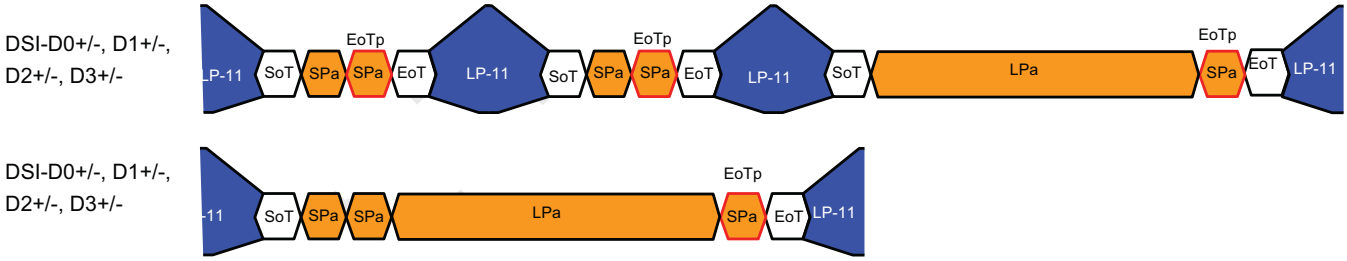
Example of single Short Packet Transmission and single Long Packet Transmission.



Key:
LP-11 – Low Power Mode
SoT – Start of Transmission
SPa – Short Packet
LPa – Long Packet
EoTp – End of Transmission Packet
EoT – End of Transmission

Figure 11 Single Packet Transmission.

Example of the same multiple Short and Long Packet Transmissions sent in Separate and Single transmissions.



Key:
LP-11 – Low Power Mode
SoT – Start of Transmission
SPa – Short Packet
LPa – Long Packet
EoTp – End of Transmission Packet
EoT – End of Transmission

Figure 12 Multiple Packet Transmission.

8.2.7.1 Data Byte Order in HSDT

When 3 channels are in use, data is always transmitted in the order of the First Byte appears on DSI Lane 0, the second byte on DSI data Lane 1, third on Data Lane 2 , fourth on DSI data lane 0 and so on.
Both DSI-D0+/-, DSI-D1+/-, DSI-D2+/- and DSI-D3+/- will always start data transmission simultaneously with SoT however depending upon the number of bytes being transferred one lane may complete transfer before the other lane.

8.2.7.2 Packet Bit and Byte Order

For each byte in a packet, the bit order is the LSB is sent first and the MSB is sent last. For packets with multiple bytes, the least significant byte is sent first and the most significant byte is sent last..

8.2.7.3 Short Packet Format

Short packets are 4 bytes in length. They are used mainly for sending commands with either none or one parameter. The structure of the packet is as follows, this example is using High Speed Data Transfer, Low Power Data Transfer can also be used.:-

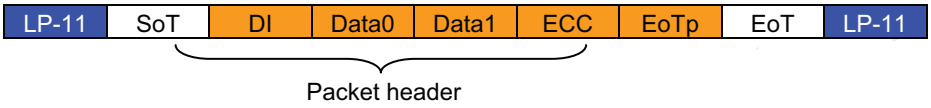


Figure 13 Short Packet Format.

Where:-
DI = Data Identifier Byte
Contains the Virtual Channel Identifier and the Data Type information.
Data0 = LSB Byte
Data1 = MSB Byte
ECC = Error Correction Code
8-Bit Error Code Correction for the correction of single-bit error and the detection of 2-bit errors.

Bit order on the short packet appears as shown in the following example:-

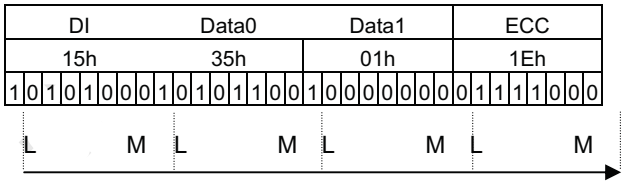


Figure 14 Short Packet Example.

8.2.7.4 Long Packet Format

Long packets are minimum 6bytes in length and can contain up to a maximum of 65,536 data bytes. The structure of the packet is as follows, this example is using High Speed Data Transfer, Low Power Data Transfer can also be used:-

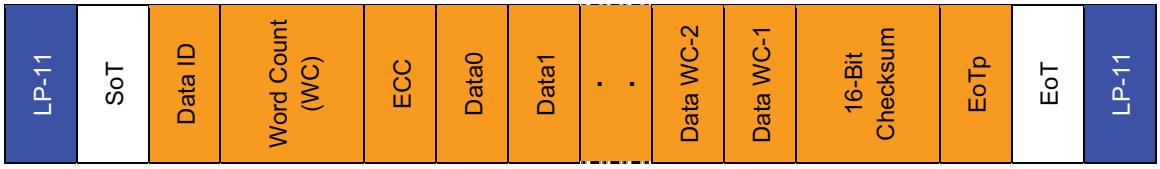


Figure 15 Long Packet Format.

Where:-

Data ID = Data Identifier Byte

Contains the Virtual Channel Identifier and the Data Type information.

WC = 16-Bit Word Count

The word count informs how many data bytes will be sent in the packet payload from this the Display Module can determine the packet end.

ECC = Error Correction Code

8-Bit Error Code Correction for the correction of single-bit error and the detection of 2-bit errors within the Packet Header.

Data0→Data WC-1 = Packet Data (Payload)

16-Bit Checksum = Checksum for the transmitted packet data payload.

The Display module will calculate the Checksum value from the received data and compare with the transmitted Checksum value from the host. The display module will report an error at the next Bus Turnaround if the values are not equal.

Bit order on the long packet appears as shown in the following example:-

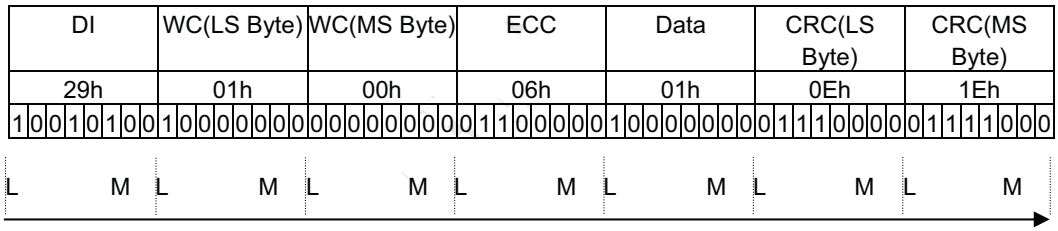


Figure 16 Long Packet Example.

8.2.7.5 Data Identifier Byte

The Data Identifier Byte serves 2 purposes. One is the Virtual Channel Identification and the other specifies the Data type:-

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Virtual Channel (VC)		Data Type (DT)					

8.2.7.5.1 Virtual Channel Identifier (VC)

The Virtual Channel can allow addressing up to 4 channels, in other words 4 different devices connected to the same receiver.
This display module uses virtual channel 0, i.e. Bits 7 and 6 = '00'.
When the display module sends information back to the host it will also assign Virtual Channel 0 in its packet header.

8.2.7.5.2 Data type Field (DT)

The Data Type Field informs if the packet is a Short (SPa) or Long Packet (LPa), it also contains information about the type of data transaction from the host to the display module and also from the display module to the host. The supported data transaction types are listed in the following tables:-
Data Types from the Host to the Display Module.

Data Type	Data type (binary)						Description	Packet Size	Note
(Hex]	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
01h	0	0	0	0	0	1	Sync Event, V Sync Start	Short	
21h	1	0	0	0	0	1	Sync Event, H Sync Start	Short	
08h	0	0	1	0	0	0	End of Transmission Packet (Note 1).	Short	
23h	1	0	0	0	1	1	Generic Short WRITE, 2 parameters	Short	1, 3
29h	1	0	1	0	0	1	Generic Long Write	Long	1
14h	0	1	0	1	0	0	Generic Short READ, 1 parameter	Short	1, 2
24h	1	0	0	1	0	0	Generic Short READ, 2 parameter	Short	1, 3
05h	0	0	0	1	0	1	DCS WRITE with No Parameter.	Short	
15h	0	1	0	1	0	1	DCS WRITE with One Parameter.	Short	
06h	0	0	0	1	1	0	DCS READ with No Parameter.	Short	
37h	1	1	0	1	1	1	Set Maximum Return Packet Size	Short	
09h	0	0	1	0	0	1	Null Packet, No data (Note 2).	Long	
19h	0	1	1	0	0	1	Blanking Packet, no data	Long	
39h	1	1	1	0	0	1	DCS WRITE Long	Long	
3Eh	1	1	1	1	1	0	Packed Pixel Stream,24bit RGB 8-8-8 Format	Long	
other	x	x	x	x	x	x	DO NOT USE All unspecified codes are reserved		

Notes:

1.The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).
2. Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.
3. Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.
4. The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.

Data Types from the Display Module to the Host.

Data Type	Data Type (Binary)						Description	Packet Size	Symbol
(Hex)	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
02h	0	0	0	0	1	0	Acknowledge with Error Report.	Short	AwER
08h	0	0	1	0	0	0	End of Transmission (EoT) Packet	Short	EoT
1Ch	0	1	1	1	0	0	DCS READ Long Response.	Long	DCSRR-L
21h	1	0	0	0	0	1	DCS READ Short Response, 1 Byte Returned.	Short	DCSRR1-S
22h	1	0	0	0	1	0	DCS READ Short Response, 2 Bytes Returned.	Short	DSCRR2-S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Long	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response, 1byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response, 2byte returned	Short	GENRR2-S

Notes:
The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or "Data Type (DT) from the Display Module (or Other Devices) to the MCU".

8.2.7.6 Packet Data on the Short Packet (Spa)

Packet data is 2 bytes long in a short packet. If the length of data to be sent requires only 1 byte, then the data in the 2nd byte (Data 1) will be set as all zero.
Packet data is always sent in the order Data0 first, followed by Data1as shown in the below example:-

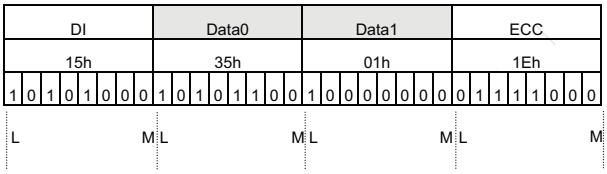


Figure 17 Data on the Short Packet.

8.2.7.7 Word Count (WC) on the Long packet

The word count is used to indicate how many bytes of data will be sent after the Packet header.
The word count is 2 bytes long and can define a minimum of 0 bytes to a maximum of 65,536 bytes to be sent.
The sending order of the 2 word count bytes is the Least Significant Byte is always sent first followed by the most Significant Byte.

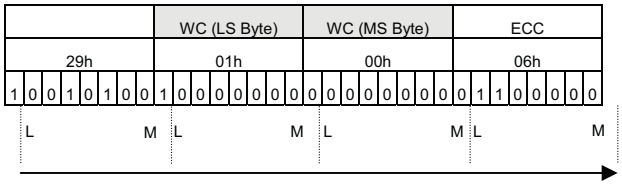


Figure 18 Word Count on the Long Packet.

8.2.7.8 Error Correction Code (ECC)

The Error Correction Code allows single-bit errors to be corrected and 2 or more-bit errors to be detected in the Packet Header. It is used for both Short (Spa) and Long (Lpa) packets.

When receiving data transmission from the host, the display module will generate ECC byte from the received packet header Data Identifier (DI) and Data0, Data1 bytes in the case of SPa and Data Identifier (DI), WC (LS Byte), WC (MS Byte) in the case of LPa. It will compare this generated ECC byte with that sent on the Packet Header to determine if error has occurred or not.

When sending Data Transmission to the host, the Display Module will generate the ECC byte from the packet data to be sent and appends to the packet header. The ECC byte is always the last transmitted byte on the packet header as highlighted in this example for the Short Packet (SPa):-

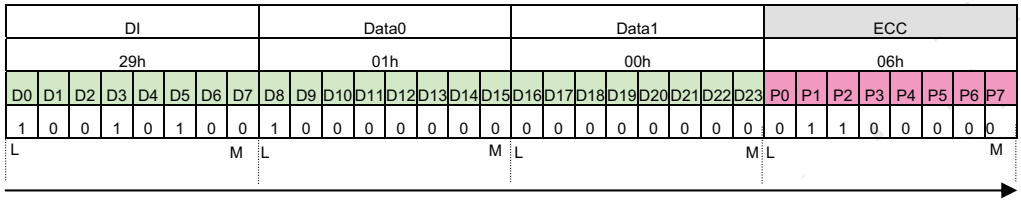


Figure 19 Error Correction Code on the Short Packet.

The Pink colored bits are the error correction bits.
The Green colored bits are the bits that can be corrected by the ECC.

The device transmitting the data sends data D[23..0] and ECC P[7..0]. An 8-bit ECC allows correction for up to 64bits, however in this application only 24bits require to be checked for correction, so bits P7 and P6 are always set to ‘00’ on the ECC.
The remaining bits are generated as follows:-

P7=0
P6=0
P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2=D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

where “^” = XOR function.

The receiving device generates the ECC from the received data D[23..0] by the same function as above to generate IECC (internal ECC). The function ECC^IECC is performed and the result OP[7..0]determines if error has occurred or not.

- If the result of ECC^IECC = 00h, then there is no error in the data received.
- If the result of ECC^IECC 00h and is listed on the table in Fig20, then the error is a single bit error and that corresponding bit can be corrected. Also the ECC error, single bit (detected and corrected)” bit is flagged.
- If the result of ECC^IECC ≠ 00h and is not listed on the table in Fig20, then the error is in 2bits or more and cannot be corrected, the packet is ignored and the “ECC error, multi-bit (detected, not corrected)” bit is flagged.

Data Bit	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	ECC^IECC
D0	0	0	0	0	0	1	1	1	07h
D1	0	0	0	0	1	0	1	1	0Bh
D2	0	0	0	0	1	1	0	1	0Dh
D3	0	0	0	0	1	1	1	0	0Eh
D4	0	0	0	1	0	0	1	1	13h
D5	0	0	0	1	0	1	0	1	15h
D6	0	0	0	1	0	1	1	0	16h
D7	0	0	0	1	1	0	0	1	19h
D8	0	0	0	1	1	0	1	0	1Ah
D9	0	0	0	1	1	1	0	0	1Ch
D10	0	0	1	0	0	0	1	1	23h
D11	0	0	1	0	0	1	0	1	25h
D12	0	0	1	0	0	1	1	0	26h
D13	0	0	1	0	1	0	0	1	29h
D14	0	0	1	0	1	0	1	0	2Ah
D15	0	0	1	0	1	1	0	0	2Ch
D16	0	0	1	1	0	0	0	1	31h
D17	0	0	1	1	0	0	1	0	32h
D18	0	0	1	1	0	1	0	0	34h
D19	0	0	1	1	1	0	0	0	38h
D20	0	0	0	1	1	1	1	1	1Fh
D21	0	0	1	0	1	1	1	1	2Fh
D22	0	0	1	1	0	1	1	1	37h
D23	0	0	1	1	1	0	1	1	3Bh

Figure 20 Table of One Bit Error Value for ECC

For example if the value of the function ECC^IECC (OP[7..0]) = 1Fh, then by referring to the above table, this means there has been a one bit error on bit D20. The receiver can correct this error by complementing the bit value of D20 and storing the modified value.

8.2.7.9 Footer on Long Packet (LPa)

To detect errors in transmission of Long Packets, a checksum is calculated over the payload portion of the data packet. Long packets can transmit from 0 to 65,536 bytes, on the special case where there are 0 bytes transmitted, the Checksum value will be fixed to FFFFh.

The checksum can only detect the presence of one or more errors on a transmitted data payload, it cannot make any correction.

The checksum is realized by a 16-bit Cyclic Redundancy Check calculation by the polynomial x^16+x^12+x^5+x^0

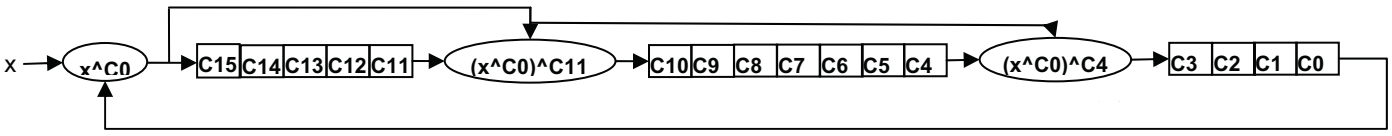


Figure 21 Bit Cyclic Redundancy Check Calculation

In the transmitting device, before Packet Data transmission starts, the CRC shift register is initialized to FFFFh, then packet data (excluding the Packet Header) enters as a bitwise stream at "x" in above figure from the Least Significant Bit first.

After all the Bytes in the packet payload have passed through the CRC shift register, then the shift register contains the Checksum Value C[15..0]. This is appended to the data stream and passed to the receiver.

The receiver will calculate Checksum by the same method and compare its calculated value versus the transmitted value. If an error is detected, then the "Checksum Error" bit is flagged.

8.2.8 Host to Display Module Packet Trnsmissions

8.2.8.1 Display Command Set (DCS)

The Display Command Set is described in Section 2.2.7.5.2 / 2.4, it is used for sending commands from the Host to the Display Module. The Command is always set on Data0 and parameters are set on the following bytes.
In the case of Short Packet Transfer (SPa), if the command has no parameter, then the second byte (Data1) is set to 00h.
If the command requires more than one parameter, then the Long Packet Transfer (LPa) is used.

The following transfer types are supported; please refer to the table in Section 2.2.7.5.2 for the various Data Field Type Code

8.2.8.2 DCS Command WRITE with No Parameter, (DT=05h).

DCS Command WRITE with No Parameter is used for writing a command which has no parameter to the Display Module, always using Short Packet (SPa). The following commands can be sent by this method:-

Example of sending Sleep In (10h) command:-

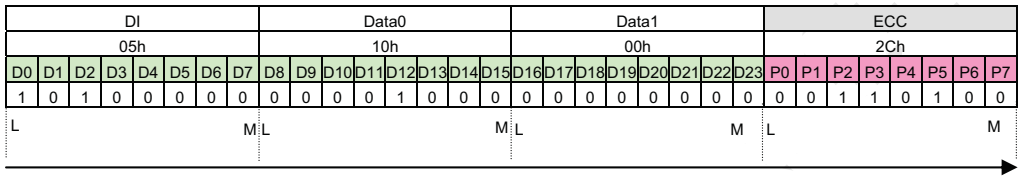


Figure 22 DCS Command WRITE with No Parameter.

8.2.8.3 DCS Command Write with 1 Parameter, (DT=15h).

DCS Command WRITE with 1 Parameter is used for writing a command which has 1 parameter to the Display Module, always using Short Packet (SPa).

Example of sending Gamma Set (26h) command:-

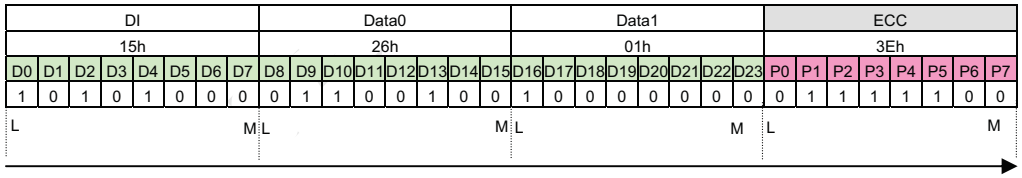


Figure 23 DCS Command WRITE with No Parameter

8.2.8.4 DCS Command Read with No Parameter, (DT=06h) & Set Maximum Return Size (DT=37h).

DCS Command Read with no Parameter is used to request data from the Display Module, always using Short Packet (SPa). Before sending this Data Type, the host has to define to the Display Module what is the maximum size of the return packet. This is defined by Data Type Set Maximum Return Size (DT=37h). Following this read request, the Bus Turnaround shall be performed so the Display Module can send back the requested data. The following read commands can be requested by this method:-

Example of requesting Read ID1 (DAh) command:-

Firstly send the maximum return size (DT=37h) then Read Command with no parameter (DT=06h).

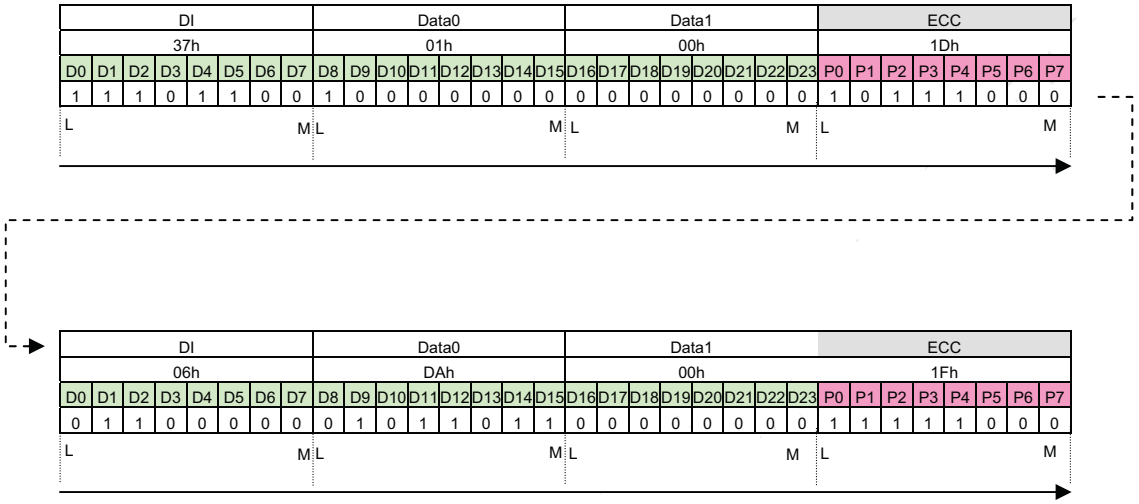


Figure 24 DCS Command Read.

After sending the Bus Turnaround Command, the Display Module will reply with either of the following:-

1. An acknowledge with Error Report (AwER) in a short packet if there is an error to report. See Section 2.4.9.1
2. Read data for the requested read command in Short (SPa) or Long (LPa) packets.

Note:
The Default value of the Maximum Return Size (DT=37h) after Power On, Hardware or Software Reset is 1.

8.2.8.5 Null Packet, No data, (DT=09h)

The purpose of this command is to keep the Data Lanes in High Speed Mode if required. The format of this packet is Long Packet (LPa). Any data included in a Null Packet is completely ignored by the Display Module.

Example of Sending a Null Packet of 5 bytes in length:-

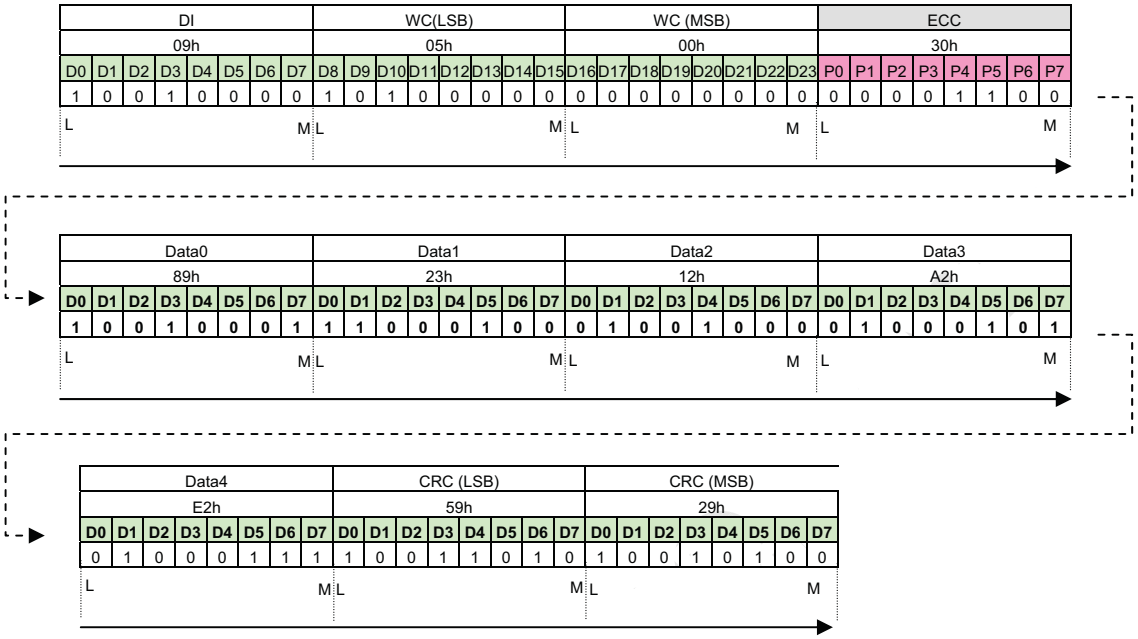


Figure 25 Null Packet, No Data.

8.2.8.6 DCS WRITE Long (DT=39h).

DCS WRITE Long is used for writing commands both with and without parameter types to the Display Module, always using Long Packet (LPa). The following commands can be sent by this method:-

Example 1 - Sending Sleep In (10h) command (DCS Command with no Parameter):-

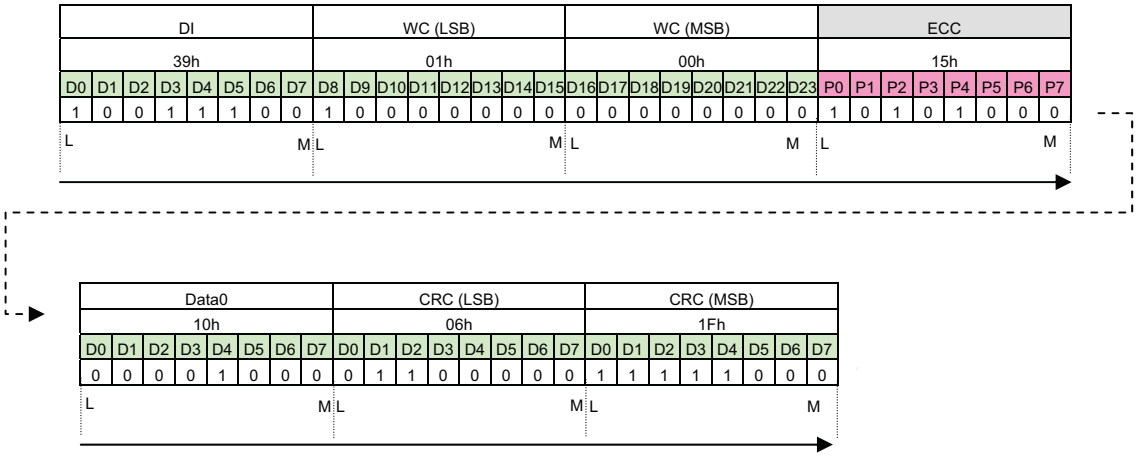


Figure 26 Long Packet Example 1.

Example 2 - Sending Gamma Set (26h) command (DCS Command with one Parameter):-

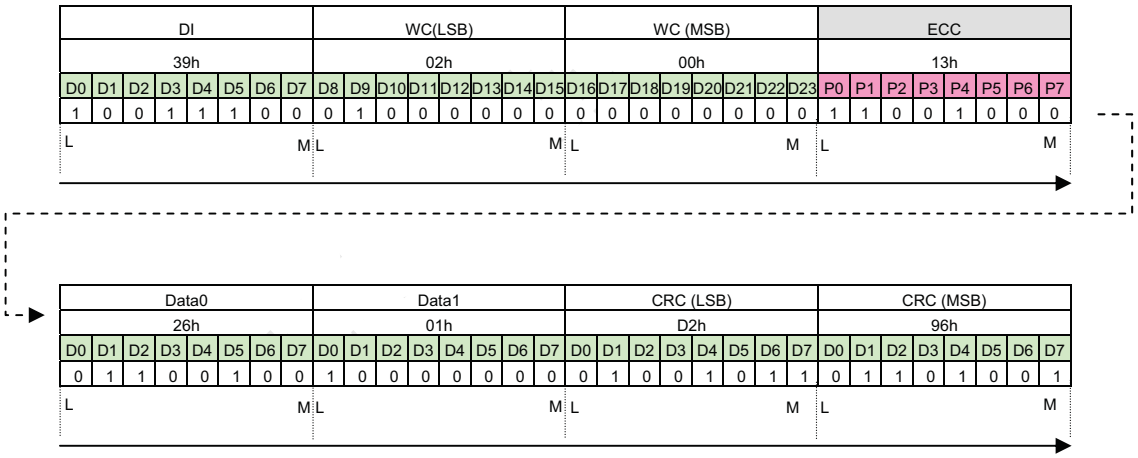


Figure 27 Long Packet Example 2.

Example 3 - Sending Column Address Set (2Ah) command (DCS Command with four Parameters):-

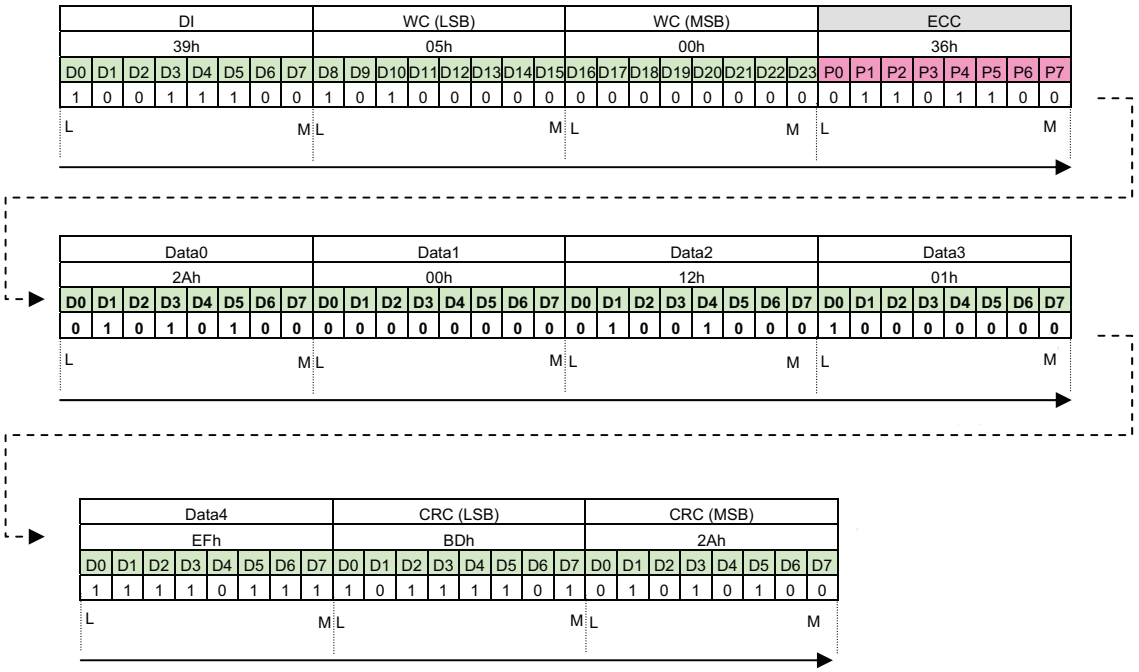


Figure 28 Long Packet Example 3.

8.2.8.7 End of Transmission Packet (DT=08h)

The purpose of the End of Transmission Packet (EoTp) is to indicate to the Display module that the host intends to terminate High Speed Data Transmission. It is always using Short Packet (SPa). This packet is always added after the last payload data and before the End of Transmission Sequence.
It is possible that the EoTp is sent in Low Power Mode, in such case there is no influence to the display module.

Example of End of Transmission Packet:-

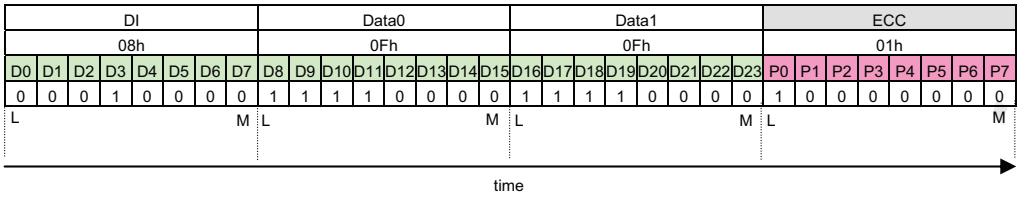


Figure 29 End of Transmission Packet.

8.2.8.8 Generic Short WRITE Packet with 1, or 2 parameters (DT=13h or 23h)

Generic Short WRITE command is a Short packet type for sending generic command and data to the LCD.
The complete packet shall be four bytes in length including an ECC byte. The two Data Type MSBs, bits [5:4], indicate the number of valid parameters (1, or 2). For single-byte parameters, the parameter shall be sent in the first data byte following the DI byte and the second data byte shall be set to 0x00.

8.2.8.9 Generic Short Read Packet with 1, or 2 parameters (DT=14h or 24h)

Generic READ request is a Short packet requesting data from the LCD.
Returned data may be of Short or Long packet format. Note the Set Max Return Packet Size command limits the size of returning packets so that the host processor can prevent buffer overflow conditions when receiving data from the peripheral. If the returning block of data is larger than the maximum return packet size specified, the read response will require more than one transmission. The host processor shall send multiple Generic READ requests in separate transmissions if the requested data block is larger than the maximum packet size.

8.2.8.10 Generic Long Write (DT=29h)

Generic Long Write Packet is used to transmit arbitrary blocks of data from a host processor to a peripheral in a Long packet. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum as DCS Long Write.

8.2.9 Host to Display Module Packet Transmissions for Video mode operation

8.2.9.1 Sync Event (V Start, H Start) (DT=01h, 21h)

Sync Events are Short packets to represent timing information as accurately as possible a V sync and H Sync Start event. Timing position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the LCD. See section for timing details of interlaced video formats. Sync events may be concatenated with blanking packets to transport inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however.

8.2.9.2 Blanking Packet (Long) (DT=19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload.

8.2.9.3 Packed Pixel Stream, 24bit RGB 8-8-8 Format (Long) (DT=3Eh)

Packed Pixel Stream 24-Bit Format shown in Figure 28 is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

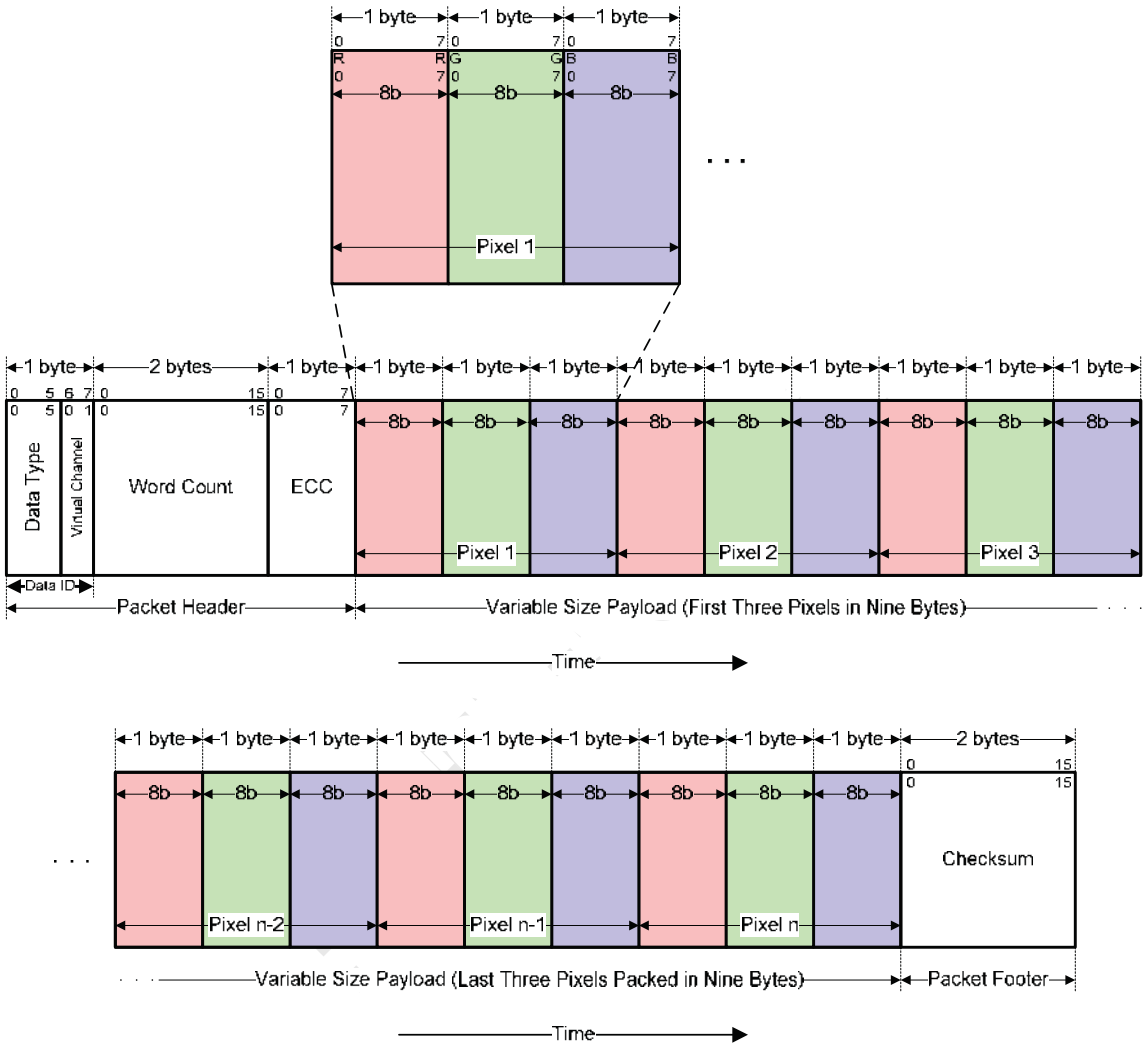


Figure 31 24-bit per Pixel – RGB Color Format, Long Packet

8.2.10 Display Module to Host Packet LP Transmissions

8.2.10.1 Acknowledge and Error Report (DT=02h)

The purpose of the Acknowledge and Error Report is to feedback to the Host if any errors occurred in data transmissions from the Host to the Display Module since the previous communication from the Display Module to the Host. It is always using Short Packet (SPa).

Example of Acknowledge and Error Report:-

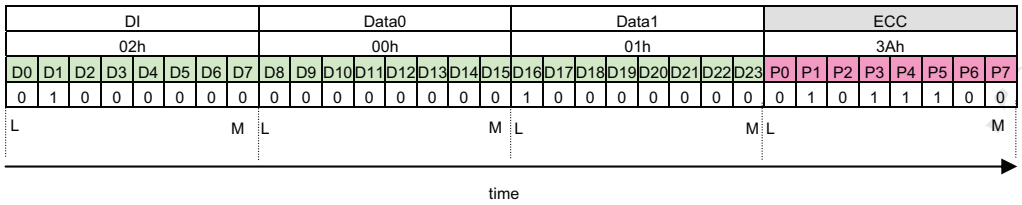


Figure 32 End of Transmission Packet.

In general, after there has been communication from the Host to the Display Module followed by a Bus Turnaround BTA, the Display Module will respond with either an Acknowledge if there have been no recorded error or an “Acknowledge and Error Report” Packet if there are errors to report.
The following table provides a list of the bit assignments for the “Acknowledge and Error Report” packet:-

Bit	Description	Implementation
0	SoT Error	No
1	SoT Sync Error	No
2	EoT Sync Error	No
3	Escape Mode Entry Command Error	Yes
4	Low-Power Transmit Sync Error	Yes
5	HS Receive Timeout Error	No
6	False Control Error	No
7	Reserved	-
8	ECC Error, single-bit (detected and corrected)	Yes
9	ECC Error, multi-bit (detected, not corrected)	Yes
10	Checksum Error (Long Packet only)	Yes
11	DSI Data Type Not Recognized	Yes
12	DSI Virtual Channel (VC) ID Invalid	Yes
13	Invalid Transmission Length	No
		-
15	DSI Protocol Violation.	No

8.2.10.2 DCS Read Long Response (DT=1Ch)

DCS Read Long Response is used for sending requested read data from the Display Module back to the Host. The format is the same as Long Packet (LPa) writing from the Host to the Display Module i.e. It has a packet header containing the Data Identifier, two byte Word Count and an ECC byte.

Example – Sending 5 bytes of data:-

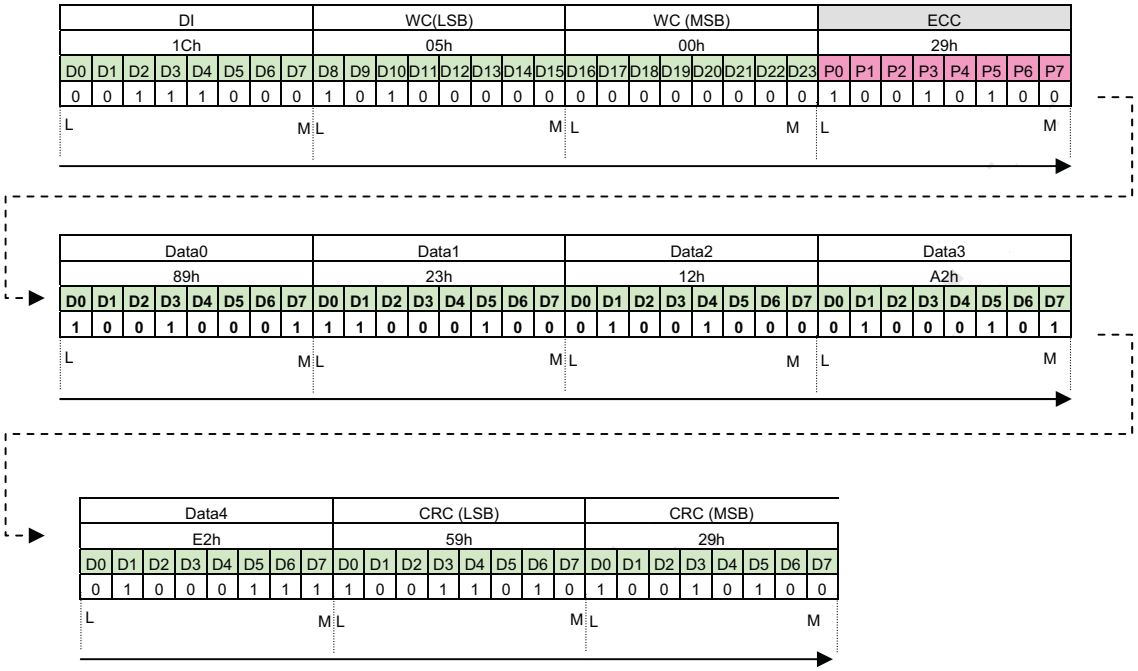


Figure 33 DCS Read Long Response.

8.2.10.3 DCS Read Short Response, 1 Byte Returned (DT=21h)

DCS Read Short Response with 1 byte Returned is used for sending requested read data of 1 byte in length, always using Short Packet (SPa).

Example of sending DCS Read Short Response with 1 byte Returned:-

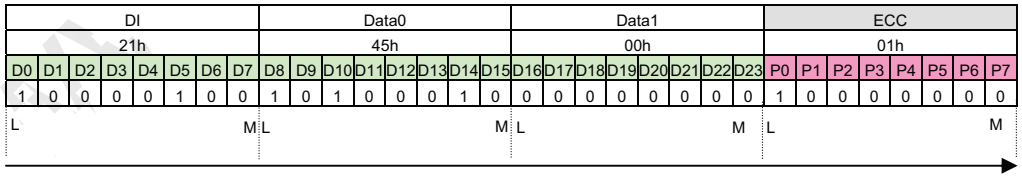


Figure 34 DCS Read Short Response, 1 byte Returned.

8.2.10.4 DCS Read Short Response, 2 Byte Returned (DT=22h)

DCS Read Short Response with 2 bytes Returned is used for sending requested read data of 2 bytes in length, always using Short Packet (SPa).

Example of sending DCS Read Short Response with 2 bytes Returned:-

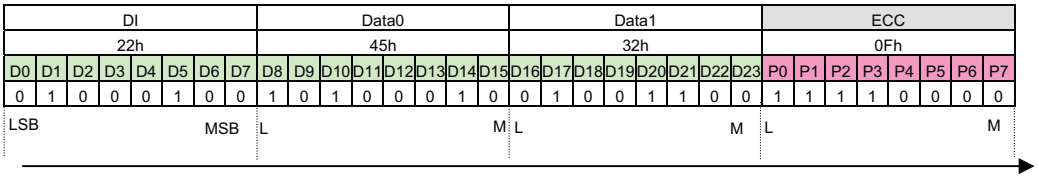


Figure 35 DCS Read Short Response, 2 bytes Returned.

8.3 MIPI INTERFACE TIMING ON VIDEO MODE

The RSP LCD driver supports Video Mode for moving pictures. There are three formats of transmission packet sequences. The RSP LCD driver supports two of these formats. See the following table.

Transmission packet sequence in video mode	RSP LCD driver implementation
Non-burst mode with sync pulses	Not supported
Non-burst mode with sync events	Supported
Burst mode	Supported

8.4 COMMANDS

Command Table 1

Address [Hex]	Parameter	Instruction	D7	D6	D5	D4	D3	D2	D1	D0
00h		NOP	No Argument							
01h		SOFT_RESET	No Argument							
10h		ENTER_SLEEP_MODE	No Argument							
11h		EXIT_SLEEP_MODE	No Argument							
28h		SET_DISPLAY_OFF	No Argument							
29h		SET_DISPLYA_ON	No Argument							
2Ah	1st Parameter	SET_COLUMN _ADDRESS	0	0	0	0	0	SC_10	SC_9	SC_8
	2nd Parameter		SC_7	SC_6	SC_5	SC_4	SC_3	SC_2	SC_1	SC_0
	3rd Parameter		0	0	0	0	0	EC_10	EC_9	EC_8
	4th Parameter		EC_7	EC_6	EC_5	EC_4	EC_3	EC_2	EC_1	EC_0
2Bh	1st Parameter	SET_PAGE _ADDRESS	0	0	0	0	0	SP_10	SP_9	SP_8
	2nd Parameter		SP_7	SP_6	SP_5	SP_4	SP_3	SP_2	SP_1	SP_0
	3rd Parameter		0	0	0	0	0	EP_10	EP_9	EC_8
	4th Parameter		EP_7	EP_6	EP_5	EP_4	EP_3	EP_2	EP_1	EP_0
34h		SET_TEAR_OFF	No Argument							
35h	1st Parameter	SET_TEAR_ON	x	x	x	x	x	x	x	TELOM
3Ah	1st Parameter	SET_PIXEL_FORMAT	0	D6	D5	D4	0	D2	D1	D0
44h	1st Parameter	SET_TEAR_SCANLINE	0	0	0	0	0	STS_10	STS_9	STS_8
	2nd Parameter		STS_7	STS_6	STS_5	STS_4	STS_3	STS_2	STS_1	STS_0
51h	1st Parameter	WRITE_DISPLAY_BRIGHTNESS	DBV_7	DBV_6	DBV_5	DBV_4	DBV_3	DBV_2	DBV_1	DBV_0
52h	Dummy parameter	READ_DISPLAY_BRIGHTNESS_VALUE	x	x	x	x	x	x	x	x
	1st Parameter		RD_DBV 7	RD_DBV 6	RD_DBV 5	RD_DBV 4	RD_DBV 3	RD_DBV 2	RD_DBV 1	RD_DBV 0
	2nd Parameter		RD_DBV _L_3	RD_DBV _L_2	RD_DBV _L_1	RD_DBV _L_0	0	0	0	0
53h	1st Parameter	WRITE_CONTROL _DISPLAY	x	x	BCTRL	x	DD	BL	x	x
54h	Dummy parameter	READ_CONTROL _VALUE_DISPLAY	x	x	x	x	x	x	x	x
	1st Parameter		x	x	BCTRL	x	DD	BL	x	x
55h	1st Parameter	WRITE_CONTENT_ADAPTIVE_BRIGHTNESS _CONTROL	x	SRE _ON	SRE_1	SRE_0	x	x	C1	C0

Command Table 2

Address [Hex]	Parameter	Instruction	D7	D6	D5	D4	D3	D2	D1	D0
A1h	Dummy parameter	READ_DDB_START	x	x	x	x	x	x	x	X
	1st Parameter		ID1_15	ID1_14	ID1_13	ID1_12	ID1_11	ID1_10	ID1_9	ID1_8
	2nd Parameter		ID1_7	ID1_6	ID1_5	ID1_4	ID1_3	ID1_2	ID1_1	ID1_0
	3rd Parameter		ID2_15	ID2_14	ID2_13	ID2_12	ID2_11	ID2_10	ID2_9	ID2_8
	4th Parameter		ID2_7	ID2_6	ID2_5	ID2_4	ID2_3	ID2_2	ID2_1	ID2_0
	5th Parameter		ID3_7	ID3_6	ID3_5	ID3_4	ID3_3	ID3_2	ID3_1	ID3_0
	6th Parameter		ID4_7	ID4_6	ID4_5	ID4_4	ID4_3	ID4_2	ID4_1	ID4_0
	7th Parameter		0	0	0	0	0	0	0	0
	8th Parameter		RD_DDB6_7	RD_DDB6_6	RD_DDB6_5	RD_DDB6_4	RD_DDB6_3	RD_DDB6_2	RD_DDB6_1	RD_DDB6_0
	9th Parameter		RD_DDB7_7	RD_DDB7_6	RD_DDB7_5	RD_DDB7_4	RD_DDB7_3	RD_DDB7_2	RD_DDB7_1	RD_DDB7_0
	10th Parameter		RD_DDB8_7	RD_DDB8_6	RD_DDB8_5	RD_DDB8_4	RD_DDB8_3	RD_DDB8_2	RD_DDB8_1	RD_DDB8_0
	11th Parameter		RD_DDB9_7	RD_DDB9_6	RD_DDB9_5	RD_DDB9_4	RD_DDB9_3	RD_DDB9_2	RD_DDB9_1	RD_DDB9_0
	12th Parameter		RD_DDB10_7	RD_DDB10_6	RD_DDB10_5	RD_DDB10_4	RD_DDB10_3	RD_DDB10_2	RD_DDB10_1	RD_DDB10_0
	13h Parameter		RD_DDB11_7	RD_DDB11_6	RD_DDB11_5	RD_DDB11_4	RD_DDB11_3	RD_DDB11_2	RD_DDB11_1	RD_DDB11_0
	14th Parameter		RD_DDB12_7	RD_DDB12_6	RD_DDB12_5	RD_DDB12_4	RD_DDB12_3	RD_DDB12_2	RD_DDB12_1	RD_DDB12_0
	15th Parameter		RD_DDB13_7	RD_DDB13_6	RD_DDB13_5	RD_DDB13_4	RD_DDB13_3	RD_DDB13_2	RD_DDB13_1	RD_DDB13_0
	16th Parameter		RD_DDB14_7	RD_DDB14_6	RD_DDB14_5	RD_DDB14_4	RD_DDB14_3	RD_DDB14_2	RD_DDB14_1	RD_DDB14_0
	17h Parameter		RD_DDB15_7	RD_DDB15_6	RD_DDB15_5	RD_DDB15_4	RD_DDB15_3	RD_DDB15_2	RD_DDB15_1	RD_DDB15_0
	18th Parameter -25th Parameter		x	x	x	x	x	x	x	x
	26h Parameter		1	1	1	1	1	1	1	1

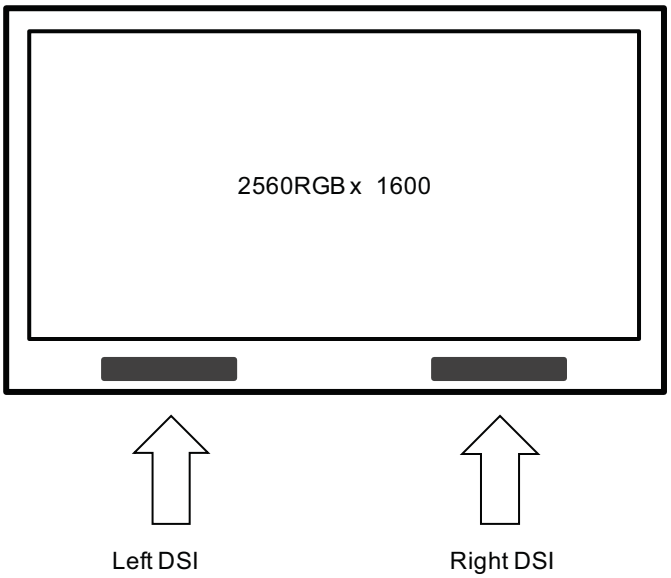
Command Table 3

Address [Hex]	Parameter	Instruction	D7	D6	D5	D4	D3	D2	D1	D0
B0h	1st Parameter	Manufacturer Command Access Protect	0	0	0	0	0	MACP2	MACP1	MACP0
B1h	1st Parameter	Low Power Mode Control	0	0	0	0	0	0	0	DSTB
B3h	1st Parameter	Interface Setting	DM3	DM2	DM1	DM0	V2CRM	1	RM1	RM0
CEh	Dummy parameter	BACK_LIGHT_CONTROL_4	x	x	x	x	x	x	x	X
	1st Parameter		0	1	1	1	1	1	0	1
	2nd Parameter		0	1	0	0	0	0	0	0
	3rd Parameter		0	1	0	0	1	0	0	0
	4th Parameter		0	1	0	1	0	1	1	0
	5th Parameter		0	1	1	0	0	1	1	1
	6th Parameter		0	1	1	1	1	0	0	0
	7th Parameter		1	0	0	0	1	0	0	0
	8th Parameter		1	0	0	1	1	0	0	0
	9th Parameter		1	0	1	0	0	1	1	1
	10th Parameter		1	0	1	1	0	1	0	1
	11th Parameter		1	1	0	0	0	0	1	1
	12th Parameter		1	1	0	1	0	0	0	1
	13h Parameter		1	1	0	1	1	1	1	0
	14th Parameter		1	1	1	0	1	0	0	1
	15th Parameter		1	1	1	1	0	0	1	0
	16th Parameter		1	1	1	1	1	0	1	0
	17h Parameter		1	1	1	1	1	1	1	1
	18th Parameter		PWM_DIV_7	PWM_DIV_6	PWM_DIV_5	PWM_DIV_4	PWM_DIV_3	PWM_DIV_2	PWM_DIV_1	PWM_DIV_0
	19h Parameter		PWM_CYCLE_7	PWM_CYCLE_6	PWM_CYCLE_5	PWM_CYCLE_4	PWM_CYCLE_3	PWM_CYCLE_2	PWM_CYCLE_1	PWM_CYCLE_0

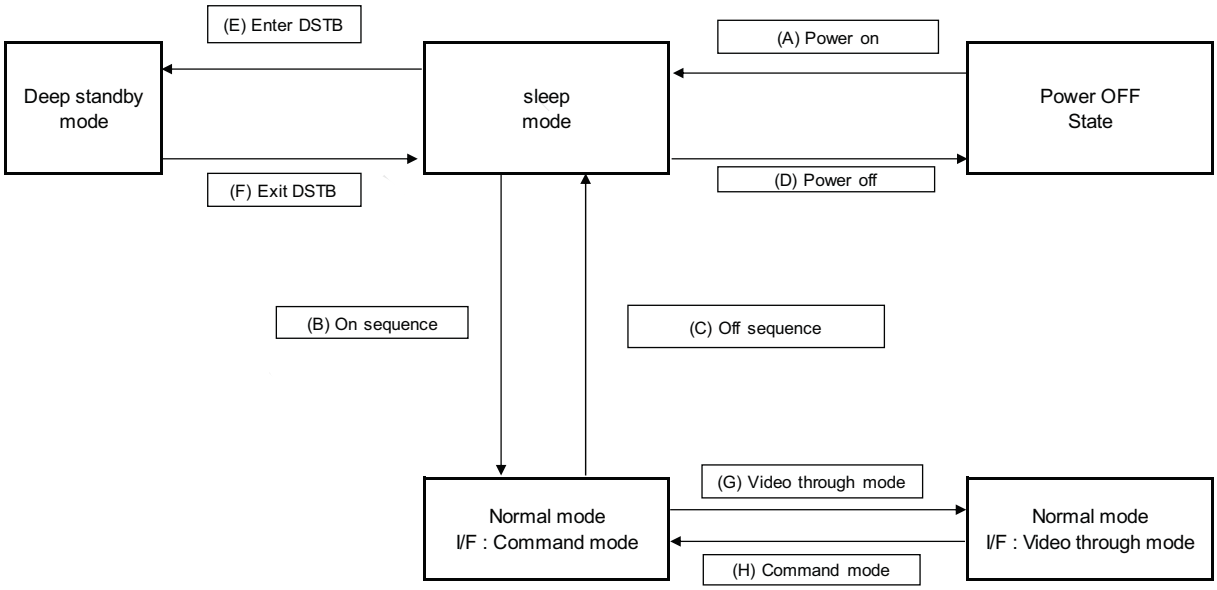
8.5 LCM Control sequence

8.5.1 LCM Circuit configuration

H:2560RGB x V:1600
R69429, 2Chip
w/RAM
Mipi-DSI 4lane x 2port



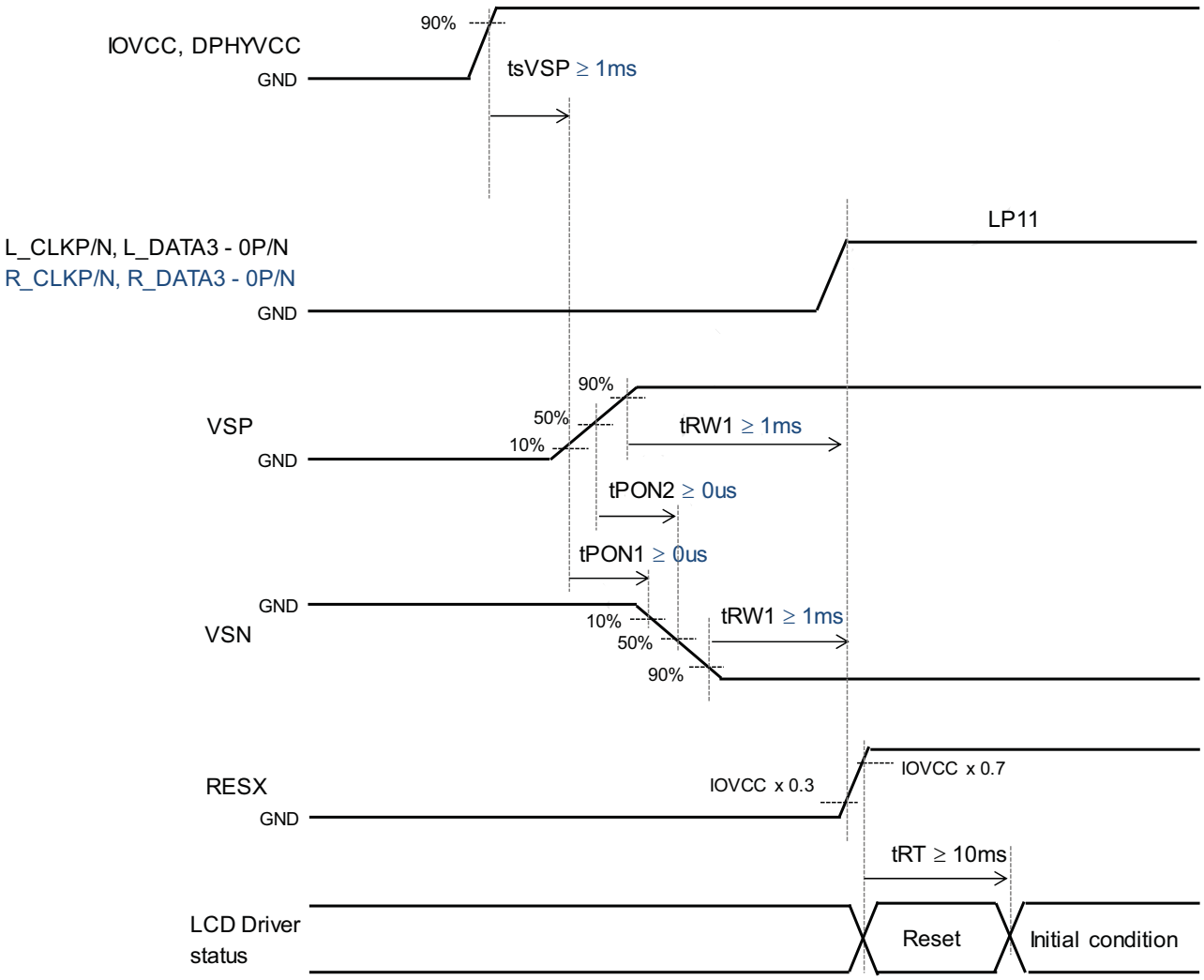
8.5.2 Status flow



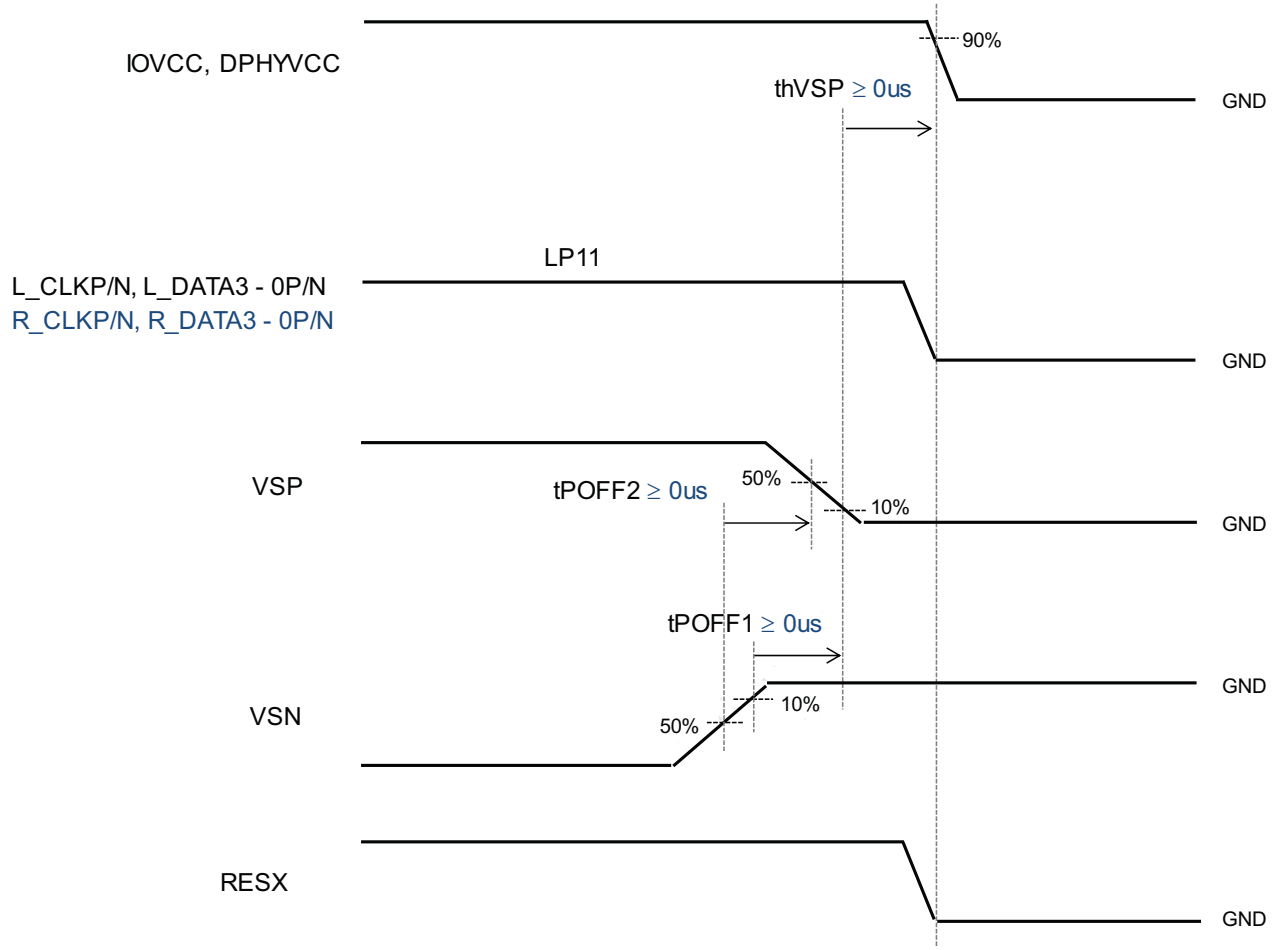
8.5.3 Power supply sequence

Note1) Connect DPHYVCC to IOVCC on Flexible Printed Circuit. DPHYVCC set the same potential as IOVCC.
Note2) Make sure that the following relationship are satisfied :
IOVCC, DPHYVCC ≥ RESET, IOVCC, DPHYVCC ≥ MIPI-DSI signals
Note3) Please set L/R_CLKP/N, L/R_DATA3 - 0P/N to LP11 at the time of reset of power on sequence.

8.5.3.1 Power supply on sequence



8.5.3.2 Power supply off sequence



8.5.4 Power and Display on sequence.

(A) Power on

sequence	DataType (hex)	index (hex)	parameters #	parameters (hex)	L/R	description	comment
POWER OFF STATE							
IOVCC, DPHYVCC on							(*1)Connect DPHYVCC to IOVCC on Flexible Printed Circuit. DPHYVCC set the same potential as IOVCC.
After IOVCC1, DPHYVCC reaches to 90% of setting voltage, wait 1 ms or more.							
VSP,VSN on							
After VSP and VSN reach to 90% of setting voltage, wait 1 ms or more.							
RESX L->H							
wait 10ms or more.							
VSP,VSN off							(*2)Can skip "VSP/VSN off" in case of going to normal mode without staying sleep status.
wait 10ms or more.							
SLEEP MODE							

(B) On sequence

sequence	DataType (hex)	index (hex)	parameters #	parameters (hex)	L/R	description	comment
SLEEP MODE							
⇩							
VSP,VSN on						VSP,VSN on	(*2)
wait 20ms							(*2)
command	05	01	-	-	L/R	soft reset	
wait 5ms							
command	15	3A	1	77	L/R	set pixel format	
command	39	2A	1	00	L/R	set column address	
			2	00			
			3	04			
			4	FF			
command	39	2B	1	00	L/R	set page address	
			2	00			
			3	06			
			4	3F			
command	15	35	1	00	R	set tear on	Recommend monitering TE timing due to the restriction in 2chip system, for details, refer "Restriction on command timing"
command	39	44	1	00	R	set tear scanline	
			2	00			
command	15	51	1	FF	L/R	write_display_brightness	
command	15	53	1	24	L/R	write_control_display	
command	15	51	1	FF	L/R	write_display_brightness	
command	15	53	1	24	L/R	write_control_display	
command	15	55	1	00	L/R	write_adaptive_brightness_control C[1:0] = 0x00 : ACO・CABC Off	Please use Auto Contrast Optimization (ACO) function and Content Adaptive Brightness Control (CABC) function
			1	01	L/R	write_adaptive_brightness_control C[1:0] = 0x01 : ACO On	
			1	02	L/R	write_adaptive_brightness_control C[1:0] = 0x02 : CABC On Max. Backlight reduction ratio : -33% setting	
			1	03	L/R	write_adaptive_brightness_control C[1:0] = 0x03 : CABC On Max. Backlight reduction ratio : -54% setting	
command	05	11	-	-	L/R	exit sleep mode	
wait 120ms							
command	23	B0	1	00	L/R	MCAP (Manufacture Command Access	This command is inputted for change of LEDPWM clock frequency. When using [C[1:0] = 0x00 : ACO・CABC Off] and [C[1:0] = 0x01 : ACO On] , it is not necessary to input this command.
command	29	CE	1	7D	L/R	Back Light Control 4	(1)This command is inputted for change of LEDPWM clock frequency. When using [C[1:0] = 0x00 : ACO・CABC Off] and [C[1:0] = 0x01 : ACO On] , it is not necessary to input this command. (2)Please optimize a LEDPWM clock frequency by PWMDIV [7:0] and PWM_CYCLE[7:0] according to the characteristic of the LED driver used in your company.
			2	40			
			3	48			
			4	56			
			5	67			
			6	78			
			7	88			
			8	98			
			9	A7			
			10	B5			
			11	C3			
			12	D1			
			13	DE			
			14	E9			
			15	F2			
			16	FA			
			17	FF			
			18	04		PWM_DIV[7:0]	
			19	00		PWM_CYCLE[7:0]	
command	23	B0	1	03	L/R	MCAP (Manufacture Command Access Protect) On	This command is inputted for change of LEDPWM clock frequency . When using [C[1:0] = 0x00 : ACO・CABC Off] and [C[1:0] = 0x01 : ACO On] , it is not necessary to input this command.
send image	39	2C/3C			L/R	write memory / write memory continue	
command	05	29	-	-	L/R	set display on	
⇩							
NORMAL MODE, I/F : Command mode							

(1)These CABC setting values are our recommended values.

CABC On -33% : Max. Backlight power reduction rate -33% setting
CABC On -54% : Max. Backlight power reduction rate -54% setting

(2)LEDPWM frequency calculation formula
LEDPWM frequency = fOSC2 / (PWMDIV + 1) / (PWM_CYCLE + 255)
fOSC2 spec. = 26.6MHz(min.) - 28MHz(typ.) - 29.4MHz(max.)

(3)LEDPWM frequency default setting :
Command 0xCE, PWMDIV[7:0]=0x04, PWM_CYCLE[7:0]=0x00
LEDPWM frequency = 28MHz (typ.) / (4+1) / (0+255) = 21.961kHz(typ.)

8.5.5 Power and Display off sequence.

(c) Off sequence

sequence	DataType (hex)	index (hex)	parameters #	parameters (hex)	L/R	description	comment
NORMAL MODE							
↓							
command	05	28	-	-	L/R	set display off	
wait 20ms or more							
command	05	10	-	-	L/R	enter sleep mode	
wait 80ms or more							In Video through mode, please continue the input of Vsync packet, Hsync packet,and DSICLK until Off sequence is completed.
VSP,VSN off							
wait 10ms or more							
↓							
SLEEP MODE							

(D) Power off

sequence	DataType (hex)	index (hex)	parameters #	parameters (hex)	L/R	description	comment
SLEEP MODE							
↓							
RESX H->L							
IOVCC, DPHYVCC off							()
↓							
POWER OFF STATE							

8.5.6 Enter DSTB and Exit DSTB sequence

(E) Enter DSTB

sequence	DataType (hex)	index (hex)	parameters #	(hex)	L/R	description	comment
SLEEP MODE							
↓							
command	23	B0	1	00	L/R	MCAP	
command	23	B1	1	01	L/R	DSTB=1	
↓							
DSTB MODE							

(F) Exit DSTB

sequence	DataType (hex)	index (hex)	parameters #	(hex)	L/R	description	comment
DSTB MODE							
↓							
RESX H -> L							
wait 10ms or more							
VSP,VSN on							
After VSP and VSN reach to 90% of setting voltage, wait 1 ms or more.							
RESX L->H							
wait 10ms or more							
VSP,VSN off							(*1)Can skip "VSP/VSN off" in case of going to normal mode without staying sleep status.
wait 10ms or more.							
↓							
SLEEP MODE							

8.5.7 Video through mode

(G) Video through mode

sequence	DataType (hex)	index (hex)	parameters #	(hex)	L/R	description	comment
NORMAL MODE, I/F : Command mode							
⇓							
Transferring video mode packets Note) it is necessary to input DSICLK / VSYNC packet / HSYNC packet, before setting B3h register.							
Triggered by detecting TE="High" Note) Command input in blank period							
command	23	B0	1	00	L/R	MCAP	
command	29	B3	1	1C	L/R	Interface setting	Video through mode setting
command	23	B0	1	03	L/R	MCAP	
Transferring video mode packets (> 1 frame)							
⇓							
NORMAL MODE, I/F : Video through mode							

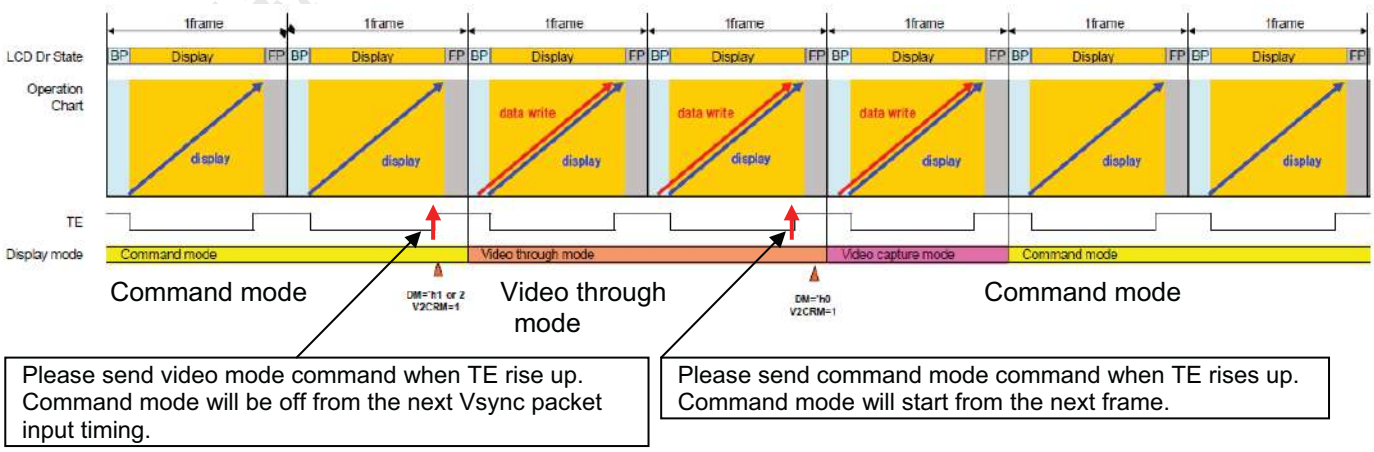
8.5.8 Command mode

(H) Command mode

sequence	DataType (hex)	index (hex)	parameters #	(hex)	L/R	description	comment
NORMAL MODE, I/F : Video through mode							
⇓							
Triggered by detecting TE="High" Note) Command input in blank period							
command	23	B0	1	00	L/R	MCAP	
command	29	B3	1	0C	L/R	Interface setting	Video capture mode setting
command	23	B0	1	03	L/R	MCAP	
Transferring video mode packets (> 1 frame) Note) it is necessary to input DSICLK / VSYNC packet / HSYNC packet, until 1frame period after setting B3h regisiter.							
⇓							
NORMAL MODE, I/F : Command mode							
Transferring command mode packets							
send image	39	2C/3C			L/R	write memory / write memory continue	

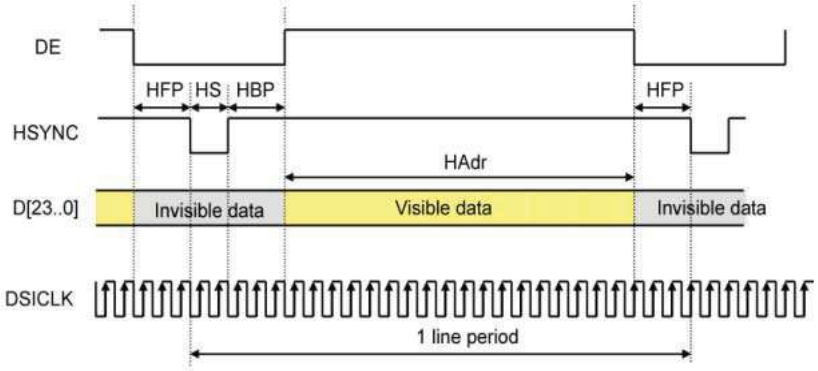
Display Interface switching Operation Chart

・Command Mode　　Video Through Mode



8.5.9 Timing restrictions in Video Mode

The blanking period is specified for the pixel data transfer to the two chips in Video Mode.
Set 45 ByteClock or less in the time that the pixel data transfer to the salve chip precedes and is behind the pixel data transfer to the master chip.



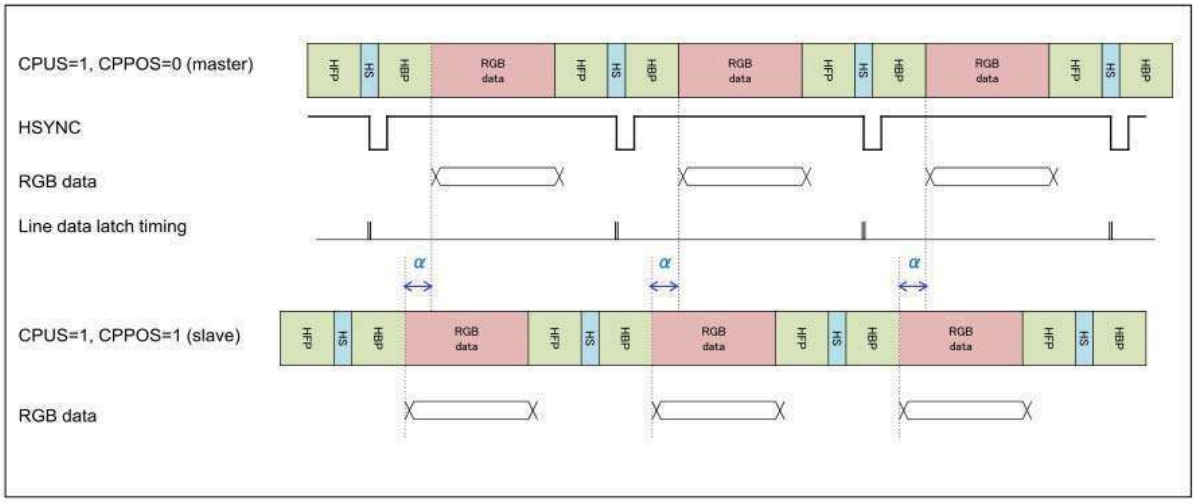
Item	Symbol	Condition	Unit	Min.
Horizontal front porch	HFP		ByteClock	4lanes:100+β
Horizontal data start point	-	HS+HBP	ByteClock	45+α

αβ ≤ 45 ByteClock

α: Time the pixel data is transferred to the slave chip (CPUS=1, CPPOS=1) precedes time the pixel data is transferred to the master chip (CPUS=1, CPPOS=0)
β: Time the pixel data is transferred to the slave chip (CPUS=1, CPPOS=1) is behind time the pixel data is transferred to the master chip (CPUS=1, CPPOS=0)
1 ByteClock = 4 DSI Clock, 1ByteClock=4/3PixelClock (4 lanes)

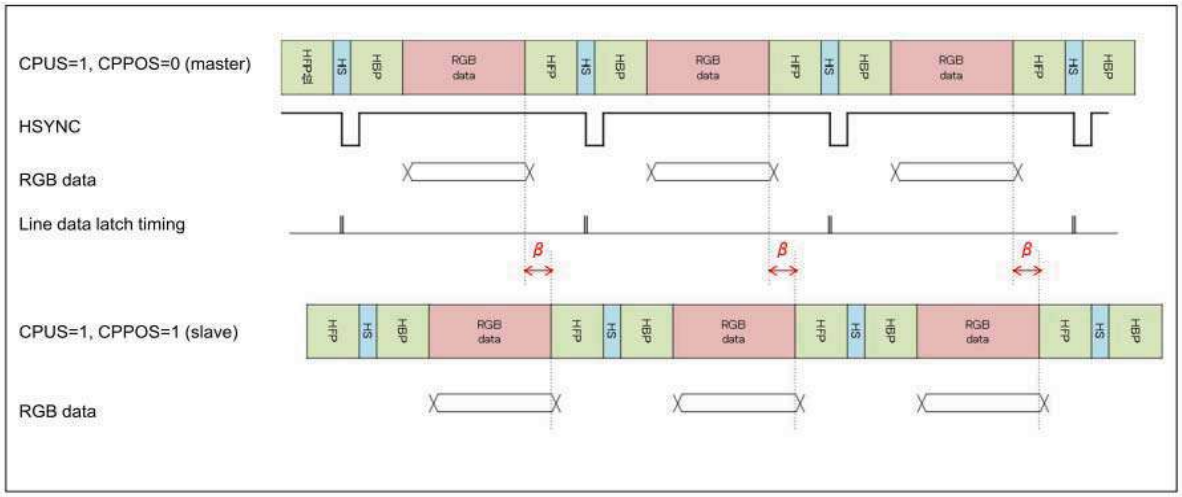
1) Video Access (Pixel Data Transfer to Slave Chip Precedes Pixel Data Transfer To Master Chip)

Add the precursor time α to the HS+HBP (horizontal data start point) setting.



2) Video Access (Pixel Data Transfer to Slave Chip is behind Pixel Data Transfer to Master Chip)

Add the delay time β to the HFP (Horizontal front porch) setting.

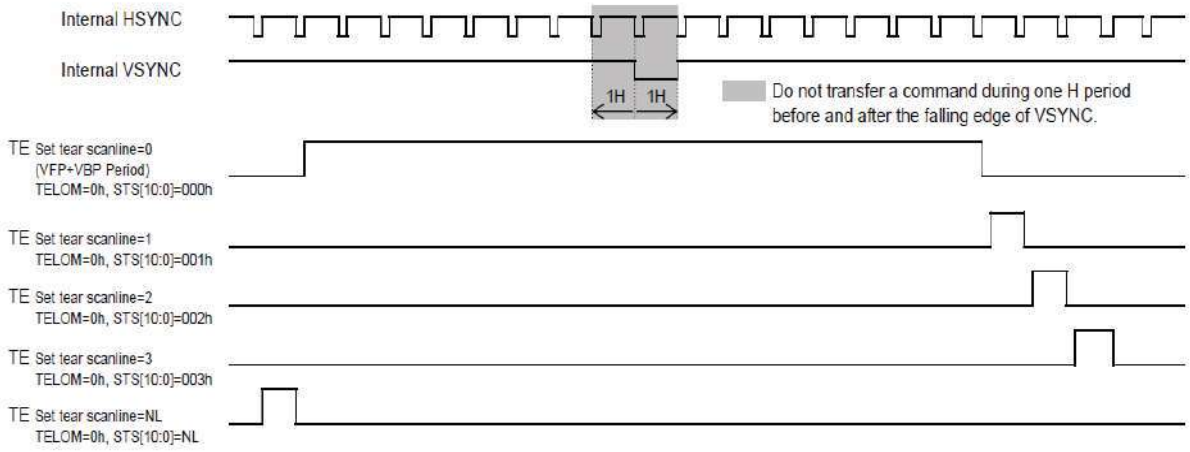


8.5.10 Restriction on command timing (Case of command mode access)

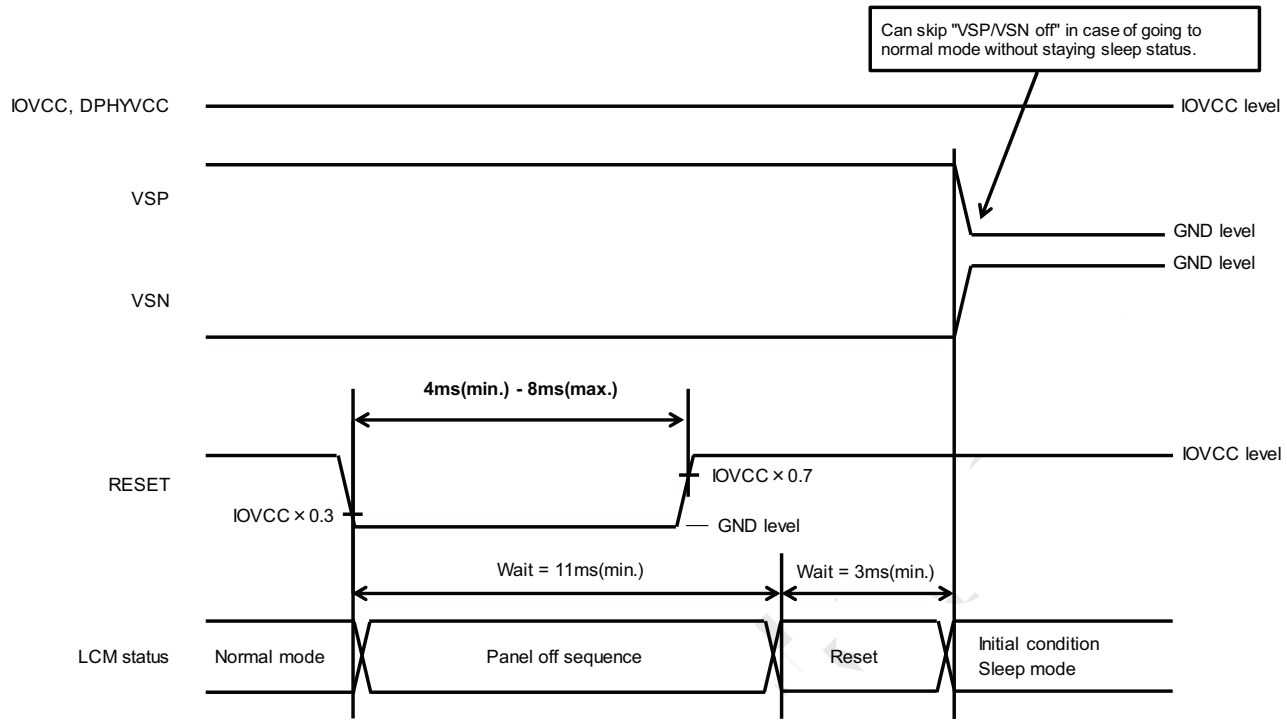
Timing Restrictions on the transfer command of Two-Chip Structure

When two chips are used (for point-to-point system), the execution of a command in a first chip may be one frame period behind that of a command in a second chip according to the timing that the host transfer a command. Therefore, the transfer command has the following timing restrictions.

2. Command Access



8.5.11 Reset timing spec. during display



8.5.12 Interface setting

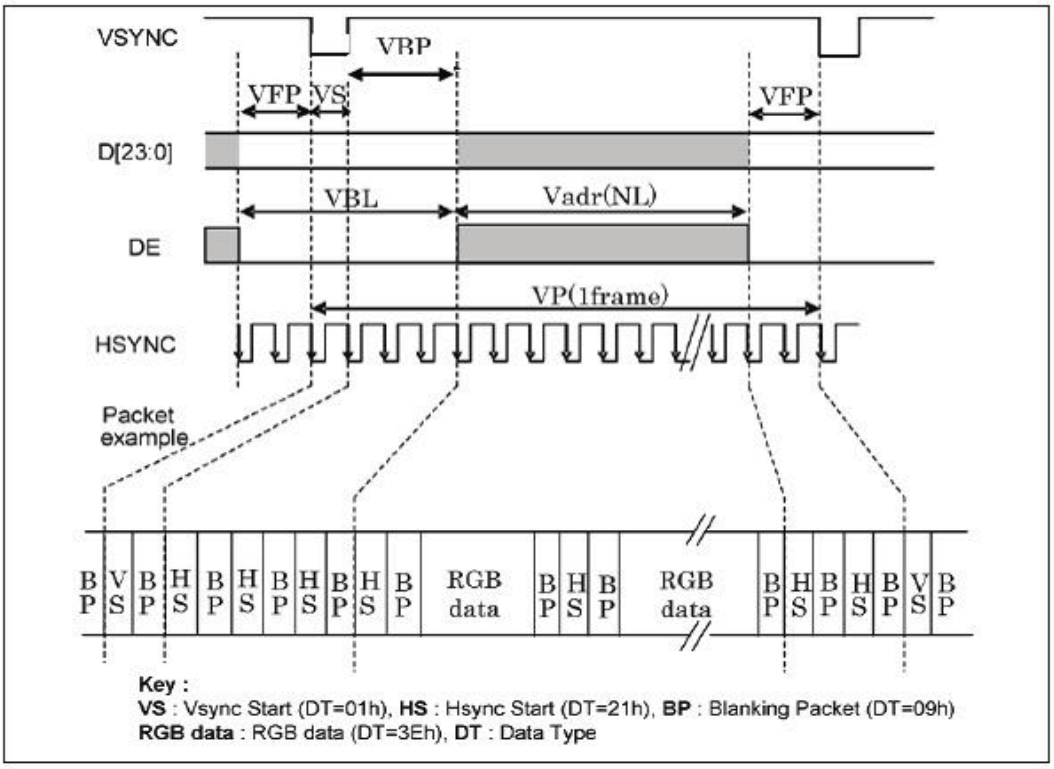
MIPI-DSI Video mode timing chart

	Min.	Typ.	Max.	Unit
# of lane	-	4	-	lane
HS+HBP	45	(69)	-	ByteClock
Hadr	-	960	-	ByteClock
	-	1280	-	pixel
HFP	100	(123)	-	ByteClock
Hp	-	(1152)	-	ByteClock
	-	10.29	-	us
VS	-	4	-	Line
VBP	-	4	-	Line
Vadr	-	1600	-	Line
VFP	-	12	-	Line
Vp	-	1620	-	Line

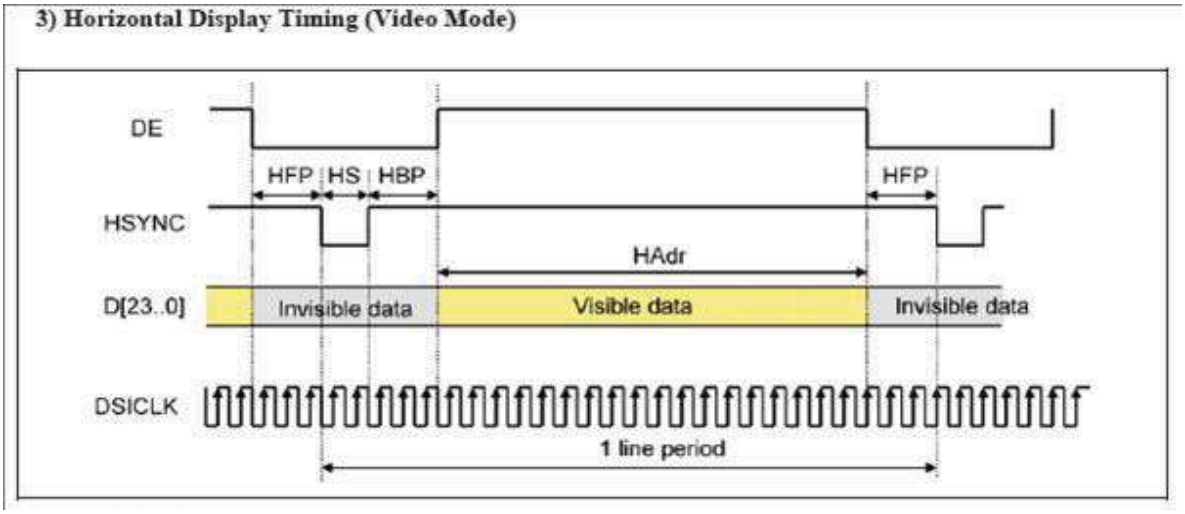
	Min.	Typ.	Max.	Unit
Vsync	-	60.0	-	Hz
Hsync	-	97.2	-	kHz
DSI Bit rate	-	896	1000	Mbps/lane
fDSICLK	-	448	-	MHz
fByteClock	-	112	-	MHz

Note: Case of 24bpp(DT=3Eh) 18bpp(DT=2Eh)
Same timing for each DSI port

2) Vertical Display Timing (Video Mode)



3) Horizontal Display Timing (Video Mode)



8.6 MIPI-DSI Characteristics

8.6.1 DC Characteristics

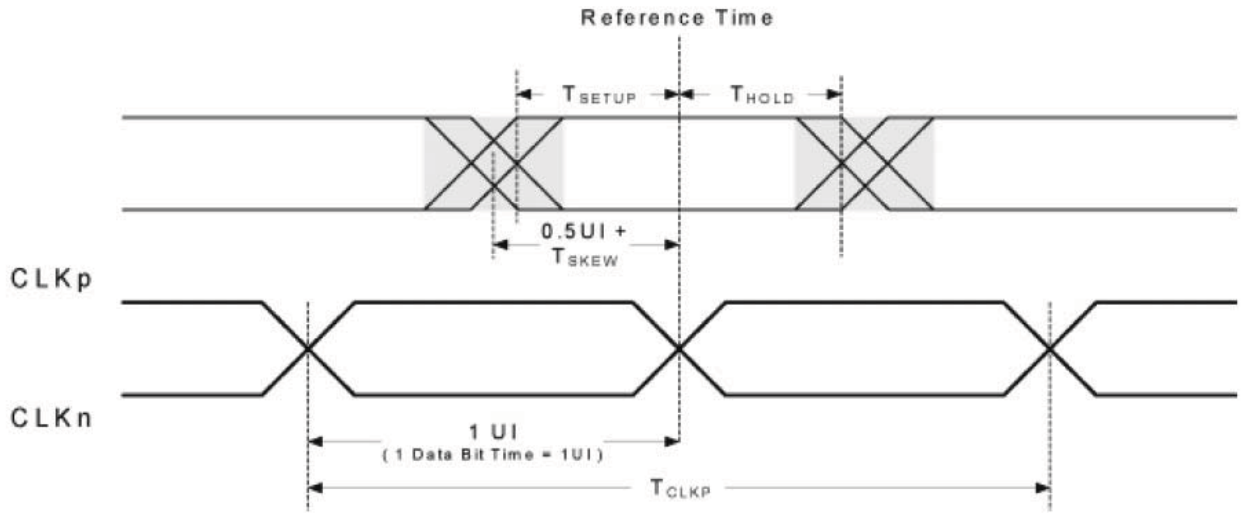
Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV		-	-	70	3
	Differential input low threshold	VIDTL	mV		-70	-	-	3
	Single-ended input low voltage	VILHS	mV		-40	-	-	
	Single-ended input high voltage	VIHHS	mV		-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV		70	-	330	1
	Differential input impedance	ZID	Ω		-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV		-50	-	550	
	Logic 1 input voltage	VIH	mV		880	-	1350	
	I/O leakage current	ILEAK	μA	Vin= -50mV – 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV		-50	-	50	
	Thevenin output high level	VOH	V		1.1	1.2	1.3	
	Output impedance of LP Transmitter	ZOLP	Ω		110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV		-	-	200	
	Logic 1 contention threshold	VIHCD	mV		450	-	-	

Notes 1) VCMRX(DC)=(VDP+VDN)/2
2) Excluding COG resistance (contact resistance and ITO wiring resistance).
3) Minimum 110mV/-110mV HS differential swing is required for display data transfer.

8.6.2 MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	100	-	500	4
DSICLK Cycle time	tCLKP	ns	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	0.15	-	-	6
		ns	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	0.15	-	-	6
		ns	0.15	-	-	5,6

Notes 4) When fDSICLK < 125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
5) Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
6) tSETUP/tHOLD Time are measured without HS-TX Jitter.



8.6.3 MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40 ns+4*UI	-	85 ns+6*UI	ns	
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145 ns+10*UI	-	-	ns	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	Max (n*8*UI, 60 ns+n*4*UI)	-	-	ns	1,2
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPTX}$				
$T_{TA-SURE}$	Time-out before new TX side starts driving	$1*T_{LPTX}$	-	$2*T_{LPTX}$		
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPTX}$				
T_{LPX}	Length of any Low-Power state period	50	-	-	ns	
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$ / T between Master and Slave side	2/3	-	3/2		
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60 ns+52UI	-	-	ns	3
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	T + time for lead HS-0 drive period before starting Clock	300	-	-	ns	
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI	
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns	
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of an HS transmission burst	60	-	-	ns	
T_{EOT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105 ns+n*12*UI		2
T_{LPTX1}	Length of Low-Power TX period in case of using DSI clock	-	48	-	UI	4
T_{LPTX2}	Length of Low-Power TX period in case of using internal OSC clock	-	1/fosc1	-	ns	

Notes
1) If a>b then max(a,b)=a, otherwise max(a,b)=b
2) Where n=1 for Forward-direction HS mode
3) The R69429 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R69429 can work without the remained process if tCLK-POST is more than 256 UI.
4) The R69429 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disable. Here,"fosc1" is the frequency of oscillator clock, typical 28MHz.

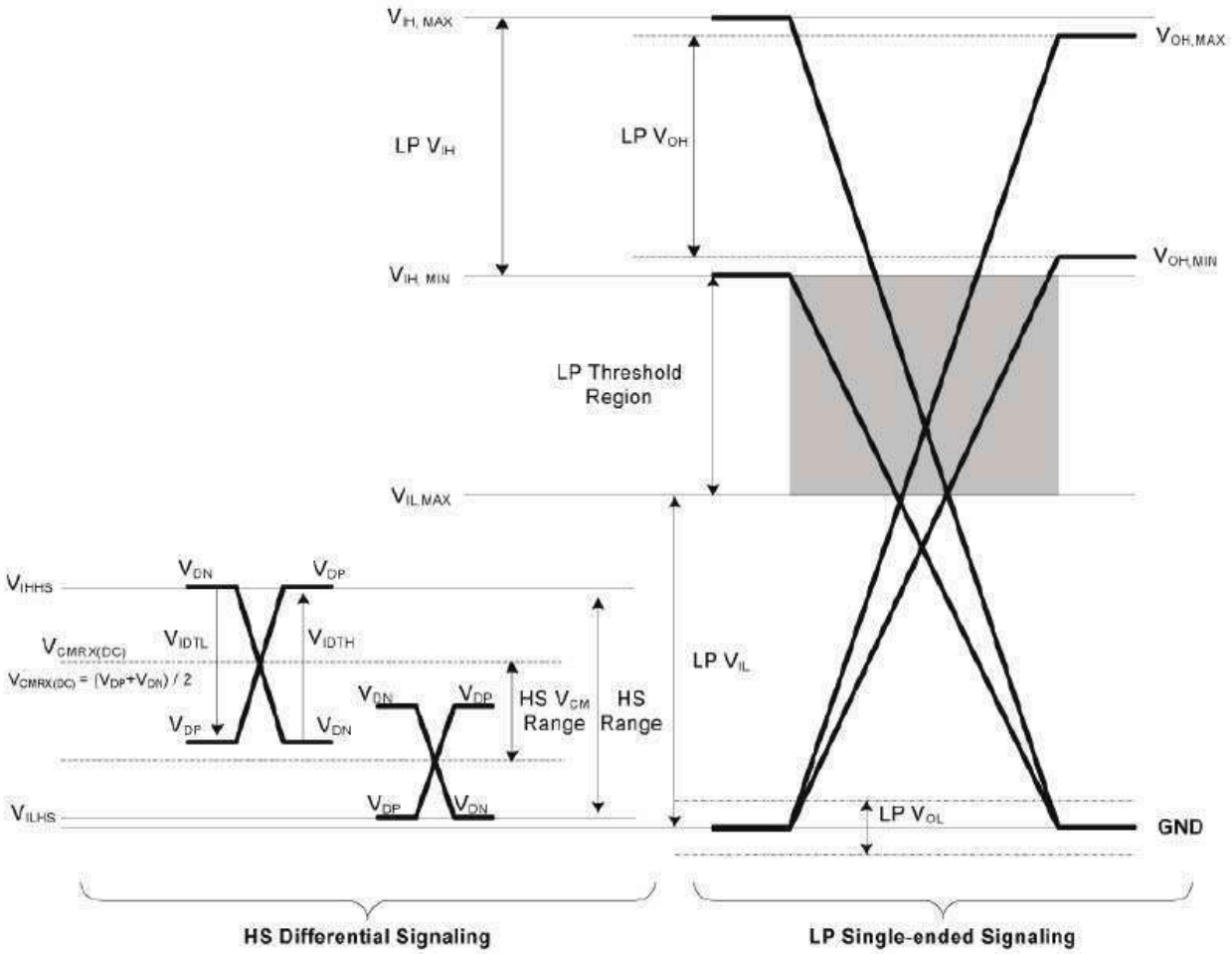
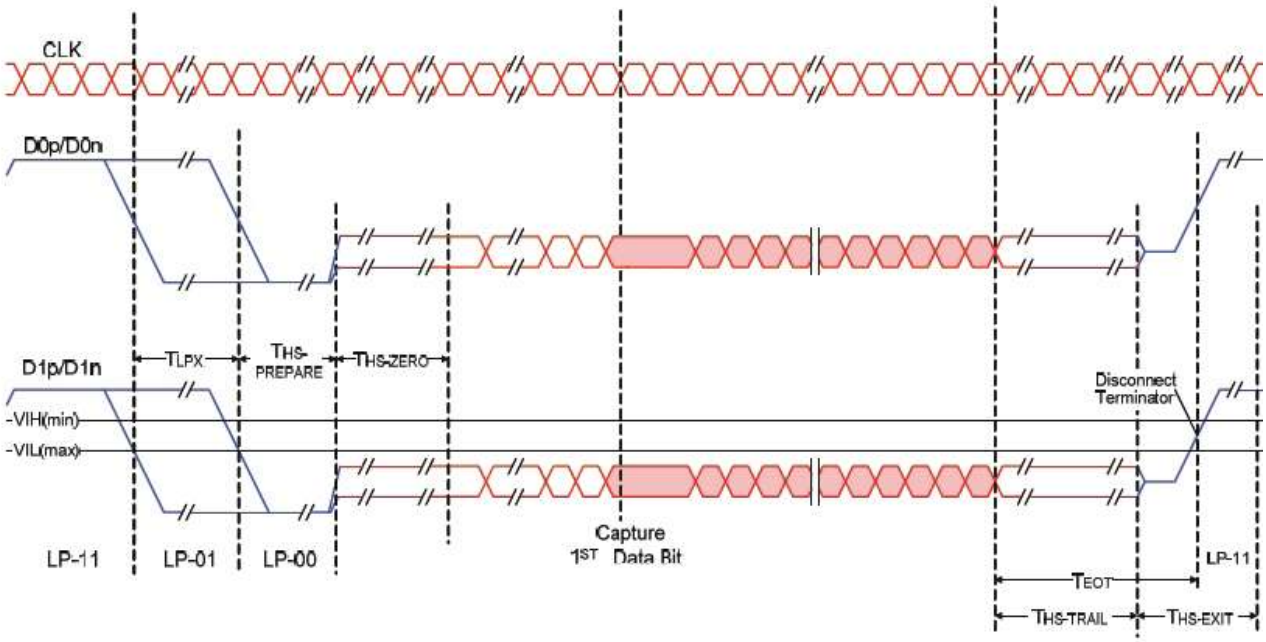


Figure.DSI LP Mode



Note: THS-SYNC: Proper match found for Sync sequence in HS stream,the following bits are payload data.

Figure. HS Data Transmission in Bursts

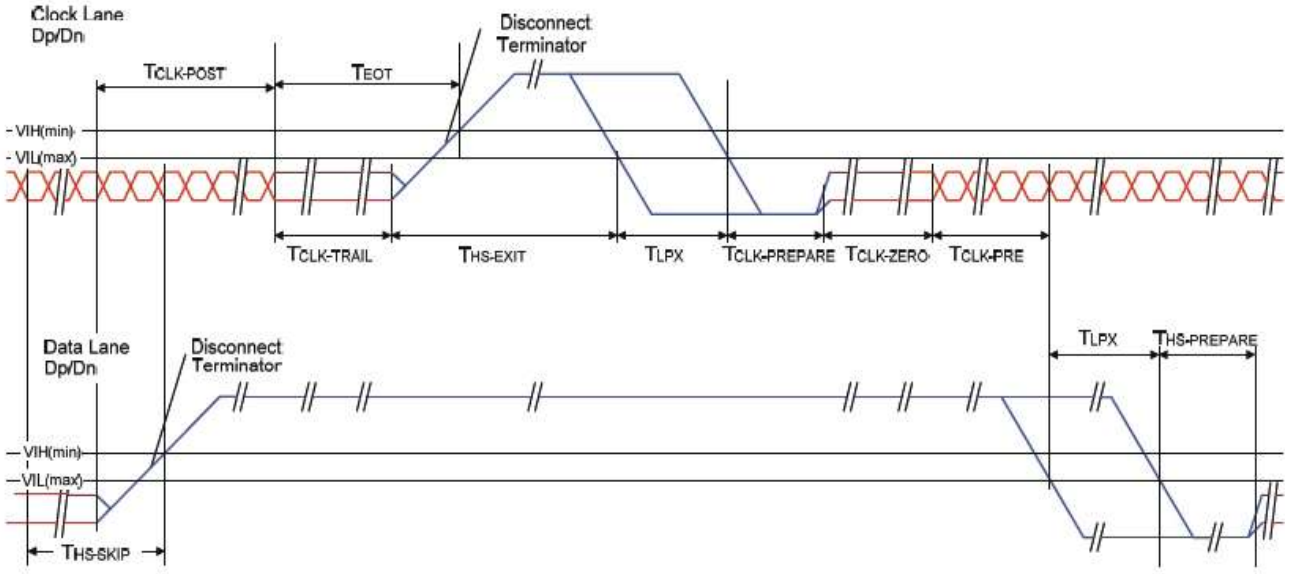
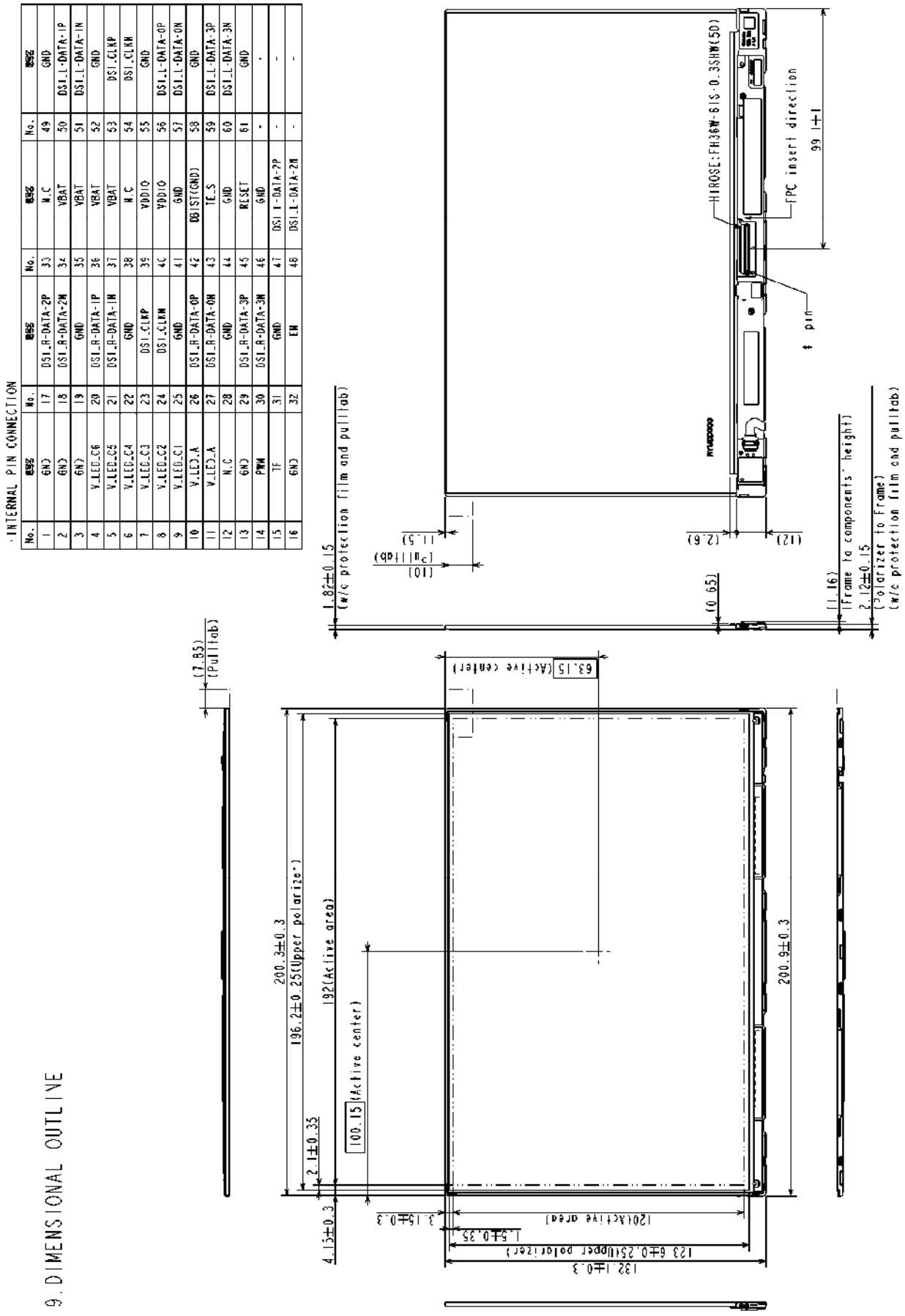


Figure. Switching the Clock Lane between Clock Transmission

9. Dimensional Outline

9.1 Outline Drawing



No.	BSE	No.	BSE	No.	BSE
1	GND	17	DSI_R-DATA-2P	33	N.C	49	GND
2	GND	18	DSI_R-DATA-2M	34	VBAT	50	DSI_L-DATA-1P
3	GND	19	GND	35	VBAT	51	DSI_L-DATA-1N
4	V_LED_C6	20	DSI_R-DATA-1P	36	VBAT	52	GND
5	V_LED_C5	21	DSI_R-DATA-1M	37	VBAT	53	DSI_CLKP
6	V_LED_C4	22	GND	38	N.C	54	DSI_CLKN
7	V_LED_C3	23	DSI_CLKP	39	VDDIO	55	GND
8	V_LED_C2	24	DSI_CLKM	40	VDDIO	56	DSI_L-DATA-0P
9	V_LED_C1	25	GND	41	GND	57	DSI_L-DATA-0N
10	V_LED_A	26	DSI_R-DATA-0P	42	DSISTC(GND)	58	GND
11	V_LED_A	27	DSI_R-DATA-0N	43	TE_S	59	DSI_L-DATA-3P
12	N.C	28	GND	44	GND	60	DSI_L-DATA-3N
13	GND	29	DSI_R-DATA-3P	45	RESET	61	GND
14	PWM	30	DSI_R-DATA-3M	46	GND	-	-
15	TF	31	GND	47	DSI_L-DATA-2P	-	-
16	GND	32	EN	48	DSI_L-DATA-2M	-	-

10. INSPECTION

10.1 DISPLAY APPEARANCE STANDARDS

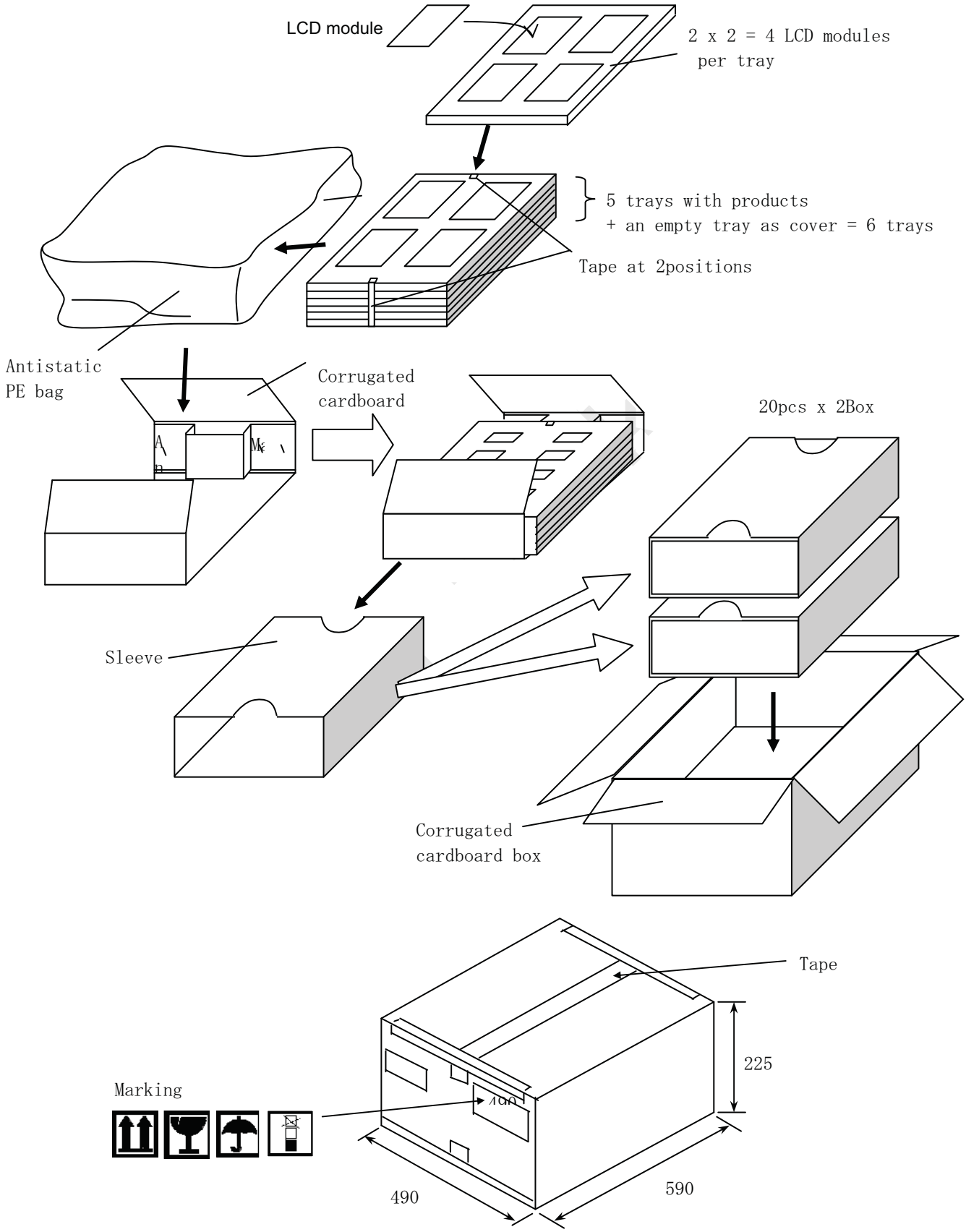
<Application scope>
The application scope is limited to the viewing area.
The product should be judged non-defective if all defects are outside of the active area and do not interfere with product quality or the assembly process.

If any item is defined with a boundary sample, the boundary sample takes precedence.

No.	ITEM	CRITERION
1	Abnormal display	Must not be abnormal function such as not function or not to get normal pattern for input signal, etc.
2	Line defect (Open, Short)	No line defect
3	Dot defect (Dot failure)	ignored
4	Dot type defect	ignored
5	Line type defect (Black/ White)	ignored
6	Mura	ignored
7	Chipping of the glass	ignored

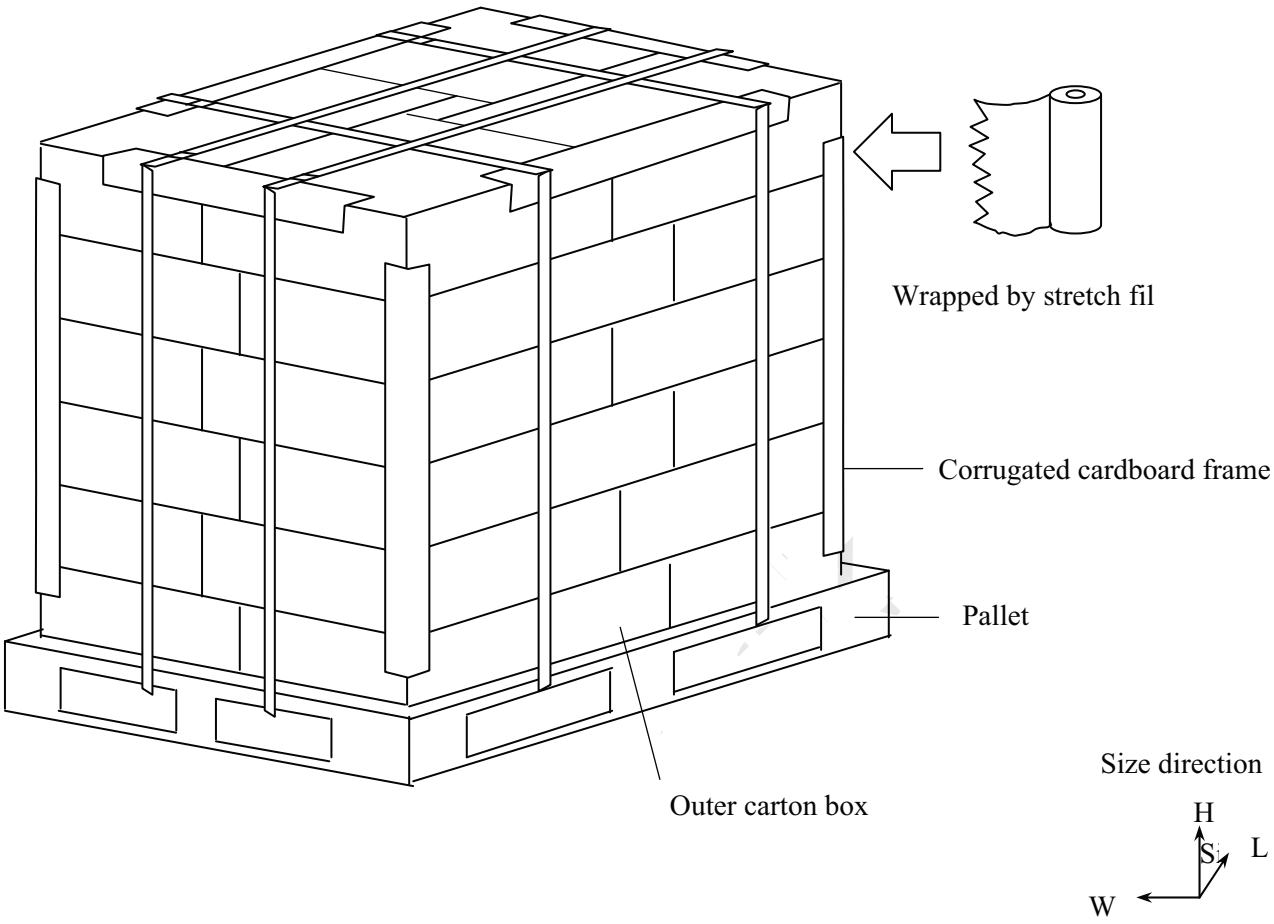
11. Packing Specification

11.1 Box style



Size (L,H,W)	590 x 490 x 225 mm
Quantity	1 to 40 pcs

11.2 Pallet style



Weight (Gross)	Approx. 242 kg
Size (L,W,H)	Approx, (1200) x (1100) x (1460) mm
Quantity	40 to 960 pcs