MODEL NO. : TM080VDSP03-00

ISSUED DATE: 2015-8-7

VERSION : Ver 1.2

■ **Preliminary Specification**
☐ **Final Product Specification**

Customer :

Approved by	Notes

TIANMA Confirmed :

Prepared by	Checked by	Approved by

This technical specification is subjected to change without notice

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2015-4-14	Preliminary Specification Release	RenCun Wu
1.1	2015-4-17	Page 7：Update Operating an Storage Temperature Page 8：Correct LED Circuit Description Page 22：Update the Reliability Test Condition	RenCun Wu
1.2	2015-8-7	Page 7：Update Backlight Forward Current Page 8：Correct LED Circuit Description Page 9：Update Power Consumption Page 18：Update Optical Characteristics	RenCun Wu

1 Features

The TM080VDSP03-00 is a 8.0 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 8.0 inch TFT-LCD panel, a driver circuit, FPC and a backlight unit. RAMless.

This module is display terminals for Tablet PC.

This module follows *RoHS*.

2 General Specifications

Feature		Spec
Display Spec.	Size	8.0 inch
	Resolution	1200 RGB (H)×1920(V)
	Interface	MIPI 31 Pin
	Color Depth	16.7M
	Technology Type	a-si TFT
	Pixel Pitch (mm)	0.0897 *0.0897mm
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	Normally Black
	Surface Treatment(Up Polarizer)	HC
	Viewing Direction	All
Mechanical Characteristics	LCM (W x H x D) (mm)	114.58×184.09×2.05
	Active Area(mm)	107.64×172.224
	With/Without TSP	Without TP
	Weight (g)	TBD
	LED Numbers	21 LEDs (7 Serial 3 Parallel)
Electronic	Driver IC	NT51021

3 Input/Output Terminals

3.1 TFT LCD Panel

No	Symbol	I/O	Description	Comment
1	GND	P	Ground	
2	D3N	I/O	MIPI DSI 3 lane(-)	
3	D3P	I/O	MIPI DSI 3 lane(+)	
4	GND	P	Ground	
5	D2N	I/O	MIPI DSI 2 lane(-)	
6	D2P	I/O	MIPI DSI 2 lane(+)	
7	GND	P	Ground	
8	CLKN	I/O	MIPI DSI CLK(-)	
9	CLKP	I/O	MIPI DSI CLK(+)	
10	GND	P	Ground	
11	D1N	I/O	MIPI DSI 1 lane(-)	
12	D1P	I/O	MIPI DSI 1 lane(+)	
13	GND	P	Ground	
14	D0N	I/O	MIPI DSI 0 lane(-)	
15	D0P	I/O	MIPI DSI 0 lane(+)	
16	GND	P	Ground	
17	RESET	I	Reset Pin(LEVEL：3.3V)	
18	LED_PWM	O	PWM signal output.	
19	GND	P	Ground	
20	ID	O	Ground	
21	SCL_PWR	I	I2C Serial communication clock input.	
22	SDA_PWR	I/O	I2C Serial communication clock input/output.	
23	HSYNC	O	Sync signal for touch panel.	
24	VCI	P	Power Voltage for digital circuit	
25	VCI	P	Power Voltage for digital circuit	
26	LED3	P	LED Cathode	

27	LED2	P	LED Cathode	
28	LED1	P	LED Cathode	
29	NC(MTP)	-	Power supply for MTP circuit, TIANMA only	
30	VLED	P	LED Anode	
31	VLED	P	LED Anode	

Note1: I/O definition: I-----Input O---Output P----Power/Ground

4 Absolute Maximum Ratings

4.1 Driving TFT LCD Panel

AGND=GND=0V, Ta = 25℃

Item	Symbol	Min	Max	Unit	Remark
Power Voltage	VDD	-0.3	5.0	V	
	AVDD	-0.3	11	V	
	VGH	-0.3	32	V	
	VGL	-16.0	0.3	V	
Backlight Forward Current	I_{LED}	–	25	mA	For each LED
Operating Temperature	T_{OPR}	-10	60	℃	
Storage Temperature	T_{STG}	-20	70	℃	

5 Electrical Characteristics

5.1 Driving TFT LCD Panel

AGND=GND=0V, Ta = 25℃

Item	Symbol	MIN	TYP	MAX	Unit
Digital Supply Voltage	VCI	3.0	3.3	3.6	V
Analog Supply Voltage	AVDD	7	-	10	V
Gate On Voltage	VGH	15	18	26	V
Gate Off Voltage	VGL	-11.5	-7	-4	V
OTP supply Voltage	VPP_MTP	7.4	7.5	7.6	V
Common Electrode Driving Signal	VCOM	--	--	--	V
Pixel CLK	--	--	990	--	MHz
Refresh Rate	--	--	60	--	Hz

5.2 Driving Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	63	-	mA	21 LEDs (7 LED Serial, 3 LED Parallel)
Forward Voltage	V_F	-	22.4	-	V	

Note1: The LED driving condition is defined for each LED module (7 LED Serial, 3 LED Parallel).For each LED: I_F (1/3) =21mA, V_F (1/7) =3.2V.

Note2: Under LCM operating, the stable forward current should be inputted. And forward voltage is for reference only.

Note3: I_F is defined for one channel LED. Optical performance should be evaluated at Ta=25℃ only If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

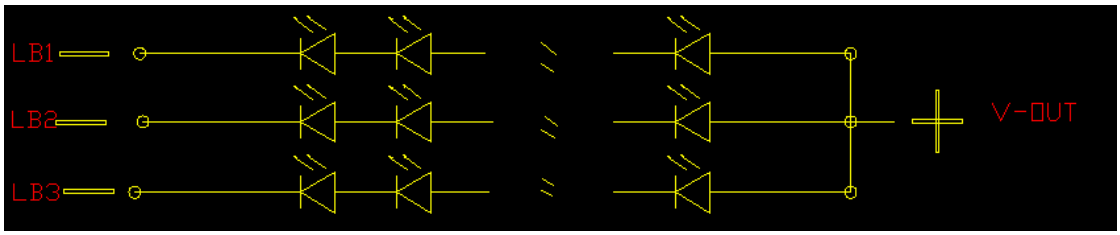


Figure 5.2 LED driver circuit

5.3 Power Consumption

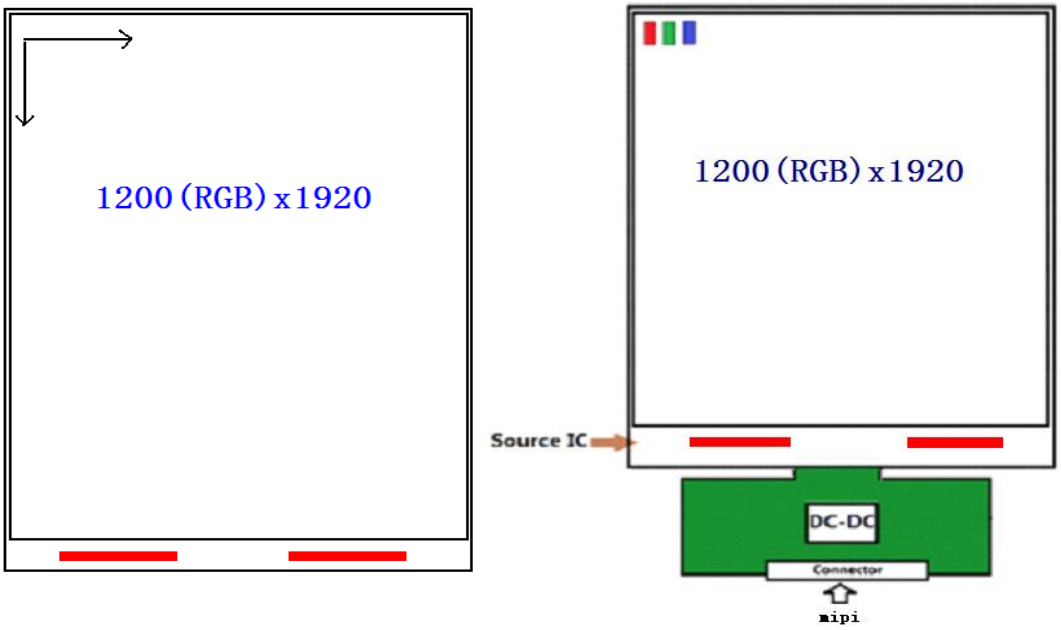
AGND=GND=0V, Ta = 25℃

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Digital Supply Current	I_{VDD}	VCI=3.3 V	-	150	-	mA	White pattern
Power Consumption	Panel & Gamma	-	-	495	-	mW	
	Backlight		-	1411.2	-	mW	
	Total		-	1.91	-	W	

Figure 5.3 Power Consumption

5.4 Block Diagram

LCD module diagram



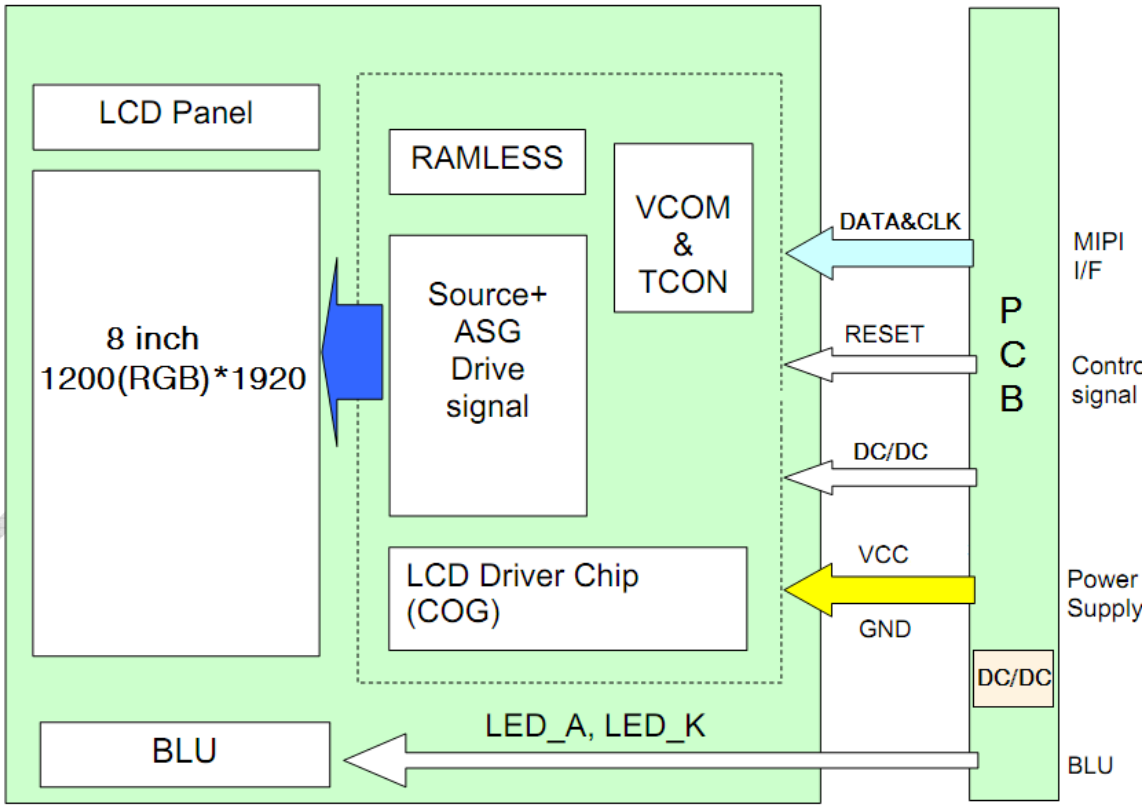


Figure 5.4 LCD module diagram

6 INTERFACE TIMMING

6.1 MIPI Interface DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
MIPI digital operation current	I_{VCCIF}	-	TBD	TBD	mA	VCC=VCC_IF=1.5V, Data Rate=500Mbps, Input pattern: 55h→AAh→55h→AAh
MIPI digital stand-by current	$I_{VCCIFST}$	-	200	-	uA	VCC_IF input current. All input signal are stopped.
MIPI Characteristics for High Speed Receiver						
Single-endedl input low voltage	V_{ILHS}	-40	-	-	mV	
Single-endedl input high voltage	V_{IHHS}	-	-	460	mV	
Common-mode voltage	V_{CMRXDC}	155	-	330	mV	
Differential input impedance	Z_{ID}	80	100	125	ohm	
Differential input high threshold	V_{IDTH}	-	-	70	mV	
Differential input low threshold	V_{IDTL}	70	-	-	mV	
MIPI Characteristics for Low Power Mode						
Pad signal voltage range	V_I	-50	-	1350	mV	
Ground shift	V_{GNDSH}	-50	-	50	mV	
Output low level	V_{OL}	-150	-	150	mV	
Output high level	V_{OH}	1.1	1.2	1.3	V	

Table 6.1 MIPI Interface DC Characteristics

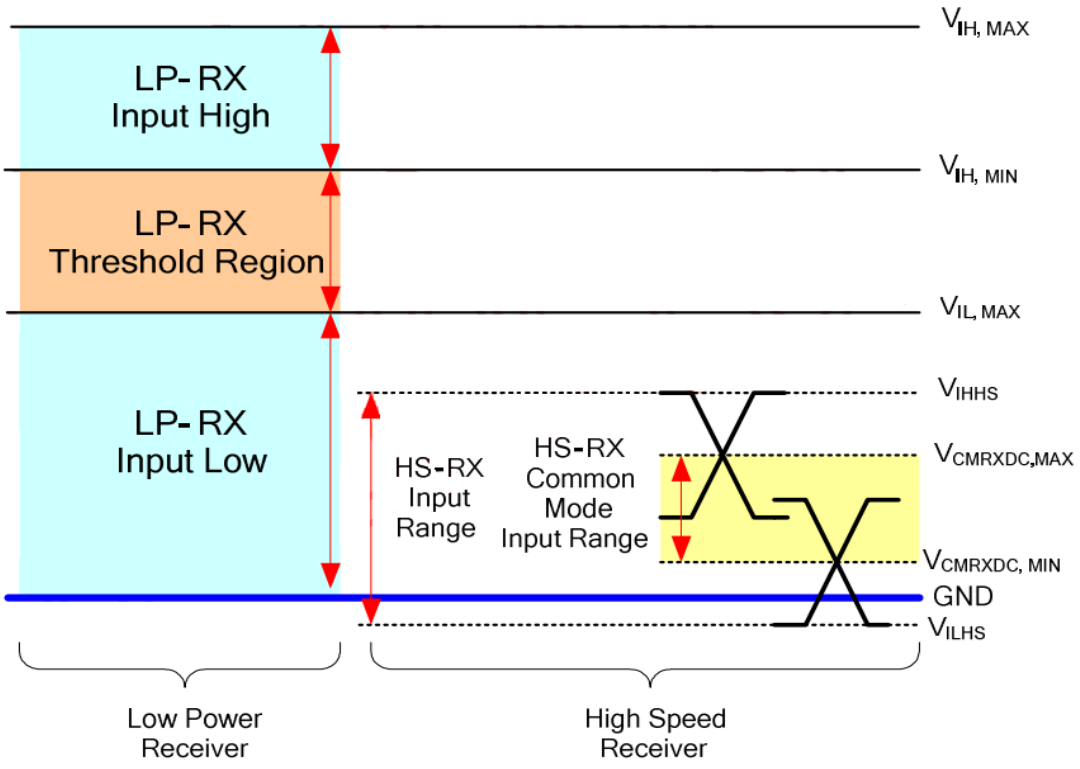


Figure 6.1 MIPI DC Diagram

6.2 MIPI Interface AC Electrical Characteristics

6.2.1 Input AC Electrical

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD power source slew time	T_{POR}	-	-	20	ms	From 0V to 90% VDD
GRB active pulse width	T_{GRB}	1	-	-	ms	VDD = 3.3V
VDD resettle time	T_{RES}	1	-	-	s	

Table 6.2 VDD/GRB AC Characteristics

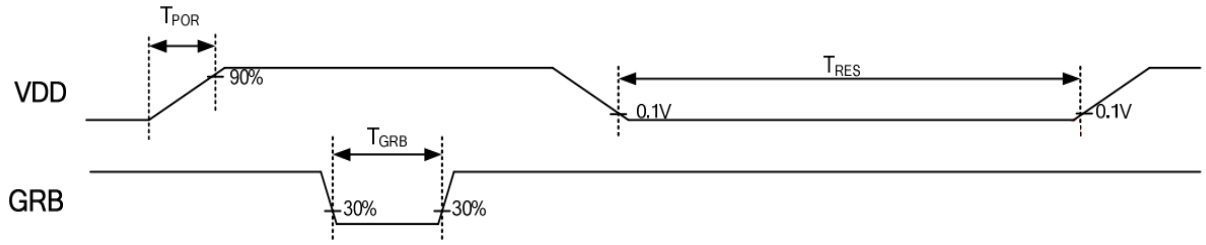


Figure 6.2.1 VDD/GRB timing

6.2.2 LP Transmission

Parameter	Symbol	Min	Typ	Max	Units
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	25	ns
Pulse width of the LP exclusive-OR clock	$T_{LP\text{-}PULSE\text{-}TX}$	50	-	-	ns
Period of the LP exclusive-OR clock	$T_{LP\text{-}PER\text{-}TX}$	100	-	-	ns

Table 5.3 LP Transmission AC Characteristics

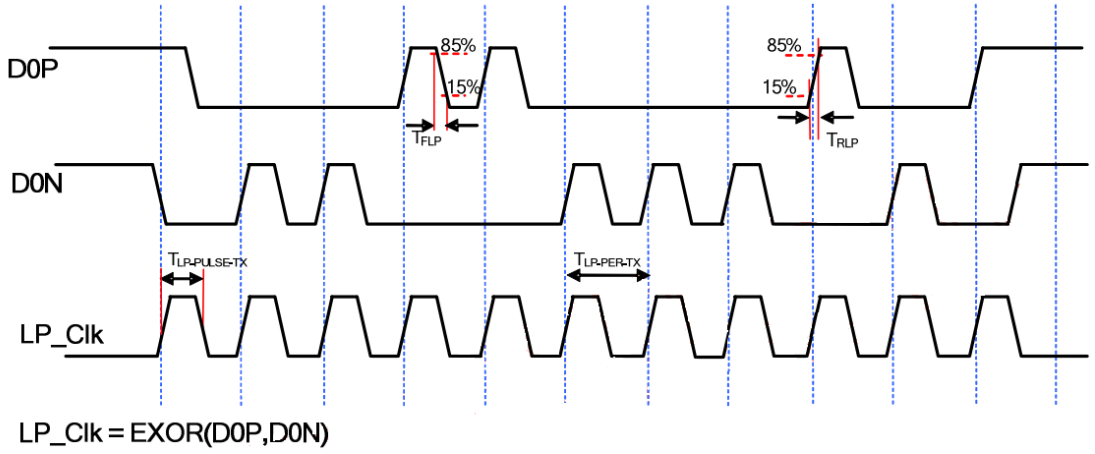


Figure 6.2.2 LP Transmitter Timing Definitions

6.2.3 Hign Speed Transmission

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	1.0	-	12.5	ns
Data to Clock Setup Time	T_{SETUP}	0.3	-	-	UI_{INST}
Data to Clock Hold Time	T_{HOLD}	0.3	-	-	UI_{INST}

Table 6.2.3 Data-Clock Timing Specifications

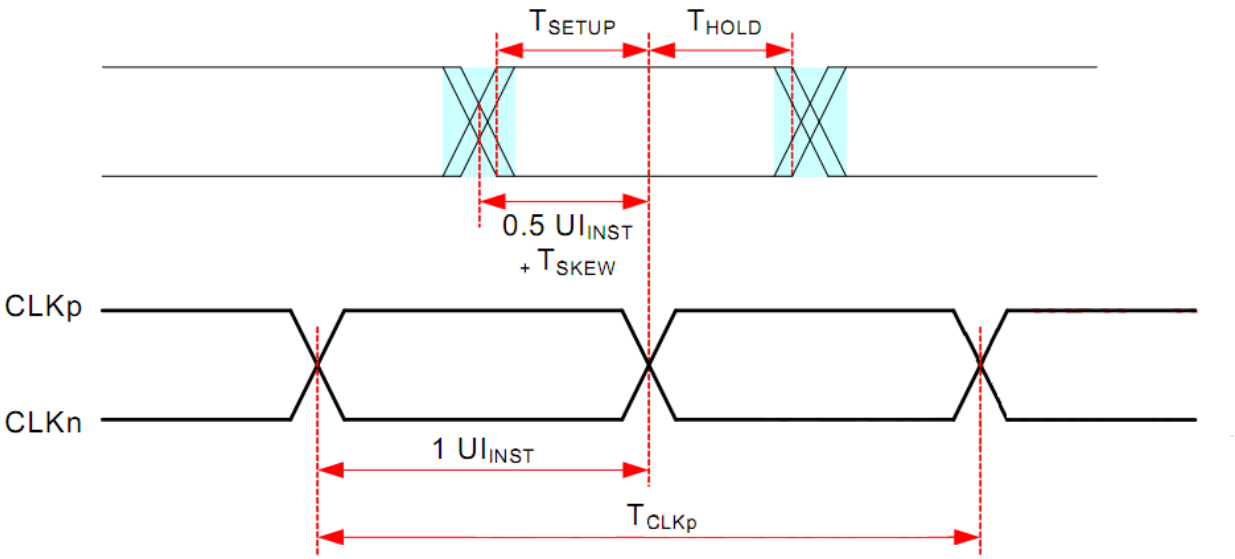


Figure 6.2.3 Data to Clock Timing Definitions

6.2.4 Hign-Speed Data Transmission in Bursts

Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40	-	55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns

Table 6.2.4 Hign-Speed Data Transmission Operation Timing Parameters

Note:
1. The minimum value depends on the bit rate.Implementations should ensure proper operation for all the supported bit rates.
2. UI means Unit Interval,equal to one half HS the clock period on the Clock Lane.
3. TLpx is an internal state machine timing reference.Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

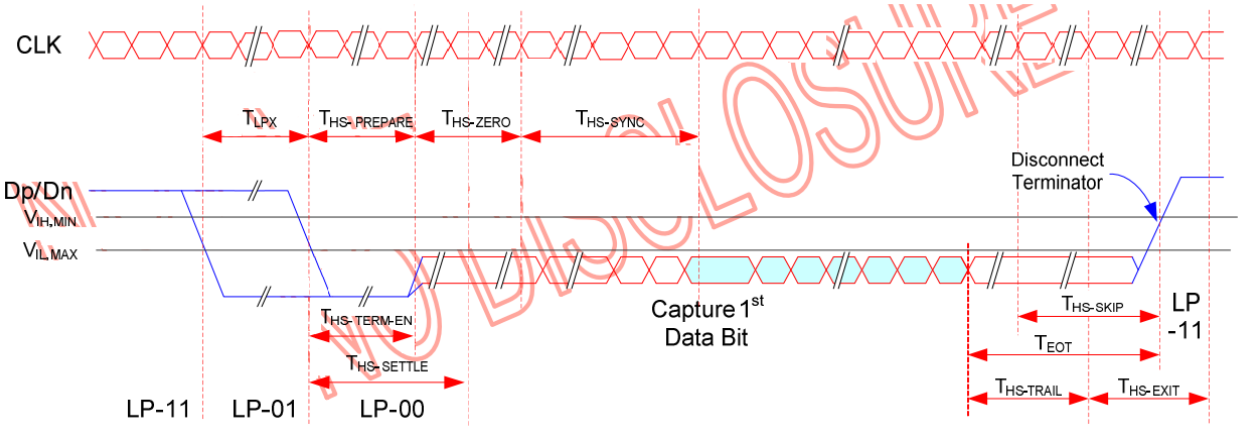


Figure 6.2.4 High-Speed data Transmission in Bursts

6.2.5 Hign-Speed Clock Transmission

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

Table 6.2.5 Switching Clock Lane Operation Timing Parameters

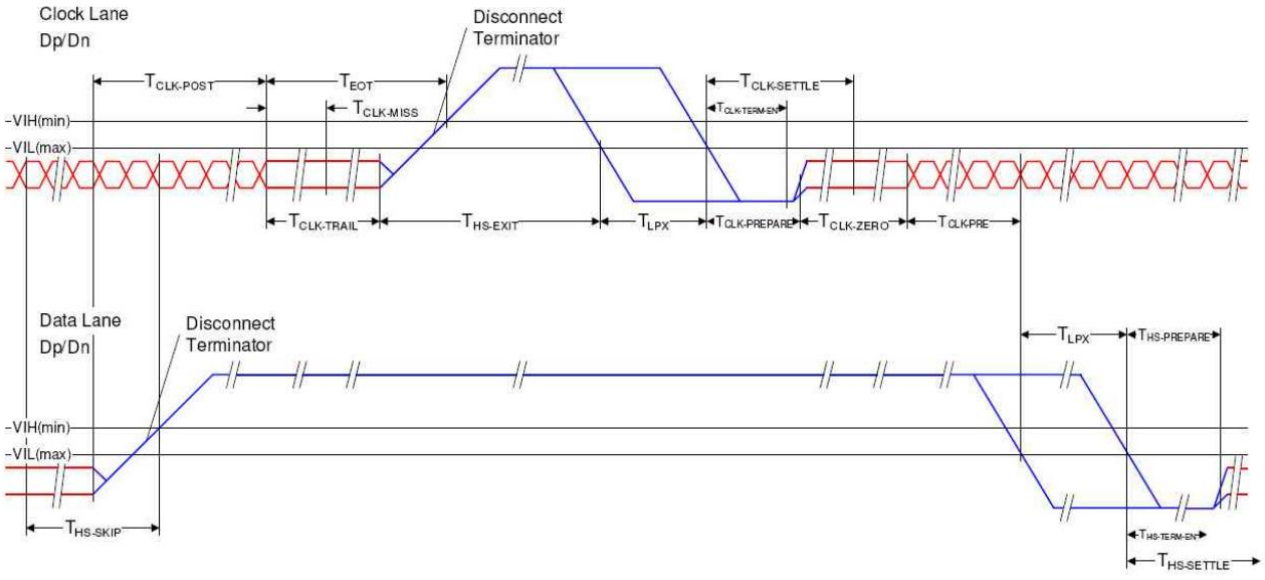


Figure 6.2.5 Switching the Clock Lane between Clock Transmission and Low-Power Mode

6.3 Input Timing Table

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI data frequency	F_{DATA}	-	999	1000	Mbps
Horizontal display area	T_{HD}		1200		pixel
HS period time	T_H	-	1341	-	pixel
HS pulse width	T_{HPW}	1	1	-	pixel
HS back porch	T_{HBP}	32	60	-	pixel
HS front porch	T_{HFP}	42	80	-	pixel
Vertical display area	T_{VD}		1920		H
VS period time	T_V	-	1981	-	H
VS pulse width	T_{VPW}	1	1	-	H
VS back porch	T_{VBP}		25		H
VS front porch	T_{VFP}	35	35	-	H

Table 6.3 1200(RGB)*1920

6.4 POWER ON/OFF SEQUENCE

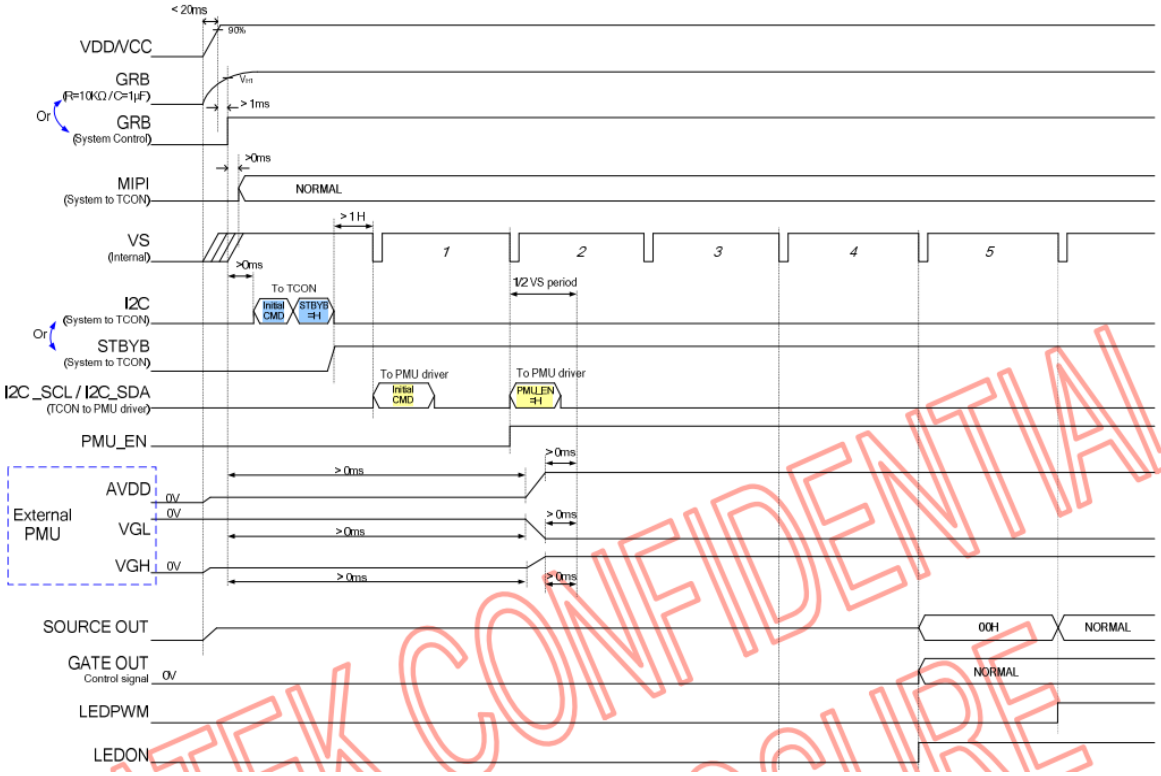
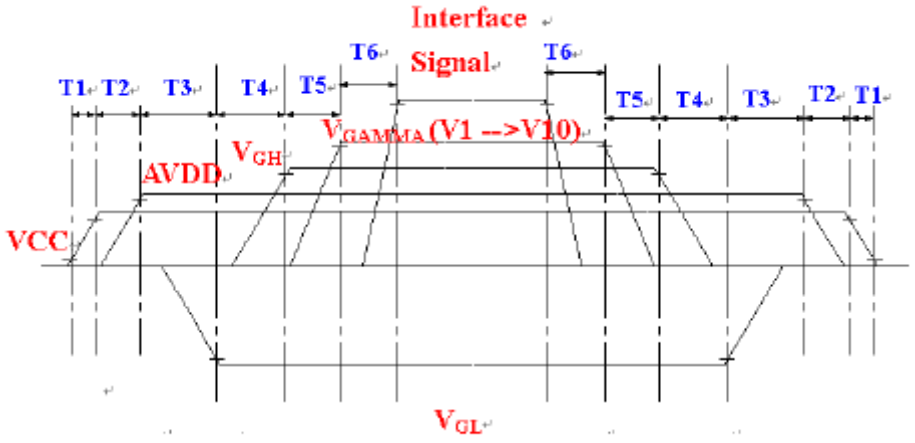


Figure 6.4.1 Power ON sequence

Figure 6.2 Power OFF sequence

6.5 System power ON/OFF sequence



	Min.	Typ.	Max.	Unit
T1	-	-	20	ms
T2	16	-	-	ms
T3	> 0			ms
T4	>0			ms
T5	>0			ms
T6	>0			ms

7 Optical Characteristics

Ta=25℃

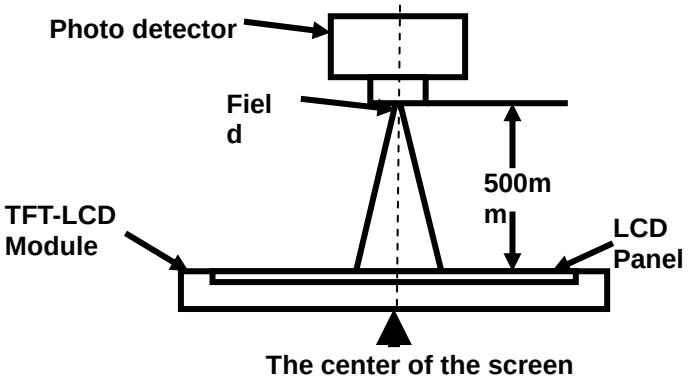
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	70	85	-	Degree	Note 2
		θB		70	85	-		
		θL		70	85	-		
		θR		70	85	-		
Contrast Ratio		CR	θ=0°	600	800	-	-	Note1 Note3
Response Time		T_{ON}	25℃	-	25	35	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.271	0.301	0.331	-	Note5 Note1
		y		0.291	0.321	0.351		
	Red	x		±0.03	0.637	±0.03		
		y			0.349			
	Green	x			0.345			
		y			0.589			
	Blue	x			0.150			
		y			0.089			
Uniformity		U	13 points	75	80	-	%	Note1 Note6
NTSC		-	-	55	60	-	%	Note 5
Luminance		L		330	390	-	cd/m^2	Note1 Note7

Test Conditions:

1. V_F=22.4V, I_F=63mA(7 LED Serial, 3 LED Parallel), the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。

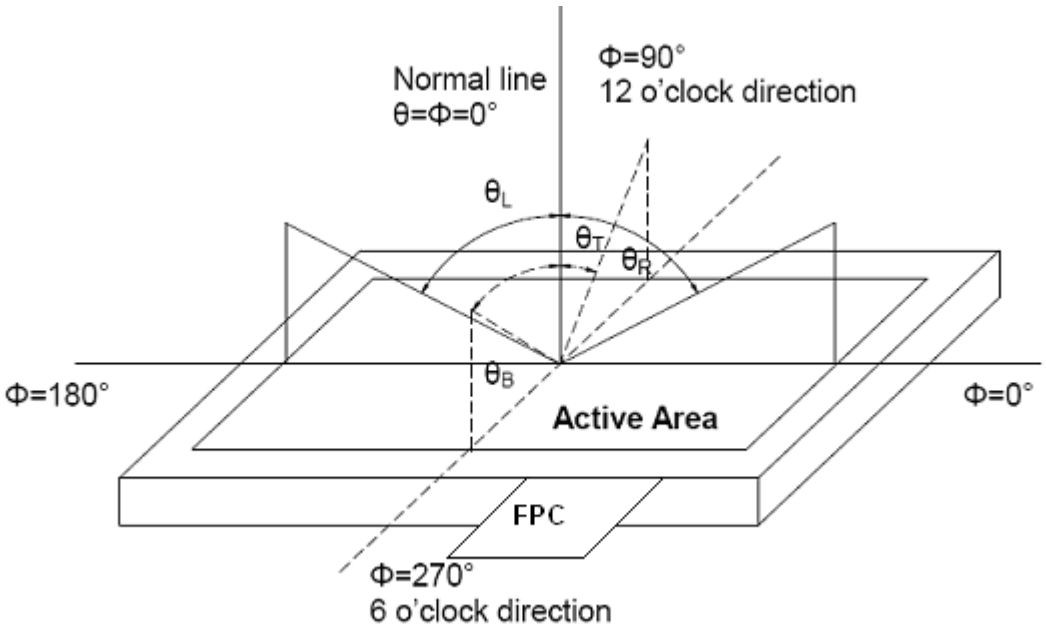


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

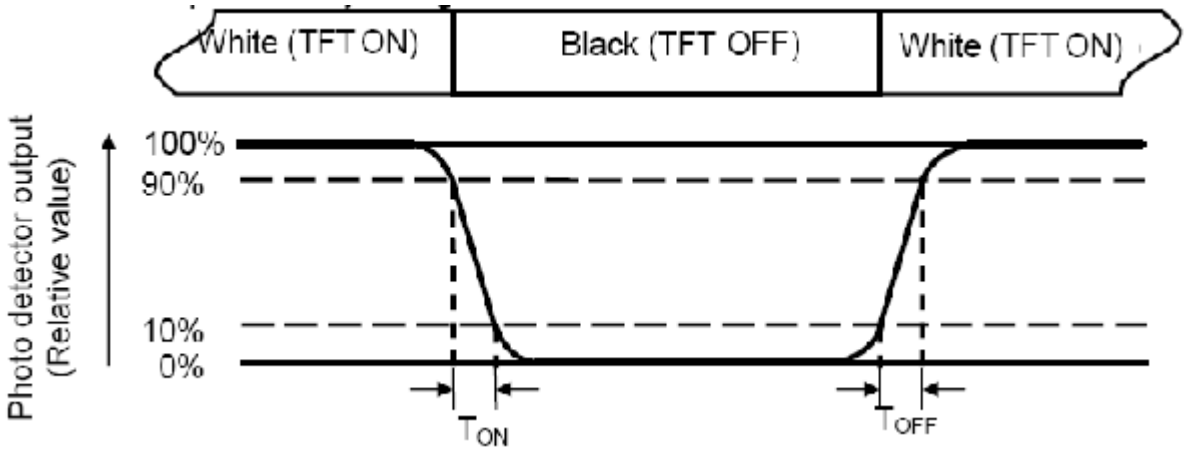
“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 13 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

W-------Active area length H----- Active area width

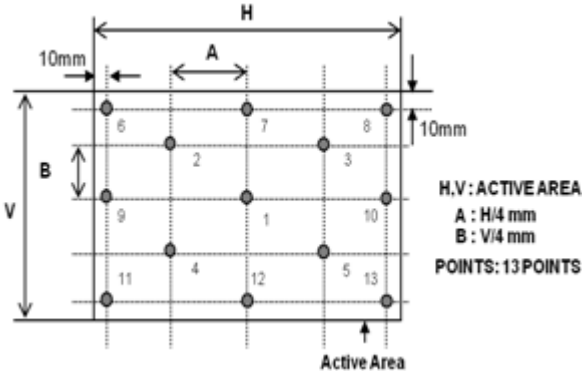


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance :

Measure the luminance of white state at center point.

8 Environmental / Reliability Test

No	Test Item	Condition	Remark
1	High Temperature Operation	Ts=+60℃, 240hrs	Note1 IEC60068-2-1,GB2423.2
2	Low Temperature Operation	Ta=-10℃, 240hrs	IEC60068-2-1 GB2423.1
3	High Temperature Storage	Ta=+70℃, 240hrs	IEC60068-2-1 GB2423.2
4	Low Temperature Storage	Ta=-20℃, 240hrs	IEC60068-2-1 GB2423.1
5	High Temperature & High Humidity Storage	Ta=+60℃, 90% RH, 240hrs	Note2 IEC60068-2-78 GB/T2423.3
6	Thermal Shock (Non-operation)	-20℃ 0.5hrs ~+70℃ 0.5hrs, Change time:5min, 50 Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22
7	Electro Static Discharge (Operation)	C=150pF, R=330Ω,5point/panel 1.Power Off Air:±4KV, 10 times, Contact:± 2KV, 10 times, 2.Power On Air:± 8KV , 10 times, Contact:± 4KV , 10 times, （Environment: 15℃～30℃, 35%～45%, 86Kpa～106Kpa）	IEC61000-4-2 GB/T17626.2
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition)	IEC60068-2-6 GB/T2423.10
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	IEC60068-2-27 GB/T2423.5
10	Package Drop Test	Height:60 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8

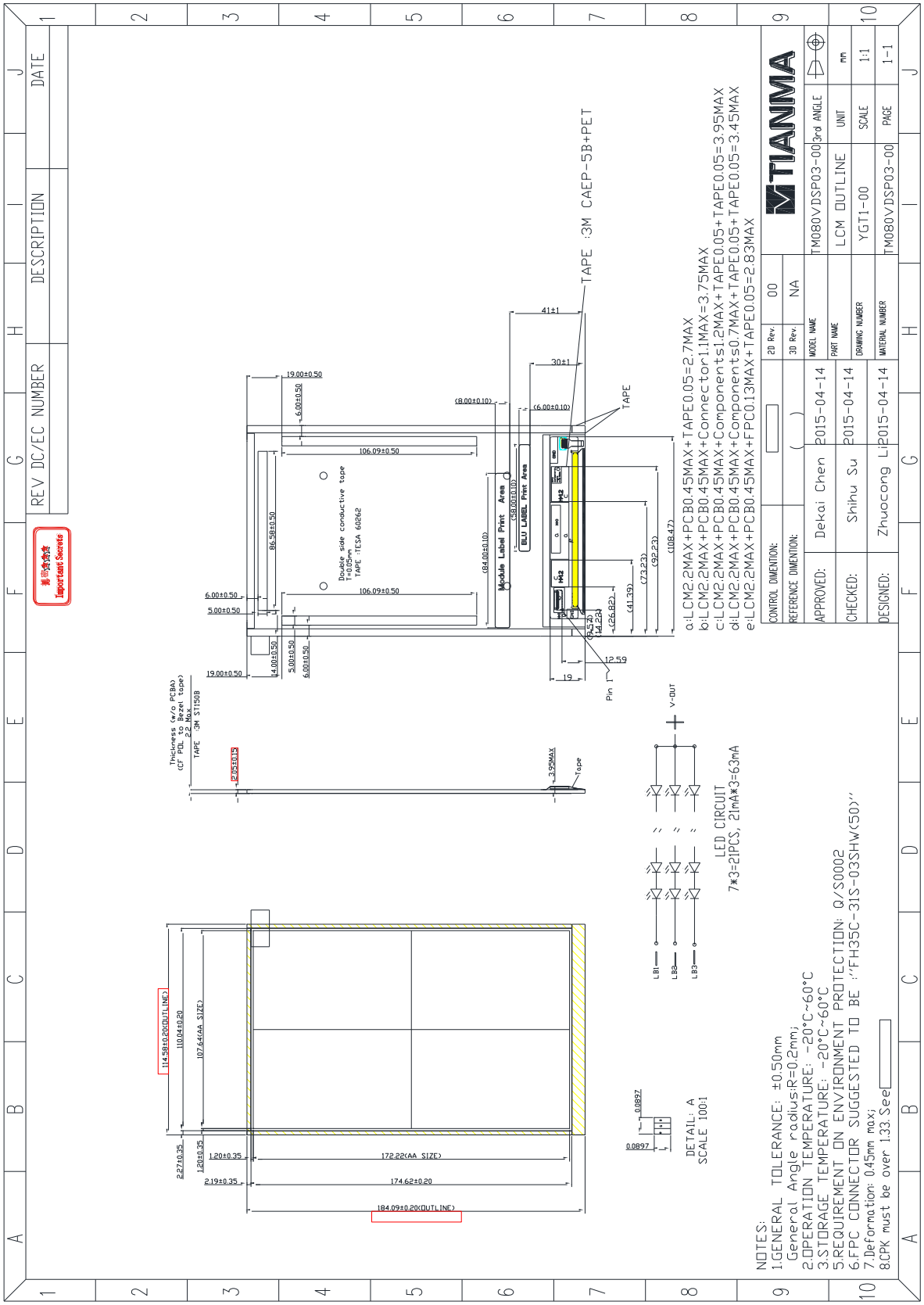
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

9 Mechanical Drawing



10 Packing Drawing

TBD

11 Precautions For Use of LCD Modules

11.1 Handling Precautions

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6 Do not attempt to disassemble the LCD Module.

11.1.7 If the logic circuit power is off, do not apply the input signals.

11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1 Be sure to ground the body when handling the LCD Modules.

11.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage precautions

11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:
Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

11.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.