TV080WUM-NL1 Product Specification

BUYER	
SUPPLIER	HEFEI BOE Optoelectronics Technology CO., LTD
FG-Code	**TV080WUM-NL1**

ITEM	BUYER SIGNATURE	DATE
_____	_____	
_____	_____	
_____	_____	_____

ITEM	SUPPLIER SIGNATURE	DATE
Prepared	_____	_____
Reviewed	_____	_____
Approved	_____	_____

HEFEI BOE OPTOELECTRONICS TECHNOLOGY

REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
1.0	-	Initial Release		

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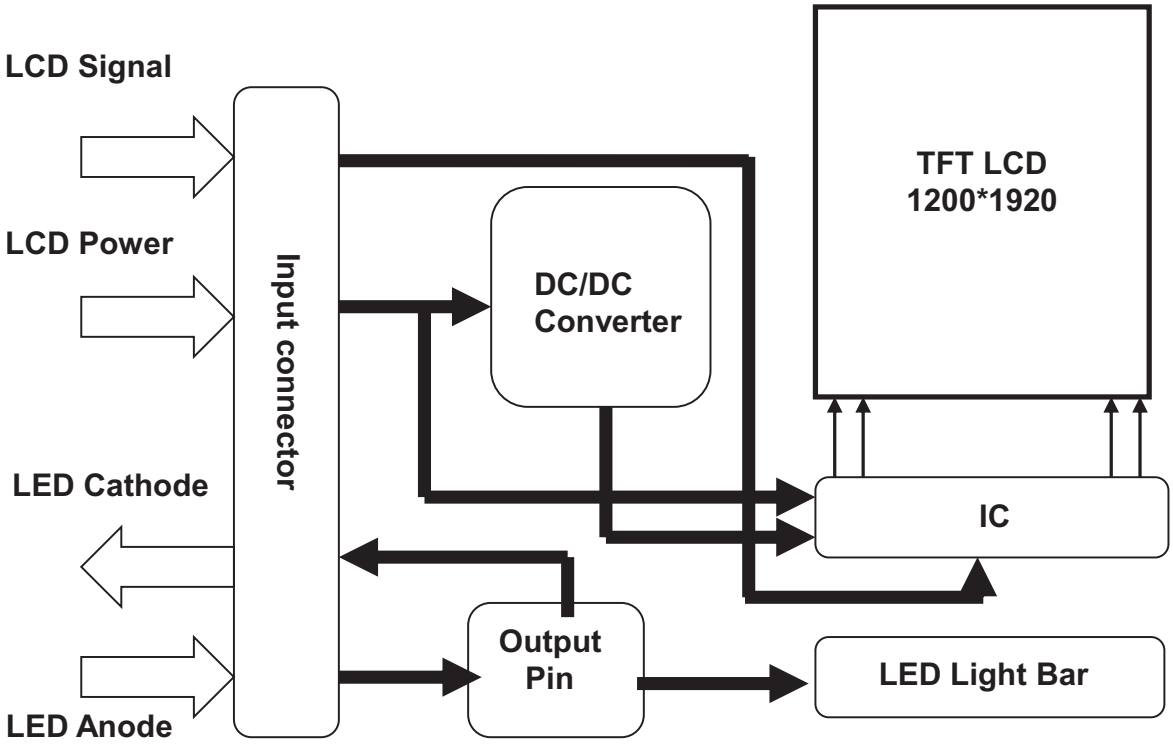
1.0. GENERAL DESCRIPTION

Block Diagram



Features

TV080WUM-NL1 is 8” color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, MIPI driver ICs, control circuit and backlight. By applying 8 bit digital data, 1200*RGB*1920,
16.7M-color images are displayed on the 8” diagonal screen

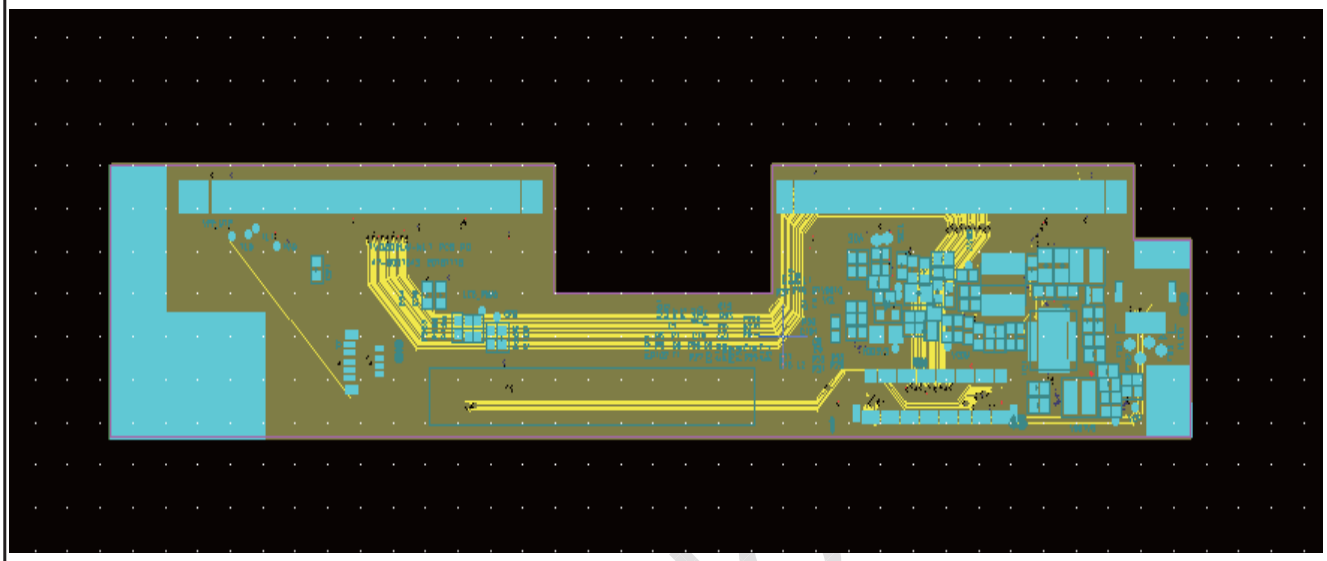
1.1 General Specifications

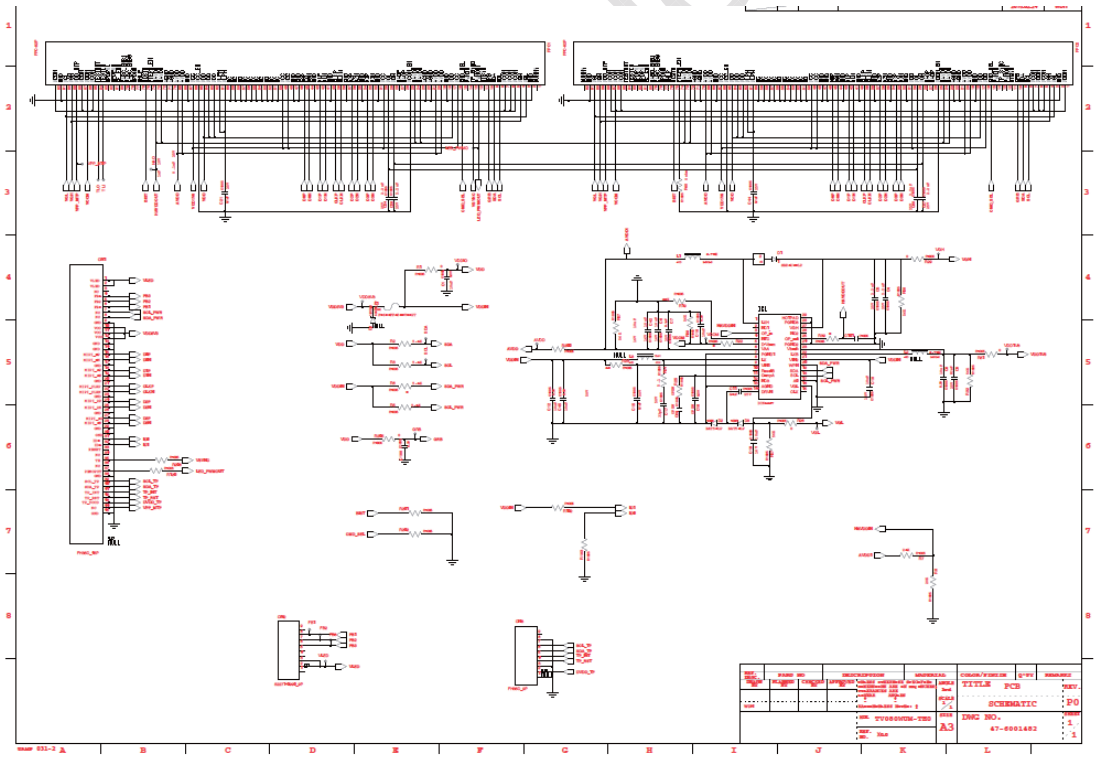
Parameter	Specification	Unit	Remarks
Screen Size	8	Inch	
Active Area	107.64*172.224	mm	
Panel Size	111.64*180.724	mm	
Outline Dimension	114.6*183.75	mm	±0.2
Display Resolution	1200*RGB*1920	pixel	
Pixel Pitch	29.9*89.7	um	
Display Method	a-Si	-	
Display Mode	Normal Black	-	
Display Color	16.7M	-	
Color Gamut	Typ. 60% , Min. 55%	%	NTSC
Luminance	Typ. 400 , Min. 350	nit	5 Point Ave. Value
Contrast Ratio	Typ. 1000:1 , Min. 800:1	-	
Viewing Angle	80/80/80/80(CR>10)	-	Single Center Point
Pol Surface Treatment	HC	-	
Weight	Max. 85	g	
D-IC	NT51021	-	2ea
Inversion Method	Colum	-	
LED Q'ty	24	ea	
Power Consumption	450+1512	mw	Logic+Back light

1.2 Key Part List

	item	Supplier	Spec/Size	Weight	Remark
Cell	TFT Glass	corning	1850*1500*0.5T		mm
	C/F Glass	corning	1850*1500*0.5T		mm
	Upper Pol	住化	109.64*174.72*0.097mm	-	HC
	Lower Pol	住化	109.84*175.42*0.108mm	-	Clear
	Liquid Crystal	Merck	F013	-	
	Sealant	Sekisui	SWB-101	-	
Circuit	FPC	倜茂沃	30.4*9.36		
	PCB	TPT/Dynamic	99.5mm x 19mm, 4layer		
	MIPI CNT	IPEX	20655-045E-01		
	TP CNT	HIROSE	FH35C-9S-0.3SHW(50)		
BLU	B/B tape	NITTO	TJW-WL58DBHL		
	Up Dif	SKC	JS560HK		
	Upper Prism	KDX	KBUO-100N		
	Lower Prism	KDX	KBUO-100N		
	Down Dif	LMS	DLAS-50D3		
	LGP	兆纪	PMMA GH-1000S		
	Mold frame	兆纪	URZ2501		
	Back Cover	兆纪	SUS304		
	Reflector	Lumirex	LumirexII -100		
	LED	聚飞	CAS306W65P00		
	LED Lightbar	聚飞	0.6 LED+0.12FPC		
Total			-		

1.3.1. PPCA Gerber/Layout and Schematic Diagram



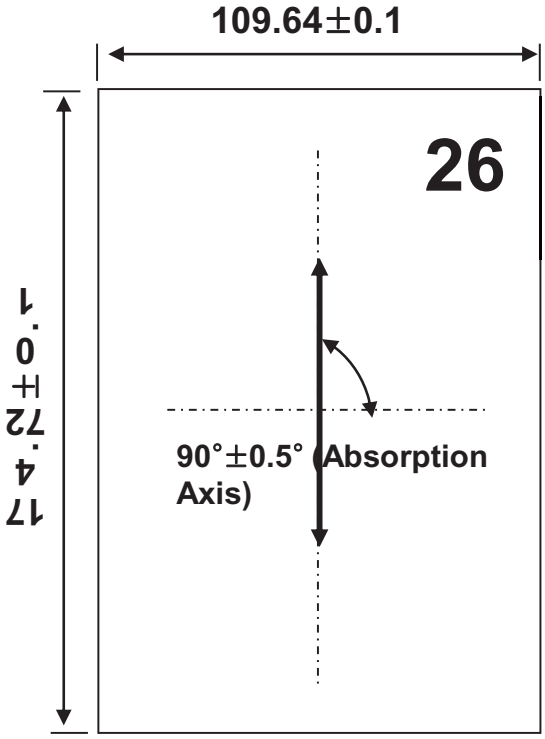


1.3.2. FPC Pin Assignment

Please pay attention that IC bump down(TFT glass up and C/F glass down)

No.1	VCOM	No.42	GND	No.77	VCC
No.2		No.43	D3N	No.78	GND
No.3-4		No.44	D3P	No.79-81	AVDD(2)
No.5	GND	No.45	GND	No.82-84	AGND(2)
No.6-7	VGL	No.46	D2N	No.85-87	HAVDD(2)
No.8-9	VGH	No.47	D2P	No.88	RTERM_EN
No.10-12	VCOM(3)	No.48	GND	No.89	BISTB
		No.49	CLKN	No.90	SHLR
No.13	SCL	No.50	CLKP	No.91	UPDNB
No.14	SDA	No.51	GND	No.92	CABC_ENB0
No.15	GRB	No.52	D1N	No.93	CABC_ENB1
No.16	STBYB	No.53	D1P	No.94	CE_ENB
No.17	PWMOUT	No.54	GND	No.95	OPDRV0
No.18	TP_SYNC	No.55	D0N	No.96	OPDRV1
No.19		No.56	D0P	No.97	
No.20	PWMIN	No.57-58	GND(2)	No.98	
No.21	CMD_SEL	No.59-60	VCC(2)	No.99	TESTIN
No.22		No.61	NC	No.100	TESTOUT
No.23	VCC	No.62	NC	No.101-103	VCOM(3)
No.24	VDD	No.63	NC		
No.25	GND	No.64	NC	No.104	VPP_MTP
No.26-27	AVDD(2)	No.65	NC	No.105-106	VGH
No.28-29	AGND(2)	No.66	NC	No.107-108	VGL
No.30-31	HAVDD(2)	No.67	NC	No.109-110	GND
No.32-34		No.68	NC	No.111-112	
No.35	VCOM_EN	No.69	NC	No.113	
No.36-38	HAOP(2)	No.70	NC	No.114	Dummy
No.39	VQH	No.71-72	VLPH(2)		
No.40	VQL	No.73-75	VDD(3)		
No.41	VCC	No.76	VCC_EN		

1.3.3. Pol General Spec

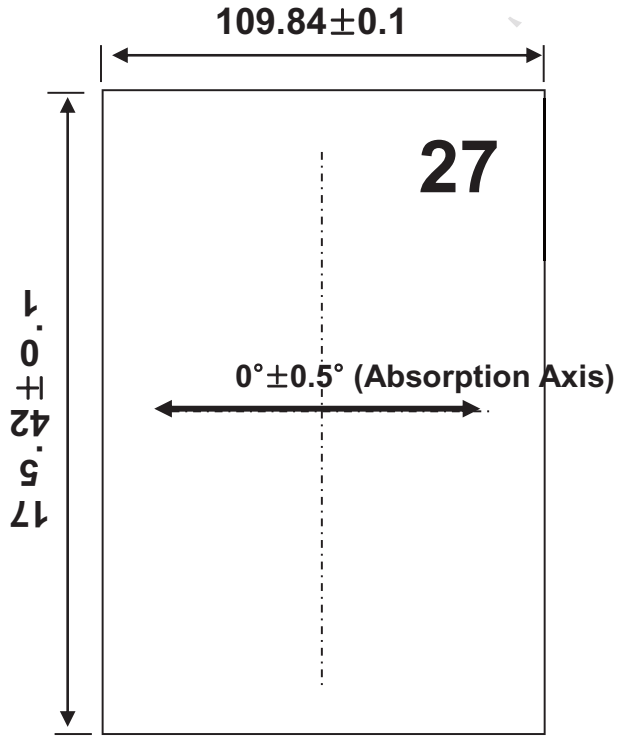


Adhesive Downwards

HC≥2H

有效厚度(97±20μm)

Protect Film
HC Layer
TAC
PVA
NRT
PSA
Separator



Adhesive Downwards

Clear

有效厚度 (108±20μm)

Protect Film
Adhesive
TAC
PVA
NRT
PSA
Separator

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage the unit. The operational and non-operational maximum voltage and current values are listed in the following table .

Parameter	Symbol	Min.	Max.	Unit	Remarks
Logic Power Supply Voltage	VDD3V3	-0.3	3.6	V	Note1
LED Forward Current of every LED string	I_{LED}	-	30	mA	Note2
LED string Reverse Voltage	V_R	-	30	V	10uA
Operating Temperature	T_{OP}	-20	+60	℃	Note3
Storage Temperature	T_{ST}	-30	+70	℃	

Notes : 1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. the max value of LED forward current is relative to ambient temperature,the correlation is show in figure 1.

3. Temperature and relative humidity range are shown in the figure below.
   95 % RH Max. (40 ℃ ≥ Ta)
   Maximum wet - bulb temperature at 39 OC or less. (Ta > 40 OC) No condensation.

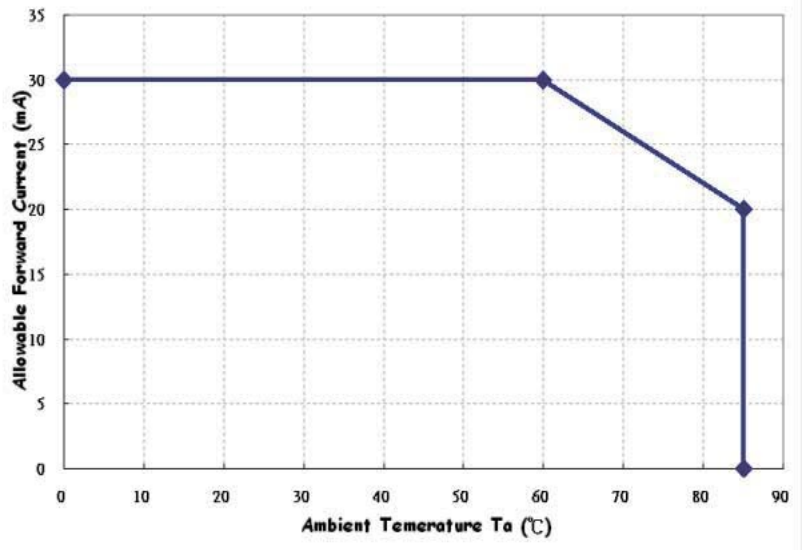


Figure 1. forward current vs ambient temperature

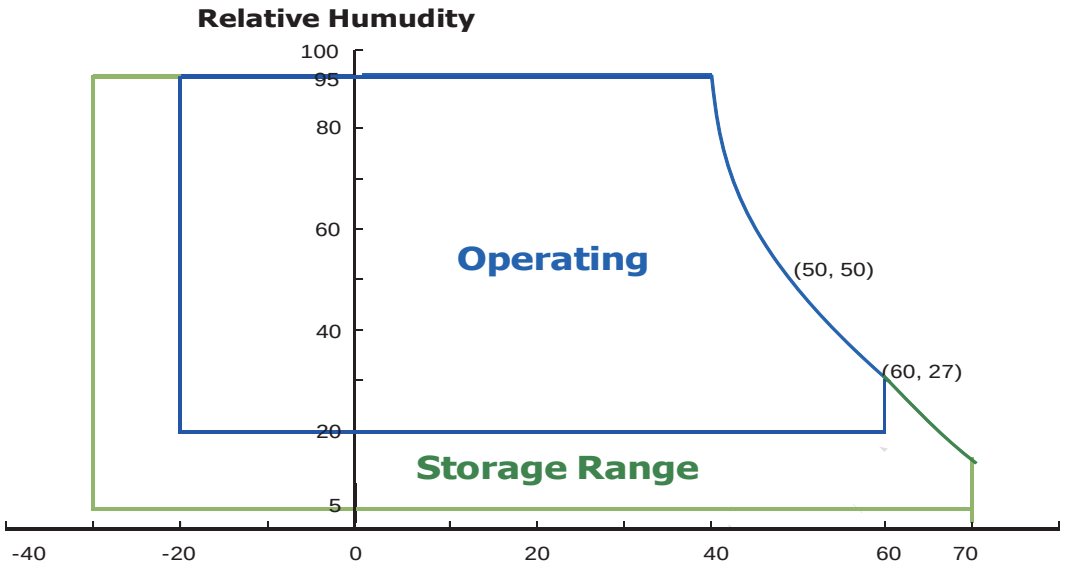


Figure 2. Operation temperature vs Humudity

3.0 Electrical Specifications

[Ta =25±2 ℃]

3.1 TFT LCD Module

Parameter	Symbol	Values			Unit	Notes
		Min	Typ.	Max		
Power Supply Input Voltage	V_{DD}	3.0	3.3	3.6	V	Note 1
Power Supply Current	I_{DD}	-	136.4		mA	
LED Forward Voltage of every LED string	V_{LED}	-	24	25.6	V	Note 2
LED Forward Current of every LED string	I_{LED}	-	21	-	mA	
Power Consumption	P_D	-	0.45	-	W	Note 3
	P_{BL}	--	1.512	--	W	
	P_{Total}	-	1.962	-	W	

3.2 BACK LIGHT UNIT

The edge-lighting type of back light unit consists of 24 LEDs which is connected in serial.

Table 3.1 Electrical Characteristics Of Back Light Unit

Parameter	Symbol	Values			Units	Notes
		Min	Typ.	Max		
LED Current	I_{LED}	-	21	30	mA	
LED Forward Voltage	V_{LED}	2.8	3.0	3.2	V	

3-2-1 LED Rank

Luminance Rank : >9.5Lm(TBD)

Color Rank :F档(TBD)

3.3. LCD INTERFACE CONNECTIONS

Interface Connector IPEX 20655-045E-01 is used for the module electronics interface.

<Table 3.2. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	VLED	Power for LED Anode
2	VLED	Power for LED Anode
3	NC	NC
4	LED1-	Power for LED1 Cathode
5	LED2-	Power for LED2 Cathode
6	LED3-	Power for LED3 Cathode
7	NC	NC
8	NC(WP)	For INX internal use only, Please keep it floating
9	GND	Ground
10	VCC	Power Supply 3.3V
11	VCC	Power Supply 3.3V
12	VCC	Power Supply 3.3V
13	GND	Ground
14	GND	Ground
15	MIPI_DATA0_P	MIPI Differential Data Input
16	MIPI_DATA0_N	MIPI Differential Data Input
17	GND	Ground
18	MIPI_DATA1_P	MIPI Differential Data Input
19	MIPI_DATA1_N	MIPI Differential Data Input
20	GND	Ground

<Table 3.2. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
21	MIPI_CLK_P	MIPI Differential Clock Input
22	MIPI_CLK_N	MIPI Differential Clock Input
23	GND	Ground
24	MIPI_DATA2_P	MIPI Differential Data Input
25	MIPI_DATA2_N	MIPI Differential Data Input
26	GND	Ground
27	MIPI_DATA3_P	MIPI Differential Data Input
28	MIPI_DATA3_N	MIPI Differential Data Input
29	GND	Ground
30	GND	Ground
31	ID0	ID0 (IOVCC/GND)
32	ID1	ID1 (IOVCC/GND)
33	RESET	RESET (BOE NC)
34	NC(SCL)	For INX internal use only, Please keep it floating
35	TE	TE
36	NC(SDA)	For INX internal use only, Please keep it floating
37	LEDPWMOUT	Output pin for PWM signal of LED driving
38	GND	Ground
39	I2C_SCL_TP	I2C CLK,TYP. 1.8V
40	I2C_SDA_TP	I2C SDA,TYP. 1.8V
41	TP_INT	Interrupt Pin
42	TP_RST	Reset Pin
43	TP_VCCD	Analog Power supply, TYP. 3.3V
44	NC	NC
45	GND	Ground

4.0. SIGNAL TIMING SPECIFICATIONS

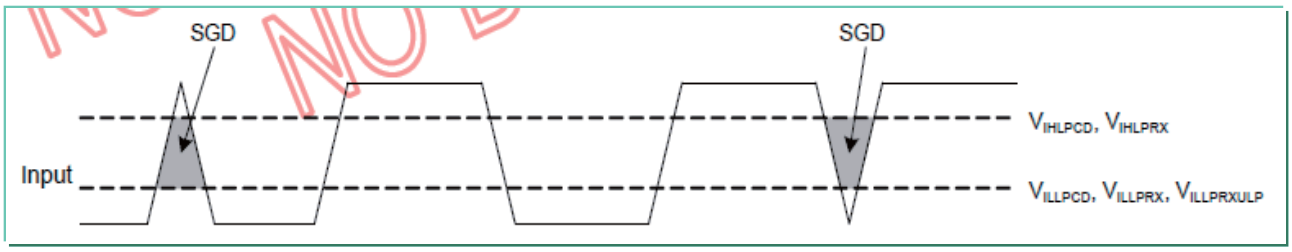
ITEM			SYNBOL	min	typ	max	UNIT
LCD	Frame Rate		-	-	60	-	Hz
	Pixels Rate		-	156.8	156.8	159.9	MHz
Timing	DCLK	Frequency	fCLK	490	490	498	MHz
		Period	Tclk	2.01	2.04	2.04	ns
	Horizontal	Horizontal total time	tHP	1343	1343	1366	t_{CLK}
		Horizontal Active time	tHadr		1200		t_{CLK}
		Horizontal Pulse Width	tHsync	1	1	1	t_{CLK}
		Horizontal Back Porch	tHBP	32	32	32	t_{CLK}
		Horizontal Front Porch	tHFP	110	110	133	t_{CLK}
	Vertical	Vertical total time	tvp	1946	1946	1951	t_H
		Vertical Active time	tVadr		1920		t_H
		Vertical Pulse Width	tVsync	1	1	1	t_H
		Vertical Back Porch	tVBP	14	14	14	t_H
		Vertical Front Porch	tVFP	11	11	16	t_H
Differential Swing			VDswing	400	500	-	mV
Bit Rate			TX SPD (MBPS)	980	980	995	Mbps
Pixel Fomat				-	24	-	Data bit/ pixel
Lane				-	4	-	Lane

4.1. MIPI Interface DC/AC Characteristic

(1) MIPI Interface Timing Sequence

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.65~3.6V, VCI=2.5 to 4.8V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 °C (to +85 °C no damage). VCI means VDDA, VDDR, VDDB and VSS means VSSAM, VSSA, VSSR, VSSB, AVSS.
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.



(2) DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

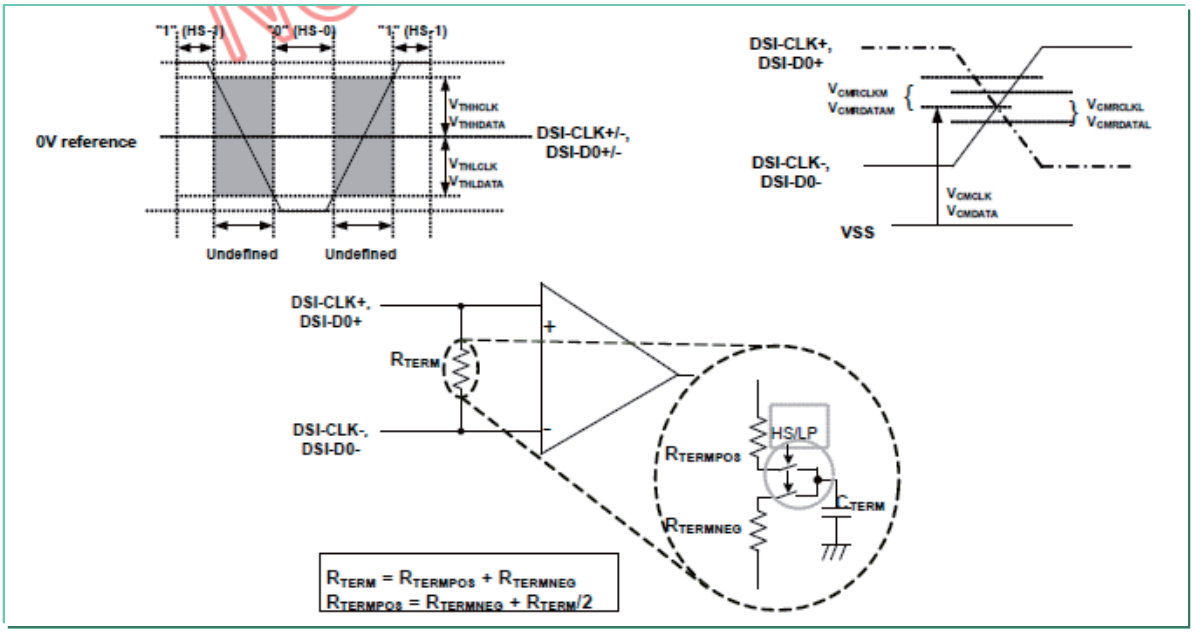
Note 1) VDDI=1.65~3.6V, VCI=2.5 to 4.8V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage). VCI means VDDA, VDDR, VDDB and VSS means VSSAM, VSSA, VSSR, VSSB, AVSS.

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.

Note 4) Without 50mV (-50mV to 50mV) ground difference.

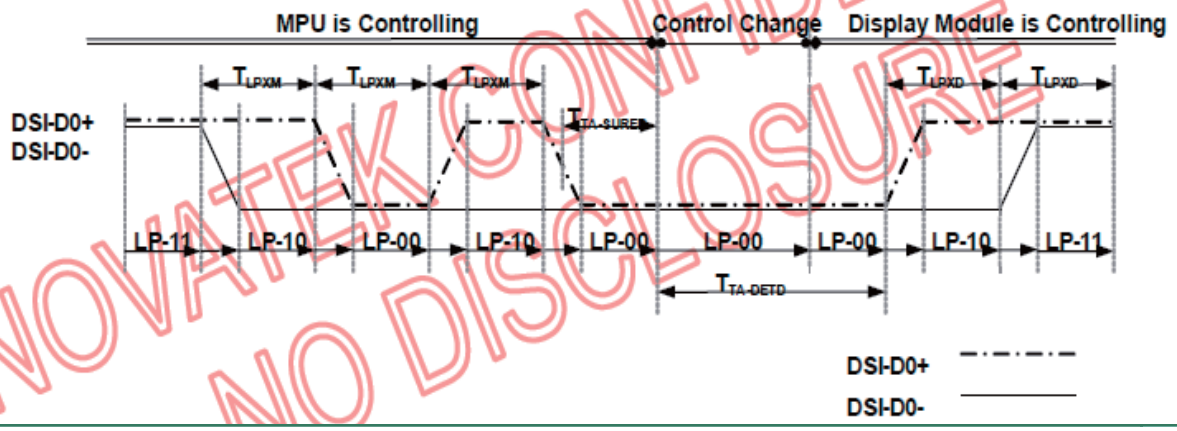
Note 5) Dn=D0, D1, D2 and D3.

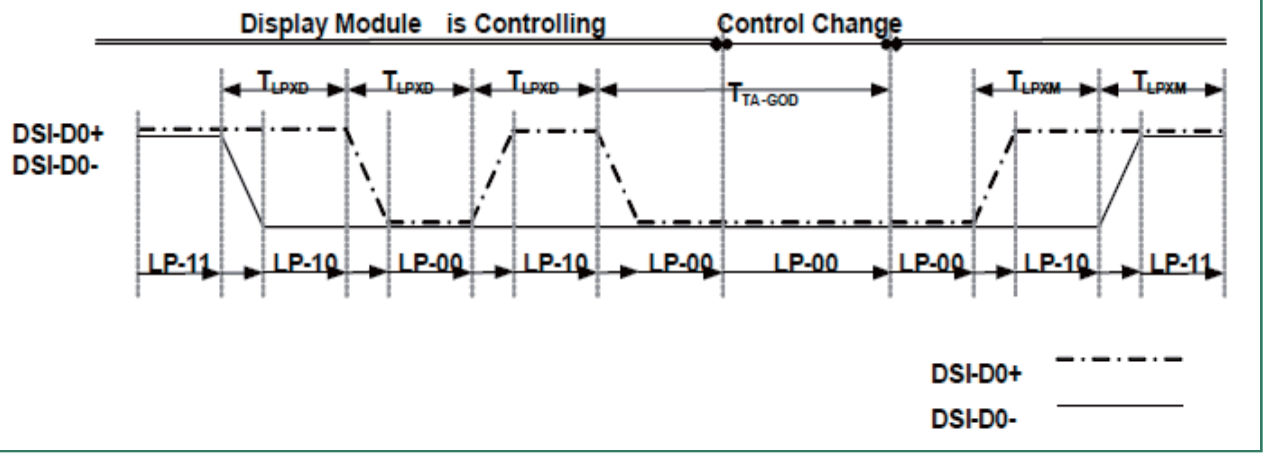


(3)Low Power Mode

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VCI=2.5V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output





(4)DSI Bursts

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VCI=2.5V to 4.8V,Ta = -30 to 70˚C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.

MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers. Systems using Command Mode write to, and read from the registers.The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

(5)MIPI Lane Configuration

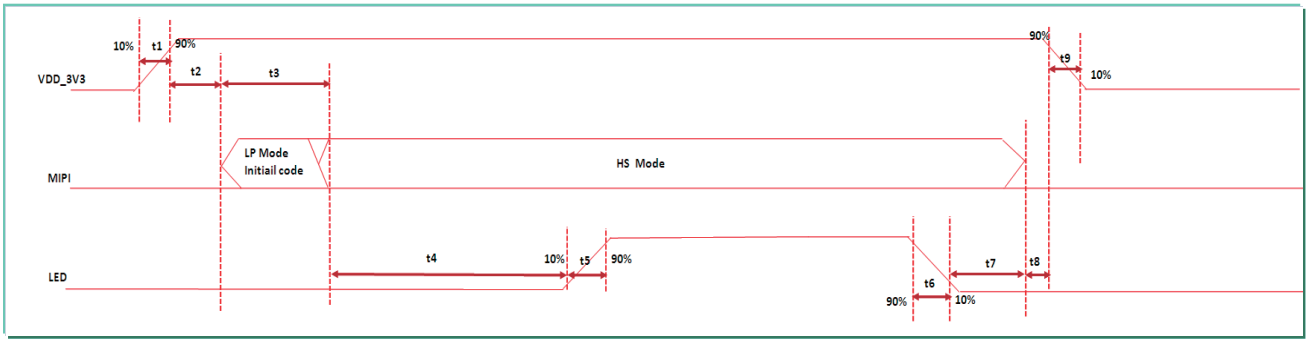
Lane Pair	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane 1 Data Lane 2 Data Lane 3	Unidirectional Lane ■ Forward High-Speed ■ Escape Mode (ULPM only) ■ No LPDT

The connection between host device and display module is as reference.

4.2. Power Sequence

(1) Power Sequence1

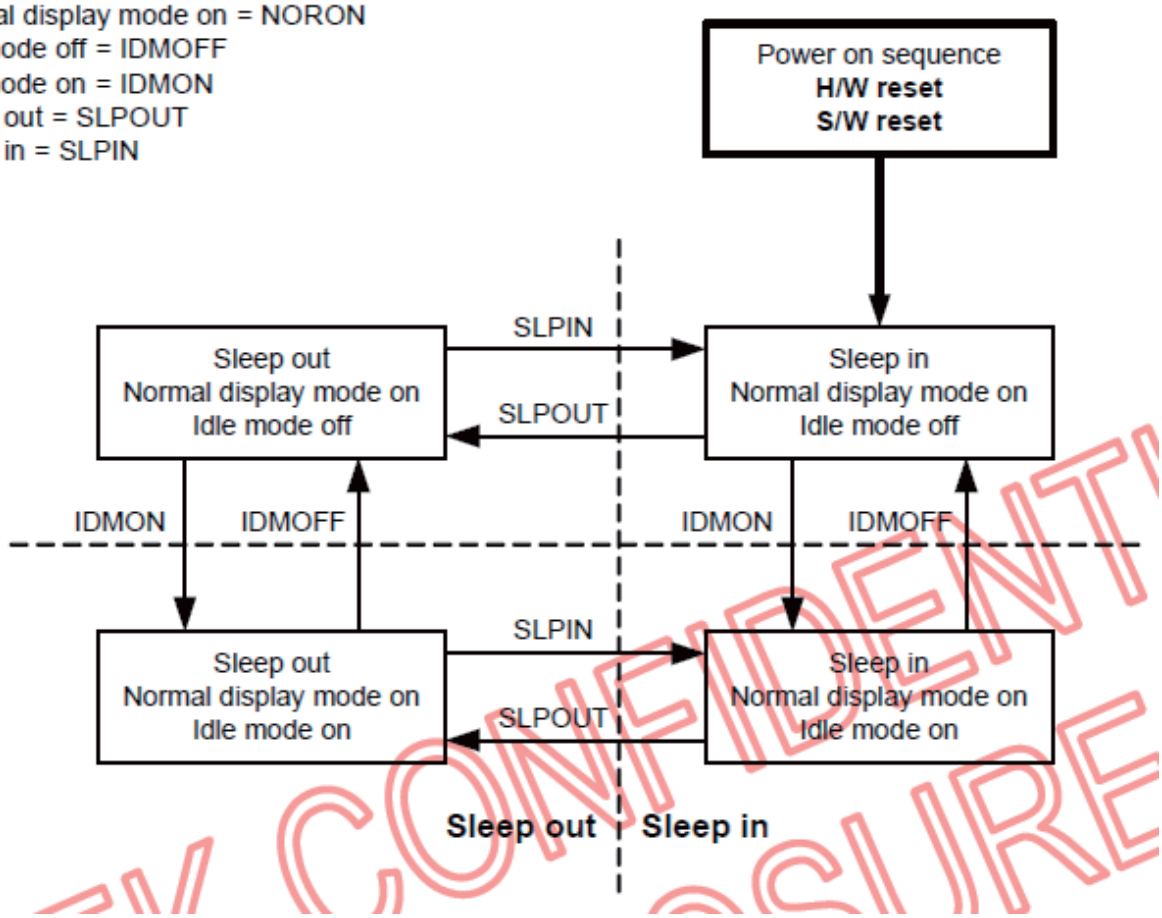
To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



Parameter	Value				Remark
	Min.	Typ.	Max.	Unit	
t1	0.1	-	20	ms	
t2	1	-	20	ms	
t3	20	-	40	ms	
t4	200	-	-	ms	
t5	0.1	-	20	ms	
t6	0.1		20	ms	
t7	200	-	-	ms	
t8	0	-	20	ms	
t9	0.1	-	20	ms	

(2). Software Flow

Commands:
Normal display mode on = NORON
Idle mode off = IDMOFF
Idle mode on = IDMON
Sleep out = SLPOUT
Sleep in = SLPIN



4.3. Initial Code

delay 100	RD9 CF	RC9 D6	RFB FA	REB 09
R8F A5	RDA D9	RCA DE	RFC FF	REC 13
delay 1	RDB E2	RCB FD	RFD FF	RED 1B
R01	RDC F3	RCC 0D	RFE FC	REE 19
delay 20	RDD FF	RCD 15	RFF 2F	REF 1F
R8F A5	RDE F8	RCE 19	R83 CC	RF0 25
DELAY 1	RDF 2F	RCF 17	R84 33	RF1 3C
R83 00	RE0 19	RD0 1B	RC0 0B	RF2 52
R84 00	RE1 1A	RD1 2C	RC1 0C	RF3 71
R8C 0E	RE2 24	RD2 42	RC2 1A	RF4 76
R97 00	RE3 33	RD3 61	RC3 27	RF5 C6
RFA 0D	RE4 40	RD4 64	RC4 34	RF6 CE
RFD 13	RE5 4B	RD5 B4	RC5 3F	RF7 D6
R9F 00	RE6 56	RD6 BA	RC6 4A	RF8 DF
R83 AA	RE7 5F	RD7 C0	RC7 53	RF9 E7
R84 11	RE8 68	RD8 C7	RC8 5C	RFA F1
RA9 4B	RE9 E2	RD9 CF	RC9 D6	RFB FA
R83 BB	REA EA	RDA D9	RCA DE	RFC FF
R84 22	REB 09	RDB E2	RCB FD	RFD FF
R91 80	REC 13	RDC F3	RCC 0D	RFE FC
R94 68	RED 1B	RDD FF	RCD 15	RFF 2F
R95 11	REE 19	RDE F8	RCE 19	R11
R96 00	REF 1F	RDF 2F	RCF 17	R8F 00
R83 AA	RF0 25	RE0 19	RD0 1B	
R84 11	RF1 3C	RE1 1A	RD1 2C	
RC0 0B	RF2 52	RE2 24	RD2 42	
RC1 0C	RF3 71	RE3 33	RD3 61	
RC2 1A	RF4 76	RE4 40	RD4 64	
RC3 27	RF5 C6	RE5 4B	RD5 B4	
RC4 34	RF6 CE	RE6 56	RD6 BA	
RC5 3F	RF7 D6	RE7 5F	RD7 C0	
RC6 4A	RF8 DF	RE8 68	RD8 C7	
RC7 53	RF9 E7	RE9 E2	RD9 CF	
RC8 5C	RFA F1	REA EA	RDA D9	
RC9 D6	RFB FA	REB 09	RDB E2	
RCA DE	RFC FF	REC 13	RDC F3	
RCB FD	RFD FF	RED 1B	RDD FF	
RCC 0D	RFE FC	REE 19	RDE F8	
RCD 15	RFF 2F	REF 1F	RDF 2F	
RCE 19	R83 BB	RF0 25	RE0 19	
RCF 17	R84 22	RF1 3C	RE1 1A	
RD0 1B	RC0 0B	RF2 52	RE2 24	
RD1 2C	RC1 0C	RF3 71	RE3 33	
RD2 42	RC2 1A	RF4 76	RE4 40	
RD3 61	RC3 27	RF5 C6	RE5 4B	
RD4 64	RC4 34	RF6 CE	RE6 56	
RD5 B4	RC5 3F	RF7 D6	RE7 5F	
RD6 BA	RC6 4A	RF8 DF	RE8 68	
RD7 C0	RC7 53	RF9 E7	RE9 E2	
RD8 C7	RC8 5C	RFA F1	REA EA	

4.4. IC General Spec and Size

FEATURES

1. Features

- Special design for middle size TFT LCD Panel with MIPI interface
- The chip Integrate 1803 channel source driver and timing controller
- Support panel resolution (HxV) :
  1200(RGB)x1920, 600(RGB)x1024, 1080(RGB)x1920, 1200(RGB)x1600
- 8-bit resolution 256 gray-scale
- Operating frequency: MIPI: 1Gbps/Lane (Max.)
- Support 2, 3 or 4 data lanes for MIPI interface
- Power for digital circuit(VCC/VCC_IF): 1.55V ~ 1.65V
- Power for digital circuit(VDD): 2.7V ~ 3.6V
- Power for analog circuit(AVDD): 7.0 ~ 10.0V
- Support RGB independent gamma correction function
- Support CABC function
- Support Color Enhancement function
- Support Advance BIST function
- Support Zig-Zag driving method
- Support GIP function
- Not support MIPI BTA function
- COG package
- Chip size = 28500 um x 775 um
- Output bump pitch = 12 um

5.0 Optical Specifications

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (CA-310、BM-5A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°.

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	-	-	Deg.	Note 1
		Θ_9		80	-	-	Deg.	
	Vertical	Θ_{12}		80	-	-	Deg.	
		Θ_6		80	-	-	Deg.	
Color Gamut				55	60	-	%	-
Luminance Contrast ratio		CR	Θ = 0°	800:1	1000:1		-	Note 2
Luminance of White	Center Point	Y_w	Θ = 0°	350	400	-	cd/m^2	Note 3
White Luminance uniformity	13 Points	ΔY13		75	-	-	%	Note 4
	5 Points	ΔY5		80	-	-	%	Note 4
White balance		Wx	Θ = 0°	0.27	0.30	0.33	-	Note 5
		Wy		0.29	0.32	0.35	-	
Reproduction of color	Red	R_x	Θ = 0°	0.592	0.622	0.652	-	Note6
		R_y		0.318	0.348	0.378		
	Green	G_x		0.312	0.342	0.372		
		G_y		0.556	0.586	0.616		
	Blue	B_x		0.110	0.140	0.170		
		B_y		0.046	0.076	0.106		
Response Time (Rising + Falling)		T_{RT}	Ta= 25°C Θ = 0°	-	30	35	ms	Note 7

Cell & BLU Optical Characteristics

Parameter	Typ	Unit	Remarks
Aperture Ratio	52	%	
Upper Pol Trans.	42.5	%	
Lower Pol Trans.	42.5	%	
Panel Trans.	-	%	w/o APF
Panel Trans.	4.8(LCM)	%	with APF

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 1point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 1 for a total of the measurements per display. The luminance is measured by CA310 when the LED current is set at 20mA.

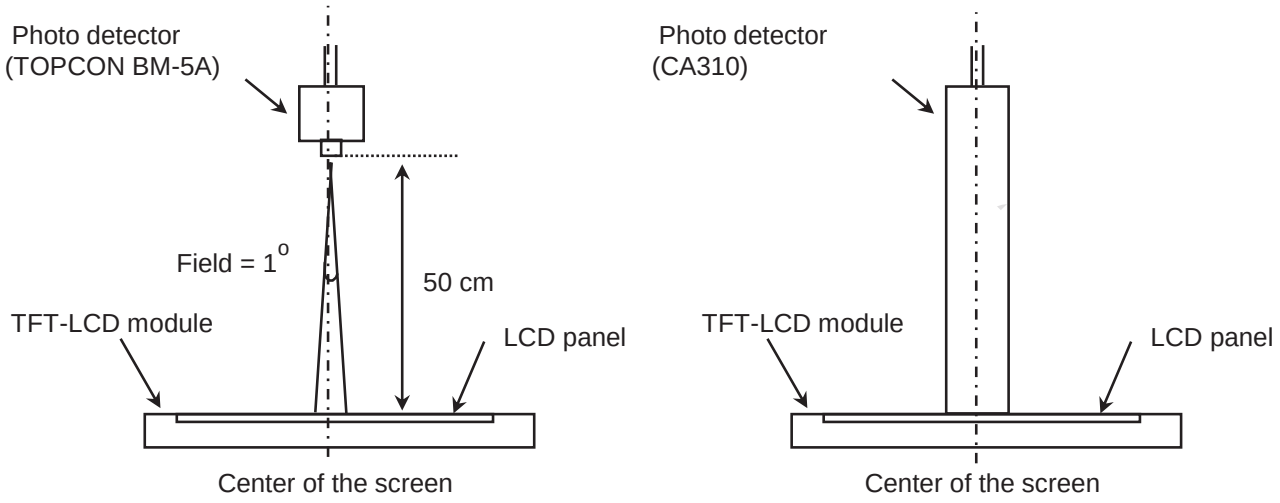
4. The White luminance uniformity on LCD surface is then expressed as : ΔY = Minimum Luminance of 9points / Maximum Luminance of 9points (see FIGURE 2).

5. The color chromaticity coordinates specified shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The color chromaticity coordinates specified shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

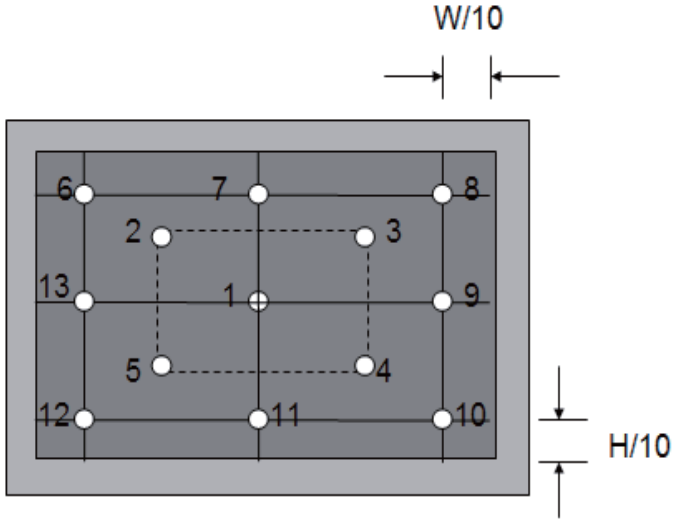
7. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Figure 1. Measurement Set Up



View angel range measurement setup Luminance , uniformity and color measurement setup

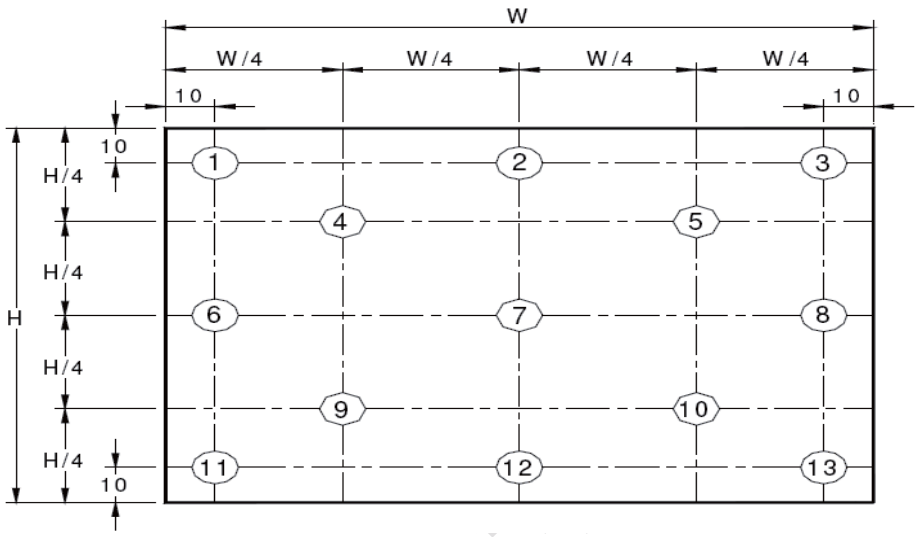
Figure 2. White Luminance and Uniformity Measurement Locations (13 points)



Center Luminance of white is defined as luminance values of center 9 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.

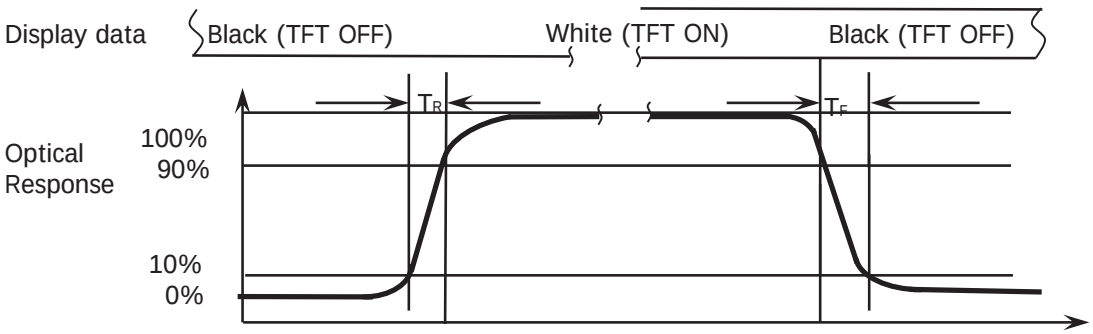
$$\text{Brightness Uniformity} = \frac{\text{Minimum Photo detector output for P1-P13 with all pixels white}}{\text{Maximum Photo detector output for P1-P13 with all pixels white}}$$

Figure 3. Uniformity Measurement Locations (13 points)



The White luminance uniformity on LCD surface is then expressed as : ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see FIGURE 3).
The White luminance uniformity of 5 point is the same test method as 13 point using FIGURE 4.

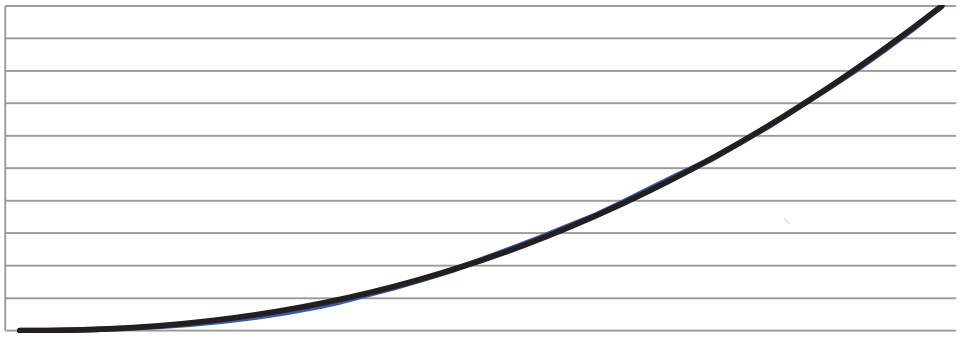
Figure 4. Response Time Testing



The electro-optical response time measurements shall be made as shown in FIGURE 4 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr and 90% to 10% is Td.

5.1. Gamma/Color Coordinate Uniformity

(1) Gamma Curve
Request: R/G/B/W, 0-255 gray scale, step 8 gray scale



(2)Color Coordinate Uniformity
Request: white pattern, 0-255 gray scale, step 8 gray scale.

Gary scale	x	y	Gary scale	x	y
0	0. 2679	0. 264	135	0. 2999	0. 32
7	0. 2766	0. 2752	143	0. 3002	0. 3206
15	0. 292	0. 2988	151	0. 3004	0. 3209
23	0. 2999	0. 3119	159	0. 3008	0. 3215
31	0. 2955	0. 3079	167	0. 3005	0. 3212
39	0. 2934	0. 306	175	0. 3004	0. 3209
47	0. 291	0. 3037	183	0. 3005	0. 3209
55	0. 2911	0. 3046	191	0. 3005	0. 321
63	0. 2923	0. 3068	199	0. 3006	0. 3212
71	0. 2933	0. 3085	207	0. 3008	0. 3213
79	0. 2946	0. 3108	215	0. 301	0. 3214
87	0. 2959	0. 3128	223	0. 3012	0. 3217
95	0. 2973	0. 3153	231	0. 3012	0. 3215
103	0. 2974	0. 3159	239	0. 3012	0. 3213
111	0. 298	0. 3168	247	0. 3009	0. 3208
119	0. 2988	0. 3181	255	0. 3007	0. 3201
127	0. 2997	0. 3198			

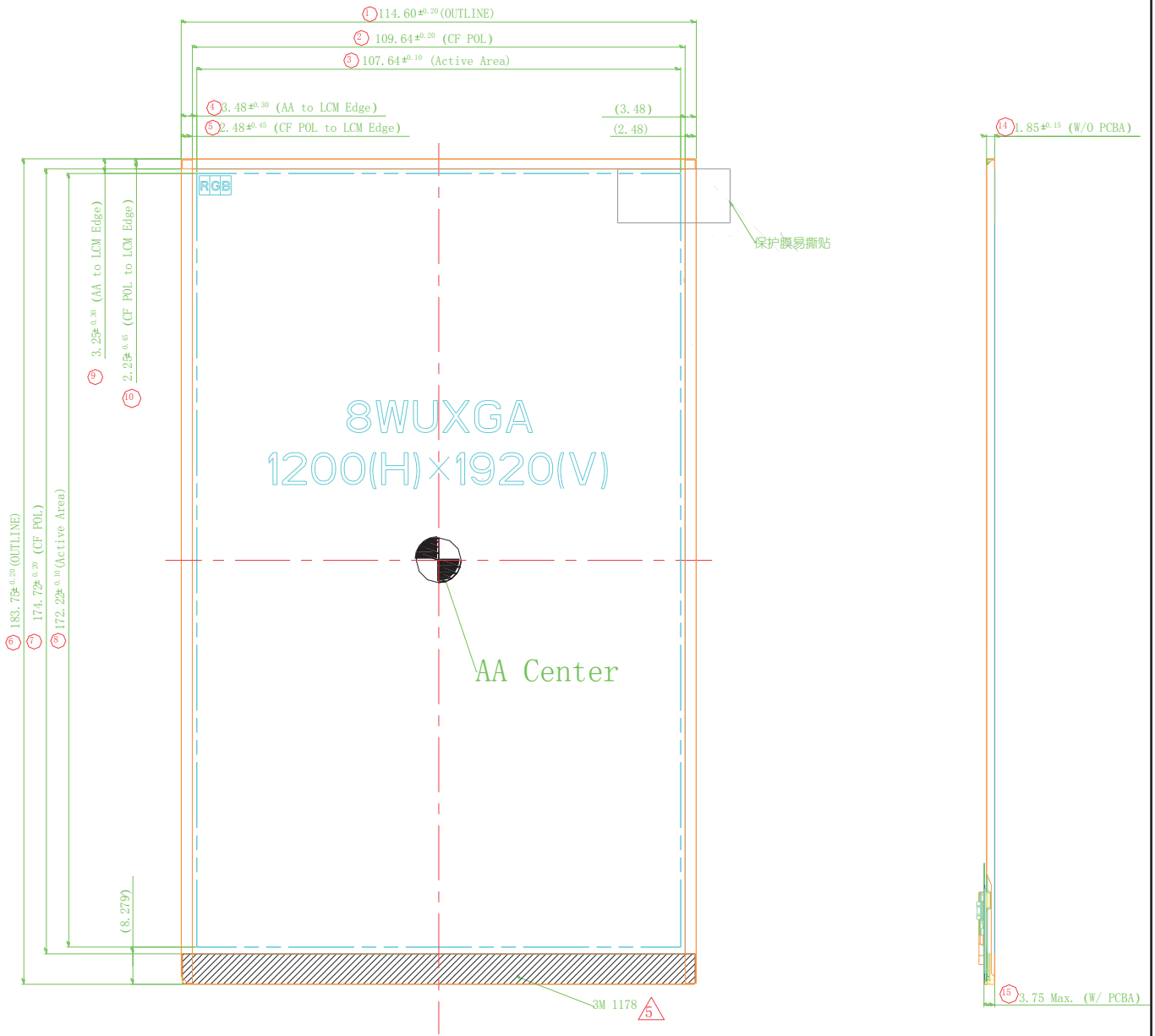
6.0 MECHANICAL CHRACTERISTICS

The contents provide general mechanical characteristics for the model.
In addition the figures in the next page are detailed mechanical drawing of the LCD.

item		Description	Typ.	Tolerance	Unit
Mother glass		Size	1850*1500	-	mm
CF and TFT thickness after slimming		thickness	0.2/ 0.2		mm
Panel	AA	A/A	107.64*172.224	-	mm
	CF	C/F	111.64*176.97	±0.2	mm
	TFT	TFT	111.64*180.274	±0.2	mm
	BM	BM(U/D/L/R)	1.4/6.8 /1.5/1.5	-	mm
	IC Bonding area	IC Bonding Area	3.3	-	mm
	Pol size	Pol Size	CF: 109.64* 174.72	±0.2	mm
	Gap between pol~glass(u/D/L/R)	Gap Between Pol~C/F border (U/D/L/R)	CF: 0.8/1.45/1.0 /1.0	±0.25	mm
Module	Horizontal	Horizontal	114.6	±0.2	mm
	Vertical	Vertical	183.75	±0.2	mm
	Thickness	Thickness	1.85	±0.15	mm
	Uv glue thickness	UV Glue Thick ness	-	-	mm

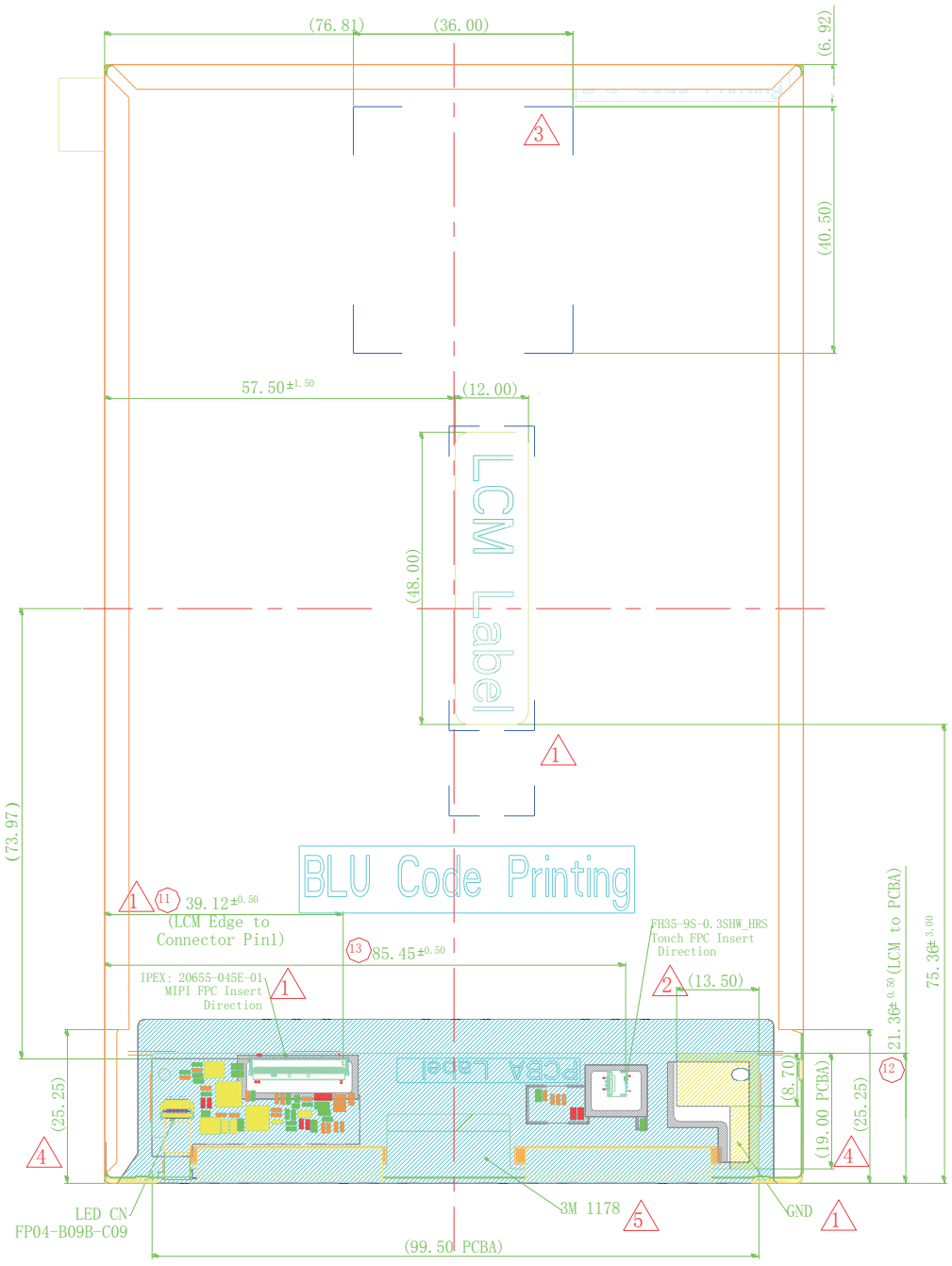
6.1 LCM Display Module Drawing

(1) Front side

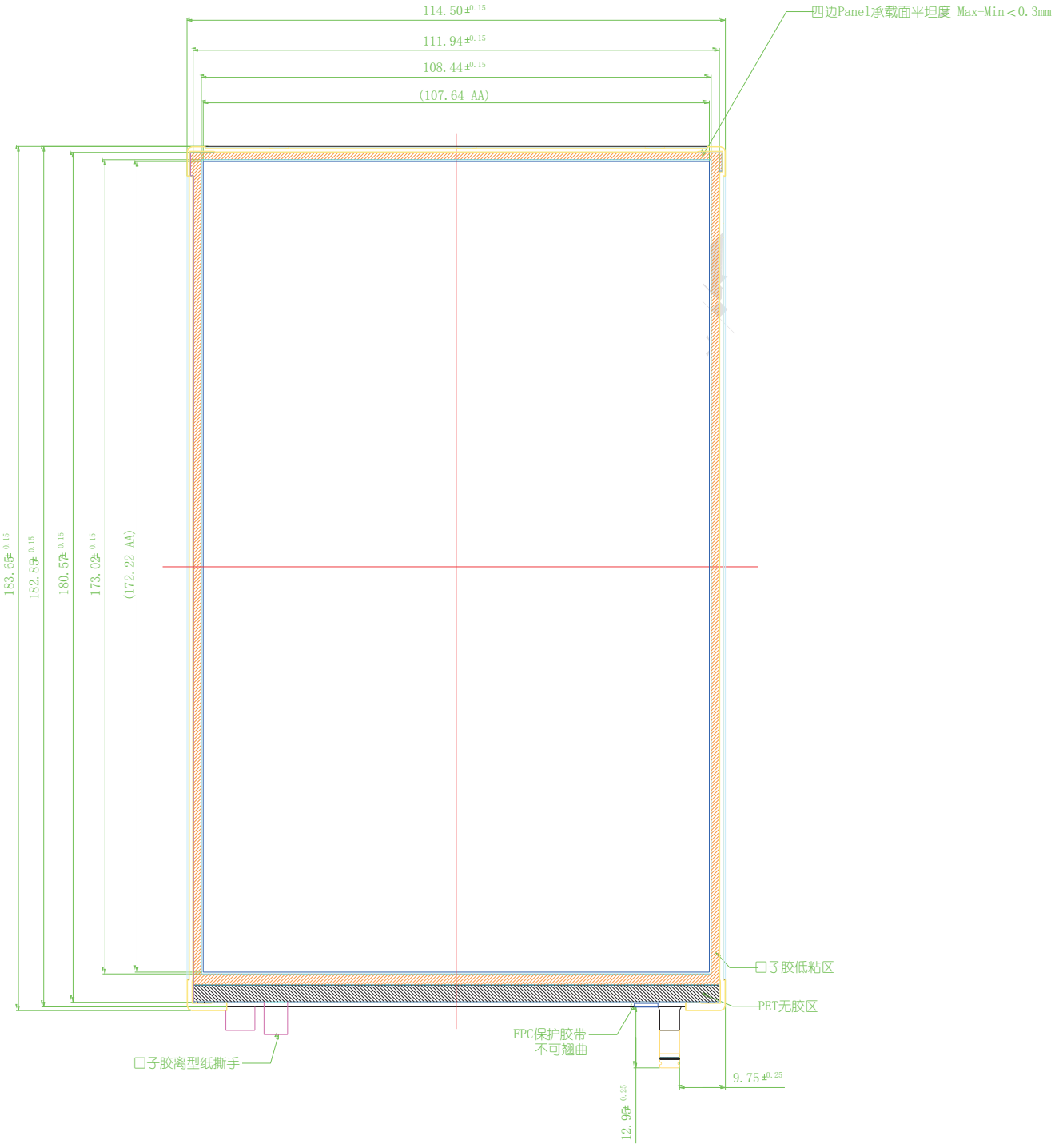


6.1 LCM Display Module Drawing

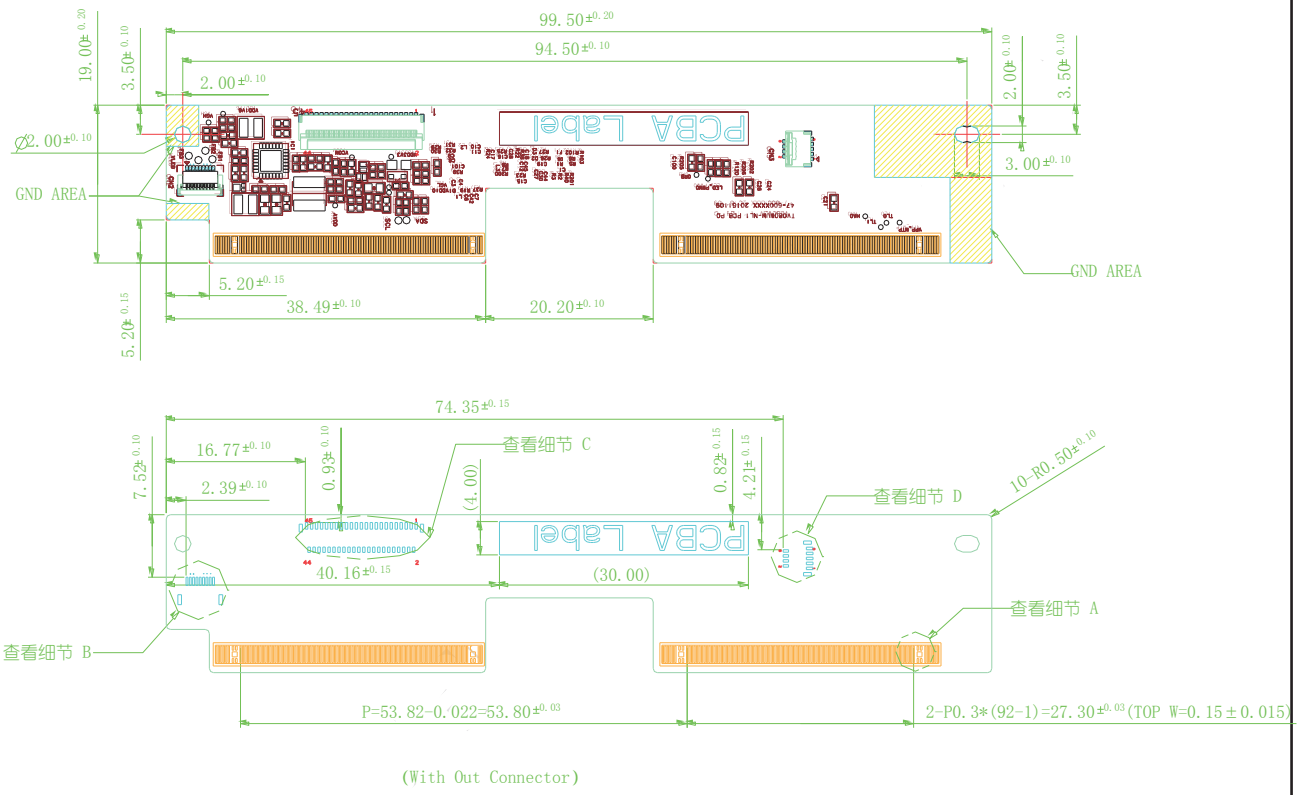
(2) Rear side

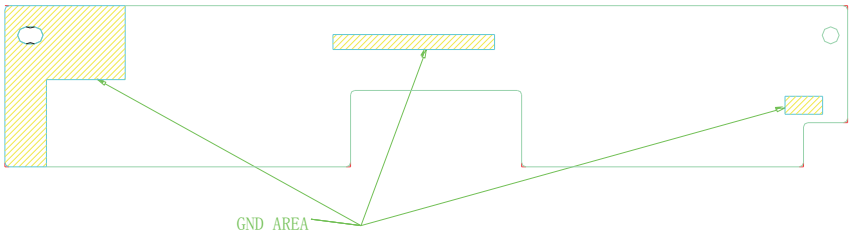


6.2 BLU Outline Dimension



6.3 PCBA Outline Dimension





7.0 Reliability Test

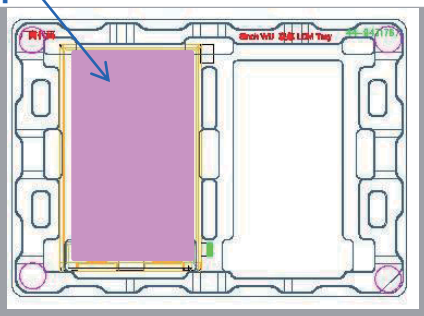
No	Test Item	Test Condition	Remark
1	High temperature storage test	Ta = 80 ℃, 240 hrs	-
2	Low temperature storage test	Ta = -30℃, 240 hrs	
3	Thermal Shock Test	-40℃/1hr → 60℃/1hr ×30Cycle	
4	High temperature Operate test	Ta = 60℃, 240hrs,	
5	Low temperature Operate test	Ta = -20 ℃, 240hrs	
6	High temperature High humidity	Ta = 60 ℃, 90%, 240hrs	

8.0. Package

-. 将 2pcs MDL 平放入Tray

-. 上面放置1pcs EPE Spacer

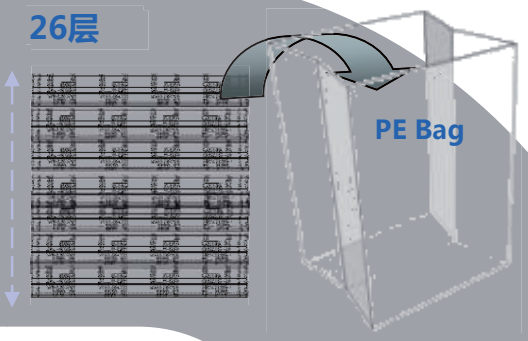
EPE Spacer



-. 将26pcs PET Tray 平放入PE Bag

-. Tray不 旋转码放

-. 顶部1pcs 空Tray



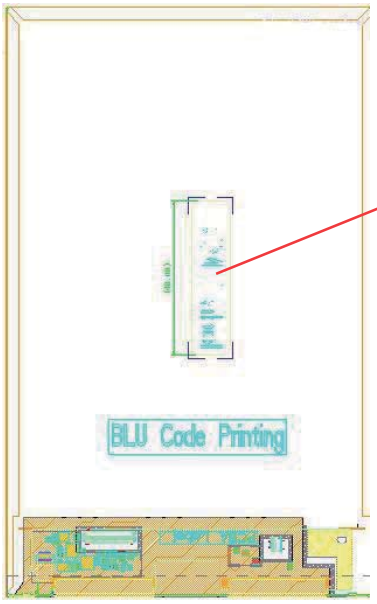
-. 每个Pallet上放3层Box
1层8箱,共计24ea Box

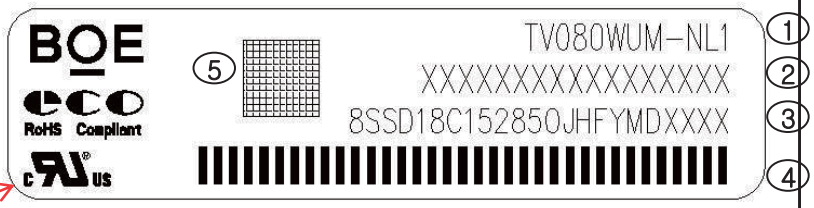
-. Pallet外进行缠膜包装

-. 1200pcs Panel / Pallet

- .将PET Tray堆码后平放入Inner Box
上下放置EPE Cover. 50pcs/Box

8.1 MDL label





Remark:
标签贴覆至背板Mark 内
标签尺寸: 48mm×12mm, 厚度: 0.08mm
1.FG-CODE: TV080WUM-NL1
2.MDL ID,编码规则如下
3.8S码,编码规则如下，料号:SD18C15285
4.MDL ID 对应条纹码
5.8S 码对应二维码

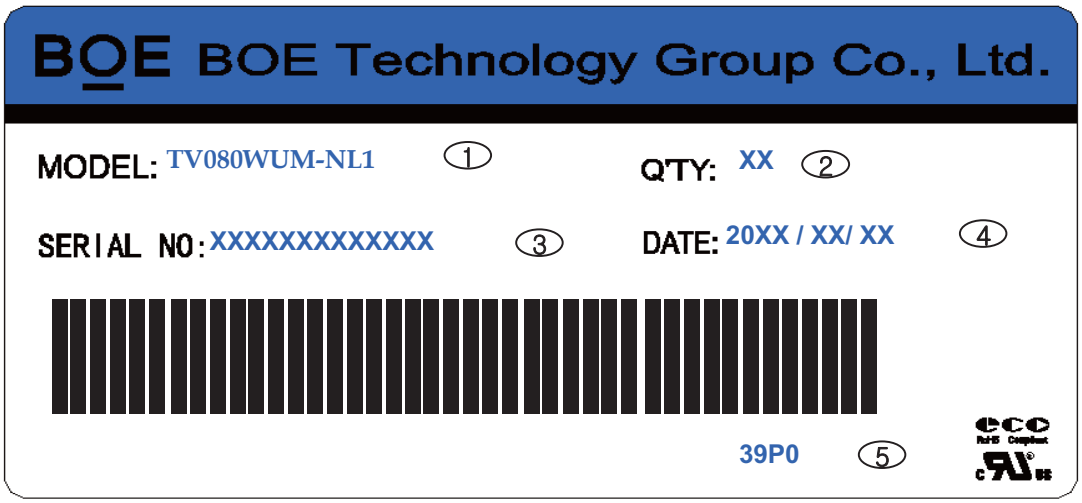
MDL ID 编码规则

序列号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
代码	X	X	P	3	1	2	7	X	X	X	X	0	0	1	E	E	J
描述	GBN代码		等级	B3	年份		月	FG Code后四位				序列号					

8S 编码规则

序列号	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
代码	8	S	S	D	1	8	C	1	5	2	8	5	O	J	H	F	Y	M	D	0	0	0	1
描述	固定值		产品客户端物料号										版本号	B3代码	供应商产地		年月日			序列号			

8.2 BOX label



1. FG-CODE
2. Box 产品数量
3. Box ID, 编码规则如下
4. Box Packing 日期
5. FG-CODE 后四位

Box ID编码规则

序列号	1	2	3	4	5	6	7	8	9	10	11	12	13
代码	X	X	S	3	1	5	B	0	0	0	1	H	D
描述	GBN代码		等级	B3	年份		月	Rev	序列号				

9.0 Handing & Cautions

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.