TECHNICAL DATA

TX38D88VC1GAF

CONTENTS

DESCRIPTION

This specification is applied to the following TFT Liquid Crystal Display Module with Back-light unit.

Note : Inverter device for Back-light is not built in and so it needs to be prepared on your side.

GENERAL SPECIFICATIONS

Type name	: TX38D88VC1GAF
Display Area	: (H)304.128 × (V)228.096 [mm]
Display Pixels (Display Dots)	: (H)1,024 × (V)768 pixels (H(1,024 × 3) × V768 [dots])
Voltage of V_{DD}	: 3.3 V
Pixel Pitch	: (H)0.297 × (V)0.297 [mm]
Color Pixel Arrangement	: R・G・B Vertical Stripe
Display Mode	: Transmissive & Normally White Mode
Color Number	: 262k Colors
Direction with Wider Viewing Angle	: Lower side of 6 o'clock (Azimuth ϕ = 270°)
Dimensions Outlines	: (H)315.8 typ. × (V)241.5 typ. × (t)9.7 max [mm]
Weight	: 800 typ. [g]
Interface	: 1ch-LVDS
Surface Polarizing Film	: Glare Polarizing Film with Antireflection Coating
Back-light	: Two Cold Cathode Fluorescent Lamps (Lower side) Back-light inverter is not contained in Module.

1. ELECTRICAL CHARACTERISTICS

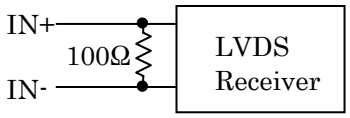
(1) TFT LIQUID CRYSTAL DISPLAY MODULE Ta=25°C, Vss=0V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	Hi	V_{IH}	–	–	+100	mV	1)
	Lo	V_{IL}	-100	–	–		
Power Supply Current		I_{DD}	–	350	500	mA	2), 3)
Vsync Frequency		f_V	–	60	65	Hz	4), 5)
Hsync Frequency		f_H	–	48.5	52.4	kHz	4)
DCLK Frequency		f_{CLK}	62	65	68	MHz	4)

Note 1) VCM=+1.25V

VCM is common mode voltage of LVDS transmitter/receiver.

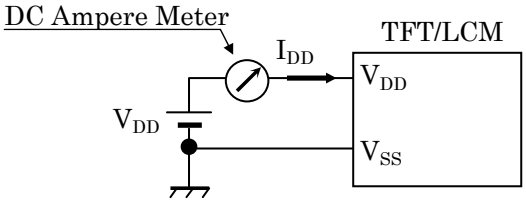
The input terminal of LVDS transmitter is terminated with 100Ω.



2) fv=60Hz, f_{CLK}=65MHz, V_{DD}=3.3V, DC Current.

Typical value is measured when displaying vertical 64 gray scale.

Maximum is measured when displaying Vertical-stripe (Black-Gray 7).



3) As this module contains 0.8A fuse, prepare current source that is enough for cutting current fuse when a trouble happens. (larger than 2.0A.)

4) For LVDS Transmitter Input

5) Vsync Frequency (f_V) (Recommendation): 60Hz

Flicker level will be worse by shift of Vsync Frequency.

(2) BACK-LIGHT UNIT (Per One CCFL) Ta=25°C, GND=0V

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Lamp Current	I_L	2.8	6.0	6.5	mArms	1), 2)
		–	–	10	mA0-peak	
Lamp Voltage	V_L	–	740	–	Vrms	
Frequency	f_L	40	–	70	kHz	3)
Starting Lamp Voltage	V_S	1085	–	–	Vrms	4)
		1310	–	–		4), 5)

Notes 1) The specification shall be applied to each CCFL. The specification is defined at ground line.

2) Higher I_L cause the short life time of CCFL.

3) Lighting frequency for a CCFL may cause the interference with scanning frequency and cause beat or flicker on the display. Therefore, Lighting frequency shall be as different as possible from scanning frequency in order to avoid the interference.

4) Starting Lamp Voltage should be more than V_S (Min.).

5) Ta=0°C

6) Distribution difference of CCFLs surface temperature should be less than 5°C.

7) When the lighting wave form of the inverter is asymmetry, the inclination of mercury is generated. Therefore, please adjust the imbalance factor ($|I_P\text{-}I_{-P}|/I_{rms}\times100$) of the lighting current wave form to 10% or less, and adjust the crest factor (I_P (or I_{-P})/I_{rms}) to 1.2~1.6.

8) The lighting wave form of the inverter is in-phase in a lamp unit.

2. INTERFACE PIN CONNECTION

(1) TFT LIQUID CRYSTAL DISPLAY MODULE

CN1 <<JAE FI-XB30SL-HF10 or Equivalent>>

Pin No.	Symbol	Function	
–	VSS	Ground	
1			
2	VDD	Power Supply 3.3V (typical)	
3			
4	VSS	Ground	
5	VSS	Ground	
6	VSS	Ground	
7	VSS	Ground	
8	ROin0-	LVDS Receiver Signal (-)	(R0 ~ R5, G0)
9	ROin0+	LVDS Receiver Signal (+)	(R0 ~ R5, G0)
10	VSS	Ground	
11	ROin1-	LVDS Receiver Signal (-)	(G1 ~ G5, B0 ~ B1)
12	ROin1+	LVDS Receiver Signal (+)	(G1 ~ G5, B0 ~ B1)
13	VSS	Ground	
14	ROin2-	LVDS Receiver Signal (-)	(B2 ~ B5, HS, VS, DE)
15	ROin2+	LVDS Receiver Signal (+)	(B2 ~ B5, HS, VS, DE)
16	VSS	Ground	
17	CLKO-	LVDS Clock Signal(-)	
18	CLKO+	LVDS Clock Signal(+)	
19	VSS	Ground	
20	REin0-	NC	
21	REin0+	NC	
22	VSS	Ground	
23	REin1-	NC	
24	REin1+	NC	
25	VSS	Ground	
26	REin2-	NC	
27	REin2+	NC	
28	VSS	Ground	
29	CLKE-	NC	
30	CLKE+	NC	
–	VSS	Ground	

Note 1) All VSS pins should be connected to GND (0V).
Metal bezel is connected internally to VSS.

2) All VDD pins should be connected to +3.3V.

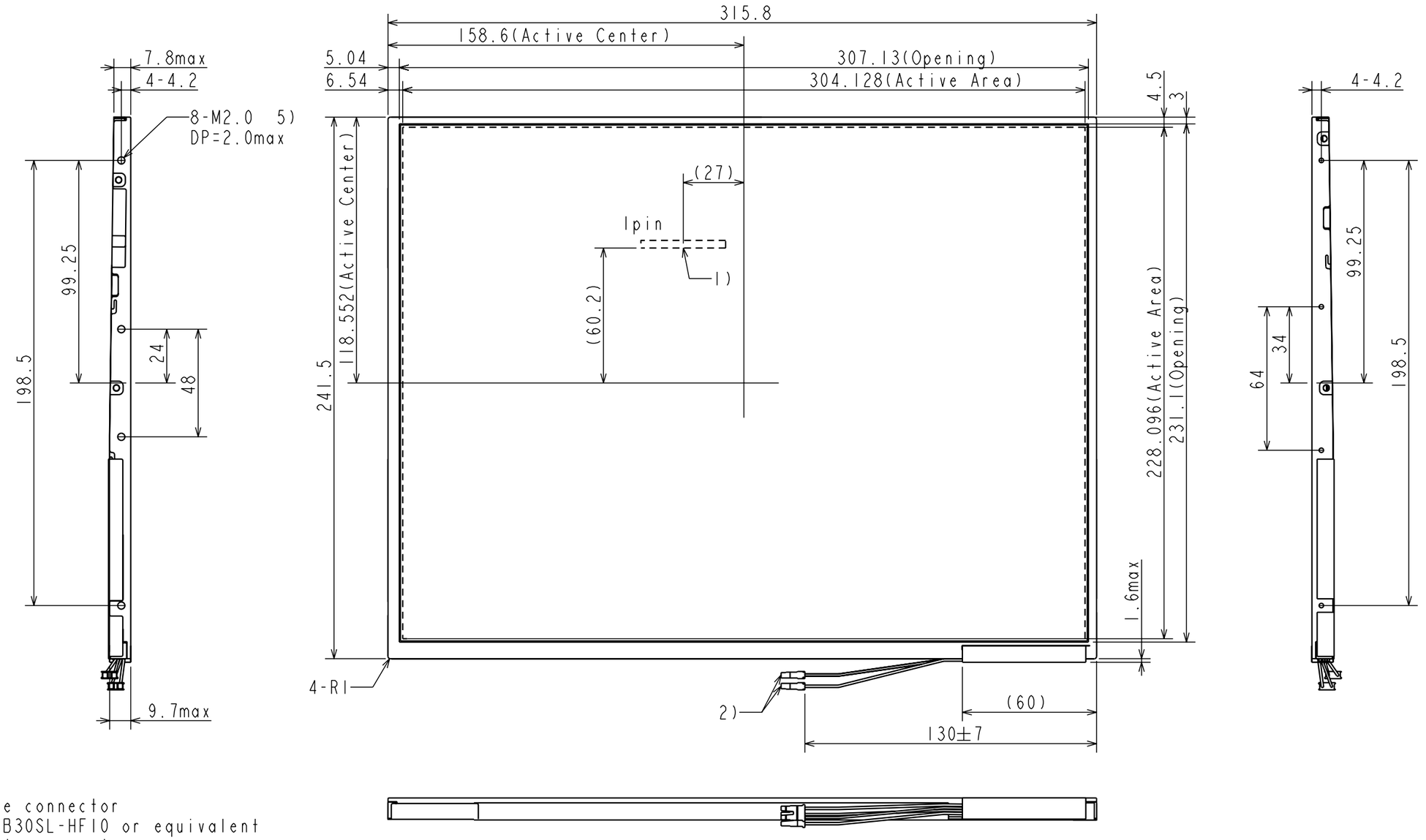
3) All NC pins should be kept Open.

(2) BACK-LIGHT UNIT

CN2, CN3 <<JST BHSR-02VS-1 or Equivalent>>

Pin No.	Symbol	DESCRIPTION	Reference
1	VL	Power Supply	
2	GND	GND (0V)	

3. DIMENSIONAL OUTLINE



Note
1)Interface connector
JAE:FI-XB30SL-HF10 or equivalent
2)CCFL cable connector
JST:BHSR-02VS-1 or equivalent
Connector pin for panel side CCFL:Hot cable (Pink)
Connector pin for back side CCFL:Hot cable (Blue)
3)The unspecified tolerance:±0.5
4)Hole in mounting panel:8 holes
5)Maximum torque for the screw in mounting panel:0.196N·m(2.0kgf·cm)

UNIT:mm