HITACHI

Hitachi Displays, Ltd.

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TECHNICAL DATA

TX80D12VC0CAB

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RECORD OF REVISION

Date	The upper section : Before revision The lower section : After revision Sheet No.	Page	Summary

DESCRIPTION

The following specifications are applied to the following Super-TFT module.

Note : Inverter for back light unit is not built in this module.

Product Name : TX80D12VC0CAB

General Specifications

Effective Display Area	: (H)687.36×(V)412.42	(mm)
Number of Pixels	: (H)1,280×(V)768	(pixels)
Pixel Pitch	: (H)0.537×(V)0.537	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Anti-Glare	
Number of Colors	: 16,777,216	(colors)
Viewing Angle Range	: Super Wide Version (Horizontal & Vertical : 170°, CR≧10)	
Input Signal	: 1-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: 16 pcs. of CCFL	
External Dimensions	: (H)764.0×(V)465.0×(t)38.0	(mm)
Weight	: 8,000g typ.	

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	℃	1),5)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	9.8 (1G)	m/s 2	3)
Shock	-	29.4(3G)	-	196 (20G)	m/s 2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	lx	

Note 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 70 ℃ on the condition of operating.
The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2) Ta≦40 ℃ · · · · · · Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta> 40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85%RH at 40 ℃.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.

5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.
However, it does not affect the characteristics and reliability of the product.

1.2 Electrical Absolute Maximum Ratings

(1)Super-TFT Module

Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	13.2	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.
2)Discharge Coefficient：200pF-250Ω, Environmental：25℃-70%RH
3)It is applied to I/F connector pins.
4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light

GND = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Current	IL	-	7.0	mArms	1)
Input Voltage	VL	-	2,000	Vrms	2)

Note 1)The specification shall be applied to each CFL. The specification is defined at ground line.
2)The specification shall be applied at connector pins for a CFL at start-up.

2. OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

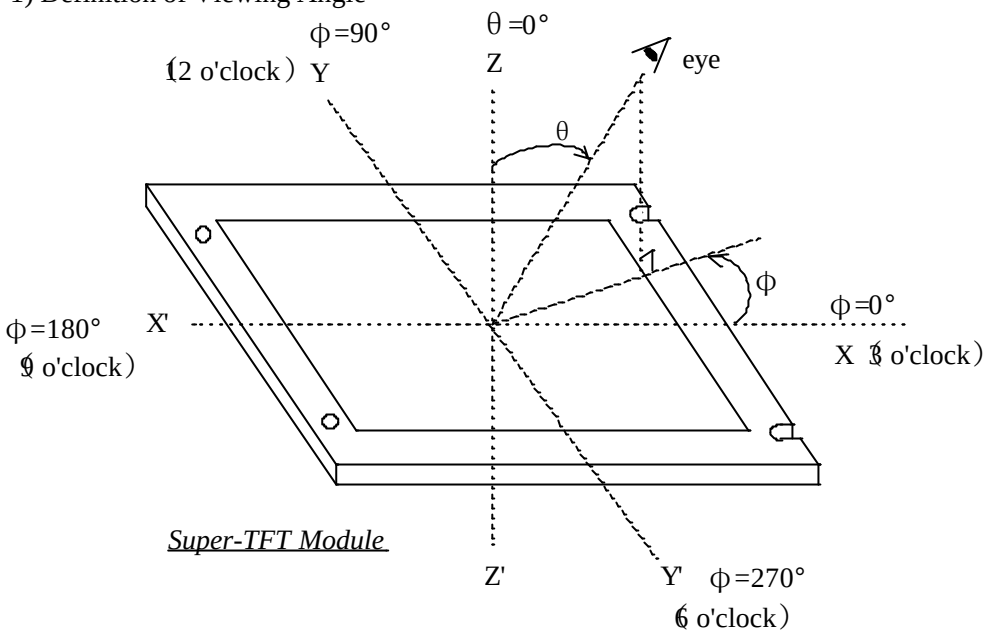
Measuring equipment :Pritchard 1980A, or equivalent

Temperature =25℃、VDD=12.0V、f V=60Hz、

IL=5.0mA (average of 16 pieces of CFLs, PWM:Duty 100%) , CTL = Low

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR		350	500	-	-	2)
Response Time	Rise	ton		-	15	30	ms	3) , CTL:High
	Fall	toff		-	15	30	ms	3) , CTL:High
Brightness of white		Bwh		350	500	-	cd/m 2	CTL:High
				300	450	-	cd/m	CTL:Low
Brightness uniformity		Buni		-	-	30	%	4)
Color Chromaticity (CIE)	Red	χ	θ＝0° 1)	0.61	0.64	0.67	-	[Gray scale =255]
		y		0.29	0.32	0.35		
	Green	χ		0.26	0.29	0.32		
		y		0.58	0.61	0.64		
	Blue	χ		0.12	0.15	0.18		
		y		0.04	0.07	0.10		
	White	χ		0.245	0.275	0.305		
		y		0.252	0.282	0.312		
Variation of Color Position (CIE)	Red	Δ χ	θ = +50° φ = 0°,90° 180°,270° 1)	-	-	0.04	-	5) [Gray scale =255]
		Δ y		-	-	0.04		
	Green	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
	Blue	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
	White	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
Contrast Ratio at 85°		CR85°		10	-	-	-	Estimated value.

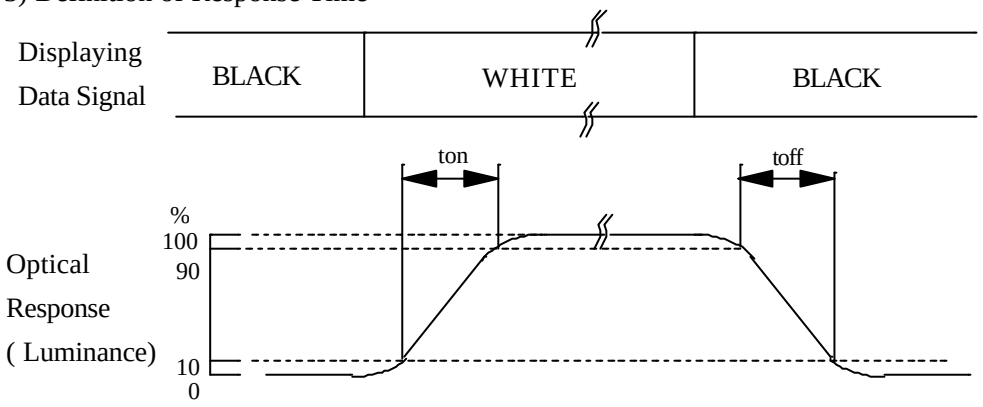
Note 1) Definition of Viewing Angle



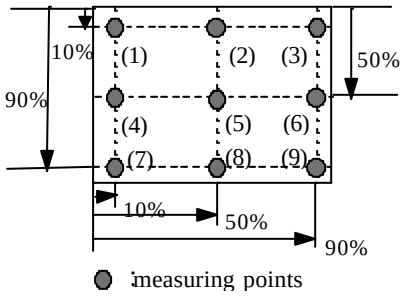
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



Display pattern is white (255 level) . The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \frac{\lceil Bmax \text{ or } Bmin - Bave \rceil}{Bave} \times 100$$

where, Bmax = Maximum brightness

Bmin = Minimum brightness

$$Bave = \text{Average brightness} = \frac{\sum_{k=1}^{9} (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at θ =0 ° and at θ = 50°& ϕ=0°,90°,180°,270°.

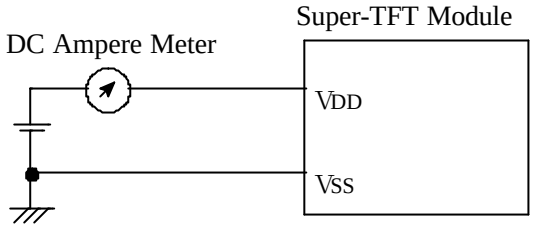
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD Module

Ta=25℃, Vss=0V

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VDD	11.4	12.0	12.6	V	
Power Supply Current	IDD	—	0.59	0.80	A	1),2)
Ripple Voltage of Power Supply	VDDR	—	—	0.15	V	

Note 1) DC current at fv=60.0Hz, fCLK=82MHz, VDD=12.0V and Display pattern is white.



2) Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of power supply.

3.2 Back Light

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Input Current	IL	3.0	5.0	6.0	mArms	1)
Input Voltage	VL	-	1290	-	Vrms	
Frequency	f0	50	55	60	kHz	2)
Kick-Off Voltage	Vs	-	-	1,600	V	3)

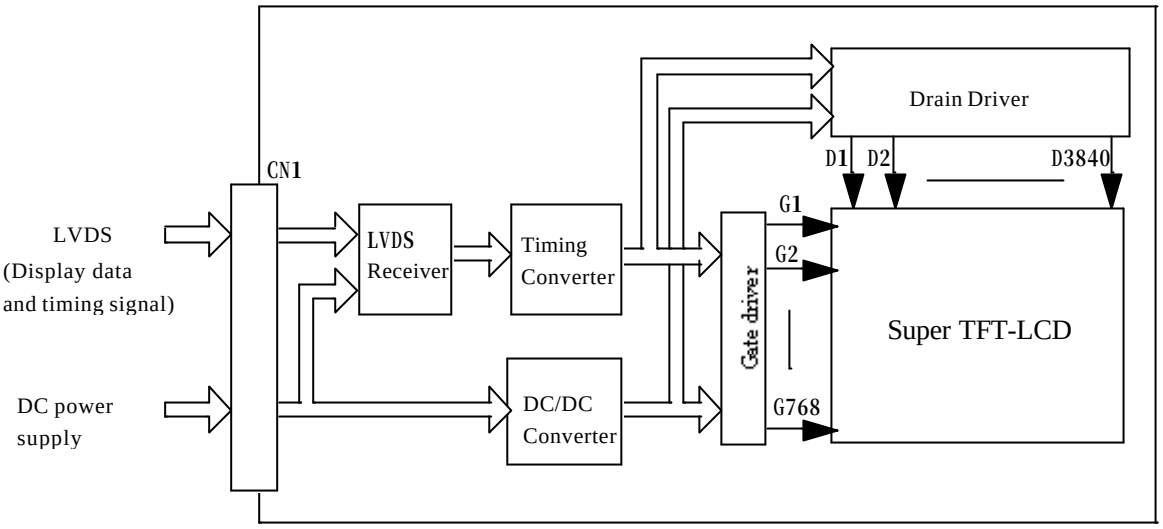
Notes 1) The specification shall be applied to each CFL. The specification is defined at ground line.

2) Frequency of power supply for a CFL may cause the interference with HSYNC frequency and cause beat or flicker on the display. Therefore, lamp frequency shall be as different as possible from HSYNC frequency in order to avoid the interference.

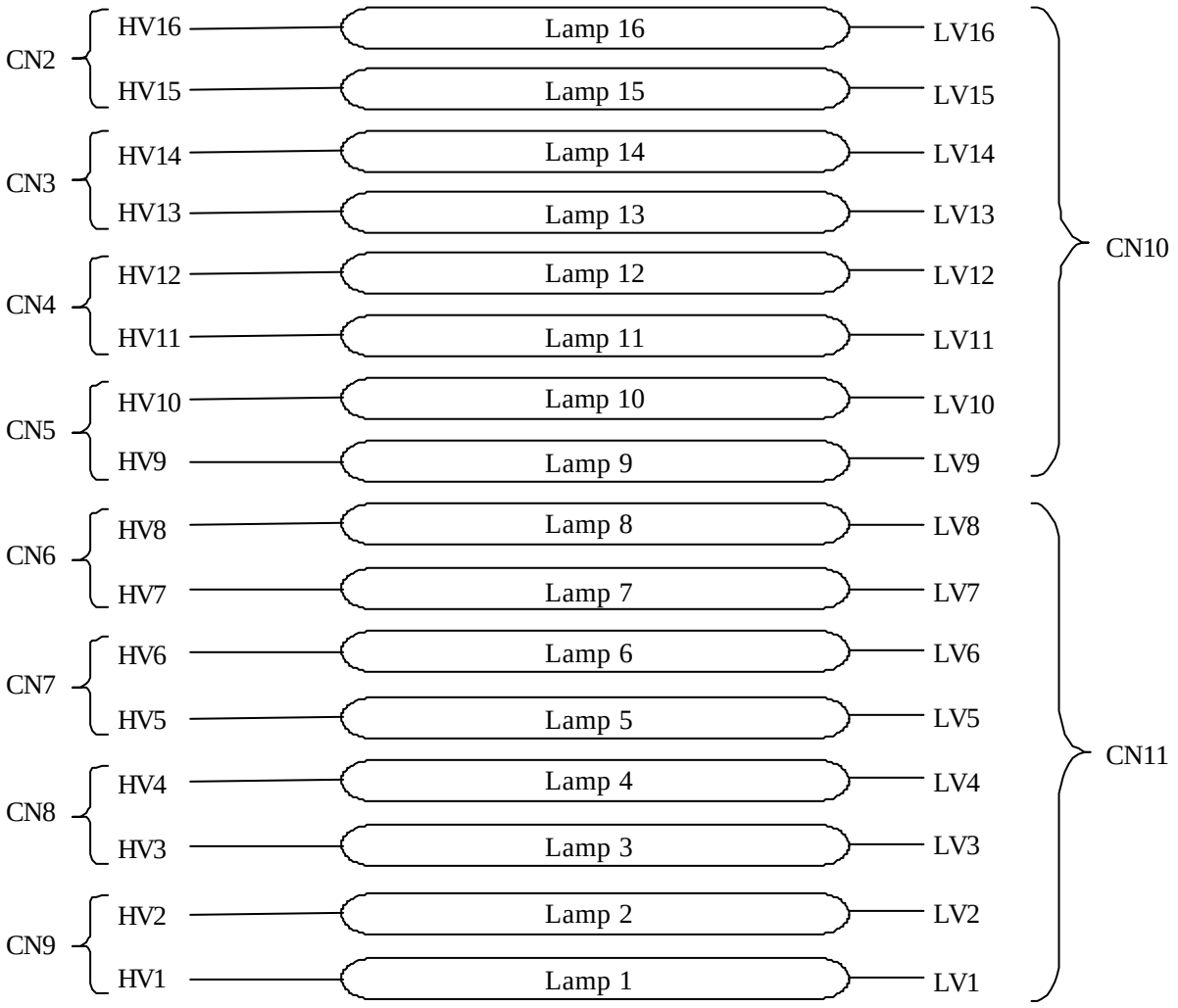
3) Ta = 0 degree

4. BLOCK DIAGRAM

(1) Super-TFT Module



(2) Back light unit



5. INTERFACE PIN ASSIGNMENT

5. 1 TFT-LCD MODULE

CN1 : JAE FI-SEB20P-HF13

(Matching connector : JAE FI-SE20M or equivalent)

Pin No.	Symbol	Description	Note
1	VDD	Power Supply (typ.+12V)	1)
2	VDD		
3	VSS	GND (0V)	2)
4	VSS		
5	Rx0-	Pixel Data	3)
6	Rx0+		
7	VSS	GND (0V)	2)
8	Rx1-	Pixel Data	3)
9	Rx1+		
10	VSS	GND (0V)	2)
11	Rx2-	Pixel Data	3)
12	Rx2+		
13	VSS	GND (0V)	2)
14	CLK-	Pixel Clock	3)
15	CLK+		
16	VSS	GND (0V)	2)
17	Rx3-	Pixel Data	3)
18	Rx3+		
19	VSS	GND (0V)	2)
20	CTL	Low:A line trace ON , High:A line trace OFF	4)

Notes 1) All VDD pins shall be connected to +12.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

3) Rx n+ and Rx n- (n=1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

4) Low level : 0～0.15V, High level : 2.5～5.0V

5. 2 BACK-LIGHT UNIT

CN2,CN3,CN4,CN5,CN6,CN7,CN8,CN9 : JST BHR-03VS-1

(Matching connector : JST SM02 (0.8) B-BHS-1-TB or equivalent)

Pin No.	SYMBOL	Function
1	HV-2(n-10)	Power Supply for Lamp Even side(High Voltage)
2	NC	
3	HV-2(n-10)-1	Power Supply for Lamp Odd side(High Voltage)

Note 1) n=CN Number

CN10,CN11 : JST ZHR-8

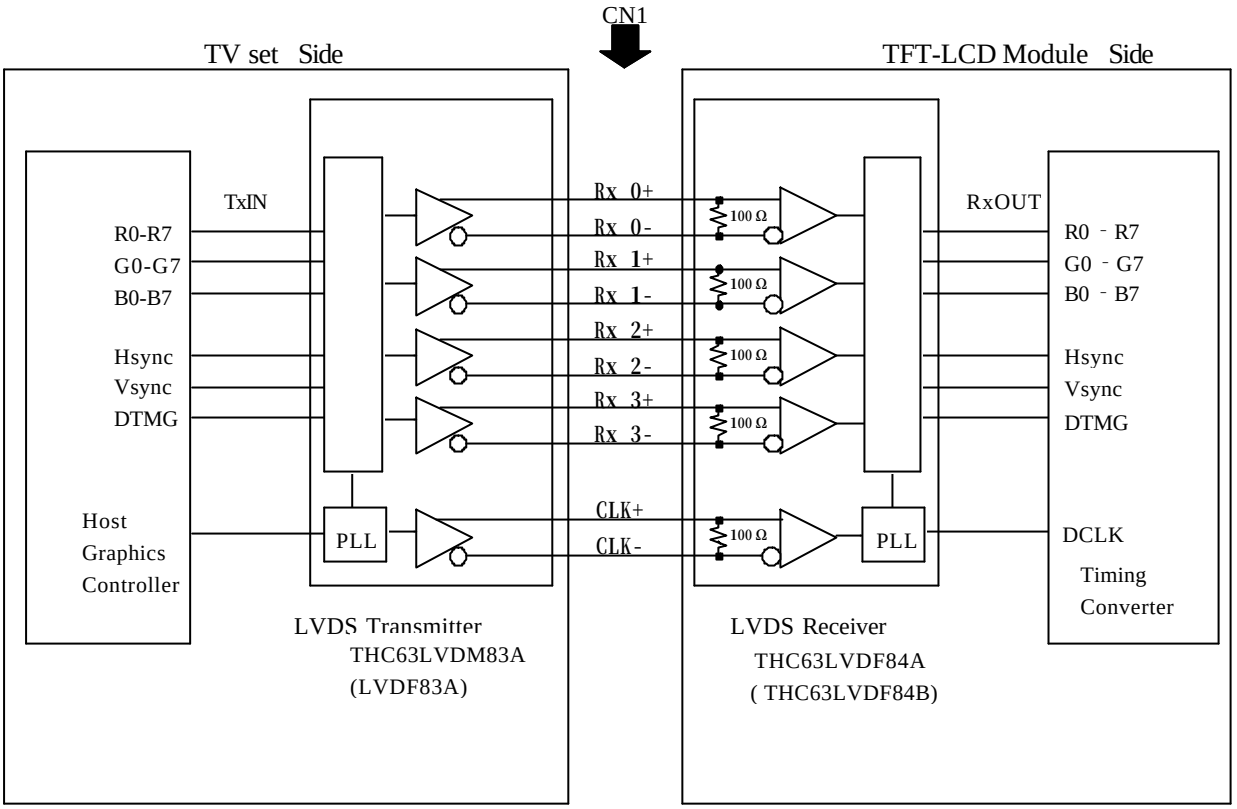
CN11

Pin No.	SYMBOL	FUNCTION
1	LV1	Lamp1 LV
2	LV2	Lamp2 LV
3	LV3	Lamp3 LV
4	LV4	Lamp4 LV
5	LV5	Lamp5 LV
6	LV6	Lamp6 LV
7	LV7	Lamp7 LV
8	LV8	Lamp8 LV

CN10

Pin No.	SYMBOL	FUNCTION
1	LV9	Lamp9 LV
2	LV10	Lamp10 LV
3	LV11	Lamp11 LV
4	LV12	Lamp12 LV
5	LV13	Lamp13 LV
6	LV14	Lamp14 LV
7	LV15	Lamp15 LV
8	LV16	Lamp16 LV

BLOCK DIAGRAM OF INTERFACE



R0～R7	: Pixel R Data
G0～G7	: Pixel G Data
B0～B7	: Pixel B Data
HSYNC	: Horizontal synchronization signal
VSYNC	: Vertical synchronization signal
DTMG	: Display timing signal

Notes 1) The system must have the transmitter to drive the module.
2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

LVDS INTERFACE

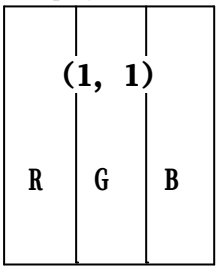
	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL
		PIN	INPUT	PC	TFT-LCD	PIN	OUTPUT	INPUT
24bit	R2	51	Tx IN0			27	Rx OUT0	R2
	R3	52	Tx IN1			29	Rx OUT1	R3
	R4	54	Tx IN2	TA OUT0+	Rx 0+	30	Rx OUT2	R4
	R5	55	Tx IN3			32	Rx OUT3	R5
	R6	56	Tx IN4			33	Rx OUT4	R6
	R7	3	Tx IN6	TA OUT0-	Rx 0-	35	Rx OUT6	R7
	G2	4	Tx IN7			37	Rx OUT7	G2
	G3	6	Tx IN8			38	Rx OUT8	G3
	G4	7	Tx IN9			39	Rx OUT9	G4
	G5	11	Tx IN12	TA OUT1+	Rx 1+	43	Rx OUT12	G5
	G6	12	Tx IN13			45	Rx OUT13	G6
	G7	14	Tx IN14			46	Rx OUT14	G7
	B2	15	Tx IN15	TA OUT1-	Rx 1-	47	Rx OUT15	B2
	B3	19	Tx IN18			51	Rx OUT18	B3
	B4	20	Tx IN19			53	Rx OUT19	B4
	B5	22	Tx IN20			54	Rx OUT20	B5
	B6	23	Tx IN21	TA OUT2+	Rx 2+	55	Rx OUT21	B6
	B7	24	Tx IN22			1	Rx OUT22	B7
	HSYNC	27	Tx IN24			3	Rx OUT24	HSYNC
	VSYNC	28	Tx IN25	TA OUT2-	Rx 2-	5	Rx OUT25	VSYNC
	DTMG	30	Tx IN26			6	Rx OUT26	DTMG
	R0	50	Tx IN27			7	Rx OUT27	R0
	R1	2	Tx IN5			34	Rx OUT5	R1
	G0	8	Tx IN10	TA OUT3+	Rx 3+	41	Rx OUT10	G0
	G1	10	Tx IN11			42	Rx OUT11	G1
	B0	16	Tx IN16			49	Rx OUT16	B0
	B1	18	Tx IN17	TA OUT3-	Rx 3-	50	Rx OUT17	B1
	RSVD 1)	25	Tx IN23			2	Rx OUT23	not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0～R7 : Pixel R Data (7 ; MSB, 0 ; LSB)
G0～G7 : Pixel G Data (7 ; MSB, 0 ; LSB)
B0～B7 : Pixel B Data (7 ; MSB, 0 ; LSB)
HSYNC : Horizontal synchronization signal
VSYNC : Vertical synchronization signal
DTMG : Display timing signal

Notes 1) RSVD(reserved) pins on the transmitter shall be "H" or "L".

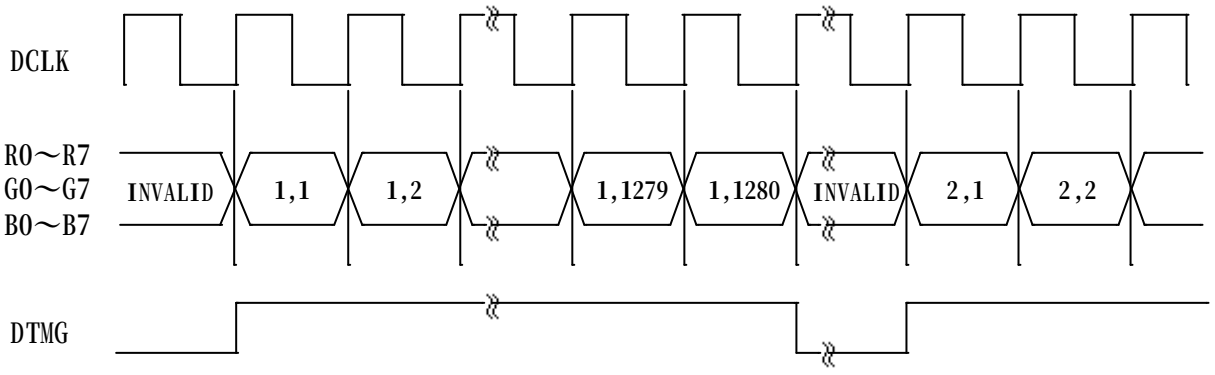
CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent one pixel is latched during one cycle of DCLK.



pixel : R0～R7 :R data
G0～G7 :G data
B0～B7 :B data

1,1	1,2	1,3	———	1,1280
2,1	2,2	2,3	———	2,1280
3,1	3,2	3,3	———	3,1280
768,1	768,2	768,3	———	768,1280



RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color	Input	Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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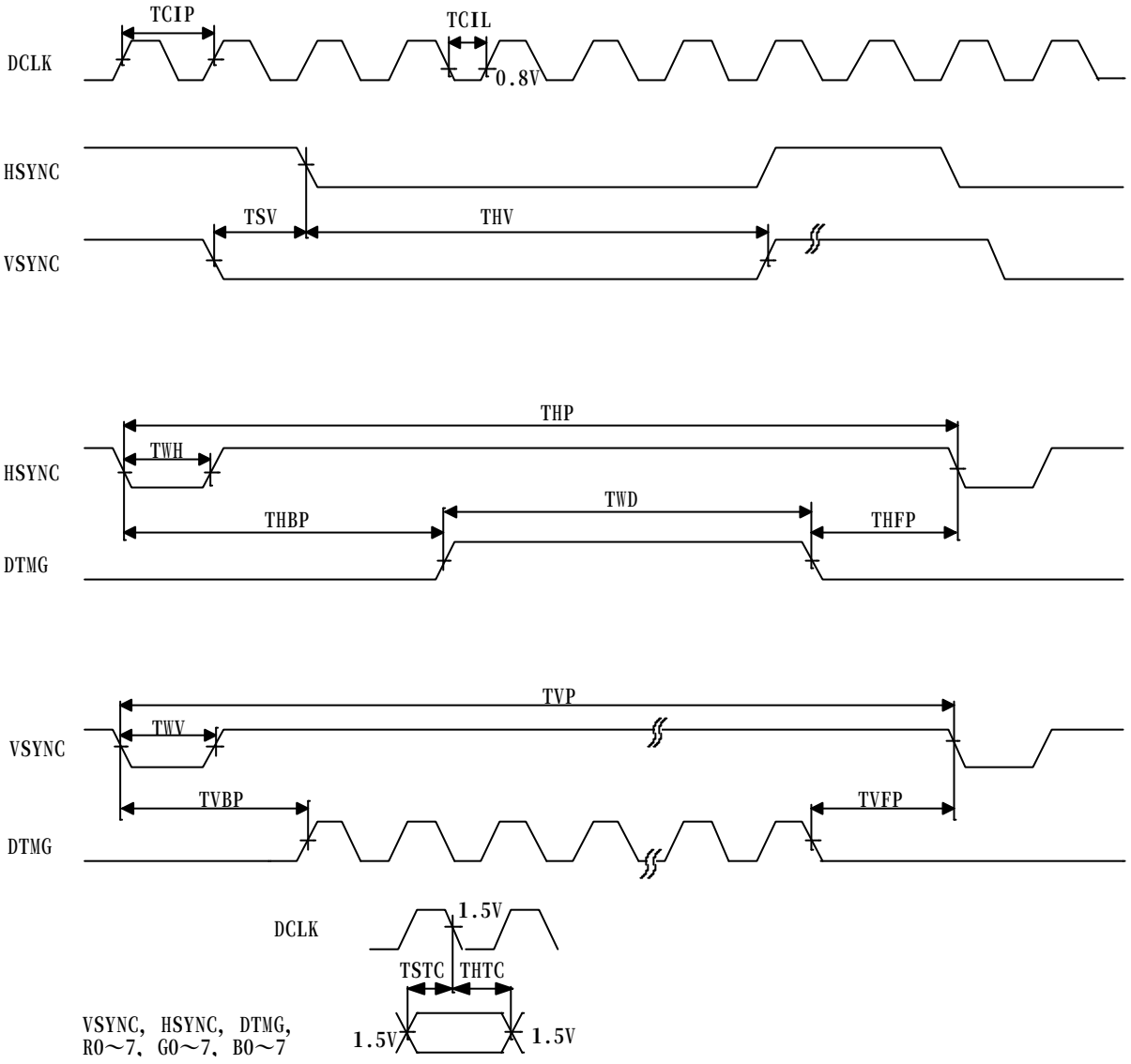
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes 1) Definition of gray scale:
Color(n) • • • • Number in parenthesis indicates gray scale level. Larger n corresponds to brighter level.

2) Data: 1:High, 0:Low

6. INTERFACE TIMING

6.1 TIMING CHART



Notes 1) Reference level for each timing signal is 1.5V unless it is stated on the chart , high level voltage(VIH) and low level voltage(VIL) are defined as follows:

$V_{IH} \geqq 2.0\ V$ $V_{IL} \leqq 0.8\ V$

The above definition conforms to the specifications of LVDS transmitter (THC63LVDM83A / by THine Microsystems, Inc.).

2) The timing of DCLK to other signals conforms to the specifications of LVDS transmitter.

3) HSYNC, VSYNC timing is specified in negative polarity.

4) HSYNC pulse is needed while data is invalid (blanking period).

6.2 INTERFACE TIMING SPECIFICATIONS

6.2.1 CTL=Low

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	fCLK	73.7	82	82.6	MHz	
	Duty	D	0.35	0.5	0.65	-	D=TCIL/TCIP
HSYNC	Frequency	fH	44.8	49.7	53.6	kHz	
	Period	THP	1646	-	1708	TCIP	
	Width-Active	TWH	8	-	240	TCIP	
VSYNC	Frequency	fV	58	60	62	Hz	4)
	Set up Time	TSV	0	-	-	TCIP	to HSYNC
	Hold Time	THV	8	-	-	TCIP	
	Period	TVP	772	-	900	THP	
	Width-Active	TWV	1	-	120	THP	
DTMG	Horizontal Back porch	THBP	16	-	-	TCIP	
	Horizontal Front Porch	THFP	0	-	-	TCIP	
	Vertical Back Porch	TVBP	2	-	1)	THP	
	Vertical Front porch	TVFP	2	-	1)	THP	
	Width-Active	TWD	1280	1280	1280	TCIP	
COMMON	Set up Time	TSTC	5	-	2)	ns	
	Hold Time	THTC	3	-	2)	ns	

6.2.2 CTL=High

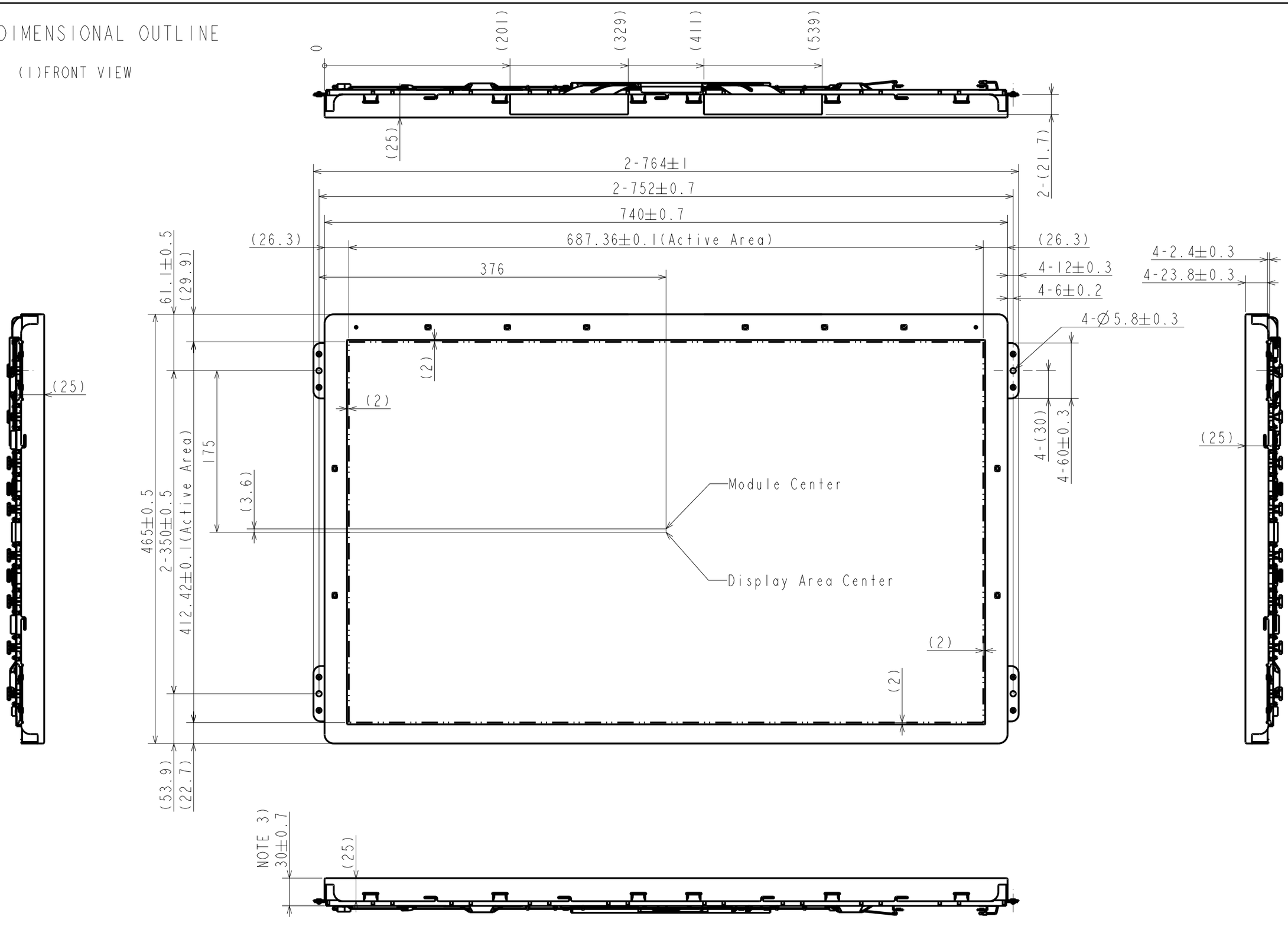
Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	fCLK	73.7	82	82.6	MHz	
	Duty	D	0.35	0.5	0.65	-	D=TCIL/TCIP
HSYNC	Frequency	fH	41	49.7	53.6	kHz	
	Period	THP	1646	-	2000	TCIP	
	Width-Active	TWH	8	-	240	TCIP	
VSYNC	Frequency	fV	48	60	62	Hz	4)
	Set up Time	TSV	0	-	-	TCIP	to HSYNC
	Hold Time	THV	8	-	-	TCIP	
	Period	TVP	772	-	900	THP	
	Width-Active	TWV	1	-	120	THP	
DTMG	Horizontal Back porch	THBP	16	-	-	TCIP	
	Horizontal Front Porch	THFP	0	-	-	TCIP	
	Vertical Back Porch	TVBP	2	-	1)	THP	
	Vertical Front porch	TVFP	2	-	1)	THP	
	Width-Active	TWD	1280	1280	1280	TCIP	
COMMON	Set up Time	TSTC	5	-	2)	ns	
	Hold Time	THTC	3	-	2)	ns	

In addition to the above, these timing should conforms to the followings.

1) TVBP+TVFP≧4 THP
2) TSTC and THTC conforms to the specifications of LVDS transmitter.
   It is preferable to check the specifications of LVDS transmitter in your system.
3) TVP fluctuation should be kept within ±1 line.
4) A line trace function does not allowed in PAL.

7. DIMENSIONAL OUTLINE

(1)FRONT VIEW



NOTE 1)Dimensions in parentheses are referense value.
2)Tolerance not specified is ±0.8mm.
3)Measure the values with 9.8×10^4Pa(1.0kgf/cm^2).

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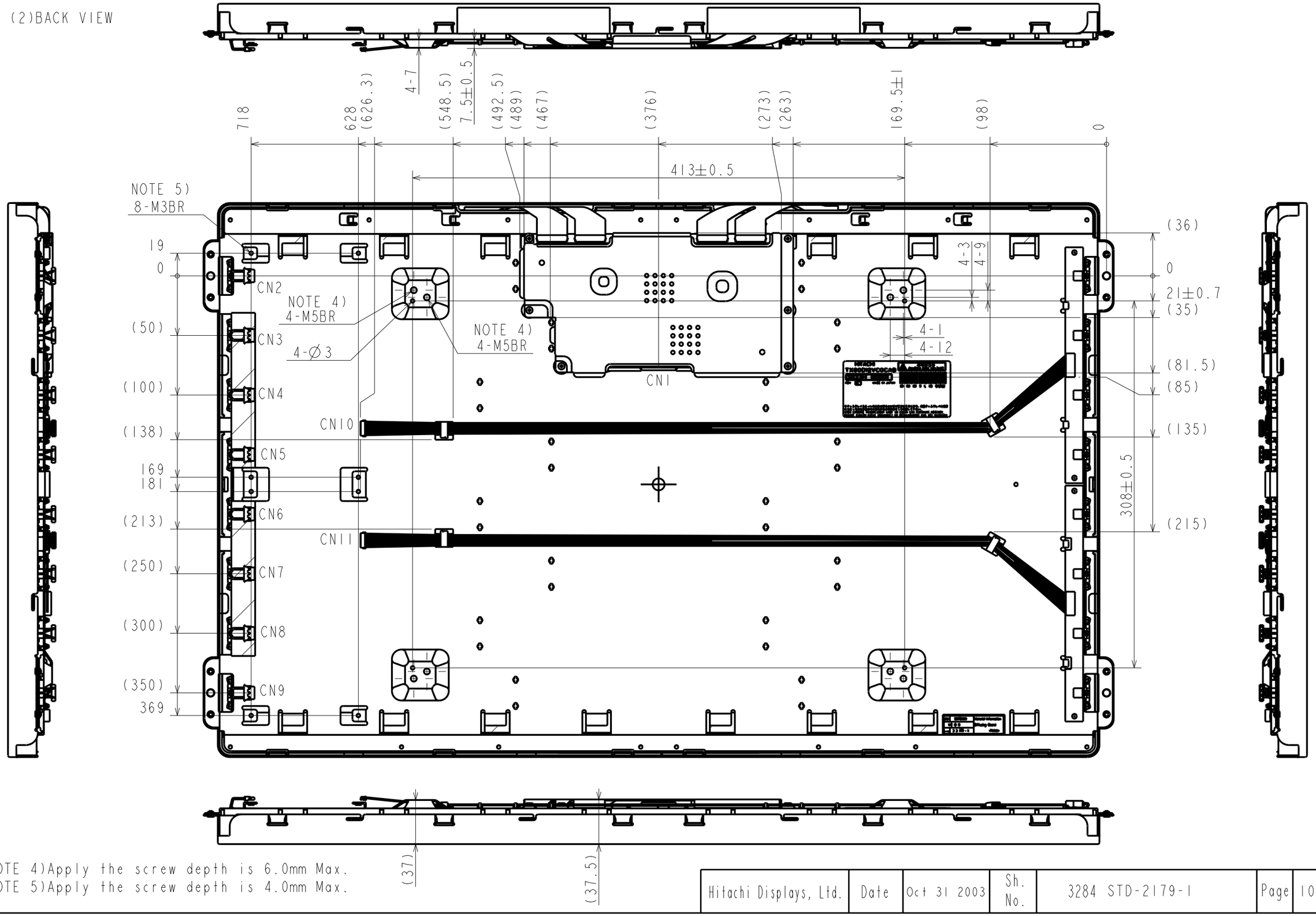
(2)BACK VIEW



NOTE 4)Apply the screw depth is 6.0mm Max.
NOTE 5)Apply the screw depth is 4.0mm Max.

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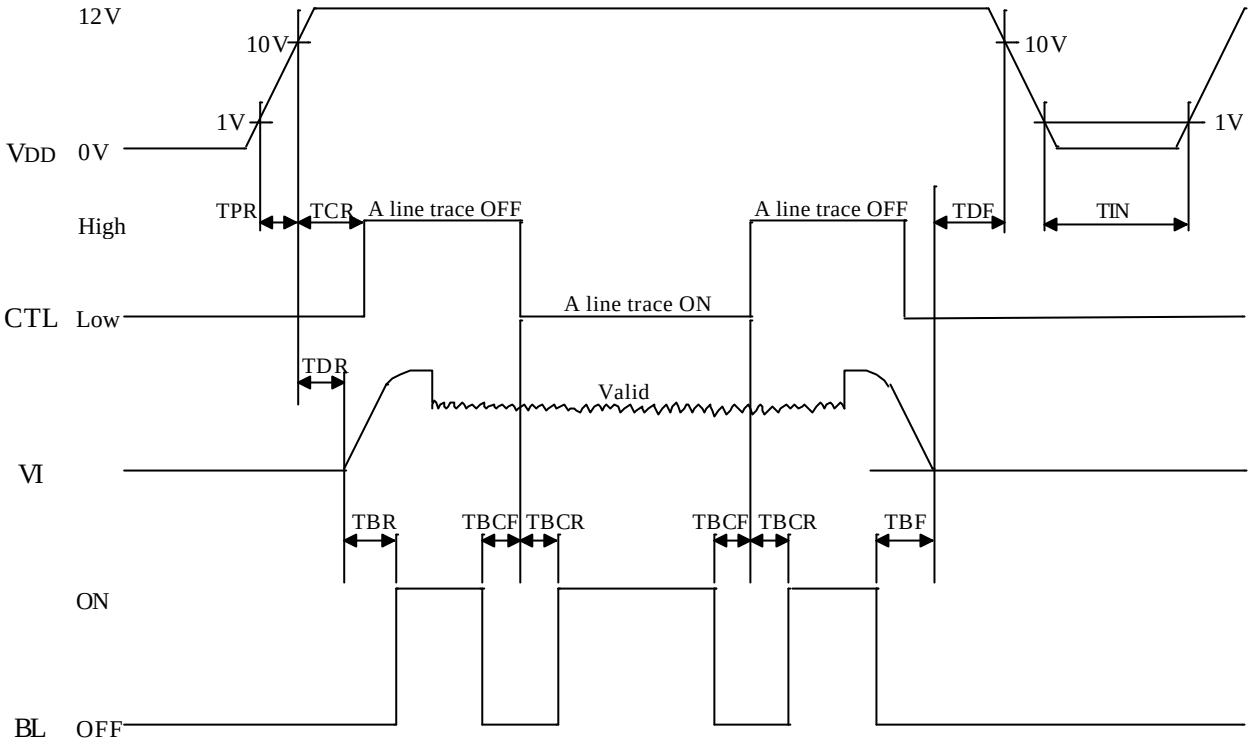
6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Timing of power supply voltage and input signals should be used under the following specifications.

$$0ms \leqq TPR \leqq 10ms$$

$$10ms \leqq TDR \leqq 50ms$$

$$0ms \leqq TDF \leqq 50ms$$

$$TIN \geqq 1s$$

$$200ms \leqq TBR \leqq 500ms$$

$$TBF \leqq 100ms$$

$$4ms \leqq TCR \leqq 10ms$$

$$0ms \leqq TBCF$$

$$200ms \leqq TBCR$$

During CTL switching, follows timing should be kept.

- $1646 \leqq THP \leqq 2046$
- Don't continuously output timing $TVP \leqq 79$ or $TVP \geqq 2047$
- Don't change DCLK frequency.